RA6W1 Hardware Design Guide

This document is an RA6W1 guide that provides hardware design considerations for RA6W1.

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Figures

Tables

1. References

[1] RA6W1 Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

2. Terms and Definitions

BPF	Band Pass Filters
DK	Development Kit
ESR	Equivalent Series Resistance
ESD	Electrostatic Discharge
GPIO	General Purpose Input Output (pin)
GND	Ground
IC	Integrated Circuit
JTAG	Joint Test Action Group
NP	Not Populated
OTP	One-Time Programmable Memory
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembled
POR	Power-On Reset
PPA	Programmable Pin Assignment
RF	Radio Frequency
SDIO	Secure Digital Input Output
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver Transmitter

3. Introduction

RA6W1 is a highly integrated ultra-low-power Wi-Fi MCU integrating an Arm® Cortex®-M33 system processor with a dual band 802.11 a/b/g/n/ax Wi-Fi subsystem, on-chip memory, flexible peripheral interfaces, and power management features.

This provides a standalone single chip solution which can support complex low-power IoT solutions that require Wi-Fi network connectivity.

Extremely low-power operation is accomplished by dynamically disabling elements of the MCU which are not in use, thus allowing a near zero level of power consumption when not actively transmitting or receiving data. Such a low-power operation can extend the battery life up to a year or more depending on the application.

Built from the ground up for the Internet of Things (IoT), theRA6W1 is ideal for door locks, thermostats, sensors, pet trackers, asset trackers, sprinkler systems, connected lighting, video cameras, video doorbells, wearables, and other IoT devices.

Table 1. RA6W1 product group

Part number	Package	Description	Wireless support	Chip marking
R7SA6W1CEDZNR#HA0	66pin QFN	Arm Cortex-M33 MCU, Wi-Fi 6 dual band 2.4/5 GHz 802.11a/b/g/n/ax, 66pin QFN	Wi-Fi 6 2.4/5 GHz Dual band	RA6W1C
R7SA6W1CEDZDD#HA0	70pin WLCSP	Arm Cortex-M33 MCU, Wi-Fi 6 dual band 2.4/5 GHz 802.11a/b/g/n/ax, 70pin WLCSP	Wi-Fi 6 2.4/5 GHz Dual band	RA6W1C
R7SA6W1BEDZNR#HA0	66pin QFN	Arm Cortex -M33 MCU, Wi-Fi 6 2.4 GHz 802.11a/b/g/n/ax, 66pin QFN	Wi-Fi 6 2.4 GHz Single band	RA6W1B
R7SA6W1BEDZDD#HA0	70pin WLCSP	Arm Cortex-M33 MCU, Wi-Fi 6 2.4 GHz 802.11a/b/g/n/ax, 70pin WLCSP	Wi-Fi 6 2.4 GHz Single band	RA6W1B
R7SA6W1AEDZNR#HA0	66pin QFN	Arm Cortex-M33 MCU, Wi-Fi 4 2.4 GHz 802.11/b/g/n	Wi-Fi 4 2.4 GHz Single band	RA6W1A
R7SA6W1AEDZDD#HA0	70pin WLCSP	Arm Cortex -M33 MCU, Wi-Fi 4 2.4 GHz 802.11/b/g/n 70pin WLCSP	Wi-Fi 4 2.4 GHz Single band	RA6W1A

There are two available packages for the RA6W1: QFN and WLCSP. Figure 2 shows the ball and pin assignments of both packages and Table 2 shows the differences in features for both versions.

Table 2. RA6W1 package characteristics

Features	RA6W1 QFN	RA6W1 WLCSP
Number of balls or pins	66 Pin	70 balls
Number of GPIOs	28	28
SRAM	704 kB	704 kB
Package size	5.6 mm × 6.4 mm	3.471 mm × 4.065 mm
Ball/Pin pitch	0.4 mm pitch	0.424 mm pitch

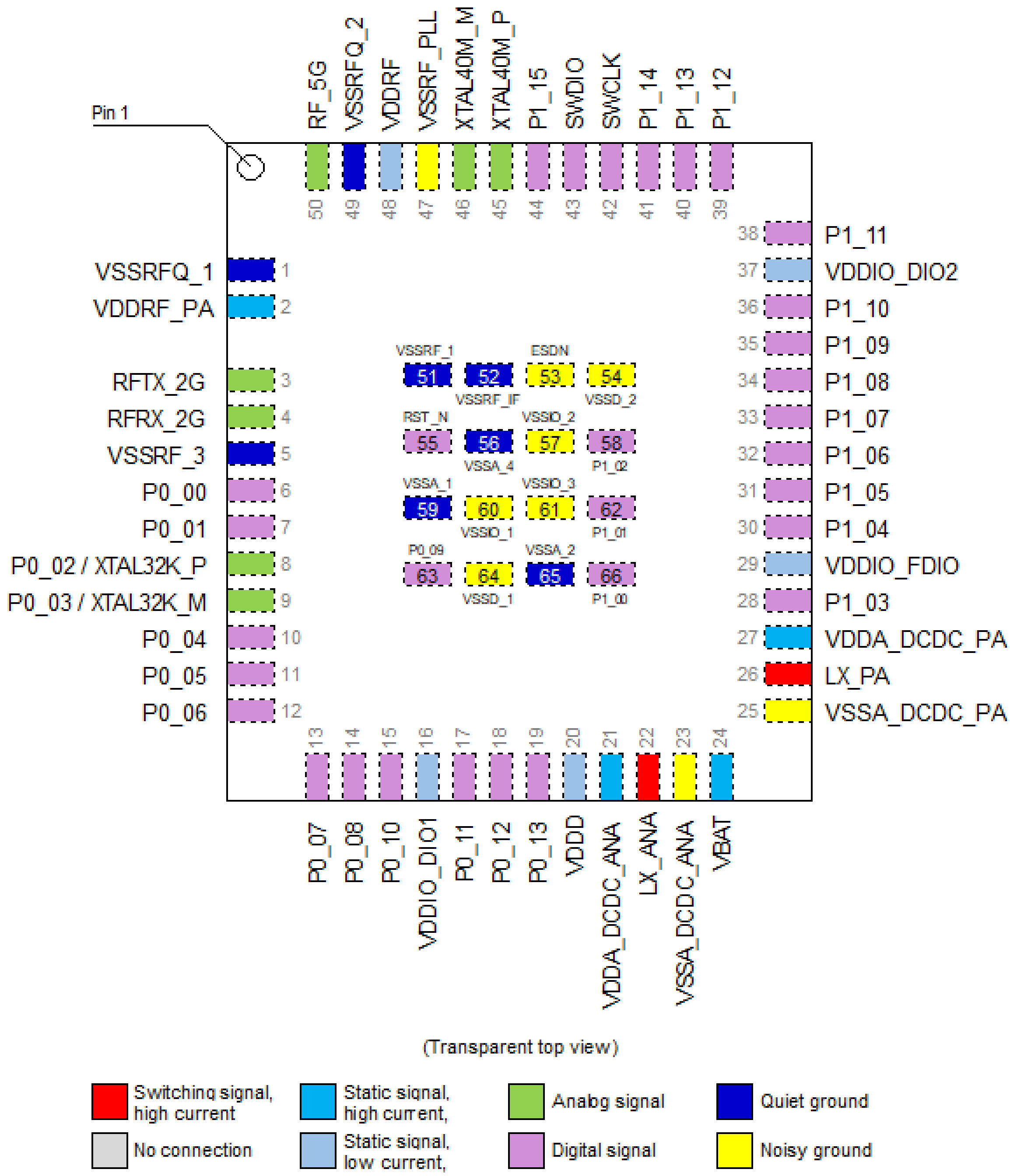

Figure 1. QFN pin assignment

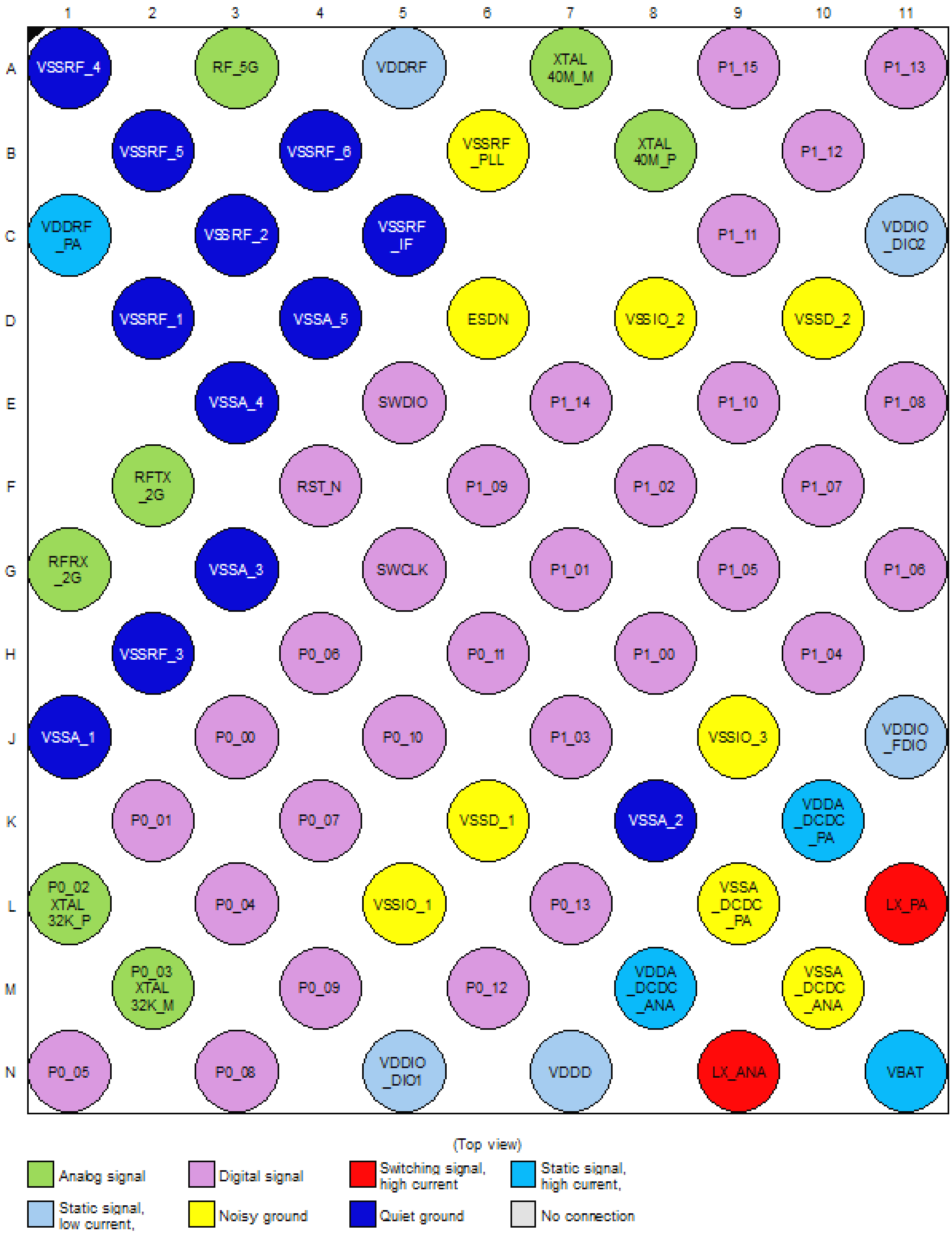

Figure 2. WLCSP ball assignment

4. Device Revision Numbering and Marking

The revision number of the chip can be read from the device by reading the Arm Cortex registers in Table 3 and Table 4. The chip's commercial version number is a combination of such information; example can be read from Table 3.

Table 3. CHIP_REVISION_REG (0x40070214)

Bit	Mode	Symbol		Reset
7:0	R	CHIP_REVISION	Chip version, corresponds with type number in ASCII 0x41 = A, 0x42 = B.	

Table 4. CHIP_TEST1_REG (0x400702f8)

Bit	Mode	Symbol/Description	Reset
7:0	R	CHIP_LAYOUT_REVISION Chip layout revision corresponds to type number in ASCII. 0x41 = A, 0x43 = C, and so forth for the WLCSP package 0x42 = B, 0x44 = D, and so forth for the VFBGA package	

Table 5. Chip revision numbering

Commercial number		CHIP_REVISION_REG (0x50040214)	CHIP_TEST_REG (0x500402F8)
R7SA6W1CEDZNR#HA0	66pin QFN	0x41 (A)	0x42 (B)
R7SA6W1CEDZDD#HA0	70pin WLCSP	0x41 (A)	0x42 (B)

5. Minimal Design for RA6W1 MCU

The RA6W1 MCU requires a minimum number of external components for proper operation. The necessary sections required for the minimal system operation are the following:

- Power section
- Crystals and Clocks
- Radio section
- JTAG
- UART
- Memory
- Reset pin
- Proper PCB routing

5.1 Power Section and Passive Components

The RA6W1 MCU contains internally all power management for proper and safe system operation.

Figure 3 and Figure 4 show the required external components, such as the decoupling capacitors and the power inductor.

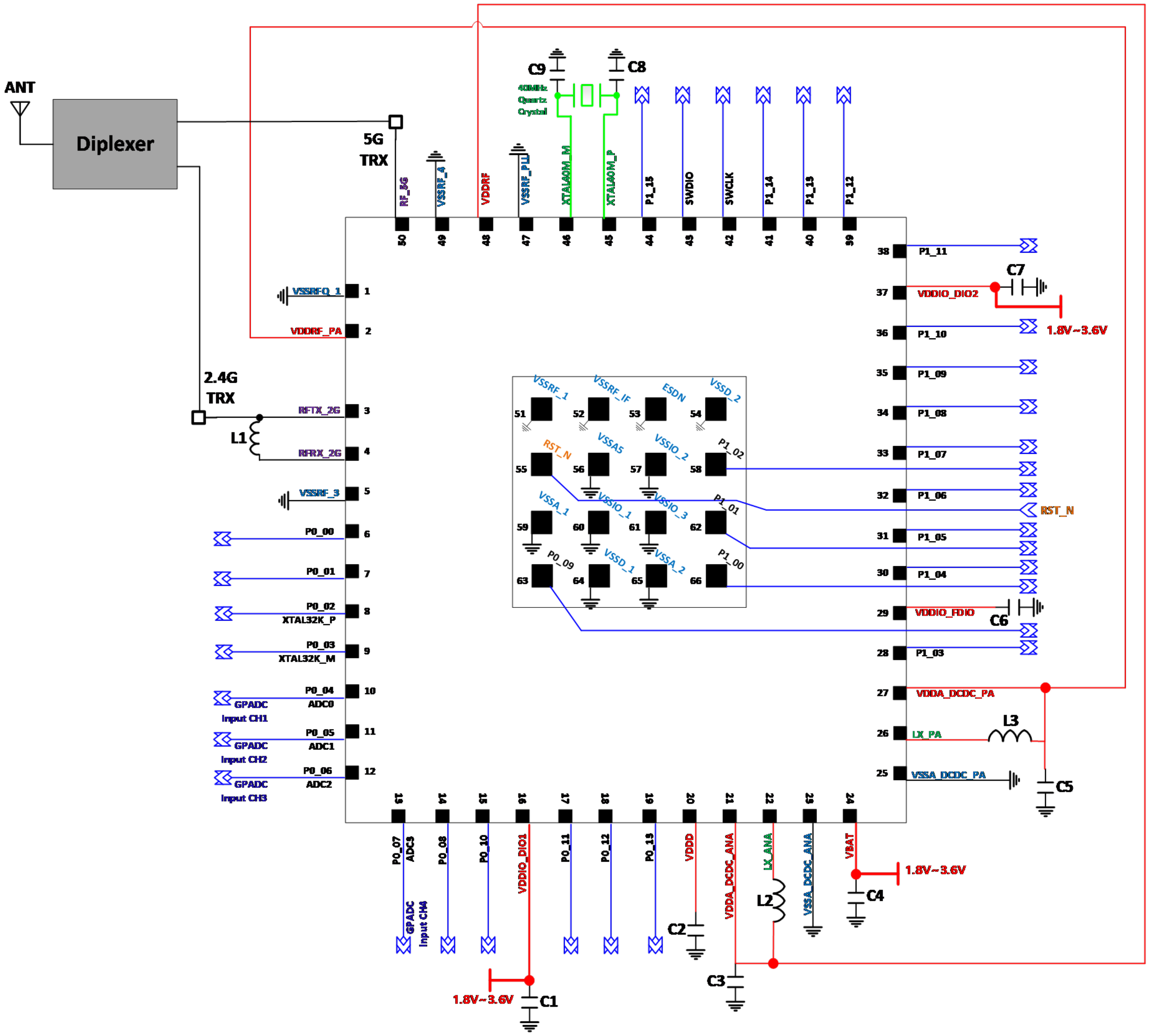

Figure 3. Typical Wi-Fi application – QFN

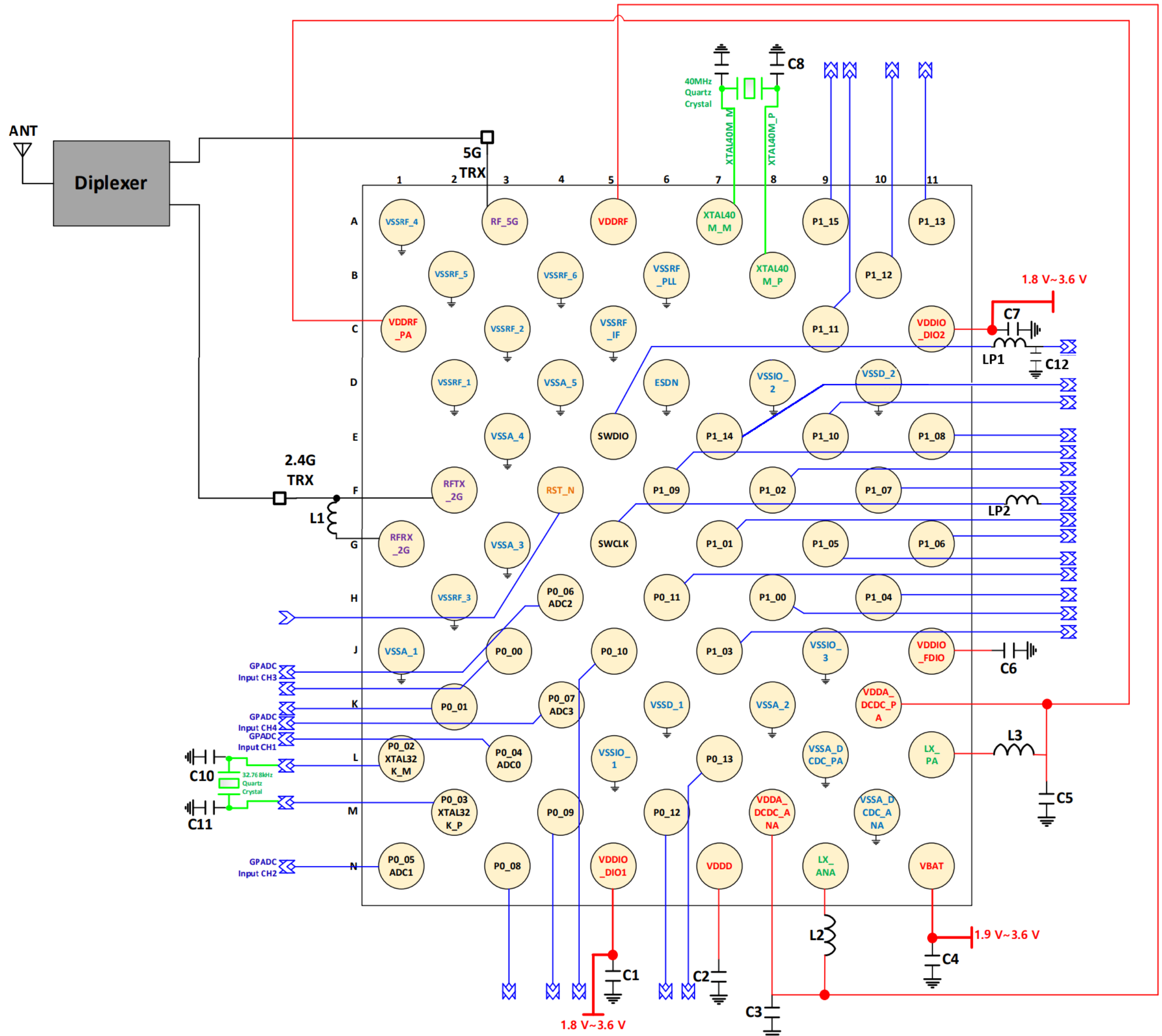

Figure 4. Typical Wi-Fi application – WLCSP

Stresses beyond those listed under Absolute Maximum Ratings (see Ref. 1].) may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

There are three main power inputs, namely, VBAT, VDDIO_DIO1, and VDDIO_DIO2 that are shown in Table 6.

Table 6. Recommended input power supply operating conditions

Parameter	WLCSP ball No	QFN-66 pins pin No	Min	Typ	Max	Units
VBAT	N11	24	1.9	3.3	3.6	V
VDDIO_DIO1	N5	16	1.62	3.3	3.6	V
VDDIO_DIO2	C11	37	1.62	3.3	3.6	V
VDDRF_PA	C1	2		1.35		V
VDDRF	A5	48		1.37		V

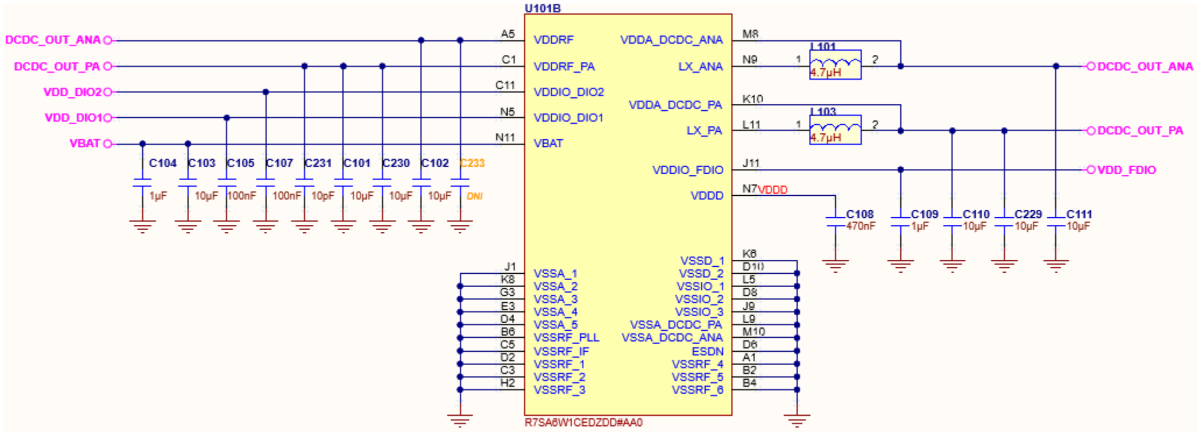

Figure 5. RA6W1 power section schematic

VBAT: main supply from the battery that voltage range for VBAT is 1.9 V to 3.6 V. A 10- µF decoupling capacitor is required to be placed close to the pin.

VDDIO_DIO1: this is the input supply pin for P0_04 to P0_13 Digital IO power. The VDDIO_DIO1 rail needs to be decoupled with a 0.1-µF ceramic capacitor and typical voltage is 3.3 V.

VDDIO_DIO2: this is the input supply pin for P1_10 to P1_17 Digital IO power. The VDDIO_DIO2 rail needs to be decoupled with a 0.1-µF ceramic capacitors and typical voltage is 3.3 V.

DCDC_PA and VDDRF_PA: no external load to be connected to this rail.
The DCDC_OUT_PA output and the VDDRF_PA input must be connected externally. The DCDC_OUT_PA rail output 1.35 V to VDDRF_PA. A 4.7-µH inductor with low DC resistance is connected to the LX_PA pins. One 22 µF or two 10 µF capacitors per pin (DCDC_PA and VDDRF_PA) must be allocated. Due to cost, the approach of 2 x10 µF instead of a 22 µF is suggested. GRM155R61A106ME11 can be used for the ceramic capacitor of 10 µF, 0402.

DCDC_ANA and VDDRF: no external load to be connected to this rail.

The DCDC_OUT_ANA output and the VDDRF input must be connected externally. The DCDC_OUT_ANA rail output 1.37 V to VDDRF. A 4.7-µH inductor with low DC resistance, is connected to the LX_ANA pins. Two ceramic capacitors of 10 µF, one per pin (DCDC_ANA and VDDRF) must be allocated. GRM155R61A106ME11 can be used for the ceramic capacitor of 10 µF, 0402.

Same inductor is used for DCDC DCDC converters.

Table 7. DCDC Inductor examples and characteristics

Manufacturer	Description	Value	Package	Part number
Murata	Shielded, 0.8A, RDC 230 mΩ max	4.7 µH	2015	LQM21PN4R7MGH
SunLord	Shielded, 0.75A, RDC 500 mΩ max	4.7 µH	2015	MPH201214S4R7MT

VDDIO_FDIO: this power rail supplies P1_00 to P1_09 and the external Flash memory. It is connected by default to the internal FDIO_LDO with voltage equal to 1.8 V. A - µF capacitor is used for decoupling.

By connecting a 3.3-V external voltage rail, VDD_FDIO can operate to 3.3 V. In this case, a 3.3-V QSPI Flash must be used.

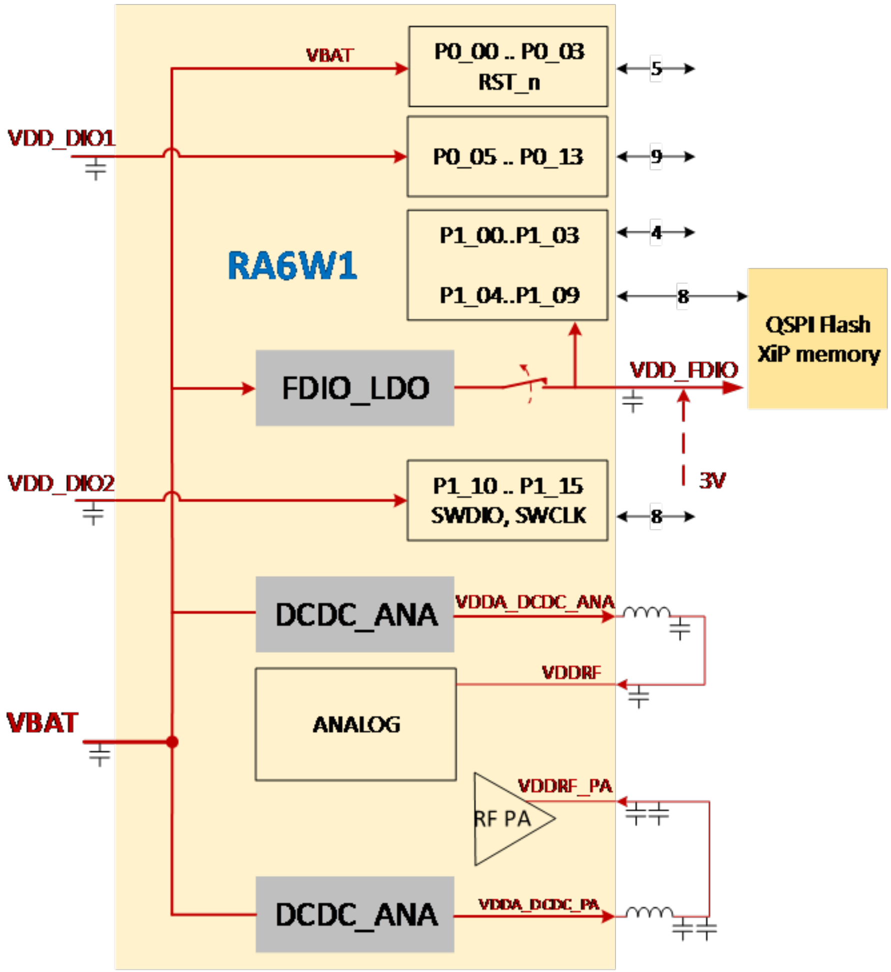

Figure 6. RA6W1 power configuration

Table 8. Suggested decoupling capacitors for the power section

Power pins	Value	Description	Part number
VBAT	10 µF	CAP. CER. ±20 % 10 V X5R, 0402 (1005M)	GRM155R61A106ME11
	1 µF	CAP. CER. ±20 % 10 V X5R, 0402 (1005M)	GRM153R61A105ME95D
VDD_DIO1	0.1 µF	CAP. CER. ±10 % 50V X5R, 0402 (1005M)	GRM155R61H104KE14D
	15 pF	CAP. CER. ±5 % 25 V C0G, 0201 (0603M)	GJM0335C1E150JB01D
VDD_DIO2	0.1 µF	CAP. CER. ±10 % 50 V X5R, 0402 (1005M)	GRM155R61H104KE14D
	15 pF	CAP. CER. ±5 % 25 V C0G, 0201 (0603M)	GJM0335C1E150JB01D
VDD_FDIO	1 µF	CAP. CER. ±20 % 10 V X5R 0402 (1005M)	GRM153R61A105ME95D
VDDA_DCDC_PA	2x10 µF	CAP. CER. ±20 % 10 V X5R, 0402 (1005M)	GRM155R61A106ME11
VDDRF_PA	2x10 µF	CAP. CER. ±20 % 10 V X5R, 0402 (1005M)	GRM155R61A106ME11
	10 pF	CAP. CER. ±5% 50 V COG, 0201 (0603M)	GRM0335C1H100JA01D
VDDA_DCDC_ANA	10 µF	CAP. CER. ±20 % 10 V X5R, 0402 (1005M)	GRM155R61A106ME11
VDDRF	10 µF	CAP. CER. ±20 % 10V X5R, 0402 (1005M)	GRM155R61A106ME11
VDDD	470 µF	CAP. CER. ±10 % 25 V X5R, 0402 (1005M)	GRT155R61E474KE01D

The ceramic capacitors must be placed closest possible to the pins of the chip to reduce the parasitic inductance and to improve performance. Capacitors with the smallest possible package, which meets the voltage range and effective capacitance, can be used.

The selected capacitor values are higher than the required ones because of the capacitance derating phenomenon when a DC bias voltage is applied to the ceramic capacitor. For example, VDCDC_ANA requires effective capacitance of 10 µF. GRM155R61A106ME11 presents 7-µF effective capacitance on 25°C and 1.37 V. Consequently, on the circuit, two capacitors of 10 µF are used.

The capacitance de-rating is highly dependent on the dielectric type (for example, X5R vs. X7R) and the size of the multi-layer ceramic capacitor. Figure 7 shows the capacitance de-rating for two different packages, 0402 and 0603, of a 10 µF/10 V /X5R muRata ceramic capacitor. To compensate or reduce the negative effect of this DC-bias de-rating, it is recommended to apply either a capacitor having a larger size (0603 instead of 0402), or a different type of capacitor.

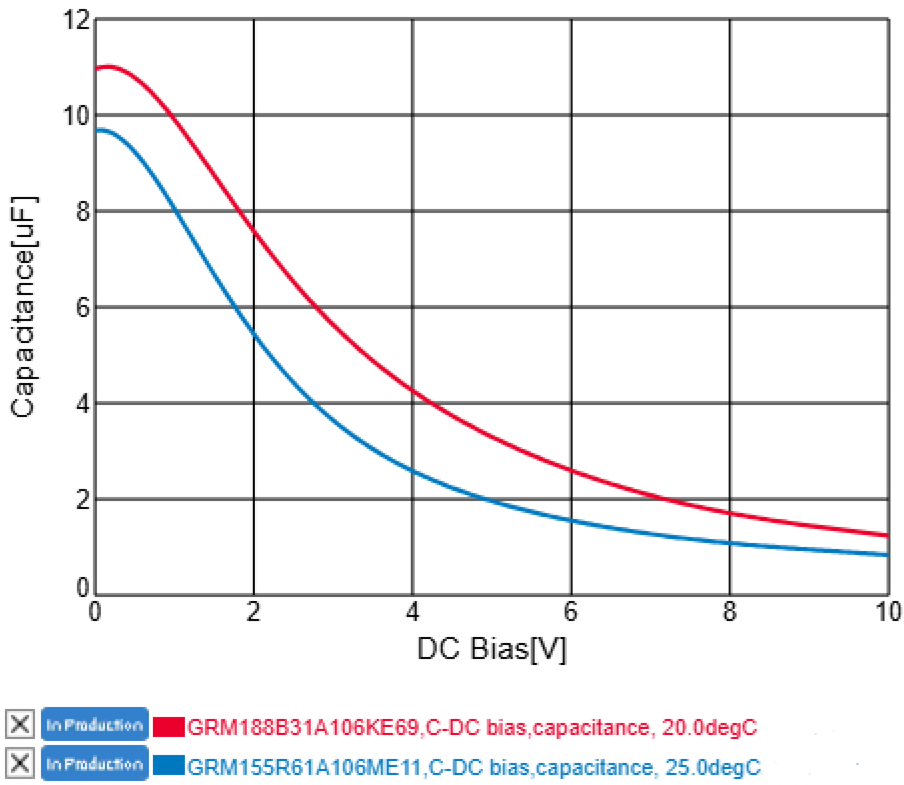

Figure 7. Effective capacitance for 10 µF, 0402 (GRM155R61A106ME11) and 0603 (GRM188B31A106KE69)

Finally, RA6W1-WLCSP presents emissions on the 5-GHz band, close to the ETSI radiated limits. To meet ETSI certification requirements, PCB design must be applied (as described in Section 6.1 RA6W1 - WLCSP). Additionally, include passive components on the SWDIO and SWCLK lines, as it is on Figure 3 and Figure 8

The components must be placed closest possible to the pads of the RA6W1-WLCSP MCU. The additional components are not needed for the 2-GHz band.

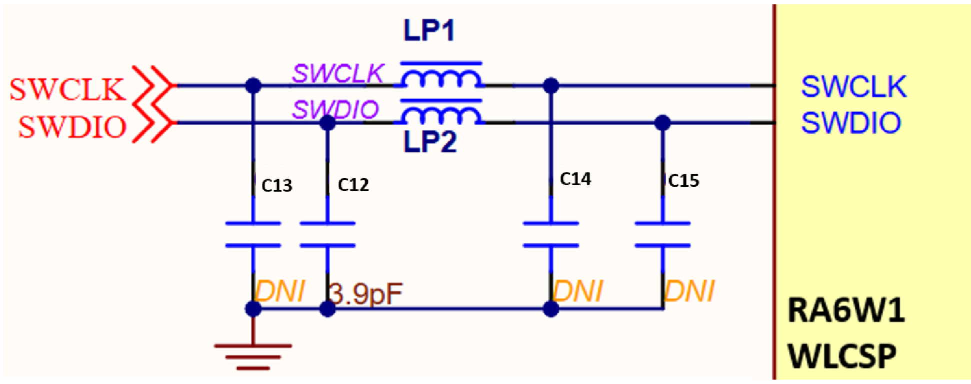

Figure 8. Components on SWDIO and SWCLK

Table 9. Suggested components for SWDIO and SWCLK

Description	Component	Part number
SWDIO Capacitor	C12	GJM1555C1H3R9CB01
SWDIO Ferrite bead	LP2	BLM15AG601SN1D
SWCLK Ferrite bead	LP1	BLM15AG601SN1D

5.2 Crystals and Clocks

The RA6W1 MCU is equipped with two Crystal Oscillators, one at 40 MHz (XTAL40M) and the other at 32.768 kHz (XTAL32K). XTAL32K has no trimming capabilities and is used as the low power clock for Low-power Sleep mode. XTAL40M can be trimmed by using the internal capacitor bank.

5.2.1 40-MHz Clock

The RA6W1needs an accurate 40-MHz clock for proper operation. The clock can be generated either by an external 40-MHz crystal or by applying an external 40-MHz clock signal.

The CLOAD value (CL) of the used 40 -MHz crystal preferably would be 8 pF typical, see Table 10. The crystal's ESR must not exceed 50 Ω, see Table 10.

For the specification of 40-MHz crystals, see Section 3.4 in Ref. 1].

Table 10. XTAL40M recommended operating conditions

Parameter	Description	Min	Typ	Max	Unit
Frequency	Crystal oscillator frequency		40		MHz
ΔfXTAL(40M)	Crystal frequency tolerance	-20		20	ppm
ESR (40M)	Equivalent series resistance			50	Ω
CL(40M)	Load capacitance	6	8	10	pF

For the specification of 40-MHz crystals, see Section 3.4 in Ref. 1].Table 11 lists examples of suitable 40-MHz crystals.

Table 11. 40-MHz crystal example and characteristics

40-MHz crystals	TAI-SAW	KYOCERA AVX	EPSON
Part number	TZ1269D	CX2016SA40000D0FLJG1	FA-20H 40.0000MF10Z-K0
Frequency	40 MHz	40 MHz	40 MHz
Frequency tolerance	+/-10 ppm at 25 °C	+/-10 ppm at 25 °C	+/-10 ppm at 25 °C
Temperature frequency drift	+/-15 ppm	+/-15 ppm	+/-10 ppm
Load capacitance	9 pF	8 pF	6 pF
Drive level	50 µW typical (100 µW max)	10 µW typical	10 µW typical
Temperature range	-40 °C ~ +85 °C	-30 °C ~ +85 °C	-40 °C ~ +85 °C
Size L x W x H (mm)	2.0 x 1.6 x 0.4	2.0 x 1.6 x 0.45	2.5 x 2.0 x 0.55

The 40-MHz crystal oscillator frequency is trimmed by two on-board capacitors of 4.7 pF and the settings of XTAL40M_CCTRL. XTAL40M_CCTRL is a field on register XTAL40M_CTRL_REG (0x400C0204). The valid range of values of the XTAL40M_CCTRL is 0x00 ~ 0x7F which corresponds to a range of 80 ppm. The implementation of TZ1269DA is on Figure 9.

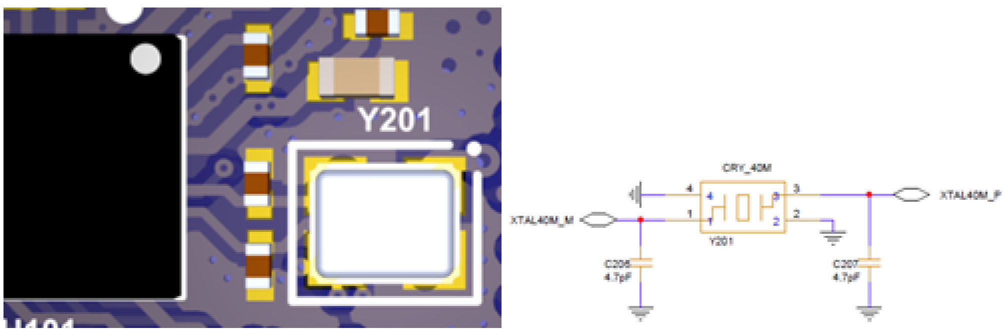

Figure 9. TZ1269DA, 40-MHz crystal implementation

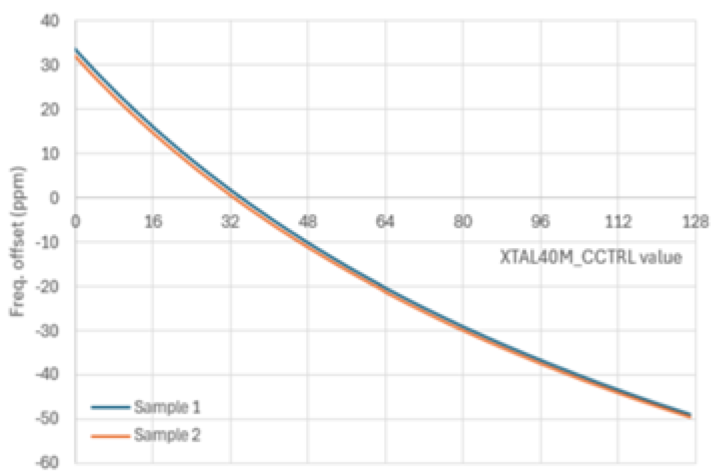

Figure 10. Crystal oscillator frequency range for the complete XTAL40M_CCTRL range of values

The value of the capacitors (4.7 pF) is dependent on the crystal as well as the PCB layout. Designers must check the frequency range and adjust the capacitors' value in such a way that final trimming value of XTAL40M_CCTRL to be closer possible to the middle of its dynamic range (64 decimal).

5.2.2 32.768-kHz Clock

For supporting ultra-low power Wi-Fi connected operation like DPM and TWT, an external 32-kHz XTAL must be connected to the RA6W1 pins P0_02 and P0_03. The better accuracy of the crystal the tighter timing is achieved.

Recommended crystal specification in Table 12. Example of a 32-kHz crystal is in Table 13.

Table 12. XTAL32K – recommended specification

Parameter	Description	Value
Frequency	Crystal frequency	32.768 kHz
Frequency tolerance	Crystal frequency tolerance	±20 ppm
ESR	Equivalent series resistance	100 kΩ
CL	Load capacitor	10 pF

Table 13. Example of suitable 32.768-kHz crystals

32.768-kHz crystals	Abracon corp.
Part number	ABS06
Frequency	32.768 kHz
Frequency tolerance	+/-20 ppm at 25 °C
Load capacitance	12.5 pF
ESR	90 kΩ max
Drive level	0.1 μW typ, 0.5 μW max
Temperature range	-40 °C ~ +85 °C
Size L x W x H (mm)	2.0 x 1.2 x 0.6

Two shunt capacitors to GND, 15 pF each, are required for ensuring proper operation of the crystal.

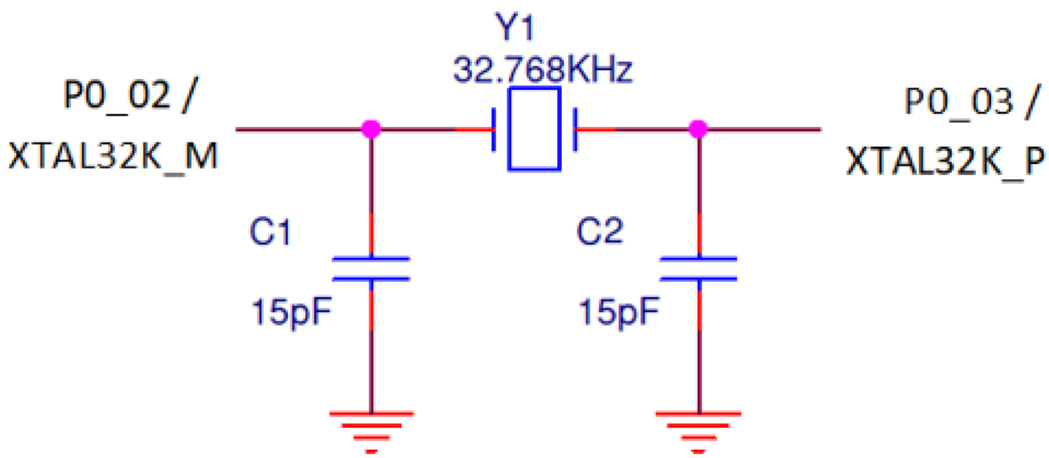

Figure 11. 32.768-kHz crystal configuration

External clock can also be connected to the RA6W1 by connecting the signal to P0_02. In this case, for utilizing the clock direct input mode, the internal XTAL circuit must be disabled by setting CLK_XTAL32K_REG register to 0x18. P0_03 can be used as GPIO.

5.3 GPIOs

RA6W1 provides 32 GPIOs. The functions assigned to the GPIO pins are fully configurable and are controlled by the Programmable Pin Assignment (PPA). PPA provides a multiplexing function for the I/O pins of the on-chip peripherals. Any of the peripheral input or output signals can be freely mapped to any available GPIO port, except ADC, QSPI, SDIO, eMMC, and SWD which have fixed assignment. See information for the peripherals in Ref. 1].

When a pin is configured to function as a GPIO, it has the following configurable features:

- Direction (input/output)
- Push pull/Open drain
- Pull-up/Pull-down
- Selectable 25 kΩ pull-up/pull-down resistors per pin up to selected voltage rail
- Drive strength (2 mA, 4 mA, 8 mA, 14 mA)
- Slew rate (Fast/Slow)
- Input selection (CMOS/Schmitt Trigger).
- Pin state is kept when the system enters Low-power Sleep 4 and 5 modes

After a power on reset (POR), the default state of the pins of RA6W1 MCU, is shown in Table 14.

Noticeable characteristics of GPIOs:

- RSTn and P0_00 to P0_03 are referred to VBAT.
- P1_00 to P1_09 are referred to VDD_FDIO , which is by default equal to 1.8 V.
- Quad SPI Controller is assigned only to P0_08 to P0_13.
- There is only one SDIO interface which can be assigned to either P0_08 to P0_13 or P1_10 to P1_15 .
- Not all pins can be used for waking up the MCU. Wake-up signals are digital signals, and they are activated by logic state change. On the other hand, analog wake-up signals are activated when a programmable voltage level is crossed.
- ADCs can be assigned only to P0_04 to P0_07.
- P0_00 and P0_01 are assigned to Booting UART.
- P0_16 and P0_17 are assigned to SWD.
- P_02 and P0_03 can be either XTAL32kHz or GPIO pins.

Table 14. Pin configuration

Pin	Support wake-up	Power domain	Alternate function 0	Alternate function 1	Alternate function 2	POR default
RST_N		VBAT	RST_N			RST_N
P0_00	Yes	VBAT	RTC_WAKE_UP			GPIO
P0_01		VBAT	sen_out			sen_out
P0_02		VBAT	xtal32k_m			xtal32k_m
P0_03		VBAT	xtal32k_p			xtal32k_p
P0_04	ana wake	VDDIO_DIO1	ADC0		eMMC_DIO4	GPIO
P0_05	ana wake	VDDIO_DIO1	ADC1		eMMC_DIO5	GPIO
P0_06	ana wake	VDDIO_DIO1	ADC2		eMMC_DIO6	GPIO
P0_07	ana wake	VDDIO_DIO1	ADC3	MCLK	eMMC_DIO7	GPIO
P0_08	Yes	VDDIO_DIO1	QSPIR_CLK	SDIO0_CLK	eMMC_CLK	GPIO
P0_09	Yes	VDDIO_DIO1	QSPIR_CS	SDIO0_CMD	eMMC_CMD	GPIO
P0_10	Yes	VDDIO_DIO1	QSPIR_D0	SDIO0_D0	eMMC_DIO0	GPIO
P0_11	Yes	VDDIO_DIO1	QSPIR_D1	SDIO0_D1	eMMC_DIO1	GPIO
P0_12	Yes	VDDIO_DIO1	QSPIR_D2	SDIO0_D2	eMMC_DIO2	GPIO
P0_13	Yes	VDDIO_DIO1	QSPIR_D3	SDIO0_D3	eMMC_DIO3	GPIO
P1_00		VDD_FDIO	OQSPI_D4	eMMC_DIO4		GPIO
P1_01		VDD_FDIO	OQSPI_D5	eMMC_DIO5		GPIO
P1_02		VDD_FDIO	OQSPI_D6	eMMC_DIO6		GPIO
P1_03		VDD_FDIO	OQSPI_D7	eMMC_DIO7		GPIO
P1_04		VDD_FDIO	OQSPI_D0			
P1_05		VDD_FDIO	OQSPI_D1			
P1_06		VDD_FDIO	OQSPI_D2			
P1_07		VDD_FDIO	OQSPI_D3			
P1_08		VDD_FDIO	OQSPI_CLK			
P1_09		VDD_FDIO	OQSPI_CS			
P1_10	Yes	VDDIO_DIO2	eMMC_CMD	SDIO1_CMD		GPIO
P1_11	Yes	VDDIO_DIO2	eMMC_CLK	SDIO1_CLK		GPIO
P1_12	Yes	VDDIO_DIO2	eMMC_DIO0	SDIO1_D0		GPIO
P1_13	Yes	VDDIO_DIO2	eMMC_DIO1	SDIO1_D1		GPIO
P1_14		VDDIO_DIO2	eMMC_DIO2	SDIO1_D2		GPIO
P1_15		VDDIO_DIO2	eMMC_DIO3	SDIO1_D3		GPIO
P1_16		VDDIO_DIO2	SWCLK			SWCLK
P1_17		VDDIO_DIO2	SWDIO			SWDIO

5.4 Reset Pin (RST_N)

The RA6W1 has an active-low reset pin (RST_N pad), and it is referred to VBAT power domain. There is not any pull-up internally to RA6W1 MCU. An external pull-up resistor from 10 kΩ to 30 kΩ must be added.

5.5 UART

The UART interface provides an industry compliant serial interface for communicating with other devices. Three independently configurable UARTs are available which support the RS-232 and RS-485 protocols. There are two different UART configurations possible:

- 2-wire UART (URX and UTX)
- 4-wire UART (URX, UTX, RTS and CTS).

The UART pins can be assigned to any of the unused GPIO pins through the Programmable Pin Assignment (PPA) function. The assignment can be done by setting the proper field on the mode register of the correspondent GPIO, example for P0_00 on Figure 13. Good practice is to select GPIOs of same voltage range.

Bit	Mode	Symbol/Description	Reset
6:0	R/W	PID 0: GPIO (I/O) 1: UART_RX (IA) 2: UART_TX (OA) 3: UART_CTSN (IA) 4: UART_RTSN (OA) 5: UART_TXDOE (OA) 6: UART1_RX (IA) 7: UART1_TX (OA) 8: UART1_CTSN (IA) 9: UART1_RTSN (OA) 10: UART1_TXDOE (OA) 11: UART2_RX (IA) 12: UART2_TX (OA) 13: UART2_CTSN (IA) 14: UART2_RTSN (OA) 15: UART2_TXDOE (OA)	0x0

Figure 12. PID field on P0_00_Mode register for enabling UART pins

During booting, GPIOs P0_00 and P0_01 are assigned as URX and UTX respectively, providing the capability to download a software image. The baud rate during boot is 115.2 kbits/s.

5.6 SWD(JTAG)

SWD consists of two pins P1_16 (SWCLK) and P1_17 (SWDIO).
A standard Serial Wire Debug (SWD) is provided to allow debugging of user applications during the development phase of a product. When development is complete, and the device is set to secure mode and the SWD interface is disabled to protect the device from being tampered with.

5.7 Octa/Quad SPI Flash

The Octa/Quad SPI Controller (OQSPIC) provides a low pin count interface to standard Serial Peripheral Interface (SPI) and a high-performance Dual/Quad/Octa SPI Interface.

The Quad SPI Controller supports the following SPI modes:

- Single: Data transfer through two unidirectional pins.
- Dual: Data transfer through two bidirectional pins.
- Quad: Data transfer through four bidirectional pins.
- Octa: Data transfer using eight bidirectional pins.

Table 15 shows the pin configurations for the OQSPI interface.

Table 15. OQSPI pin configuration

Function	GPIO	Description	QFN pin No	WLCSP ball No
OQSPI_CLK	P1_08	Output serial clock	34	E11
OQSPI_CS	P1_09	Active Low output Chip select	35	F6
OQSPI_D0	P1_04	MOSI (output) in single SPI mode D0 (bidirectional) in Quad/Octa SPI mode	30	H10
OQSPI_D1	P1_05	MISO (input) in single SPI mode D1 (bidirectional) in Quad/Octa SPI mode	31	G9
OQSPI_D2	P1_06	WPn Write Protect output in single SPI mode D2 (bidirectional) in Quad/Octa SPI mode	32	G11
OQSPI_D3	P1_07	HOLDn/Resetn output in Single SPI mode D3 (bidirectional) at Quad/Octa SPI mode	33	F10
OQSPI_D4	P1_00	D4 (bidirectional) at Octa SPI mode	66	H8
OQSPI_D5	P1_01	D5 (bidirectional) at Octa SPI mode	62	G7
OQSPI_D6	P1_02	D6 (bidirectional) at Octa SPI mode	58	F8
OQSPI_D7	P1_03	D7(bidirectional) at Octa SPI mode	28	J7

As the maximum operating frequency of the QSPI interface in the RA6W1 is 80 MHz. Table 16 shows successfully tested and supported flashes.

Table 16. Examples of suitable QSPI Flash

Part number	Capacity	Provider
AT25SL0641C	64 Mbit	Renesas Electronics

To avoid signal integrity issues, keep the distance between the processor and the QSPI Flash memory as short as possible, try to have the length of the traces as equal as possible, and route with enough spacing to avoid crosstalk.

The QSPI device must be supplied by the VDD_FDIO rail. VDD_FDIO by default is 1.8 V.

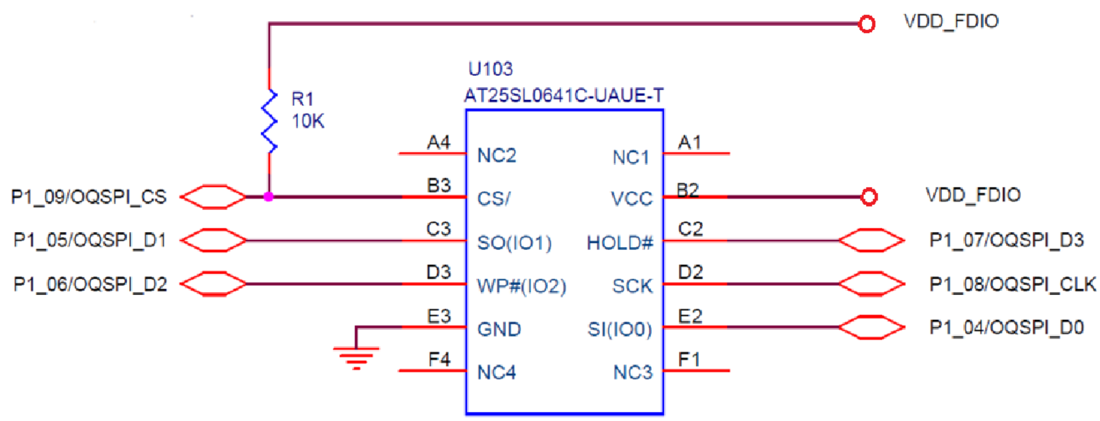

Figure 13. QSPI Flash memory used in RA6W1 daughterboard

5.8 SPI Functions

RA6W1 provides two SPI interfaces (SPI/SPI2), with master and slave capability for connection to SPI devices in Master mode or being connected to a host MCU in Slave mode. They have separate RX/TX FIFOs (32 B) and support SPI clock rates up to 48 MHz for 3.3 V, and 40 MHz for 1.8 V.

The SPI interface supports all four modes of operation and the corresponding polarity (CPOL) and phase (CPHA) of the SPI clock (SPI_CLK).

All available GPIOs can be used as SPI signals, by setting the proper PID field on the correspondent GPIO mode register, example for P0_00 on Figure 13 and Figure 14.

Bit	Mode	Symbol/Description	Reset
		16: SPI_DI (IA) 17: SPI_DO (OA) 18: SPI_CLK (I/O) 19: SPI_CSN0 (I/O) 20: SPI_CSN1 (OA) 21: SPI2_DI (IA) 22: SPI2_DO (OA) 23: SPI2_CLK (I/O) 24: SPI2_CSN0 (I/O) 25: SPI2_CSN1 (OA)	

Figure 14. PID field on P0_00_Mode register for enabling SPI signals

For operating SPI bus in high frequency, for ensuring signal integrity, it would be helpful to have a provision for termination in-series resistors. Resistors can be between of 10 to 33 Ω and they must be placed close to transmission port.

5.9 Interface of QSPI Controller

Besides OQSPI controller, which is used for connecting a XiP Flash, RA6W1 MCU provides an additional QSPI Controller (QSPIC). QSPIC can interface with an external non secure Flash or PSRAM with capability of up to 64 MB. The QSPIC supports the standard SPI and a high-performance Dual/Quad SPI Interface, in Master mode only.

QSPIC interface is assigned on specific pins of RA6W1, see Table 17.

Table 17. Pin assignment of QSPIC interface

Pin name	Pin assignment	SPI	QSPI
QSPI_CLK	P0_08	Output serial clock	Output serial clock
QSPI_CS	P0_09	Active low output Chip select	Active low output Chip select
QSPI_D0	P0_10	MOSI (output)	D0 (bidirectional)
QSPI _D1	P0_11	MISO (input)	D1 (bidirectional)
QSPI _D2	P0_12	WPn Write Protect output	D2 (bidirectional)
QSPI _D3	P0_13	HOLDn/Resetn output	D3 (bidirectional)

As the voltage range of the interface is defined by VDD_DIO1, memory must be supplied from same rail or another rail with equal voltage.

For avoiding signal integrity issues, keep distance between RA6W1 MCU and memory short, avoid stubs and cross talk between the traces. It would be also helpful to have provision for termination in-series resistors. Resistors values can be between of 10 to 33 Ω. Example of PSRAM connectivity is presented on Figure 15.

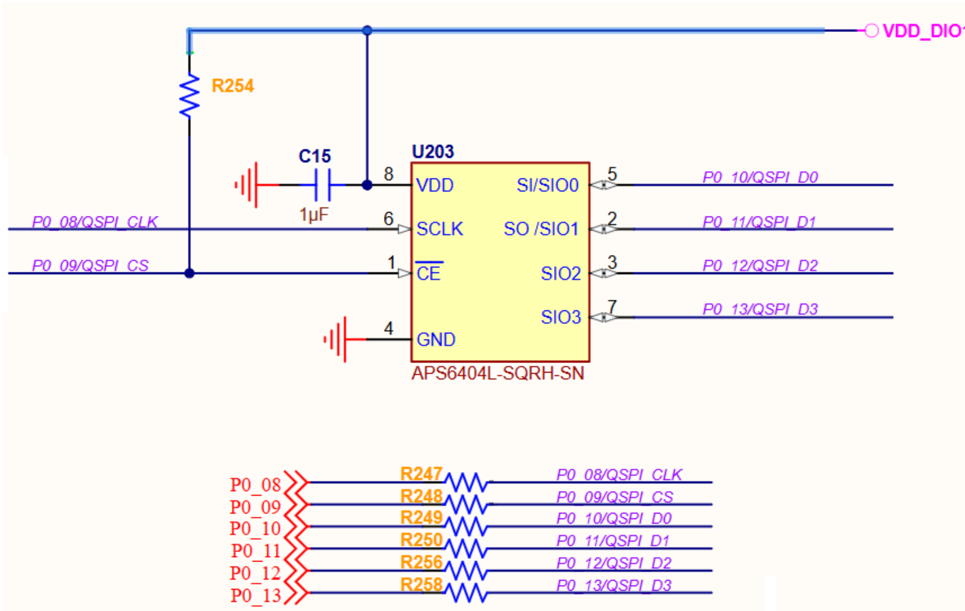

Figure 15. QSPIC interface connectivity to PSRAM

5.10 SDIO Function

RA6W1 supports an SDIO 3.0 card interface suitable for memory card and I/O card applications with low-power consumption. The SDIO interface supports SPI, 1-bit SD, and 4-bit SD transfer modes at the full clock range of 0 to 80 MHz.

The SDIO interface requires pull-up resistors to be connected among the signal lines and the supply to enable communication. Pull-up resistor values may vary based on the board layout. Do not apply a pull up on SDIO_CLK, see Figure 16.

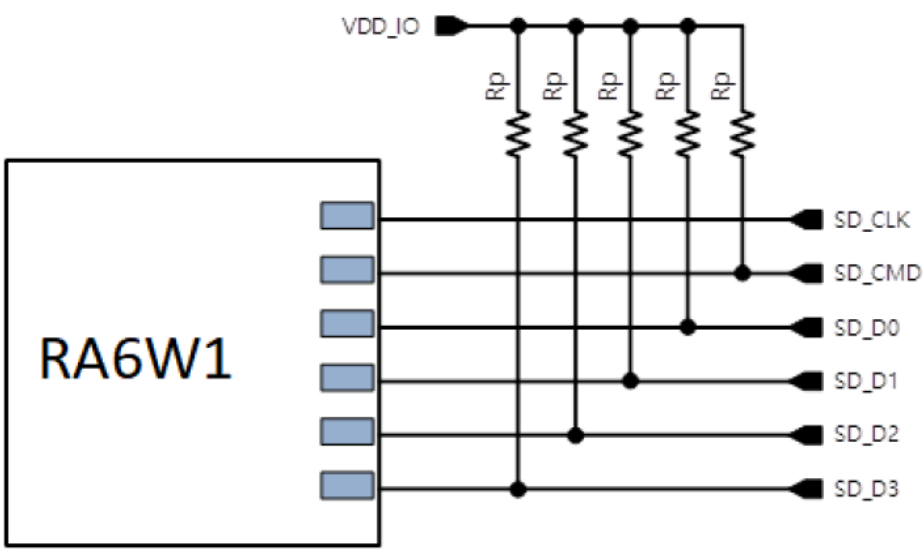

Figure 16. SDIO pull-up resistor

Table 18. SDIO Pin configuration

Pin name	Pin assignment (Alt 1/Alt 2)	I/O	Description
SDIO_CMD	P1_10/P0_08	I/O	Command line
SDIO_CLK	P1_11/P0_09	I	Input serial clock
SDIO_D0	P1_12/P0_10	I/O	Bi-directional data line
SDIO_D1	P1_13/P0_11	I/O	Bi-directional data line
SDIO_D2	P1_14/P0_12	I/O	Bi-directional data line
SDIO_D3	P1_15/P0_13	I/O	Bi-directional data line

5.11 RF Section

Ther are two RF ports, one for 2.4-GHz band and one for 5-GHz band for RA6W1C. There is only 2.4-GHz RF port for the RA6W1A and RA6W1B.

2.4-GHz port consists of two pins, RFTX_2G and RFRX_2G which are combined through an LC circuit, where L=3 nH and C=1 pF, both 0201. LC circuit must be placed close to the chip. Figure 17 shows the RF output circuitry with an external diplexer to combine the 2.4-GHz and 5-GHz transmit/receive paths and a band pass filter (BPF) to ensure the rejection of out-of-band emissions on 5 GHz.

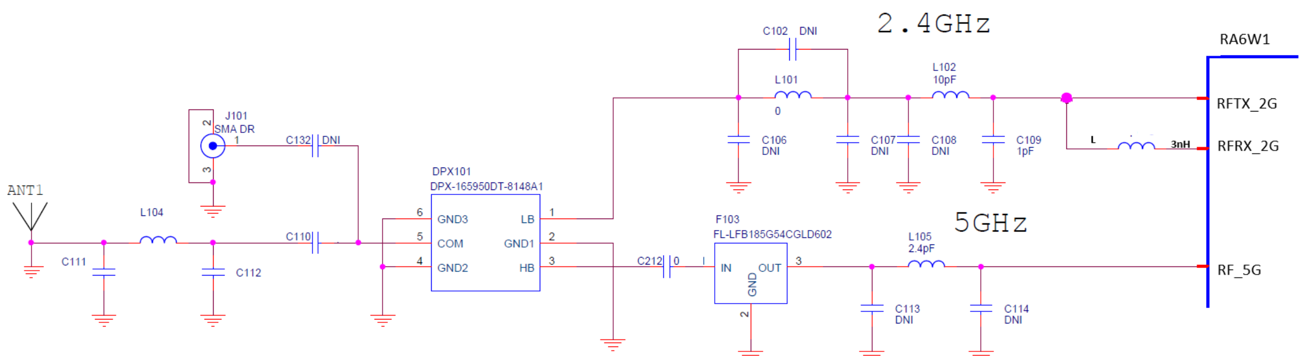

Figure 17. RFIO port and RF circuitry as applied on RA6W1 development board

Table 19. Recommended RF front-end components

Part number	Component	Provider
LFB185G54CGLD602	Band pass filter	Murata Electronics
DPX165950DT-8060C1	Diplexer	TDK

5.12 ESD Protection

If a GPIO or an antenna can be touched by users, provide an ESD protection device for them. For the RF input an ultra-low capacitance device must be used. The ESD protected signal lines should be routed directly to the transient-voltage-suppression diode. Ground connections should be made directly to the ground plane to minimize parasitic inductance.

For connectors, the transient-voltage-suppression devices should be placed as close to the connector as possible to reduce transient coupling into nearby traces. The secondary effects of radiated emissions can cause upset to other areas of the board, even if there is no direct path to the connector.

Apply Uni-Directional ESD protection devices on signals having only positive polarity. Such devices have a lower forward bias voltage to clamp negative ESD voltages.

6. PCB Routing Guidelines

6.1 RA6W1 - WLCSP

PCB layout in four-layers PCB of RA6W1 WLCSP is feasible by using microvias on pad, buried vias and careful routing. On the proposed four-layers PCB stack-up, Figure 18 shows PCB routing strategy per layer.

Layer name	layer description	material	Layer thickness(mm)	Copper weight(oz)
	Solder mask	Solder mask		
L1 TOP Layer		Copper	0.03	1
	Dielectric	FR4	0.065	
L2 Internal Layer		Copper	0.03	1
	Dielectric	FR4	0.71	
L3 Internal Layer		Copper	0.03	1
	Dielectric	FR4	0.065	
L4 BOTTOM Layer		Copper	0.03	1
	Solder mask	Solder mask		

Figure 18. Example of PCB stacking

- L1 top layer is used for component placement and routing the pins located on the periphery of the chip. Components placement must follow the guidelines for power, crystal, and RF sections. Routing of the RF traces are applied on this layer, see Figure 19.

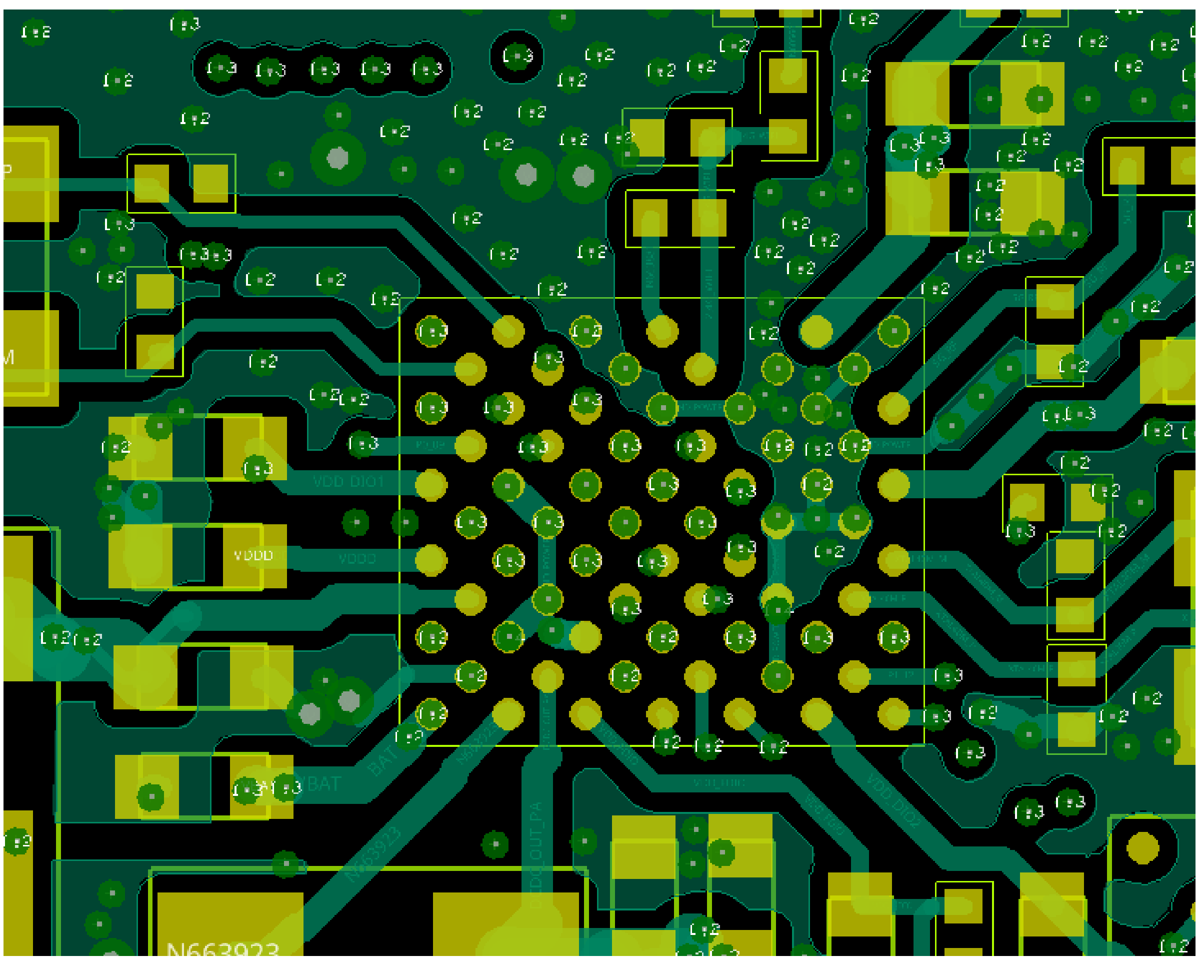

Figure 19. L1 top layer, RA6W1 - WLCSP

- L2 internal layer is considered the reference GND plane for the RF of the chip. It is free of traces under the Chip and RF front-end area. This is important so there are no GND islands, which increase the distance of the grounding current. This is the layer where the RF traces impedance is referred to. GND vias from the chip are connected to this layer, see Figure 20.

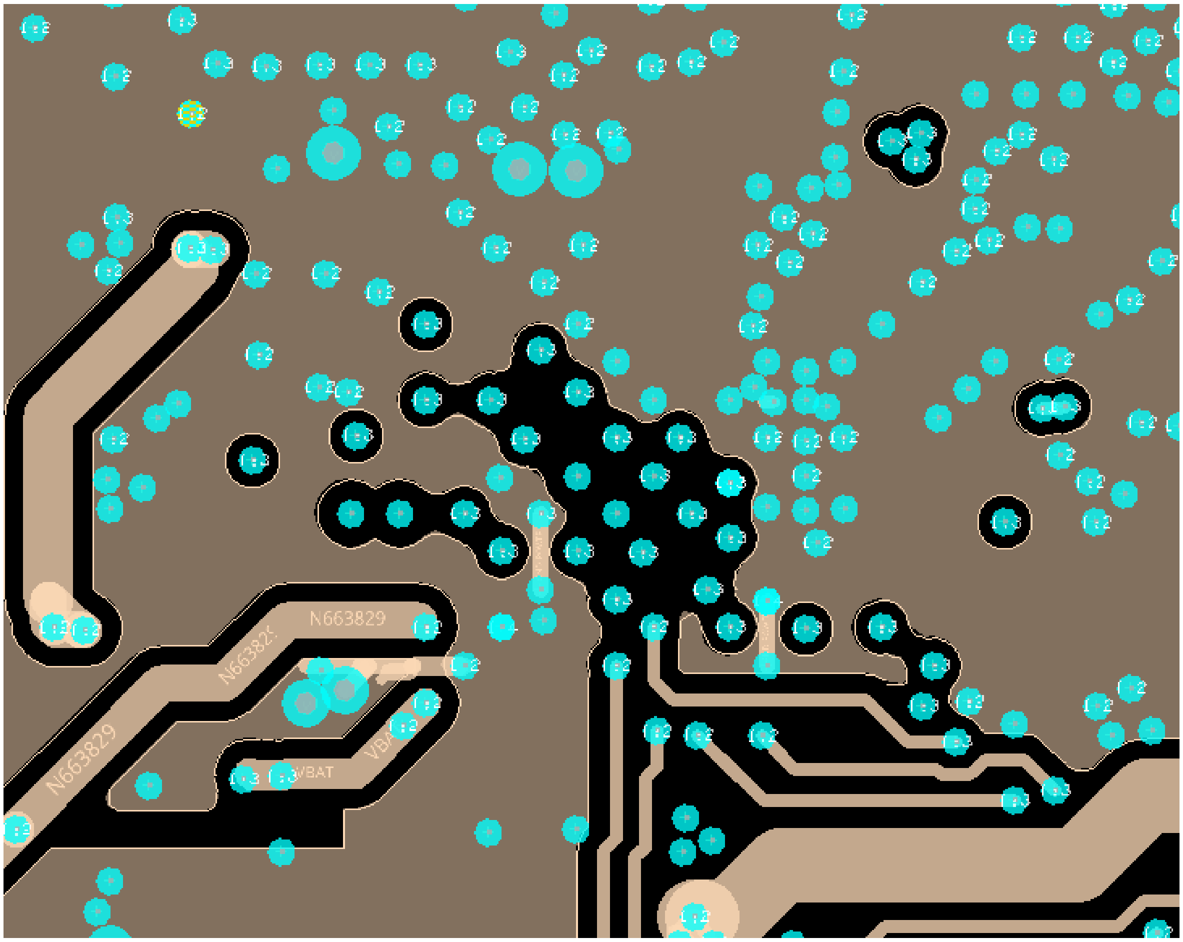

Figure 20. L2 internal layer, RA6W1- WLCSP

- L3 internal layer is used for routing all rest signals, see Figure 21.

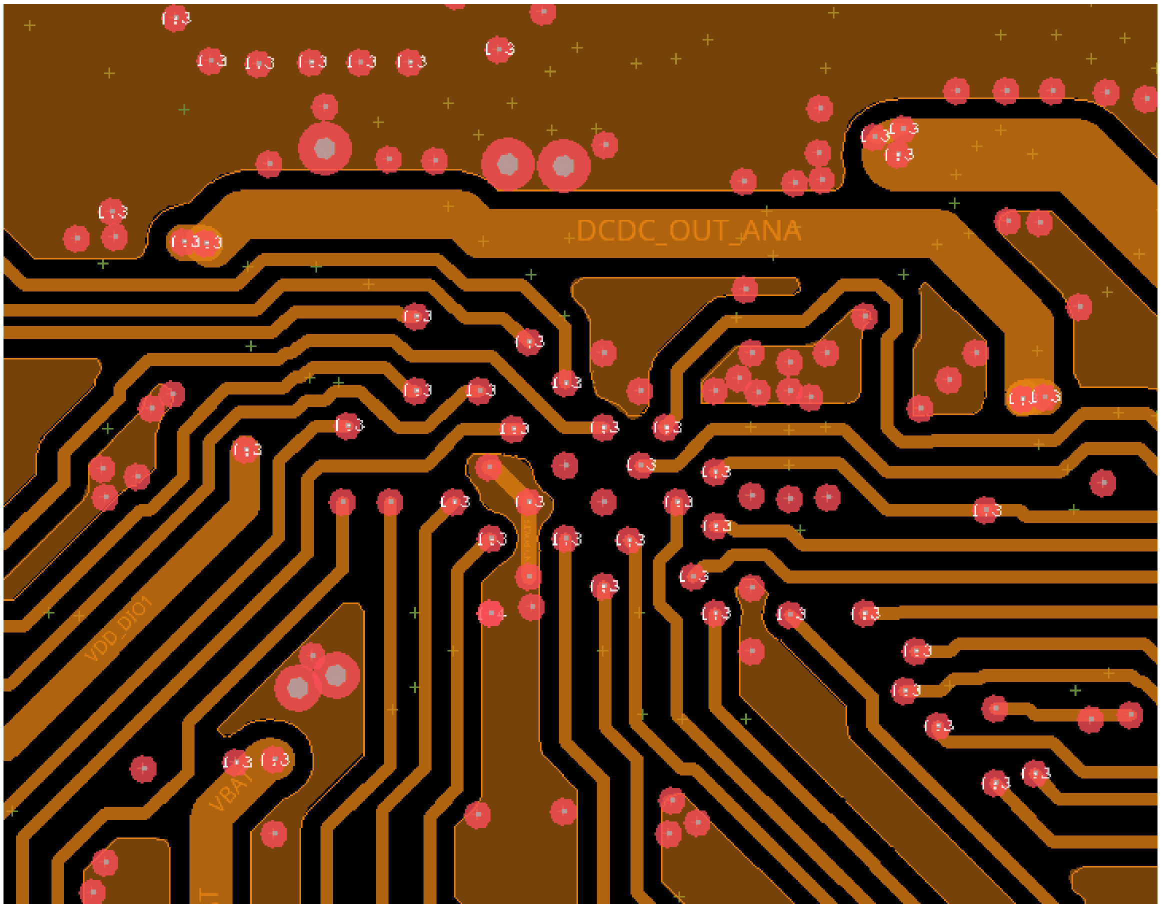

Figure 21. L3 internal layer, RA6W1 - WLCSP

- L4 bottom layer is clear from traces as much possible. This layer is used as a GND shield for EMI purposes, see Figure 22.

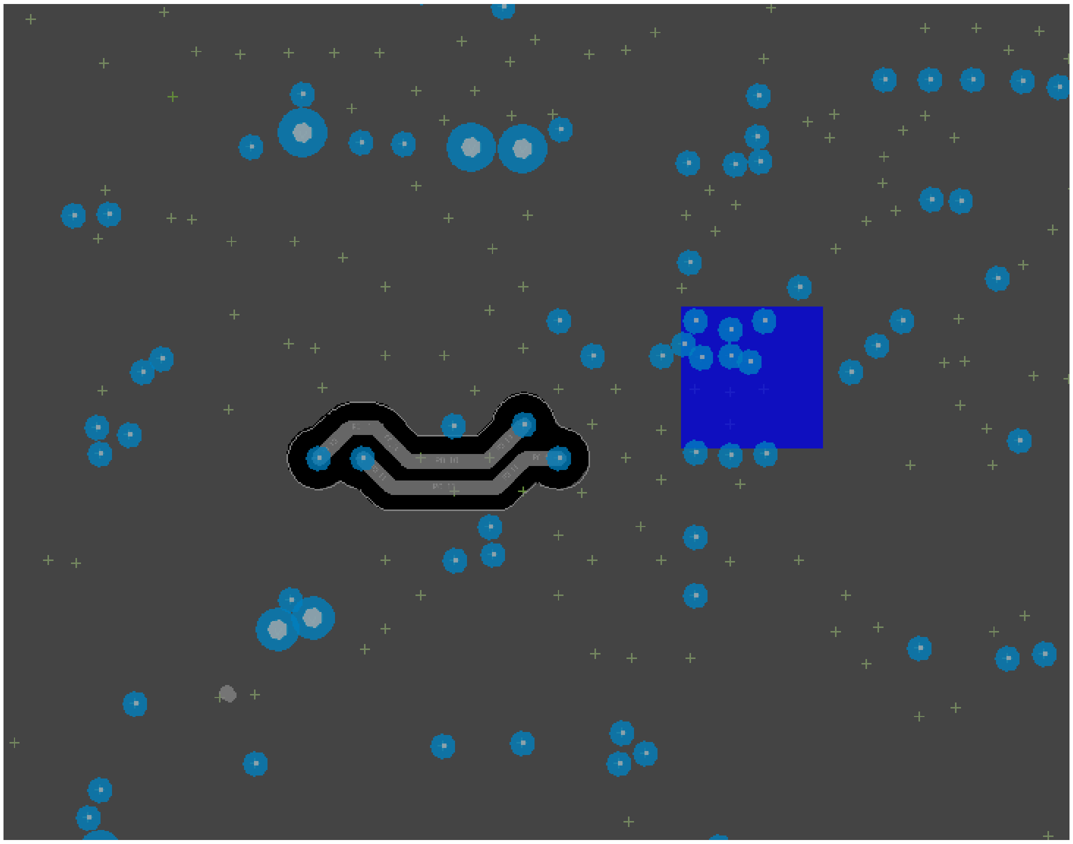

Figure 22. L4 bottom layer, RA6W1 - WLCSP

GND vias are placed on the periphery of placement area, for producing a shieled for reducing EMI.

Active components operating at high frequency should have a layout as compact as possible to prevent the cross-coupling between lines and to minimize the parasitic effects which have negative impacts on the operating parameters. Use as many vias as possible to create a solid GND under the IC itself and connect the IC to the inner GND layer. It is beneficial to system performance to provide more than one via from GND pins to the reference GND plane.

6.2 RA6W1 – QFN

PCB layout of QFN package is considered straight forward without special challenges. No microvias are required whereas, similar layers structure to WLCSP can be used. Top layer is used for components placement and routing power, RF, clock, and other digital signals. Internal layer 2 is used for reference ground.

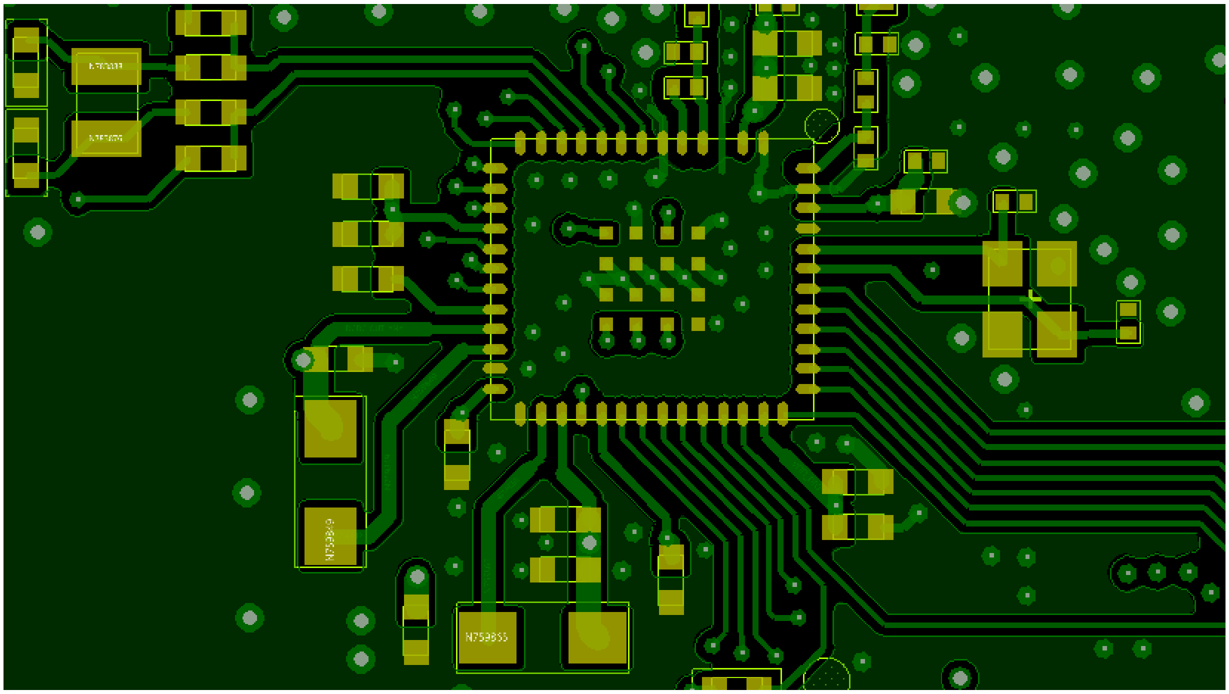

Figure 23. L1 top layer, RA6W1 - QFN

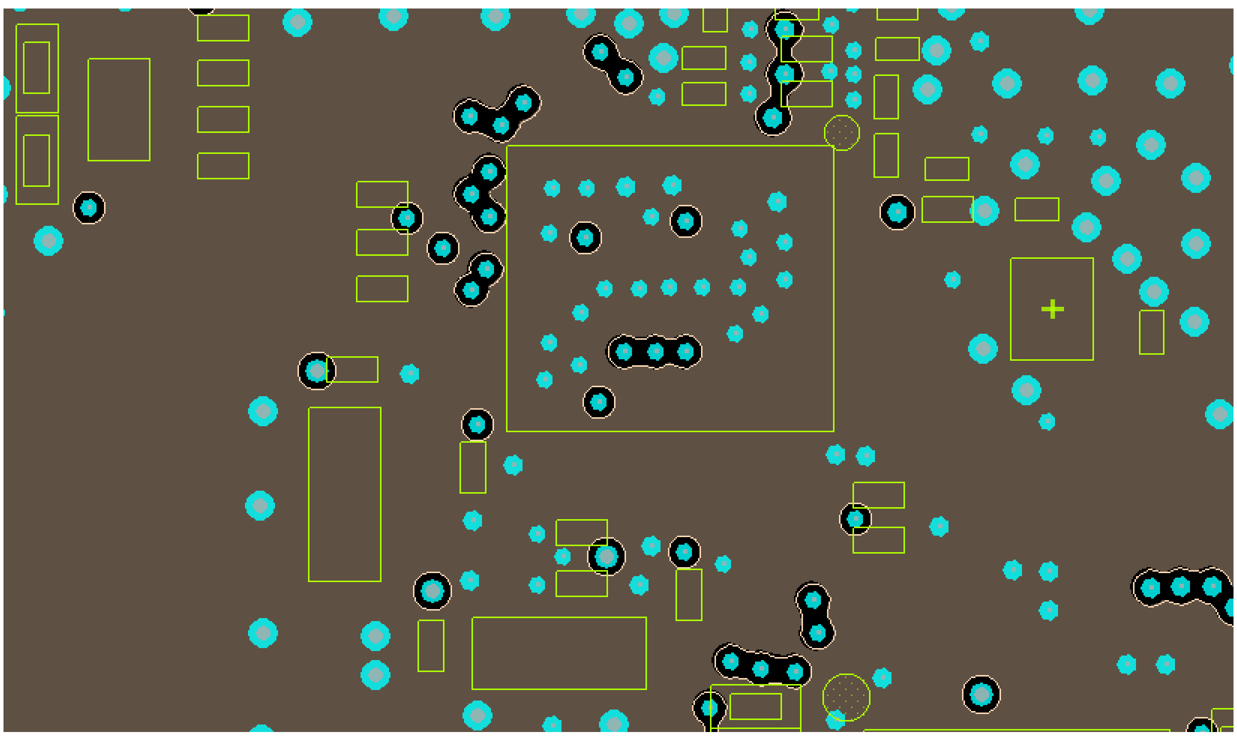

Figure 24. L2 internal layer, RA6W1 – QFN

6.3 PCB Layout Modification for GND

The PCB layout guidelines for power supply:

1. Place DCDC converters capacitors close to the chip with their GND pads oriented to chip. By this way, the noisy signals current loops are reduced, resulting to better performance.
2. Put the power inductor as close as possible to the chip. Remove grounding under the inductor to minimize any possible coupling from reference ground.

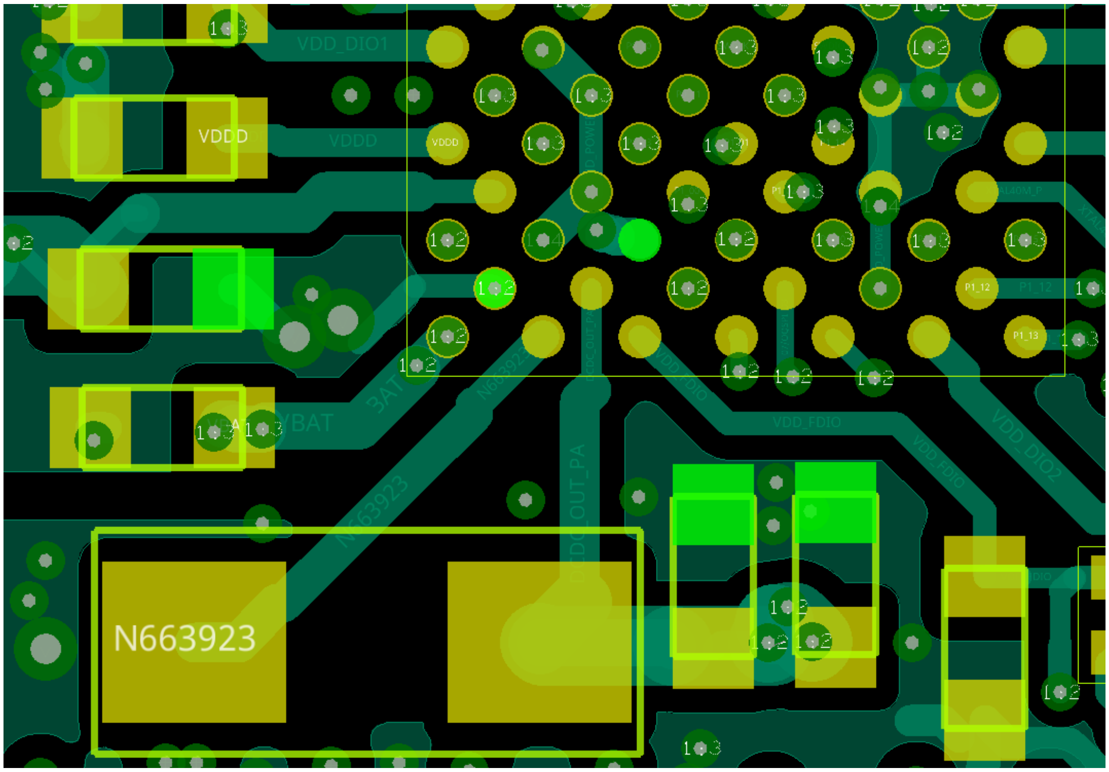

Figure 25. DCDC capacitors placement

3. Capacitors for VDDRF_PA and VDDRF must be placed closest possible to the pins.
4. Use more than one via on both sides of the power traces. Especially for VDDRF_PA, more than two vias is good practice, because the current for RF PA is of the order of several hundreds of mAmps.
5. Use widest and shortest possible traces for connecting DCDC outputs with VDDRF_PA and VDDRF. For VDDRF_PA, a 500 μm or internal layers and 400 μm wide traces is suggested. For VDDRF a 400 μm or internal layers and 300 μm wide traces are suggested . The internal layers, most of the times use thinner copper than external copper layers.

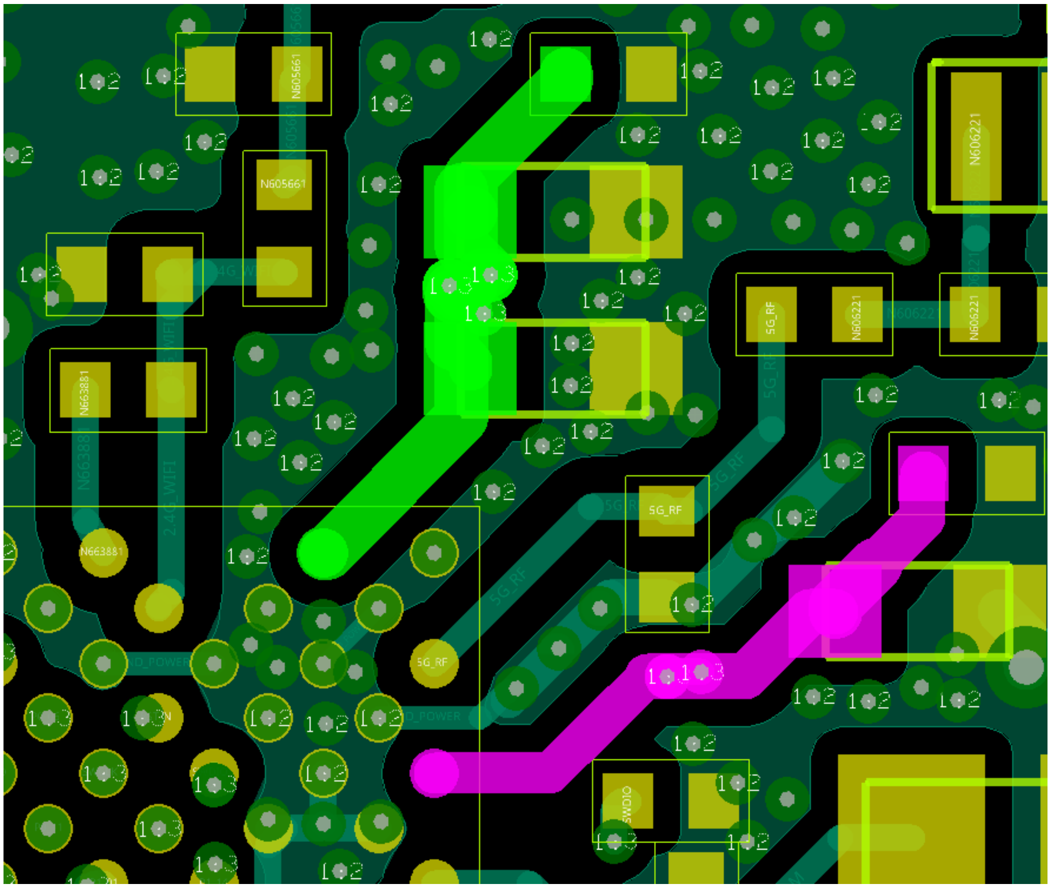

Figure 26. Components placement, vias and traces for VDDRF_PA (green) and VDDRF (purple)

6. For VDD_DIO1 and VDD_DIO2, use traces with 200-μm width.
7. Place the power vias and ground vias as close as possible to the decoupling capacitors.

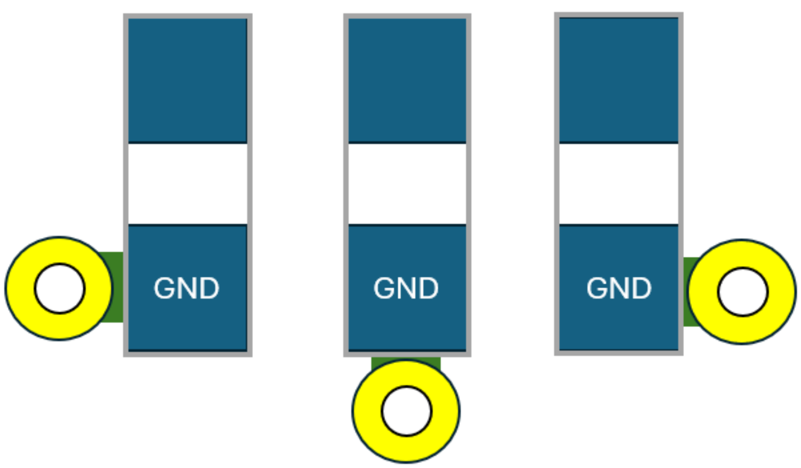

Figure 27. Recommended ground vias layout for the capacitance

6.4 PCB Layout Guidelines for Crystal

PCB layout guidelines for crystal:

1. Place XTAL as close as possible to the IC to minimize PCB parasitic capacitance on the input pins and to reduce the chance of crosstalk and interference with other signals on the board. The signals of the XTAL are not differential. Consequently, it is not necessary to be routed differentially.

2. Do not route any lines under the XTAL area – risk of coupling and interference.
3. Place the ground guard with ground stitching vias around the XTAL_IN and XTAL_OUT traces.
4. Place the crystal close to the device and keep it as far away as possible from the RF side of the device and high frequency digital signal traces such as SDIO or QSPI.

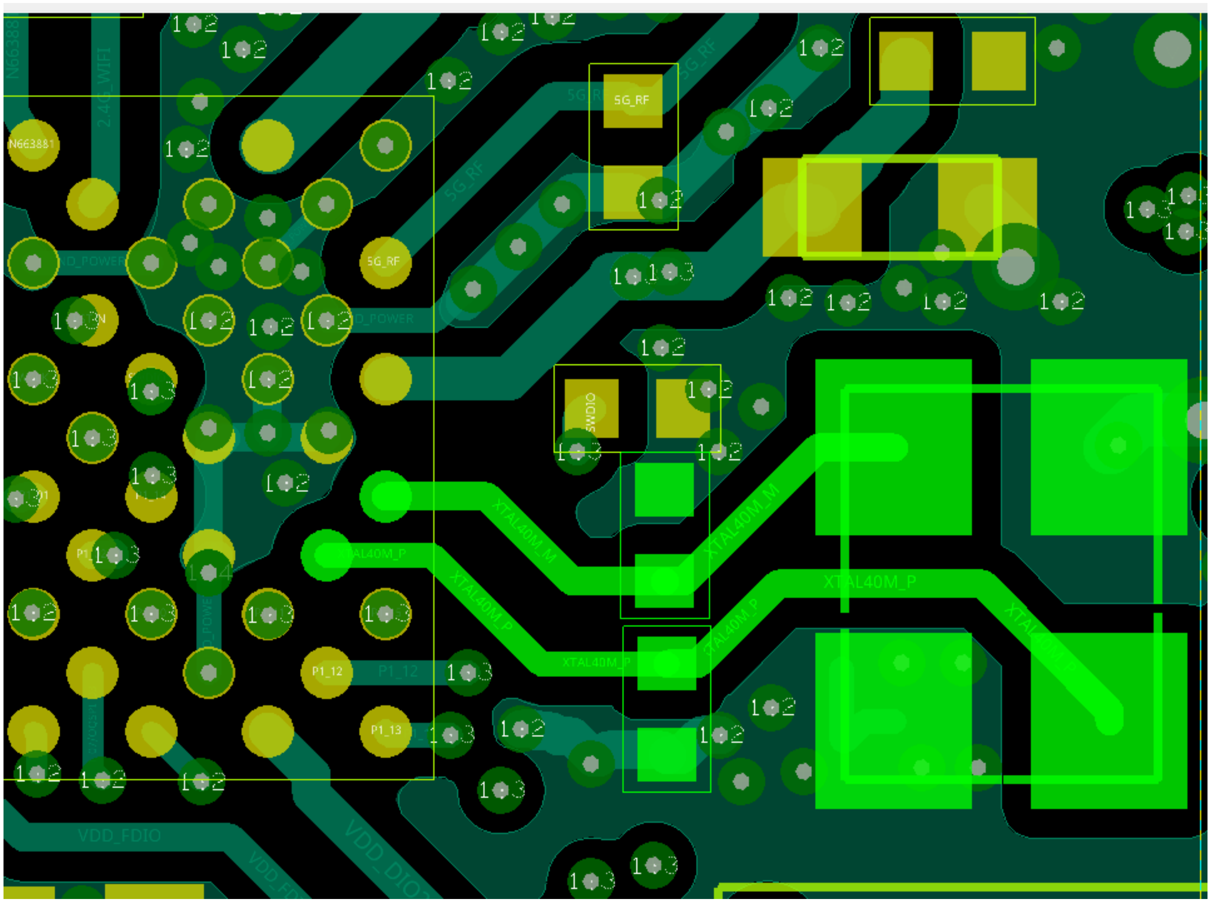

Figure 28. PCB placement and routing of the 40-MHz XTAL circuit

6.5 RF Specific Guidelines

The PCB layout guidelines for RF interface:

1. The inductor connected to RFTX_2G and RFRX_2G pins is a part of the RF circuit and it must be placed closest possible to the chip.

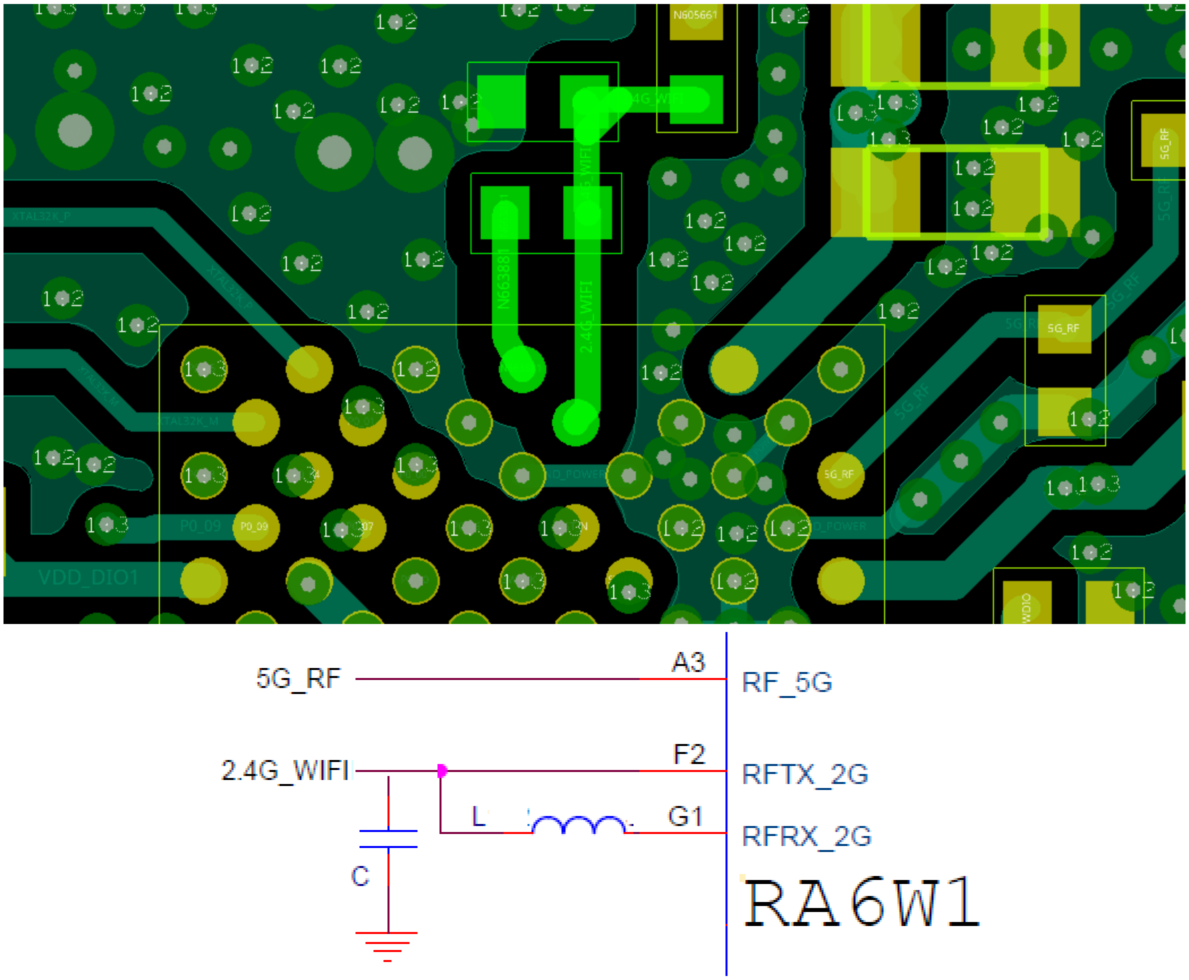

Figure 29. Placement of LC circuit close to RF pins

2. Route the RF signals on the top layer with 50-Ω impedance. A good PCB design practice is to have controlled impedance of the routed traces. It is important to properly route the RF strip line to the antenna.
3. Reference the RF signals to a solid ground plane. Apply multiple vias and add GND stitching vias to increase the performance of the system, as shown in Figure 30.
4. Keep the high-speed control signal traces as far away as possible from the RF traces.
5. Add ground vias close to the RF front-end components pins for a good return path.
6. The RF trace must present impedance equal to 50 Ω. Impedance depends on:
   a. The physical dimension of the RF trace
   b. The distance between RF Trace and GND planes located under and along the track.
   c. Dielectric constant of the PCB material.

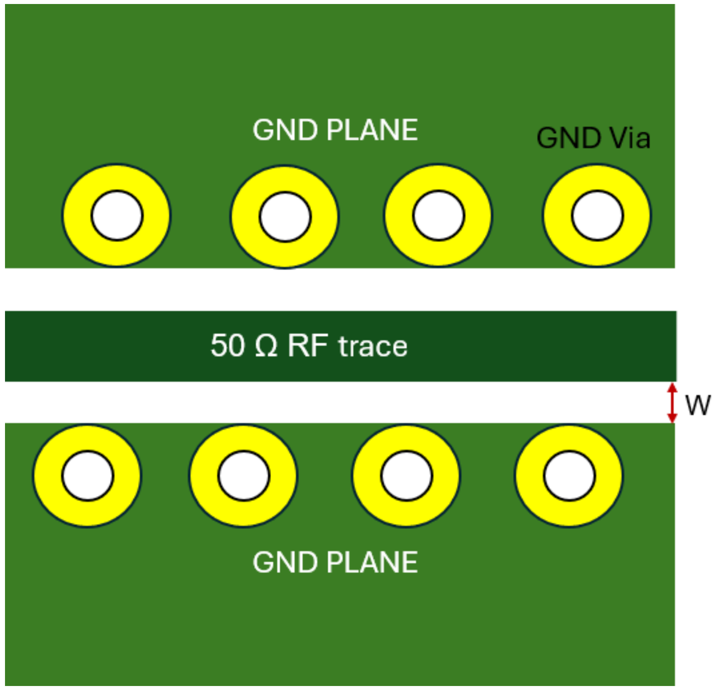

Figure 30. Ground with stitching vias

7. The RF bend trace routing should be smooth with a large radius rather than 90 degrees with a sharp edge, as shown in Figure 31.

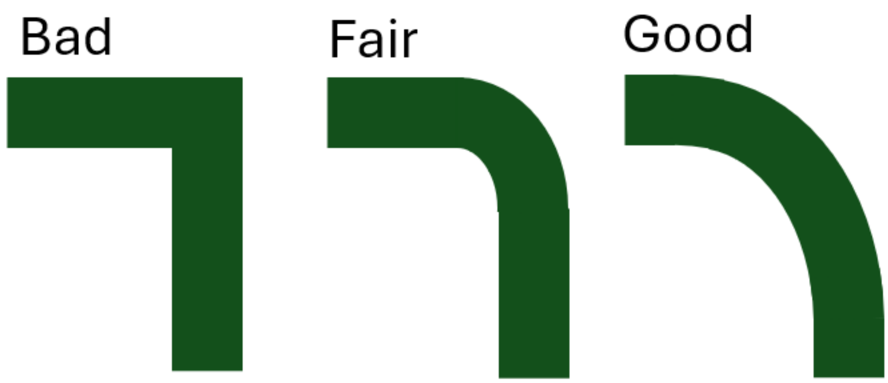

Figure 31. Example of RF trace routing

8. Minimize the stubs routing of the configuration straps to the chip lines. Where branched routing is used, minimize the length of the stub. Place the configuration strap resistor in the path or the routed trace where possible (close to the chip). See Figure 32.

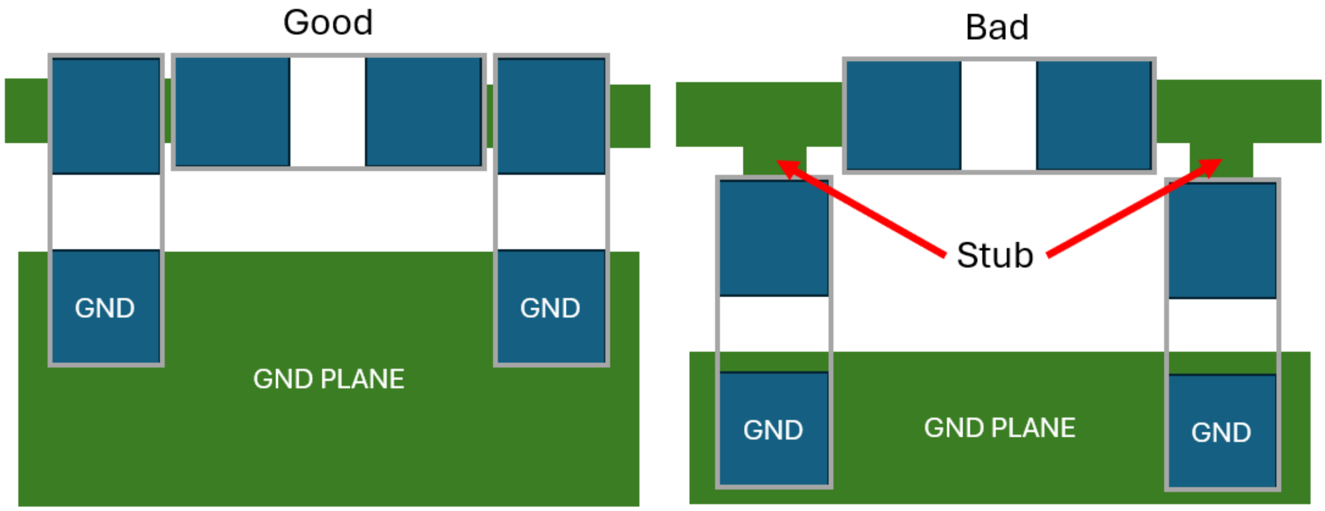

Figure 32. Recommended layout for minimizing the length of the stub

9. RF trace to RF connector pad transition must be tapered to avoid discontinuity and high insertion loss, especially at 5-GHz band.

6.5.1 Antenna Considerations

Figure 33 shows an example of an SMA antenna. Antenna hasthe following general characteristics:

- Polarization: it is the orientation of the electric field of the radio wave (vertical, horizontal, circular, or elliptical)
- Impedance: This is the antenna's resistance to the flow of electrical current at its feed point, crucial for matching with the transmission line.
- Antenna VSWR (Voltage Standing Wave Ratio): it measures impedance matching.
- Gain: it shows the antenna's ability to increase radiated power, often expressed in decibels relative to an isotropic source (dBi). It is defined either as peak or average gain.

These characteristics refer to a specific setup (size of PCB, no enclosures, no obstacles and so on.) of the antenna. The setup is critical for printed antennas and ceramic antennas. For example, the size of the reference board where antenna characteristics are measured, are different to final product. Consequently, provisions for antenna matching must be added on the final design whereas the antenna performance must be verified.

For certification purposes and specifically radiated measurements, the peak antenna gain is significant because it is added on transmitted RF power. Often conducted RF TX power must be reduced for meeting the certification requirements.

RFA-27-H60-GB70-G020

Specifications

Frequency	2400-2500 MHz	4900-5975 MHz	6000-7125 MHz
Peak gain	3.3 dBi	4.4 dBi	4.1 dBi
Average gain	1.7 dBi	1.9 dBi	1.6 dBi
VSWR	2.0 : 1 Max.	2.5 : 1 Max.	2.5 : 1 Max.
Polarization	Linear, vertical		
Impedance	50 Ω		
Connector	SMA PLUG		

Environment & Mechanical Characteristics

Temperature	- 10℃ to +55℃
Humidity	95% @ 25℃

Figure 33. Example of a SMA Wi-Fi 6 antenna

For adding an antenna (external or PCB printed antenna) apply following considerations, see Figure 34:

- Antenna must present impedance of 50 Ω.
- Do not place metal layers in the antenna area. The antenna footprint must be kept free of metal.
- Do not place metal screws, heatsink, any metal, and so on. Validate the antenna radiation pattern if any metal close to antenna.
- Do not use metal enclosures for products with antennas. Metal enclosures prevent the antenna from radiating and performing as intended.
- Use a pi-network, closest possible to the antenna, for matching purposes.

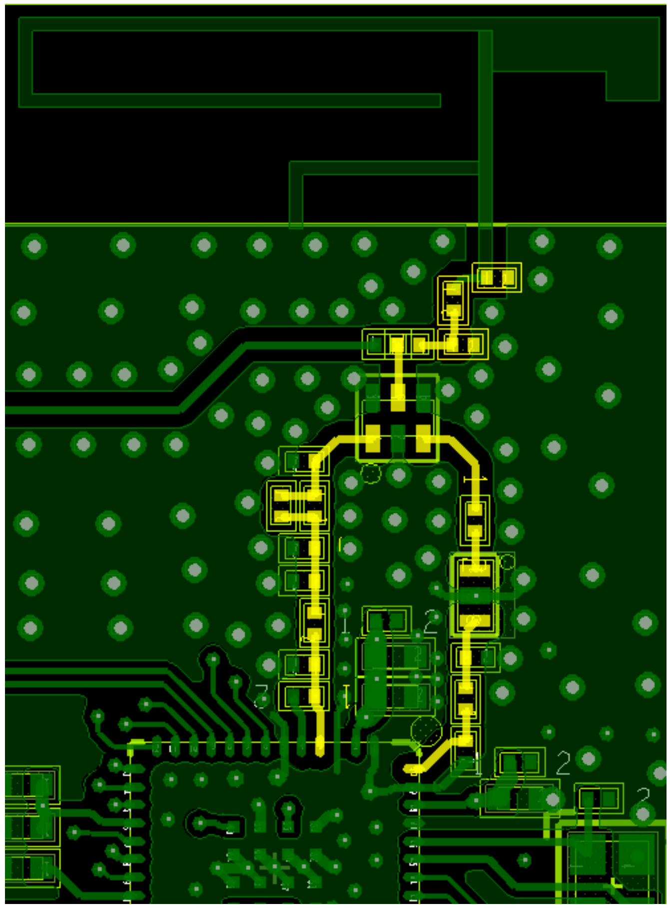

Figure 34. RF Front end and antenna for RA6W1-QFN

6.6 PCB Layout Guidelines for SDIO Interface

The PCB layout guidelines for SDIO:

1. Design SDIO signals with trace impedance of 50 Ω.
2. Keep same trace length for all SDIO signals and as short as possible.
3. Keep SDIO traces away from Radio or other noise sensitive parts of the system.

7. Revision History

Revision	Date	Description
1.01	Dec 17, 2025	Updated PCB layout, XTAL, Power supplies, GPIOs, RSTn, RF sections
1.00	Oct 24, 2024	First version.

CorporateHeadquarters

TOYOSU FORESIA, 3-2-24 Toyosu
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/