

RL78/G24

Timer RG2 Buffer Operation in PWM Mode

Introduction

This application note explains a method to output a PWM waveform using buffer operation in PWM mode of RL78/G24 Timer RG2.

Target Device

RL78/G24

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications	3
1.1 Specification overview	3
1.2 Operation overview	4
1.3 Explanation of Duty Change Processing	5
1.3.1 Duty Cycle Changes from Initial output to Duty 90%	5
1.3.2 Duty Cycle Change from 90% to 80%... to 10%, or 10% to 20%... to 90%	7
1.3.3 Duty Cycle Change from 10% to 0%	9
1.4 Duty Cycle Change from 0% to 10%	11
1.4.1 (Reference information) 100% Duty Cycle Output	13
2. Operation Confirmation Conditions	15
3. Hardware Description	16
3.1 Example of Hardware Configuration	16
3.2 List of used Pins	16
4. Software Description	17
4.1 Smart Configurator Settings	17
4.1.1 System Configuration	17
4.1.2 Component Configurations	19
4.2 Folder Structure	20
4.3 List of Option Byte Settings	21
4.4 List of Constants	21
4.5 List of Global Variables	22
4.6 List of Functions	22
4.7 Function Specifications	23
4.8 Flowchart	24
4.8.1 Main Process	24
4.8.2 R_Config_TRG_Create_UserInit Function	24
4.8.3 r_Config_TRG_interrupt function	25
5. Sample Code	26
6. Reference Documents	26
Revision History	27

1. Specifications

1.1 Specification overview

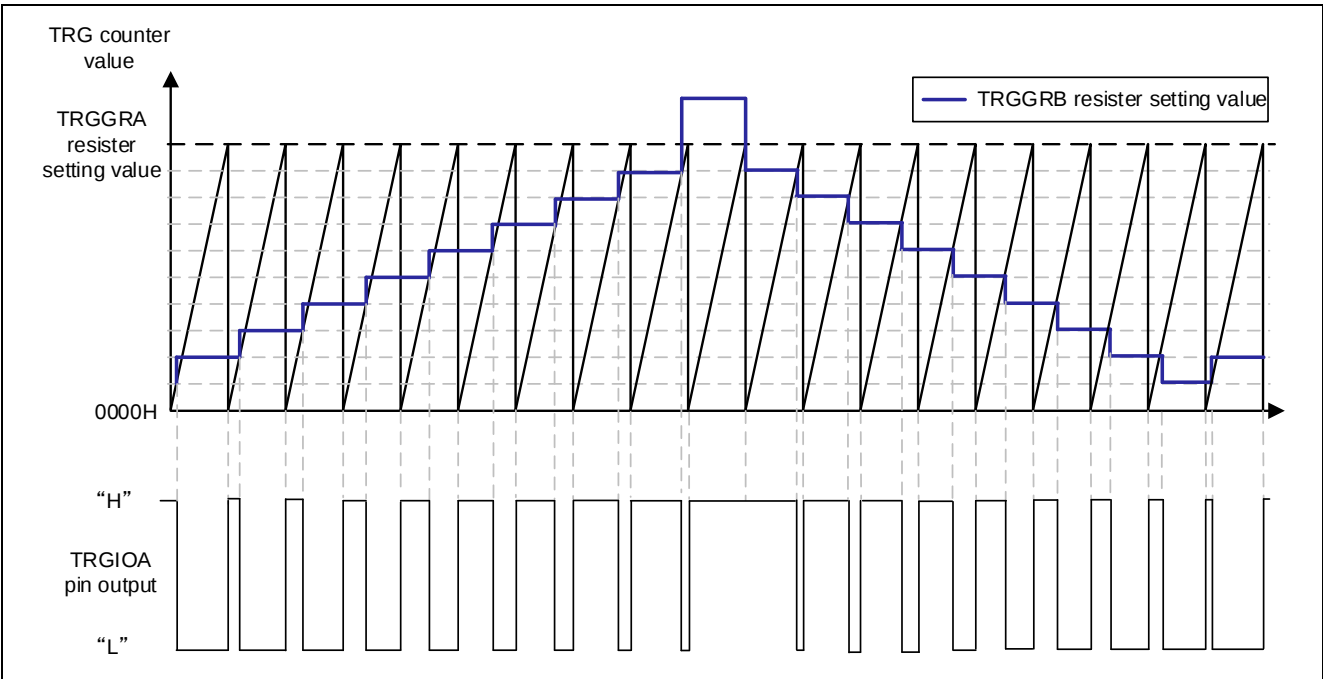
A PWM waveform with a 100μs period is output. The PWM waveform changes its duty each time the predetermined period elapses. In this application note, the active level is defined as "low" and the inactive level as "high".

Table 1-1 lists the peripheral functions and their purposes, and Figure 1-1 shows the output waveform of the PWM.

Table 1-1 Peripheral Functions and Their Usage

Peripheral	Usage
Timer RG2	PWM output

Figure 1-1 Output Waveform of PWM



1.2 Operation overview

Using PWM mode, a PWM waveform with a 100 μ s period is output from the TRG10A terminal. The duty of the PWM waveform changes sequentially: 90% -> 80% -> ... -> 10% -> 0% -> 10% -> ... -> 90% with each cycle. The duty change is triggered by the TRGGRA compare match interrupt (INTTRG).

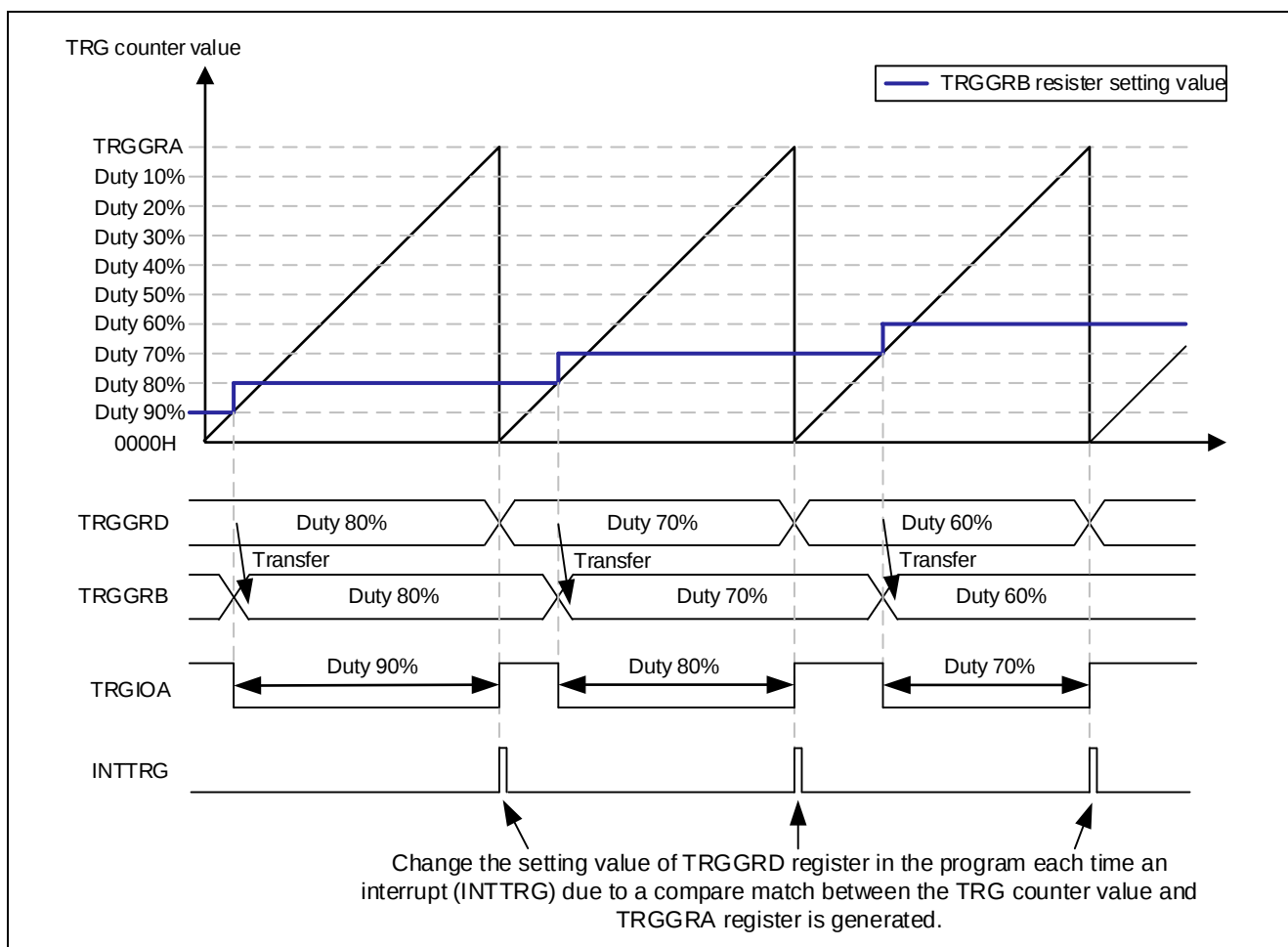
The settings are as follows:

<Settings>

- Timer RG2's count source uses fCLK (48MHz).
- The TRG counter is cleared by a compare match with the TRGGRA register.
- The TRGGRD register is used as the TRGGRB buffer register.
- The TRGGRC register is not used as the TRGGRA buffer register.
- The TRGGRA compare match interrupt (INTTRG) is utilized.

Figure 1-2 shows the buffer operation and the rewrite timing of the buffer register (TRGGRD).

Figure 1-2 Buffer operation and rewrite timing of the buffer register (TRGGRD)



1.3 Explanation of Duty Change Processing

In this section, we will explain the hardware operation and software processing during duty change, divided into several scenarios.

Additionally, the PWM cycle is commonly set to 100 [μs].

When the PWM cycle is 100 [μs], the value of the TRGGRA register is 4799, as derived from the equation below:

$$100 \text{ } [\mu\text{s}] = (1 / 48 \text{ [MHz]}) \times (\text{TRGGRA} + 1)$$

$$= 20.83 \text{ [ns]} \times (4799 + 1)$$

Table 1-2 Timing of Initial Output to 90% Duty Output

	Hardware Processing	Software Processing
Initial Setting	—	- Set the TRG counter clear condition to match the TRGGRA register. - Set the TRGGRA register (m1). - Set the TRGGRB register (m2). - Set the TRGGRD register (m3).
	Output the initial state "H" from the TRGIOA pin.	Set the operation mode to PWM mode.
	Start the counter of the Timer RG2.	Start the counter of Timer RG2.
(a)	- TRG counter matches the TRGGRB register (m2). - Transfer the TRGGRD register (m3) to the TRGGRB register. - Output "L" from the TRGIOA pin.	—
(b)	- The value of the TRG counter matches the value of the TRGGRA register (m1). - Clear the TRG counter to "0000H". - Output "H" from the TRGIOA pin.	Set the TRGGRD register (m4).

1.3.2 Duty Cycle Change from 90% to 80%... to 10%, or 10% to 20%... to 90%

Active Level L: $(100 - N) [\mu s] = (1 / 48 [\text{MHz}]) \times (\text{TRGGRB} - M)$

Inactive Level H: $N [\mu s] = (1 / 48 [\text{MHz}]) \times (\text{TRGGRB} + 1)$
 $= 20.83 [\text{ns}] \times (M + 1)$

Table 1-3 shows duty cycle and the TRGGRB register setting values.

Table 1-3 Duty Cycle and the TRGGRB Register Setting Values

Duty (%)	90	80	70	60	50	40	30	20	10
Inactive level H (N [μs])	10	20	30	40	50	60	70	80	90
TRGGRB register setting value (M)	479	959	1439	1919	2399	2879	3359	3839	4319

Figure 1-4 Table 1-4 shows the operation during the output settings from XX% duty to YY% duty (XX, YY: 10 to 90).

Figure 1-4 Output timing from XX% duty to YY% duty (XX, YY: 10 to 90)

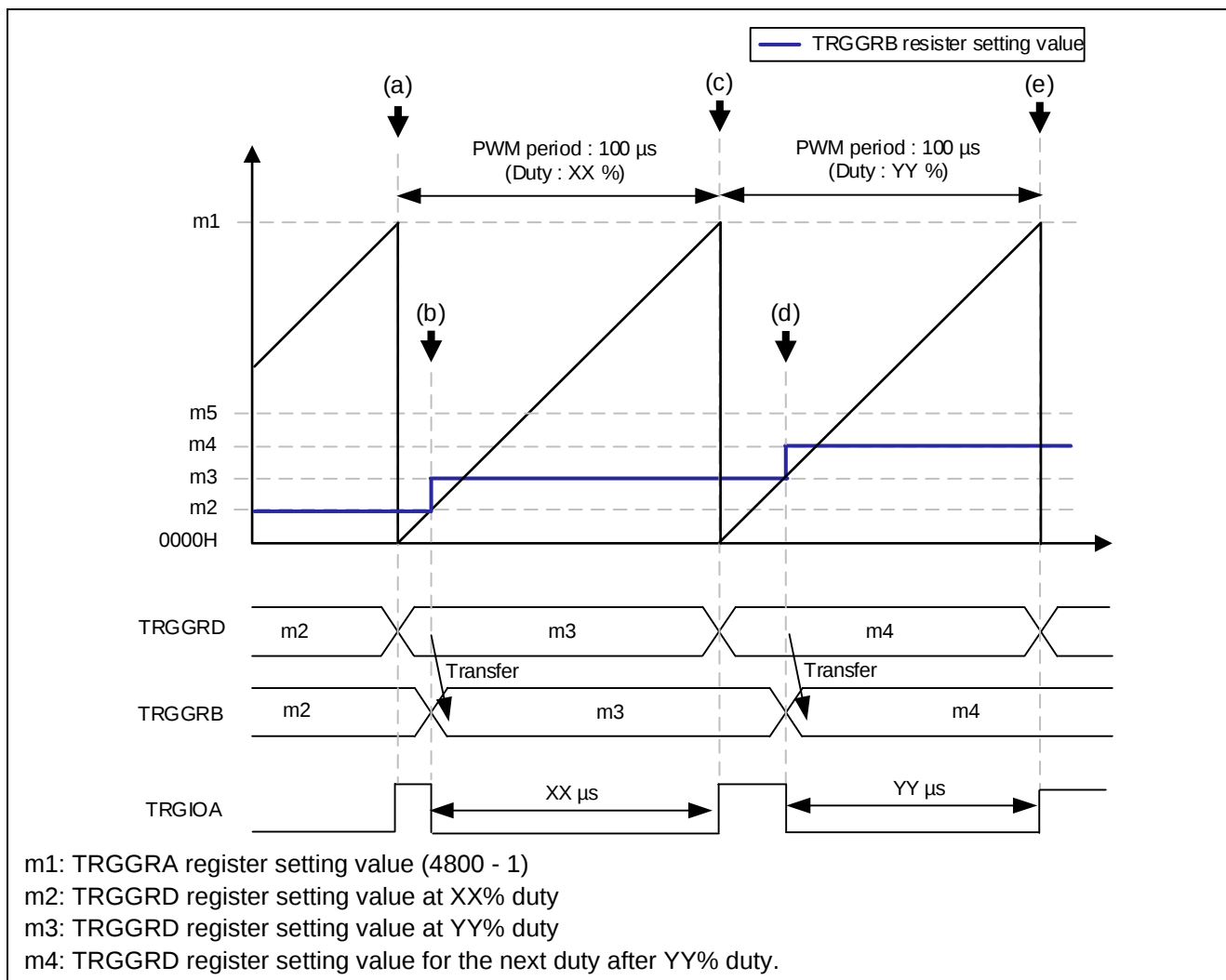


Table 1-4 Output timing from XX% duty to YY% duty (XX, YY: 10 to 90)

	Hardware Processing	Software Processing
(a)	• TRG counter matches TRGGRA register (m1) • TRG counter is cleared to "0000H". • Output "H" from TRGIOA pin	• Set TRGGRD register (m3)
(b)	• TRG counter matches TRGGRB register (m2) • Transfer TRGGRD register (m3) to TRGGRB register. • Output "L" from TRGIOA pin	—
(c)	• TRG counter matches TRGGRA register (m1) • TRG counter is cleared to "0000H". • Output "H" from TRGIOA pin	• Set TRGGRD register (m4)
(d)	• TRG counter matches TRGGRB register (m3) • Transfer TRGGRD register (m4) to TRGGRB register. • Output "L" from TRGIOA pin	—
(e)	• TRG counter matches TRGGRA register (m1) • TRG counter is cleared to "0000H". • Output "H" from TRGIOA pin.	• Set TRGGRD register (m5)

1.3.3 Duty Cycle Change from 10% to 0%

$$\begin{aligned}\text{Active level L: } 10 [\mu\text{s}] &= (1 / 48 [\text{MHz}]) \times (\text{TRGGRA} - \text{TRGGRB}) \\ &= 20.83 [\text{ns}] \times 480\end{aligned}$$

$$\begin{aligned}\text{Inactive level H: } 90 [\mu\text{s}] &= 1/48\text{MHz} \times (\text{TRGGRB} + 1) \\ &= 20.83 [\text{ns}] \times (4319 + 1)\end{aligned}$$

Figure 1-5, Table 1-5 shows the operation when the duty cycle is set from 10% to 0%.

Figure 1-5 Output timing when the duty cycle is set from 10% to 0%

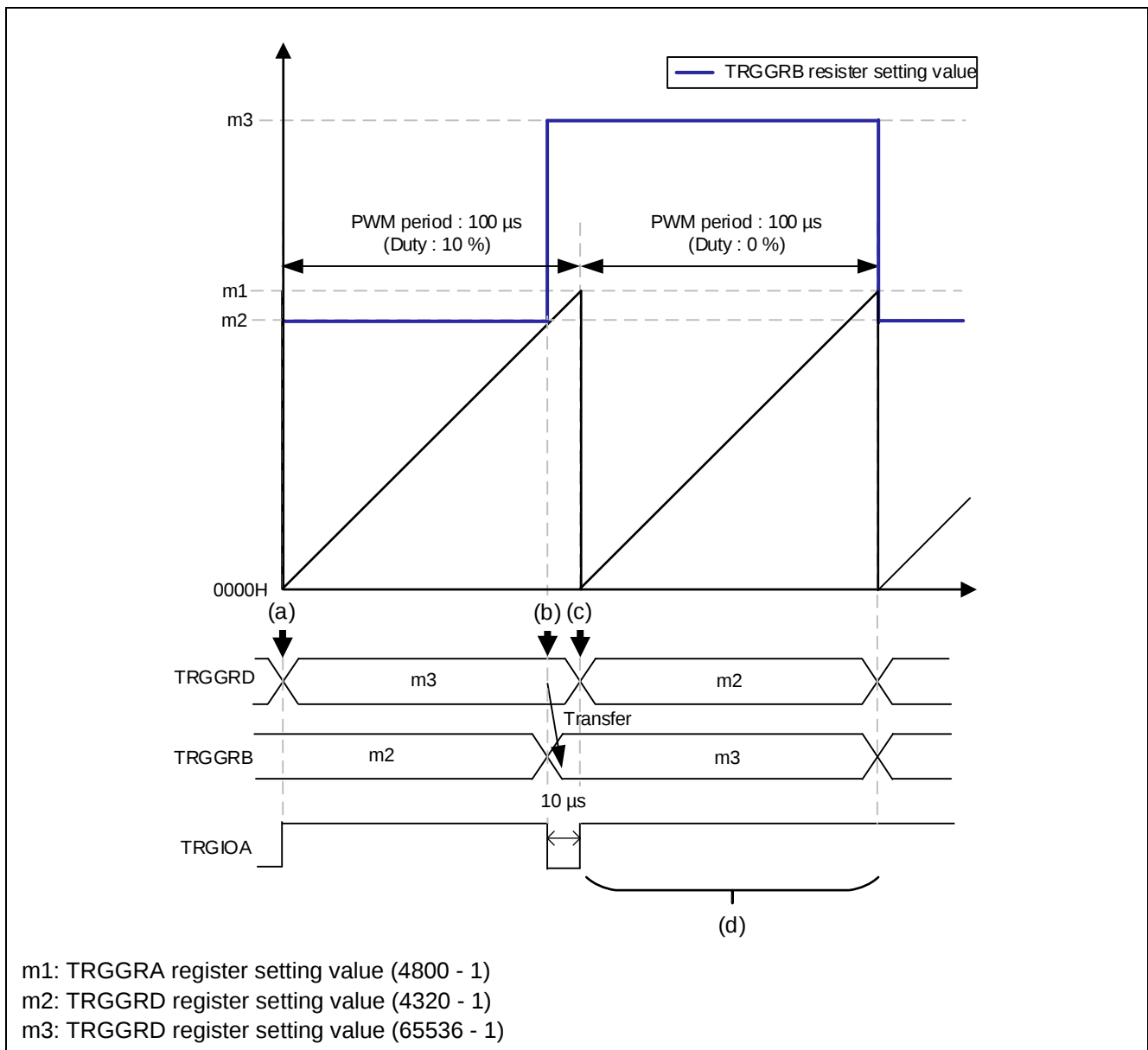


Table 1-5 Output timing when the duty cycle is set from 10% to 0%

	Hardware Processing	Software Processing
(a)	• TRG counter matches TRGGRA register (m1) • TRG counter clears to "0000H" • Output "H" from TRGIOA pin	• Set TRGGRD register (m3)
(b)	• TRG counter matches TRGGRB register (m2) • Transfer TRGGRD register (m3) value to TRGGRB register. • Output "L" from TRGIOA pin	—
(c)	• TRG counter matches TRGGRA register (m1) • TRG counter clears to "0000H" • Output "H" from TRGIOA pin	• Set TRGGRD register (m2)
(d)	• No match between TRG counter and TRGGRB register (m3) • No change in TRGIOA pin output.^{NOTE 1}	—

NOTE 1. If a value exceeding the TRGGRA register is set in the TRGGRB register, the TRG counter will never match the TRGGRB register, resulting in a duty cycle of 0%.

1.4 Duty Cycle Change from 0% to 10%

$$\begin{aligned}\text{Active level L: } 10 [\mu\text{s}] &= (1 / 48 [\text{MHz}]) \times (\text{TRGGRA} - \text{TRGGRB}) \\ &= 20.83 [\text{ns}] \times 480\end{aligned}$$

$$\begin{aligned}\text{Inactive level H: } 90 [\mu\text{s}] &= (1 / 48 [\text{MHz}]) \times (\text{TRGGRB} + 1) \\ &= 20.83 [\text{ns}] \times (4319 + 1)\end{aligned}$$

Figure 1-6, Table 1-6 shows the operation when the duty cycle is set from 0% to 10%.

Figure 1-6 Output Timing When the Duty Cycle is Set from 0% to 10%

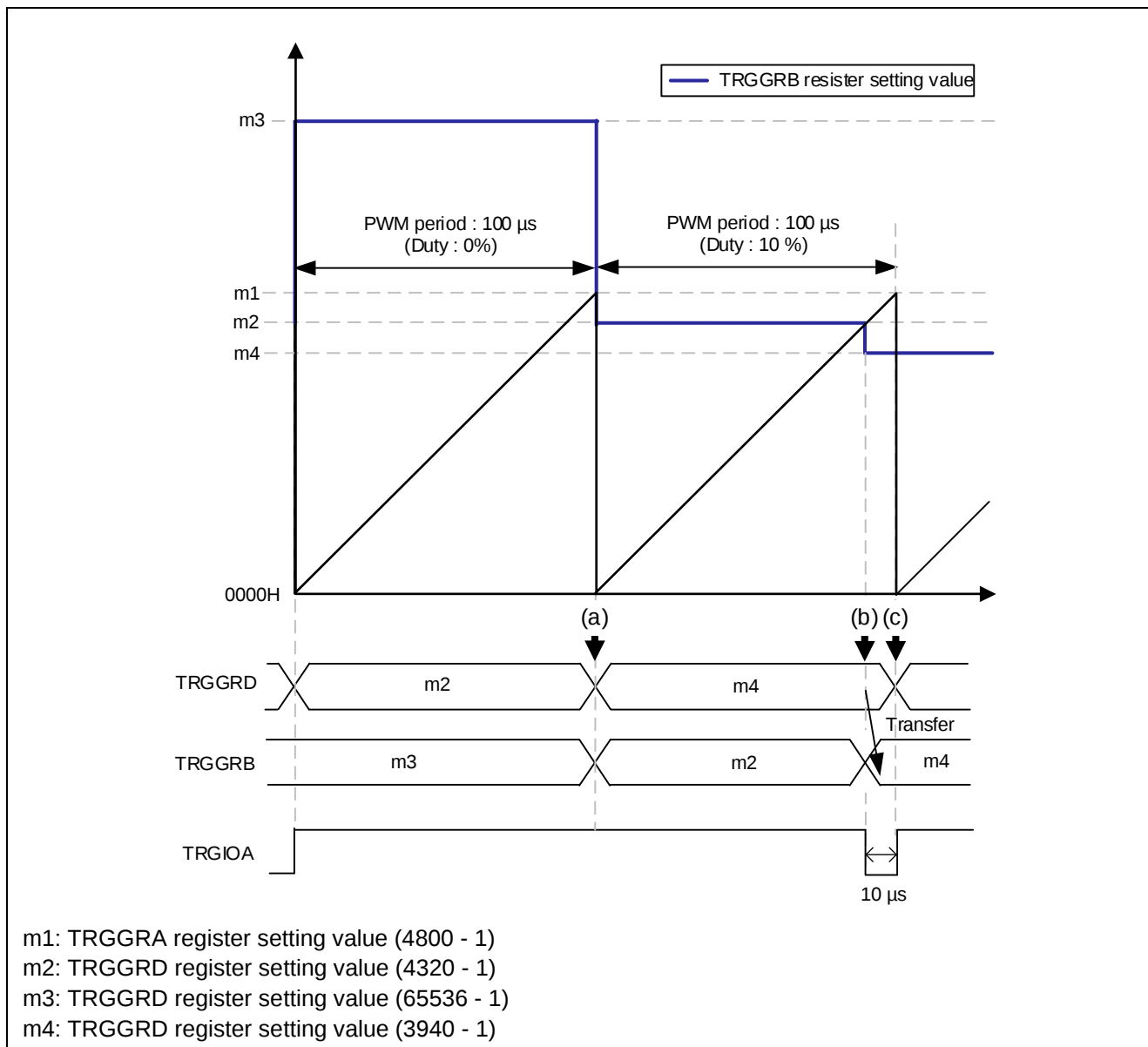


Table 1-6 Output Timing When the Duty Cycle is Set from 0% to 10%

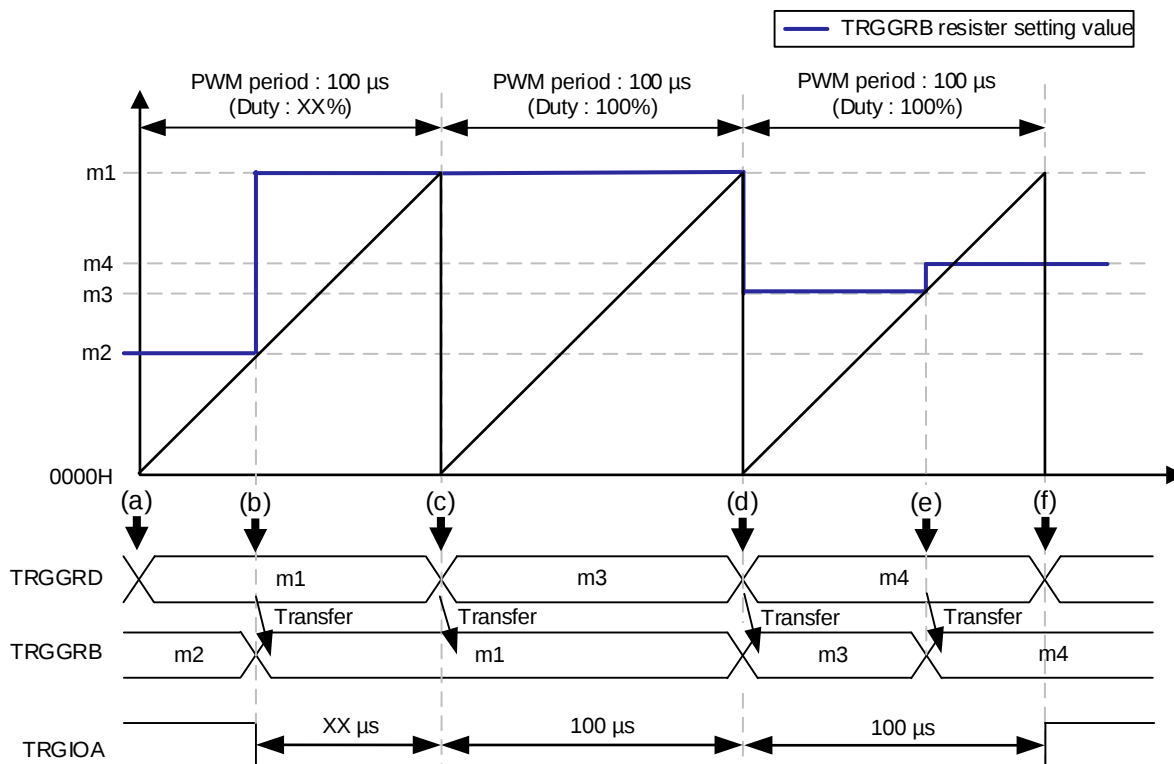
	Hardware Processing	Software Processing
(a)	—	- Set TRGGRB register (m2). ^{NOTE 1} - Set TRGGRD register (m4). ^{NOTE 1}
(b)	- TRG counter matches with TRGGRB register (m2) - Transfer TRGGRD register (m4) to TRGGRB register. - Output "L" from TRGIOA pin	—
(c)	- TRG counter matches with TRGGRA register (m1) - Clear TRG counter to "0000H" - Output "H" from TRGIOA pin	Set TRGGRD register

NOTE 1: When duty cycle is 0%, the TRG counter value will never match the TRGGRB register value, so no buffer transfer occurs. To change the duty cycle from 0%, you need to programmatically write values to the TRGGRD and TRGGRB registers.

1.4.1 (Reference information) 100% Duty Cycle Output

Although not utilized in this application note, it is possible to output a 100% duty cycle by setting the value of the TRGGRB register to the same as the value of the TRGGRA register. The timing chart of the PWM waveform output from the TRGIOA pin is shown in the following **Figure 1-7** and **Table 1-7**.

Figure 1-7 Output Timing When the Duty Cycle is set to 100%



m1: Setting value for TRGGRA and TRGGRB registers (4800 - 1)

m2: TRGGRD register setting value at duty XX%

m3: TRGGRD register setting value following m1

m4: TRGGRD register setting value following m3

Table 1-7 Output Timing When the Duty Cycle is set to 100%

	Hardware Processing	Software Processing
(a)	- The TRG counter matches the TRGGRA register (m1). - The TRG counter clears to "0000H". - The TRGIOA pin outputs "H".	Set the TRGGRD register (m1)
(b)	- The TRG counter matches the TRGGRB register (m2). - The TRGGRD (m1) register is transferred to the TRGGRB register. - The TRGIOA pin outputs "L".	—
(c)	- The TRG counter matches both the TRGGRA register and the TRGGRB register (m1). NOTE 1 - The TRG counter clears to "0000H". - The TRGGRD (m1) register is transferred to the TRGGRB register.	Set the TRGGRD register (m3)
(d)	- The TRG counter matches both the TRGGRA register and the TRGGRB register (m1). NOTE 1 - The TRG counter clears to "0000H". - The TRGGRD (m3) register is transferred to the TRGGRB register.	Set the TRGGRD register (m4)
(e)	- The TRG counter matches the TRGGRB register (m3). - The TRGGRD (m4) register is transferred to the TRGGRB register.	—
(f)	- The TRG counter matches the TRGGRA register (m1). - The TRG counter clears to "0000H". - The TRGIOA pin outputs "H".	Set the TRGGRD register

NOTE 1. When the value of the TRGGRB register and the TRGGRA register are the same, even if the TRG counter value matches the TRGGRB register value, the output value does not change.

2. Operation Confirmation Conditions

The sample code described in this application note has been confirmed under the following conditions.

Table 2-1 Operation Confirmation Conditions

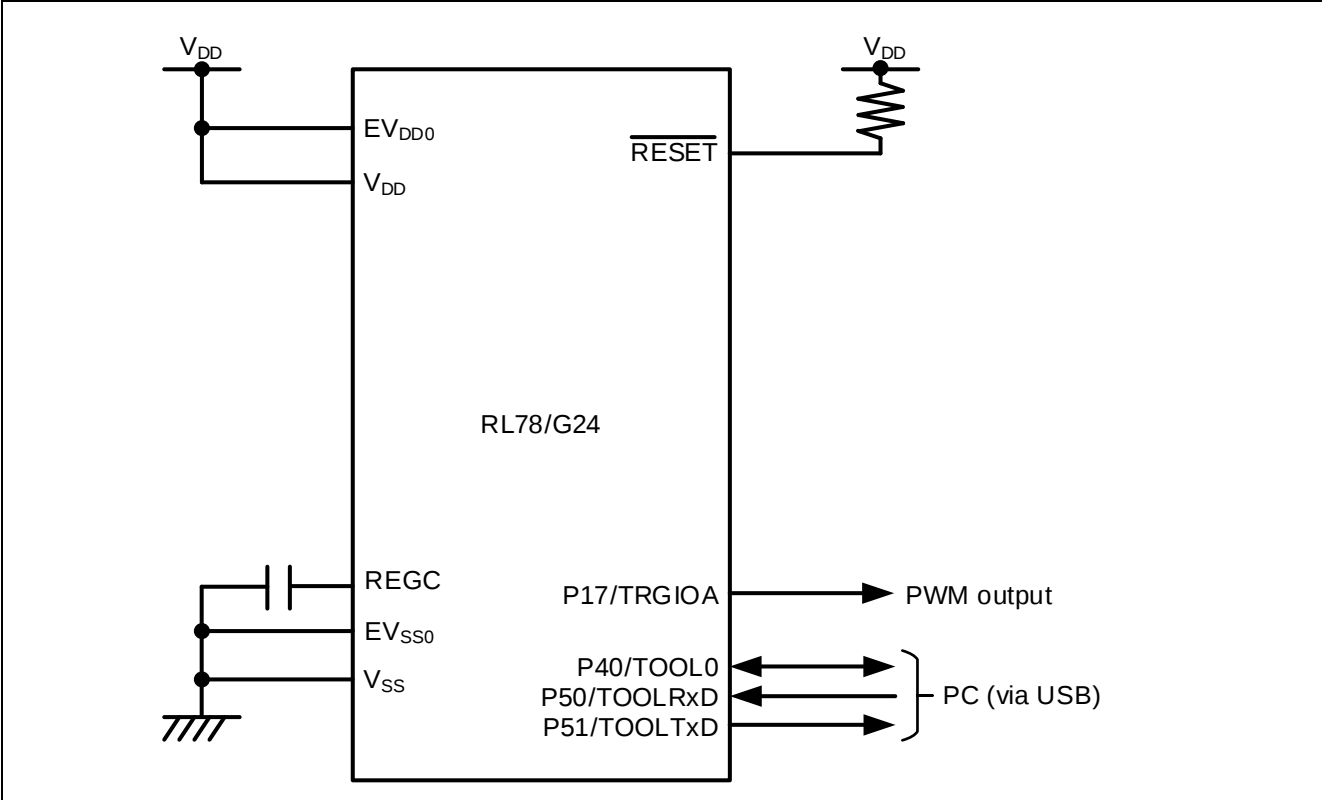
Item	Description
MCU used	RL78/G24 (R7F101GLG)
Operating frequency	- High-Speed On-Chip Oscillator Clock (fHOCO): 8MHz - PLL Oscillator Circuit Output (fPLL): 96MHz - CPU/Peripheral Hardware Clock (fCLK): 48MHz
Operating voltage	3.3V (Can operate between 2.7V to 5.5V) - LVD0 Operation (VLVD0): Reset Mode - Rising edge = 2.97V - Falling edge = 2.91V
Integrated development environment (CS+)	CS+ for CC V8.10.00 Manufactured by Renesas Electronics
C compiler (CS+)	CC-RL V1.12.01 Manufactured by Renesas Electronics
Integrated development environment (e ² studio)	e ² studio 2023-07 (23.7.0) Manufactured by Renesas Electronics
C compiler (e ² studio)	CC-RL V1.12.00 Manufactured by Renesas Electronics
Integrated development Environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.1 Manufactured by IAR Systems
C compiler (IAR)	
Smart Configurator	V.1.7.0
Board Support Package (r_bsp)	V.1.60
Emulator	CS+, e ² studio: COM port IAR: E2 Emulator Lite
Board used	RL78/G24 Fast Prototyping Board (RTK7RLG240C00000BJ)

3. Hardware Description

3.1 Example of Hardware Configuration

Figure 3-1 shows the hardware configuration example used in the sample code for this application.

Figure 3-1 Example of Hardware Configuration



Note 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes appropriate pin handling and meets electrical characteristic requirements (connect each input-only port to VDD or VSS through a resistor).

Note 2. Connect any pins whose name begins with EVSS to VSS, and any pins whose name begins with EVDD to VDD, respectively.

Note 3. VDD must not be lower than the reset release voltage (VLVD0) that is specified for the LVD0.

3.2 List of used Pins

Table 3-1 shows the pins used and their functions.

Table 3-1 Pins Used and Their Functions

Pin name	I/O	Function
P17/TRDIOA	Output	PWM output

Caution: In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Description

4.1 Smart Configurator Settings

This section presents the settings of the Smart Configurator used in this sample program. The items and settings in each table for the Smart Configurator are described as they appear in the configuration screen.

4.1.1 System Configuration

The system configuration used in this sample program are shown below.

Note that the system settings used in this sample program are the same for the integrated development environments e2 studio and CS+, but different for IAR. Please adjust the settings appropriately according to the environment you are using.

Firstly, Figure 4-1 shows the system configuration used in this sample program (for e2 studio and CS+).

If you are conducting a COM port debug on the RL78/G24 Fast Prototyping Board (RTK7RLG240C00000BJ), it is necessary to set the integrated development environments (e2 studio and CS+) appropriately. For details, please refer to the "RL78/G24 Fast Prototyping Board User's Manual (R20UT5091)", specifically "7.1 Using COM Port Debugging with the e² studio" and "7.2 Using COM Port Debugging in CS+".

Figure 4-1 System Configuration (e² studio, CS+)

The screenshot shows the 'System configuration' window with the following settings:

- On-chip debug setting**
 - On-chip debug operation setting: ☐ Unused, ☐ Use emulator, ☒ COM Port
 - Emulator setting: ☐ E2, ☒ E2 Lite
 - Pseudo-RRM/DMM function setting: ☐ Unused, ☒ Used
 - Start/Stop function setting: ☒ Unused, ☐ Used
 - Monitoring point function setting: ☒ Unused, ☐ Used
 - Trace function setting: ☐ Unused, ☒ Used
 - Security ID setting: ☒ Use security ID
 - Security ID: 0x00000000000000000000
 - Security ID authentication failure setting: ☒ Do not erase flash memory data, ☐ Erase flash memory data

Two blue boxes labeled 'Check' point to the 'COM Port' radio button and the 'Do not erase flash memory data' radio button.

Figure 4-2 shows the system configurations used in this sample program for IAR.

Figure 4-2 System Configurations (IAR)

System configuration

▼ On-chip debug setting

On-chip debug operation setting
☐ Unused ☒ Use emulator ☐ COM Port

Emulator setting
☐ E2 ☒ E2 Lite

Pseudo-RRM/DMM function setting
☐ Unused ☒ Used

Start/Stop function setting
☒ Unused ☐ Used

Monitoring point function setting
☒ Unused ☐ Used

Trace function setting
☐ Unused ☒ Used

Security ID setting
☒ Use security ID
Security ID

Security ID authentication failure setting
☒ Do not erase flash memory data ☐ Erase flash memory data

Check

4.1.2 Component Configurations

This section presents the component configurations used in this sample program.

Table 4-1 Component Configurations (Timer RG2)

Item	Content
Component	PWM output
Configuration Name	Config_TRG
Function	PWM function
Resource	TRG

Figure 4-3 Configuration of Timer RG2

The screenshot shows the 'Configure' window for Timer RG2. The following settings are highlighted with blue boxes and annotations:

- Clock source setting:**
 - Clock source: fCLK (Clock frequency: 48000 kHz)
 - External clock edge select: Rising edge
- TRG counter setting:**
 - Counter operation: Count continues at TRGGRA/TRGGRB compare match
 - Counter clearing source: Clear by TRGGRA compare match
- Register function setting:**
 - TRGGRC: General register
 - TRGGRD: Buffer register of TRGGRB (Annotated: "Change to 'Buffer resister of TRGGRB'")
- PWM output setting:**
 - Cycle value: 100 μs (Actual value: 100)
 - Duty value: 90 (%) (Actual value: 90) (Annotated: "Change to '90'")
 - (Initial output "H", Duty is the percentage of "L")
- Pulse output forced cutoff setting:**
 - ☐ Enable forced cutoff by INTPO low-level input
 - TRGIOA pin output: Forced cutoff disabled
- Interrupt setting:**
 - ☒ Enable TRGGRA compare match interrupt
 - ☐ Enable TRGGRB compare match interrupt (Annotated: "Uncheck")
 - ☐ Enable TRG overflow interrupt
 - INTTRG priority: Level 3 (low)

4.2 Folder Structure

Table 4-2 shows the structure of the source files/header files used in the sample code. Note that files automatically generated by the integrated development environment and files from the BSP environment are excluded.

Table 4-2 Folder Structure

Folder/File Name	Description	Generated by Smart Configurator
\r01an6785_trg2_pwm<DIR> ^{NOTE 1}	Sample code folder	
\src<DIR>	Program storage folder	
main.c	Sample code source file	
\smc_gen<DIR>	Smart configurator generated folder	√
\Config_TRG<DIR>	TRG program storage folder	√
Config_TRG.c	TRG source file	√
Config_TRG.h	TRG header file	√
Config_TRG_user.c	TRG interrupt source file	√
¥general<DIR>	Initialization and common program storage folder	√
¥r_bsp<DIR>	BSP program storage folder	√
¥r_config<DIR>	Program storage folder	√

Note: "<DIR>" indicates a directory.

Note 1: The sample code for IAR contains the r01an6785_trg2_pwm.ipcf file.

For details on the .ipcf file, please refer to "RL78 Smart Configurator User's Guide: IAR" (R20AN0581).

4.3 List of Option Byte Settings

Figure 4-3 shows the option byte settings.

Table 4-3 Option Byte Settings

Address	Setting Value	Description
000C0H/040C0H	1110 1111B (EFH)	Watchdog Timer stopped operation (Count stops after reset release)
000C1H/040C1H	1111 1011B (FBH)	LVD0 reset mode. Detection voltage: Rising 2.97V / Falling 2.91V
000C2H/040C2H	1110 1010B (EAH)	Flash operation mode: High-speed main mode. High-speed on-chip oscillator frequency: 8MHz
000C3H/040C3H	1000 0101B (85H)	On-chip debug operation allowed

4.4 List of Constants

Table 4-4 shows the constants used in the sample code.

Table 4-4 Constants used in the sample code

Name	Setting Value	Description
DUTY_DEC	0U	Duty decrease mode (decreasing in 10% increments)
DUTY_INC	11U	Duty increase mode (increasing in 10% increments)
DUTY_INC_END	18U	Duty increase mode end
PWM_CYCLE	$_12BF_TRG_TRG_GRA_VALUE + 1$	PWM cycle value
PWM_CYCLE_10_STEP	$PWM_CYCLE / 10$	Value of PWM cycle divided into 10 stages
DUTY_90	$(PWM_CYCLE_10_STEP * 1) - 1$	Value at 90% duty
DUTY_80	$(PWM_CYCLE_10_STEP * 2) - 1$	Value at 80% duty
DUTY_70	$(PWM_CYCLE_10_STEP * 3) - 1$	Value at 70% duty
DUTY_60	$(PWM_CYCLE_10_STEP * 4) - 1$	Value at 60% duty
DUTY_50	$(PWM_CYCLE_10_STEP * 5) - 1$	Value at 50% duty
DUTY_40	$(PWM_CYCLE_10_STEP * 6) - 1$	Value at 40% duty
DUTY_30	$(PWM_CYCLE_10_STEP * 7) - 1$	Value at 30% duty
DUTY_20	$(PWM_CYCLE_10_STEP * 8) - 1$	Value at 20% duty
DUTY_10	$(PWM_CYCLE_10_STEP * 9) - 1$	Value at 10% duty
DUTY_0	0xFFFF	Value at 0% duty

4.5 List of Global Variables

Table 4-5 shows the variables used in the sample code.

Table 4-5 Variables used in the sample code

Type	Variable Name	Contents	Function that uses the variable
uint8_t	g_duty_mode	Duty Mode Setting	r_Config_TRG_interrupt
uint8_t	g_trgsr0_dummy	Dummy variable for TRGSR0 Register	r_Config_TRG_interrupt
const uint16_t	g_trggrd_tbl[]	Duty Change Table Data	r_Config_TRG_interrupt

4.6 List of Functions

Table 4-6 lists the functions used in the sample code. However, functions generated by the Smart Configurator that have not been modified are excluded.

Table 4-6 List of Functions

Function Name	Description	Source File
main	Main Process	main.c
R_Config_TRG_Create_UserInit	Initial value setting for TRGGRD Register	Config_TRG_user.c
r_Config_TRG_interrupt	Duty Change Processing	Config_TRG_user.c

4.7 Function Specifications

The function specifications of the sample code are presented.

[Function Name] main

Outline	Main process
Header	r_smc_entry.h
Declaration	void main (void);
Explanation	Start the operation of Timer RG2.
Arguments	-
Return value	-
Remarks	-

[Function Name] R_Config_TRG_Create_UserInit

Outline	Initialize TRGGRD register
Header	Config_TRG.h
Declaration	void R_Config_TRG_Create_UserInit(void);
Explanation	Set the initial value of the TRGGRD register
Arguments	-
Return value	-
Remarks	-

[Function Name] r_Config_TRG_interrupt

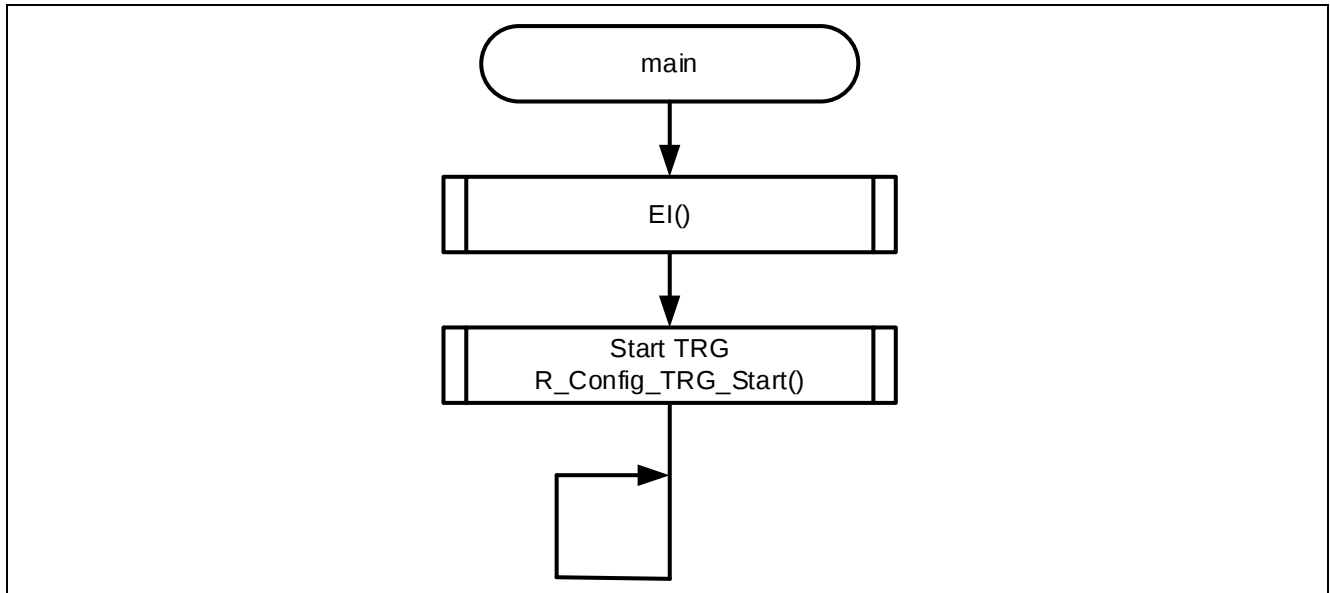
Outline	Change the Duty Cycle
Header	Config_TRG.h
Declaration	static void __near r_Config_TRG_interrupt (void);
Explanation	-
Arguments	-
Return value	-
Remarks	-

4.8 Flowchart

4.8.1 Main Process

Figure 4-4 shows the flowchart for the main process.

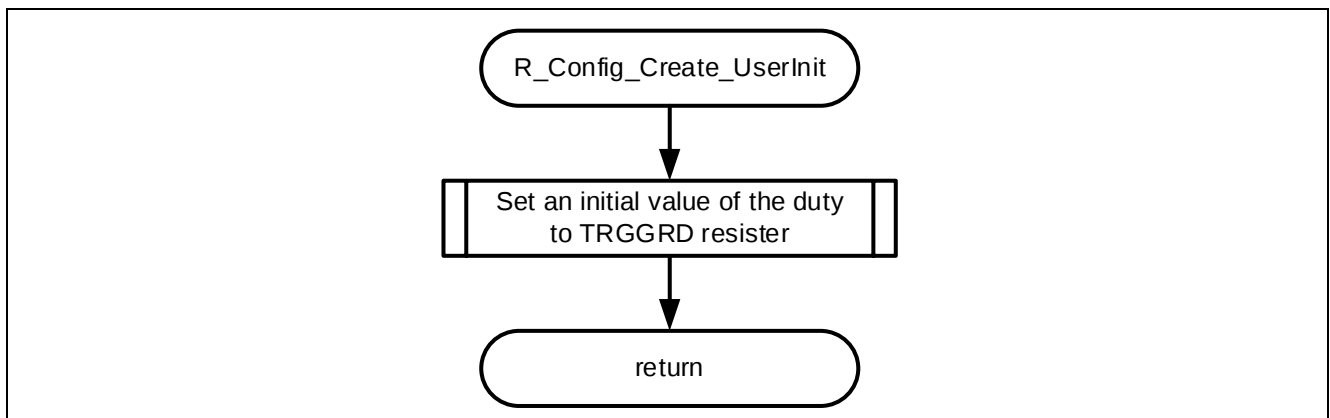
Figure 4-4 Main Process



4.8.2 R_Config_TRG_Create_UserInit Function

Figure 4-5 shows the flowchart for R_Config_TRG_Create_UserInit function.

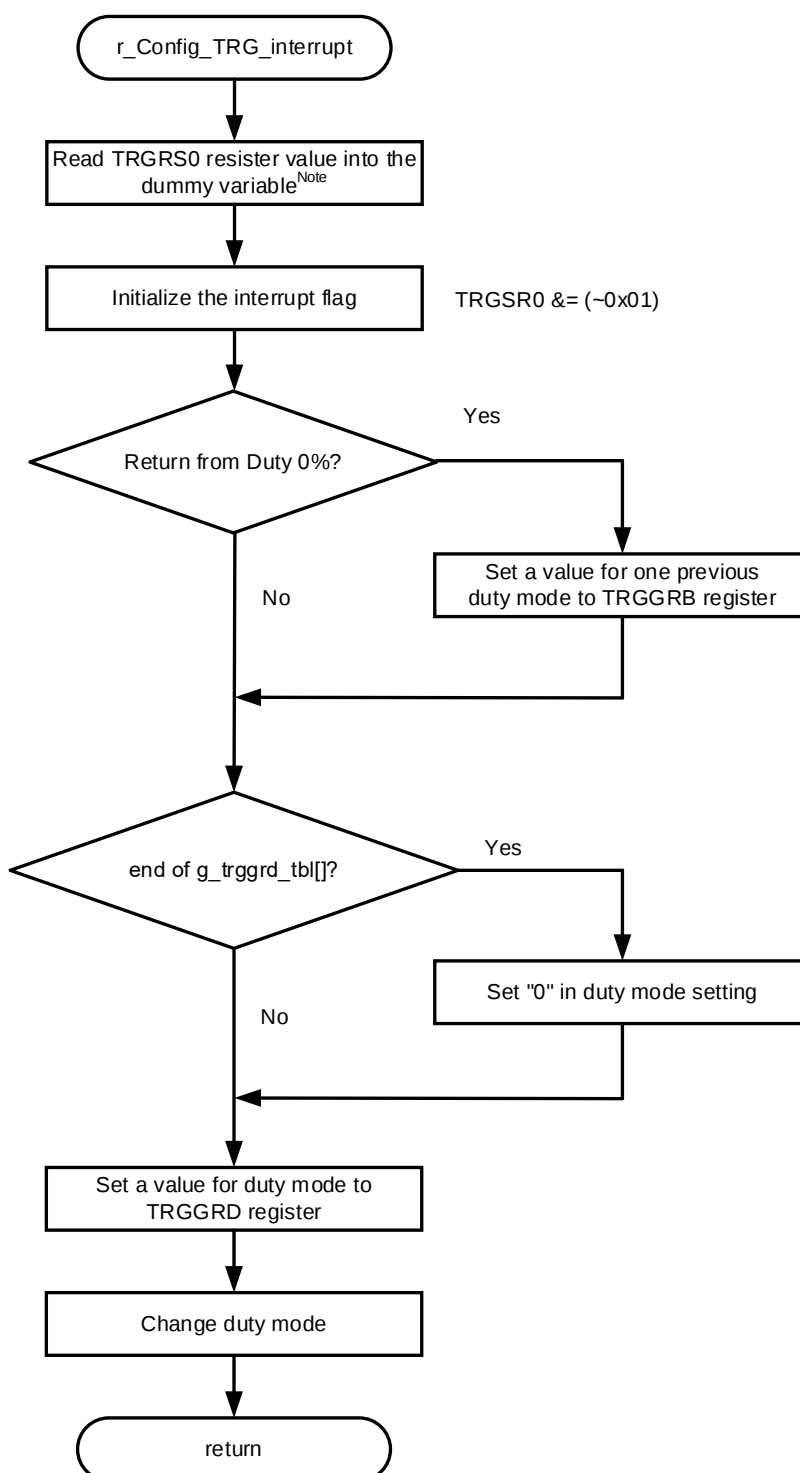
Figure 4-5 R_Config_TRG_Create_UserInit Function



4.8.3 r_Config_TRG_interrupt function

Figure 4-6 shows the flowchart for r_Config_TRG_interrupt function.

Figure 4-6 r_Config_TRG_interrupt fuction



NOTE: The condition for TRGIMFA to become 0 is "read and then write 0", but since it does not support 1-bit access, we are accessing 1 byte to read and then write 0 to the TRGSR0 register. For details, please refer to the "RL78/G24 User's Manual: Hardware (R01UH0961)".

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G24 User's Manual: Hardware (R01UH0961)

RL78 family User's Manual: Software (R01US0015)

RL78/G24 Fast Prototyping Board User's Manual (R20UT5091)

RL78 Smart Configurator User's Guide: CS+ (R20AN0580)

RL78 Smart Configurator User's Guide: e2 studio (R20AN0579)

RL78 Smart Configurator User's Guide: IAR (R20AN0581)

(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest version can be downloaded from the Renesas Electronics website.)

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep.07.23	-	First Edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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