Introduction

AC coupled terminations are used when the signal being transmitted is DC balanced. The most common occurring DC balanced signal is a clock, but there are also balanced data codes such as Manchester, AMI and 8B10B with running disparity coding. In these cases the signals can be AC coupled when the lower frequency of the signal spectral content lies sufficiently above the high pass cutoff frequency of the AC coupling network.

AC coupling affords the freedom to interface logic families that use different switching threshold levels. Each case requires series coupling capacitors followed by the re-establishment of a logic family appropriate DC level at the receiver terminals. This new DC level is generated by a bias circuit, provided either externally by the board designer or internally by the receiver. In addition, it may be necessary to introduce an attenuator to avoid overdriving the receiver.

Cases will be introduced and discussed based on the relative frequency of occurrence.

1) Simplified terminations for IDT Clk/nClk and PClk/nPClk receivers
2) A general AC termination
3) Common LVPECL AC terminations
4) AC terminations for LVPECL receivers with a V_{BB} pin
5) DC offset Terminations to minimize clock receiver oscillation

Simplified AC Terminations for IDT Receivers

IDT uses two types of IDT receivers; P type which are labeled PClk/nPCLk and N type, labeled Clk/nCLK. The common mode range of P type receivers is centered at a higher voltage than that of the N type receivers as can be seen in Table 1 below.

Table 1: Common Mode Range and Internal Bias of IDT Clock Receivers

Receiver Type	Common Mode Max (V)	Vcc = 3.3V Common Mode Max (V)	Vcc = 3.3V Common Mode Center (V)	Vcc = 3.3V Common Mode Min (V)	Vcc = 2.5V Common Mode Max (V)	Vcc = 2.5V Common Mode Center (V)	Vcc = 2.5V Common Mode Min (V)
Clk/nClk	Vcc-1.0	2.3	1.4	0.5	1.5	1	0.5
PClk/nPClk	Vcc-0.5	2.8	1.9	1	2	1.5	1

These two types of IDT receivers are paired with one of three different sets of internal resistors. These internal resistors are selected to simplify the external networks necessary for common applications as in Table 2 below.

Table 2: IDT Internal Bias Resistor Configurations

Application	IN+ Network	IN- Network
Cut off the differential input when unused	51k pull down	51k pull up
Single ended drive to IN+; bias IN- to Vcc/2	51k pull down	51k pull up and 51k pull down
Bias for single ended drive to IN+ or IN-	51k pull up and 51k pull down	51k pull up and 51k pull down

These networks can also be used to minimize the number of external resistors necessary to provide the DC bias for AC coupled inputs from differential transmission lines. The only requirement is that the DC bias lies within the common mode range of the particular receiver.

The simplest possible arrangement for termination and DC bias is accomplished by placing a 100 ohm shunt across the Clk (PClk) and nClk (nPClk) terminals of the clock receiver and letting the internal 51k resistors set the common mode bias exclusively. To see if this AC termination is viable only requires that the common mode bias with the input terminals shorted, since 100 ohms is a short relative to 51k, lies within the common mode range of each of the P and N type receivers. To that end, Table 3 below shows the DC bias when the input terminals are shorted for each internal bias type.

Table 3: Internal DC Bias Configurations

+IN	-IN	Common Mode Center	Vcc = 3.3V Common Mode Center (V)	Vcc = 2.5V Common Mode Center (V)
51k pull down	51k pull up	Vcc/2	1.65	1.25
51k pull down	51k divider	Vcc/3	1.1	0.83
51k divider	51k divider	Vcc/2	1.65	1.25

In comparing Table 1 to Table 3, it can be seen immediately that placing 100 ohms across the differential inputs will satisfy the common mode requirements of the Clk/nClk inputs regardless of the arrangement of the internal resistors or supply voltage. Further, this termination will also work for PClk/nPCLk inputs on all supply voltages when the internal resistors are arranged as a pull down on the positive input and a pull down on the negative input.

The only case for which the 100 ohm shunt does not work is PClk/nPClk when the positive terminal has a pull down and the inverting terminal has a 51k voltage divider. This case is easily handled by introducing a common mode pull up into the termination. The reason that the positive offset is introduced as common mode is simply that it does not introduce an extra parasitic on one receiver terminal, as would be the case if the external pull up were placed on one of the terminals. Secondly, the common mode placement makes layout easier because the parasitics introduced are common mode. This makes layout of the external pull up non-critical. (refer to Figure 1 and Figure 2).

Figure 1. Simplified Shunt Termination for IDT Clk/nClk Receivers

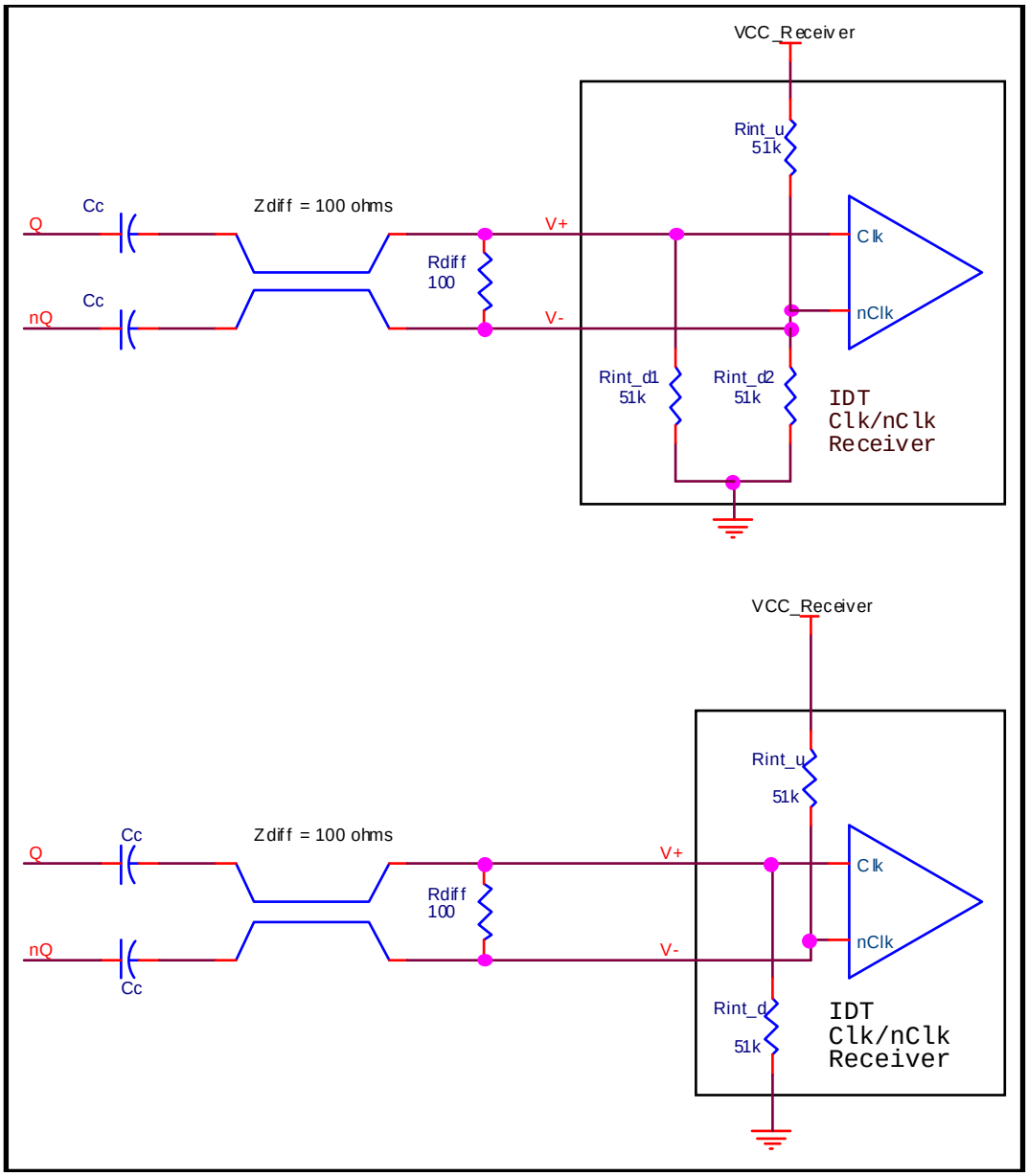
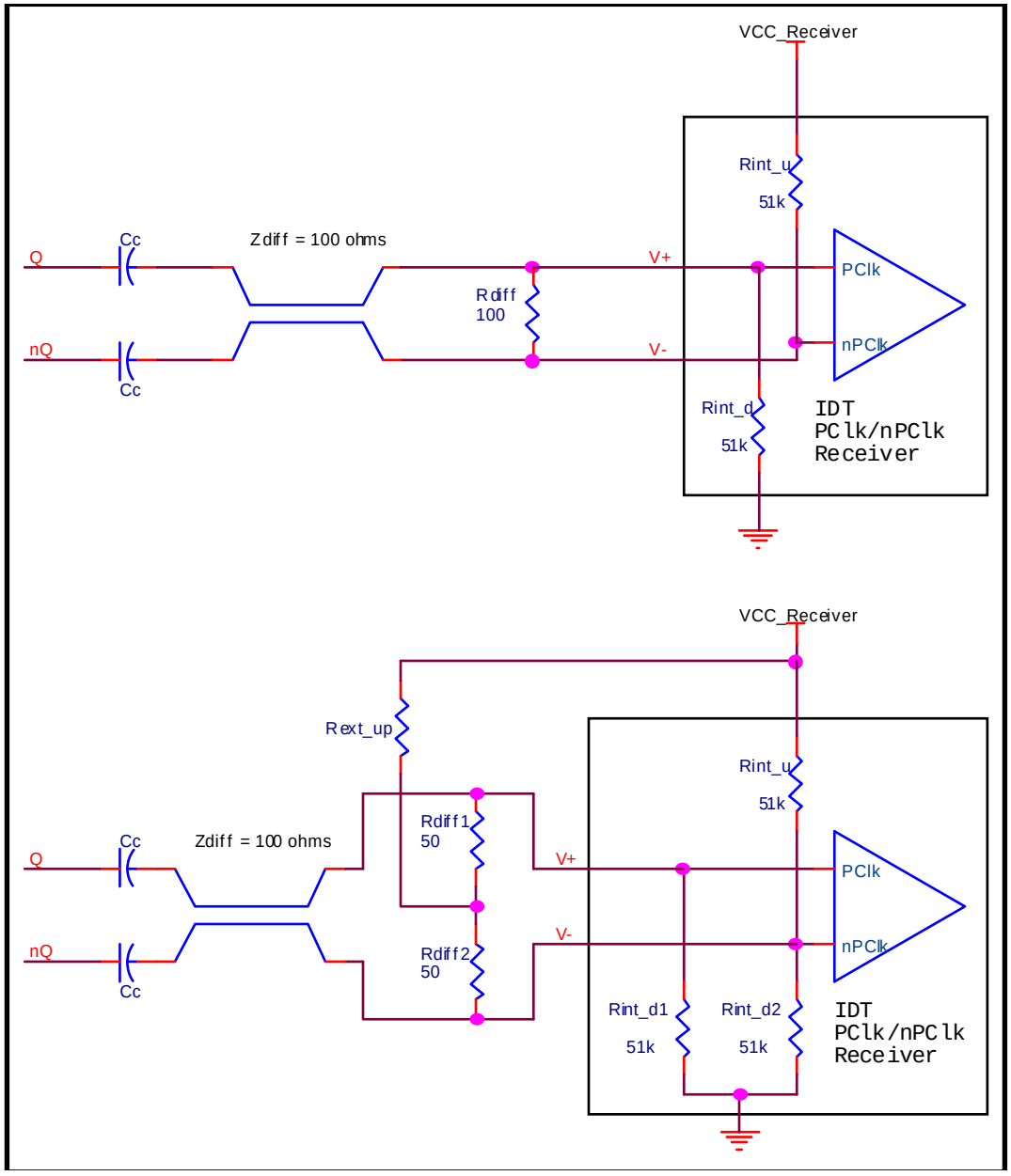


Figure 2. Simplified Shunt Termination for IDT PClk/nPClk Receivers

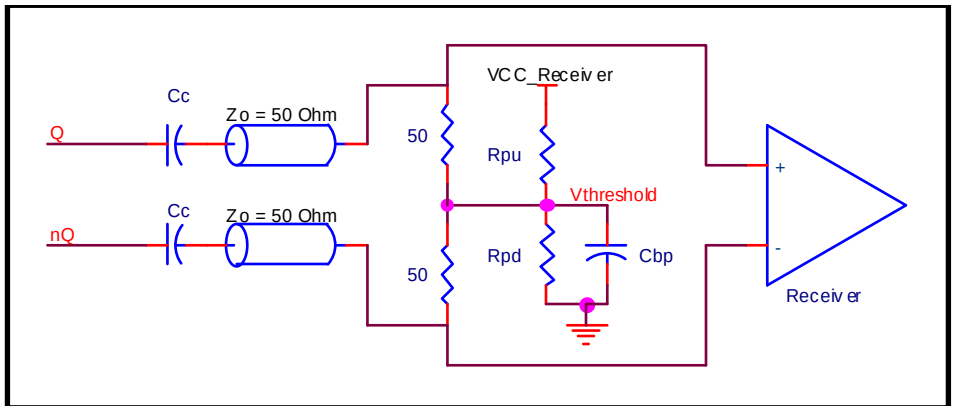


There are also some devices that use a 37k pull up and a 75k pull down on nPClk to bias nPClk to Vcc*(2/3). This case is the inverse with respect to Vcc of a pull down on IN+ and a divider of Vcc/3 on IN-. In this case, the PClk inputs can use the simple 100 ohm shunt termination and the Clk inputs require a common mode pull down.

General AC Termination

Figure 3 shows a very general AC termination with the capability of externally setting Vthreshold, the receiver threshold voltage, anywhere between the ground and VCC of the receiver. This termination scheme is to be used when the clock receiver does not provide either a 50 ohm termination or a common mode threshold bias voltage.

Figure 3. AC Coupled Example with External VTHRESHOLD Voltage Provided at the Receiver



Receiver bias network element values Rpu and Rpd are shown in Table 4 below for the most common logic families. These values center the AC swing for the receiver at the logic threshold voltage for the specified logic family. There are two other aspects in Table 4 that bear mentioning.

1. The clock driver can be any differential driver whose differential output swing does not exceed the capabilities of the receiver nor is too small to meet the receiver minimum swing. See the Section, “Attenuator Pad Design” if it is necessary to pad down the driver level to match the receiver capability.
2. The impedance level of the Vthreshold voltage divider is set for 2.5k. This is because some receivers, such as the IDT PClk/nPClk and IDT Clk/nClk receivers, incorporate internal pull up and pull down resistors. Setting the divider impedance level to 2.5k is typically adequate to ensure that the error in setting the threshold voltages is minimal relative to the common mode range of typical receivers.

Table 4: Bias Resistors for AC Coupling to Selected Logic Families

Receiver Type	VCC_Receiver (V)	VTHRESHOLD (V)	Rpu (k)	Rpd (k)
HCSL HCSL	3.3 2.5	0.35 0.35	23.7 17.4	2.8 2.87
LVDS LVDS	3.3 2.5	1.21 1.20	6.81 5.11	3.92 4.75
LVPECL LVPECL	3.3 2.5	1.39 1.00	5.90 6.19	4.32 4.12

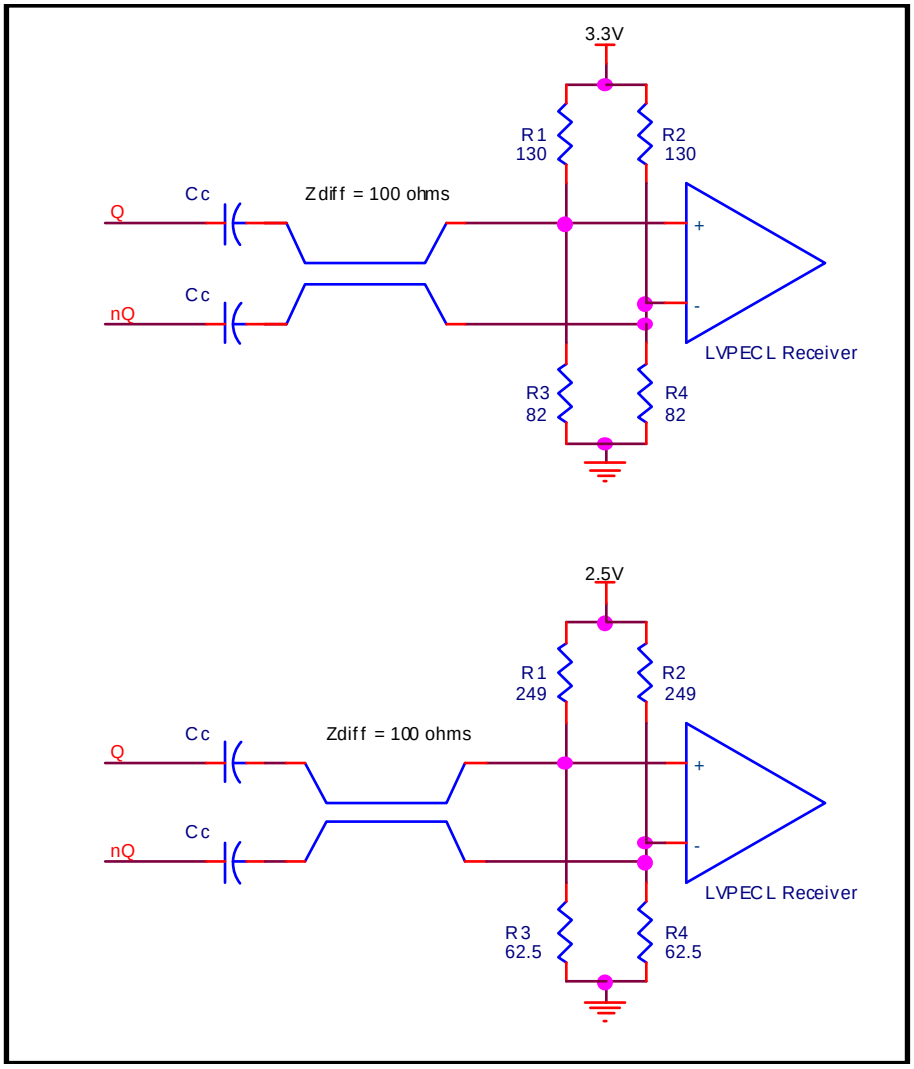
The designer should note that the extended common mode range of most differential clock receivers means that the clock receivers typically can accept more than one signaling family. Consequently the values of Rpu and Rpd need not be the exact values of Table 4; they can be selected to minimize Bill of Materials component spread as long as the new bias point is within the common mode range of the receiver.

Common Alternative LVPECL AC Termination

A common termination, shown in Figure 4, is to AC couple the driver to the standard LVPECL Vcc-2.0V Thevinin termination. There is a conceptual error with this termination; the DC voltage generated by the Thevinin termination, VTT, effectively sets the voltage level to that of the LVPECL logic 0 level. However AC coupling to the Thevinin termination re-centers the LVPECL swing to the termination DC voltage, which is effectively a LVPECL logic 0. In this manner the LVPECL swing is shifted below the DC LVPECL swing by approximately 400 mV.

In practice, these terminations typically work because the shifted level is still within the common mode range of the clock receiver. However these terminations are not recommended because the method of Figure 3 is easier to layout and has fewer differential mode parasitics.

Figure 4. AC Coupled 3.3V and 2.5V LVPECL Thevinin Terminations



AC Terminations for LVPECL Receivers with VBB Outputs

LVPECL receivers often have VBB outputs to facilitate single ended DC operation for logic. The VBB output may also be used to provide bias for both input terminals for AC coupled inputs. Figure 5 shows how the VBB terminal can be used in each of these two cases.

In the case of differential drive, the Cbypass can be connected directly to VBB. Cc is set by the clock frequency in accordance with Table 6 and Cbypass is typically set to 10 x Cc. For single ended drive Rfilter has been added to keep potentially large switching currents from being sourced or sunk from the VBB voltage generator. Rfilter can be set for 100 ohms.

There are also receivers that incorporate the differential terminations into the device with a common mode tap at a VT terminal as well as a VBB generator. Adjustments of the terminations of Figure 5 to exploit these features for single ended and differential AC coupling are shown in Figure 6.

Figure 5. External Termination with VBB Bias for Differential and Single-Ended AC Coupling

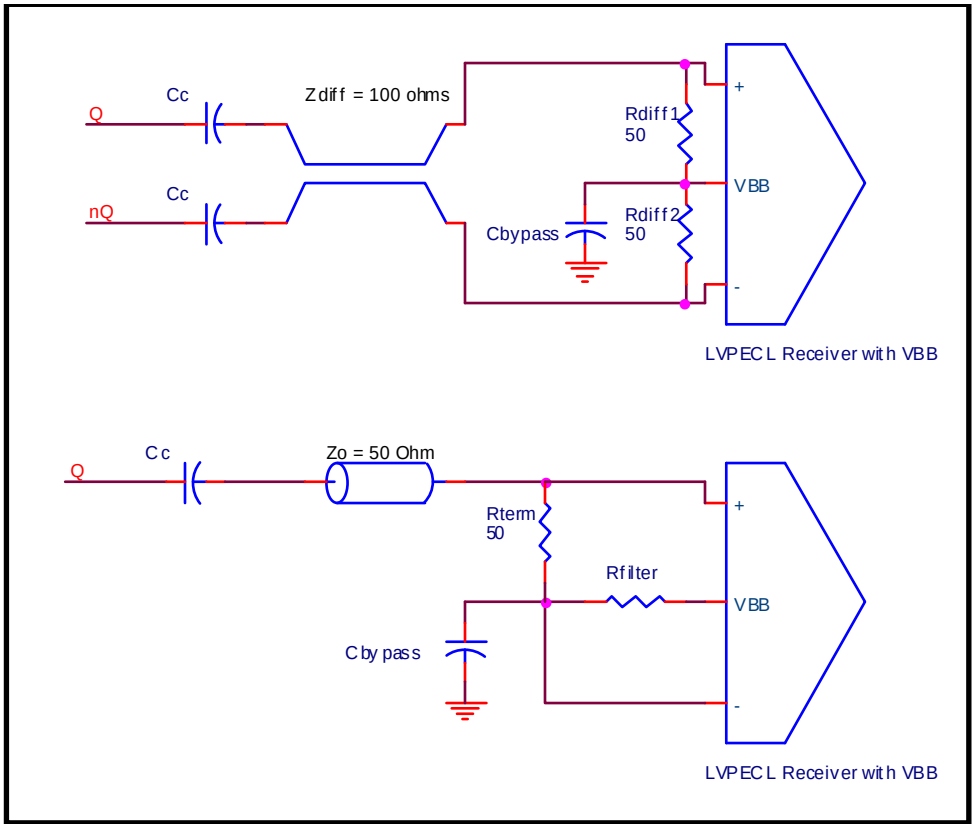
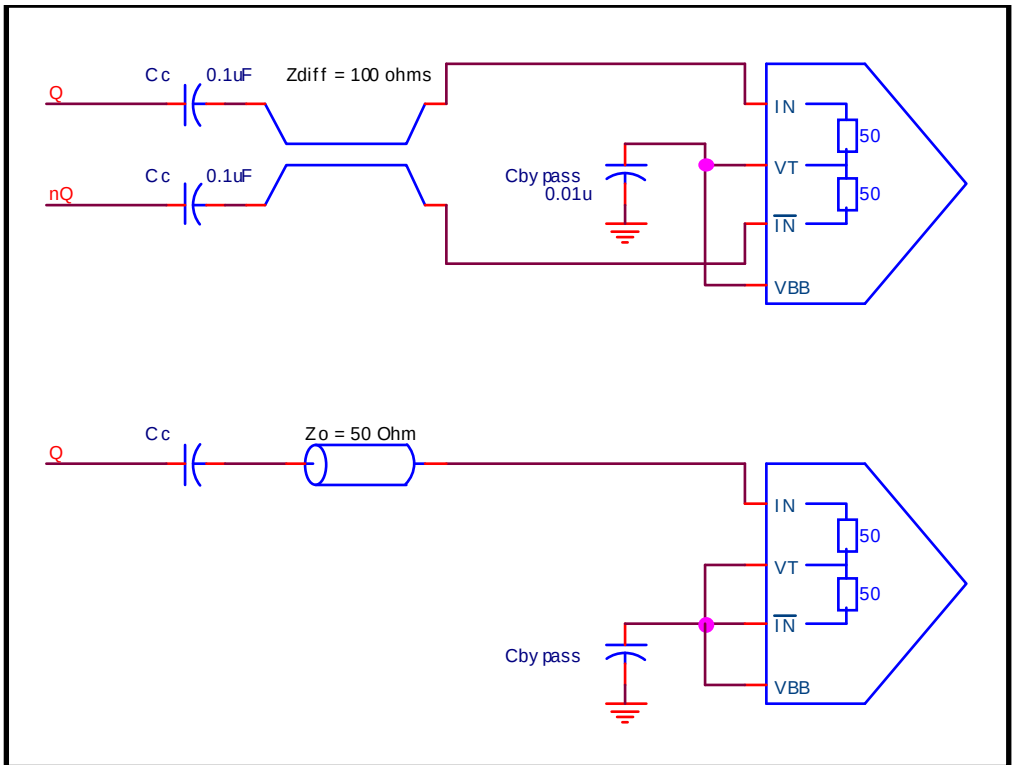


Figure 6. Internal Termination with VBB Bias for Differential and Single-Ended AC Coupling



AC Terminations to Minimize Clock Receiver Oscillation

A common application situation arises if the clock driver is disabled and AC coupled to a receiver, is that the receiver oscillates. The oscillation path is typically through parasitic capacity connecting the outputs of the device back to the inputs. To mitigate this potential problem the general terminations of Figure 7 deliberately insert an 50 mV DC input offset across the inverting and non-inverting terminals of the receiver. The values shown in Figure 5 were selected to bias the IDT differential inputs at the top and bottom of the common mode range. This is done to assist a designer when picking values or R_pu and R_pd to minimize component spread in the Bill of Materials. In addition, a nominal center is selected to force the values of R_pu and R_pd to be the same for Clk inputs and PClk inputs for each of and center of their common mode range; the most conservative design approach given that the receiver only sees the peak to peak swing of the driver. The common mode bias of the inputs can be scaled up or down in accordance with the common mode ranges listed in Table 1 to minimize component spread in the Bill of Materials.

Figure 7. IDT Clk/nCLK and PCLK/nPCK Bias to Suppress Oscillation

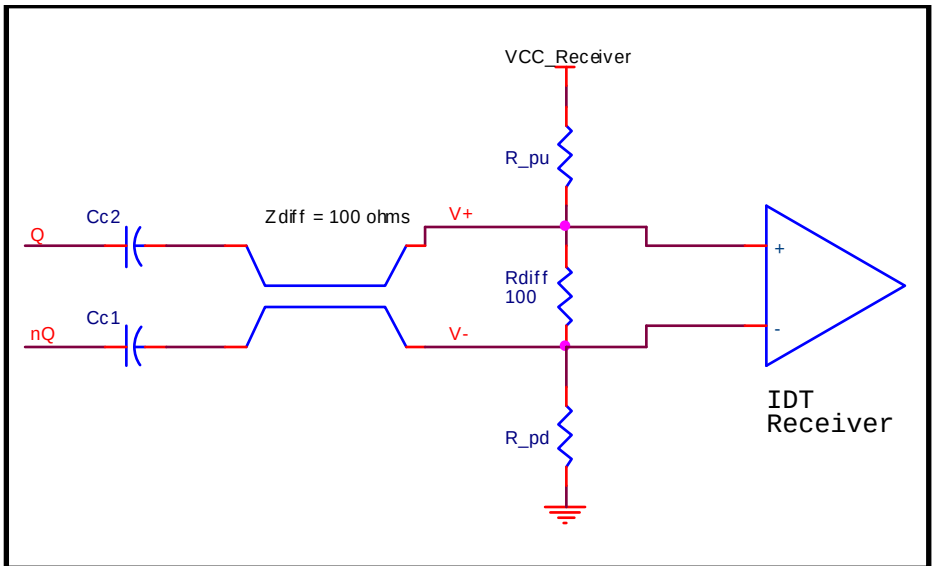


Table 5: Bias Resistor Values for Oscillation Suppression

Receiver Type	Vcc	Common Mode Bias Voltage	R_pu (kohm)	R_pd (kohm)
Clk/nClk	3.3	2.2	2.2	4.4
Clk/nClk	3.3	1.65	3.25	3.25
Clk/nClk	3.3	0.6	5.4	1.2
PClk/nPClk	3.3	2.7	1.2	5.4
PClk/nPClk	3.3	1.65	3.25	3.25
PClk/nPClk	3.3	1.1	4.4	2.2
Clk/nClk	2.5	1.4	2.2	2.8
Clk/nClk	2.5	1.25	2.45	2.45
Clk/nClk	2.5	0.6	3.8	1.2
PClk/nPClk	2.5	1.9	1.2	3.8
PClk/nPClk	2.5	1.25	2.45	2.45
PClk/nPClk	2.5	1.1	2.8	2.2

Coupling Capacitor Guidelines

Coupling capacitor selection is based on the amount of parasitic reactance that the cap is allowed to introduce into the signal path. If this maximum impedance is arbitrarily set less than or equal to 0.2 ohms, then the Table 6 associates standard cap values and their corresponding frequency ranges. Of course, if 0.2 ohms is viewed as excessively conservative for the application, this table can be scaled accordingly. Further, a larger cap can be used for a given frequency range to minimize the total number of cap values in the Bill of Materials.

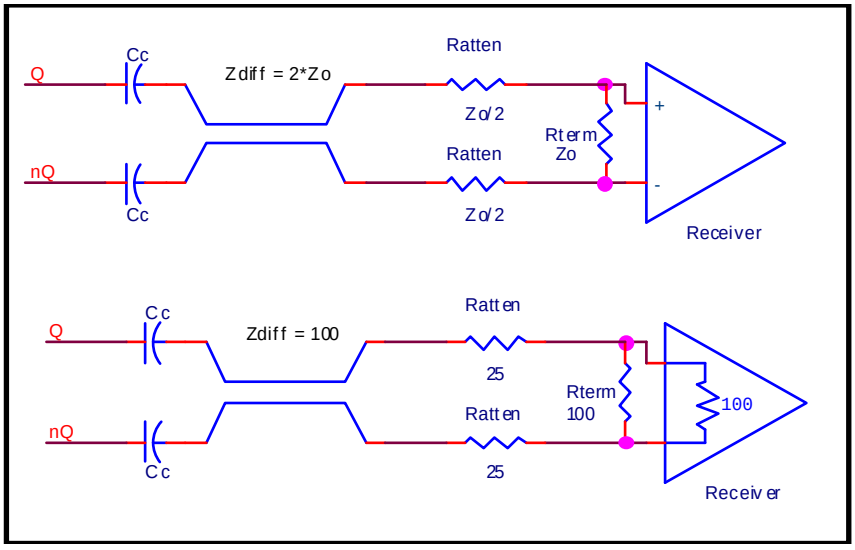
Table 6: Standard Coupling Cap values vs Frequency

Clock Freq Range (MHz)		Cc (pF)	Clock Freq Range (MHz)		Cc (nF)	Clock Freq Range (MHz)		Cc (µF)
Min	Max		Min	Max		Min	Max	
3700	5400	220	370	600	2.2	38	54	0.022
2500	3700	330	250	370	3.3	26	38	0.033
1700	2500	470	170	250	4.7	18	26	0.047
1200	1700	680	120	170	6.8	12	18	0.068
800	1200	1000	80	120	10	8	12	0.10

Attenuator Pad Design

Occasionally it is necessary to attenuate the differential swing to accommodate lower supply voltage receivers. General design practices suggest placing the attenuator at the receiver, especially if a low jitter clock is to be routed a distance in an electrically noisy environment.

Figure 8. 6dB Receiver Attenuator Examples



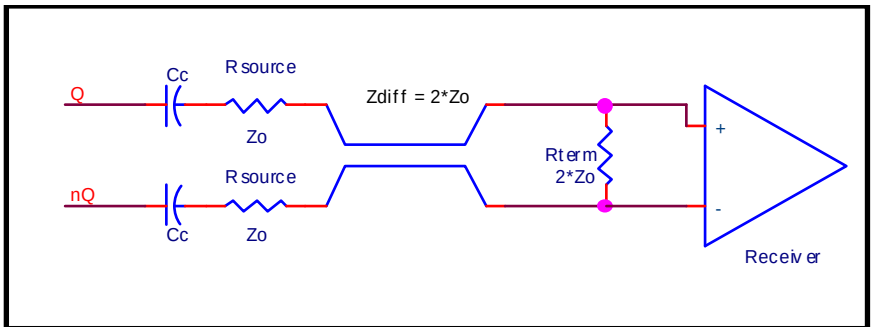
If the receiver termination is external to the clock receiver, then it is simplest to put the attenuator in the termination itself. The examples of Figure 8 illustrate the approach for 6dB of attenuation in a Zo system as well as a specific example when Zo=50 ohms and a receiver with a built in termination. The attenuations realized with standard resistor values are listed in Table 7. It is straightforward to incorporate a VBB reference source for AC coupling of the driver by referring to Figure 5 and Figure 6.

Table 7: Receiver Attenuators for 50 ohm Transmission Lines

Attenuation (dB)	Ratten	Rterm	Z
-0.5	5.6	88.7	50.0
-0.8	8.2	84.5	50.5
-1.1	10.7	78.7	50.1
-1.3	12.4	75.0	49.9
-1.6	14.3	71.5	50.1
-2.0	16.9	66.5	50.2
-2.2	18.2	63.4	49.9
-2.6	20.5	59.0	50.0
-2.9	22.1	56.2	50.2
-3.1	23.2	53.6	50.0
-3.5	24.9	49.9	49.9

If layout considerations at the receiver force the attenuator to be placed at the driver, the impedance of the output driver should be padded out with external resistors for a total source impedance of Zo. This allows for 6dB or less of attenuation. Adding this resistor will improve signal integrity; adding source resistance up to 50 ohms is approaching the ideal of both source and load termination of the transmission line. Figure 9 shows an example of a 6dB attenuator implemented at a 0 ohm output impedance driver.

Figure 9. 6dB Attenuator at the LVPECL Driver



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