Introduction

This Application Note is one of a series addressing different aspects of an emerging networking usage model for wireless infrastructure networking equipment: Low Time-Error nodes. The transmission of time / phase information over the wireless infrastructure network with minimal error from the Grand Master to every node in the network is becoming increasingly important for most network operators as they prepare their wireless infrastructure networks to support 5th Generation (5G) wireless protocols and beyond.

Please consult any or all the following documents for a full picture:

- AN-1031 – Time Alignment Background in Wireless Infrastructure
  - Discusses the importance of time-alignment in wireless infrastructure networks and key topics at the network level. Describes the various classes of alignment discussed in ITU-T document.
- AN-1032 – Time-of-Day Transfer within an Ideal Chassis-Based System
  - Discusses topics related to how to move ToD information from a master timer to various slave timers within a typical wireless infrastructure networking system. This Application Note assumes an ideal system with no wiring or silicon propagation delays on any of the transmission paths. It is necessary to understand the flow of information needed and errors that can be introduced in reading out and loading ToD information into timers. Ensure this note is read and understood before AN-1033 is read.
- AN-1033 – Delay Variation Measurement & Compensation in Non-Ideal Chassis-Based Systems
  - Expands on the discussion in AN-1032 by adding propagation delay effects and how to counter them into the discussion. While using a chassis-based system as an example, single-board systems will experience the same issues and solutions, albeit to a much lesser degree.
- AN-1034 – Minimizing Backplane Signal Usage in Chassis-Based Systems implementing low-cTE Functions (this document)
  - This Application Note proposes a method to minimize the number of signal traces needed to transport the necessary information across a system backplane for transfer of accurate ToD from master timer to slave timers. This method allows existing backplanes to be used without extra traces being required. While the method herein could be used in single-board systems, it is not usually as important to limit the number of traces in such a system as it is in a chassis.
- AN-1035 – 8A340x1 ClockMatrix Device Internal Delays and Delay Variations for Compensation Calculations
  - Calculation of exact compensation values is described in AN-1033. This Application Note provides measured values for IDT's 8A340x1 devices for use in those calculations.

Some other related Application Notes that can be of interest are:

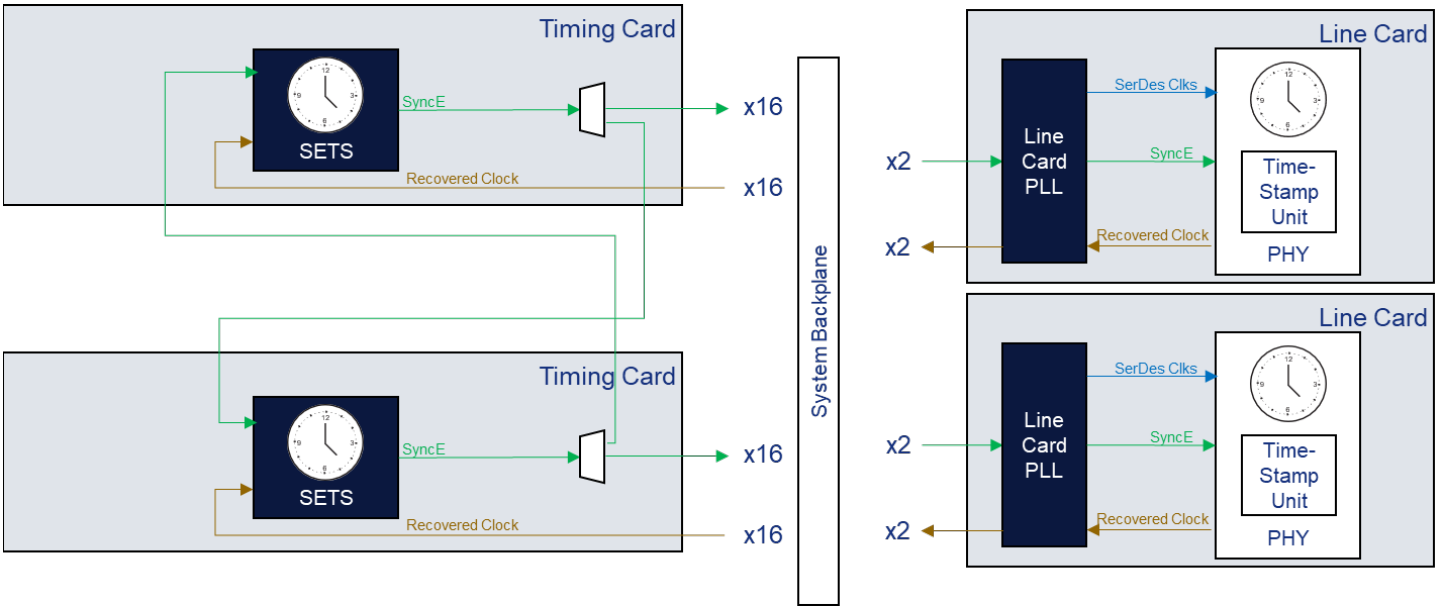
- AN-1010 – ClockMatrix Time-to-Digital Converter (TDC)
  - This Application Note describes how to use the TDC circuit in IDT's ClockMatrix family of devices as a precision phase measurement function. Includes details on setups using IDT's Timing Commander software.
- AN-1030 – Input/Input-to-Output/Output Phase Adjustments
  - This Application Note describes how phase relationships can be adjusted input-input, input-output and output-output within IDT's ClockMatrix family of devices. Includes details on setups using IDT's Timing Commander software.
- PWM User Guide
  - This User Guide describes how to use the Pulse-Width Modulation features of IDT's ClockMatrix family of products.
- AN-1036 Using GPIOs for Loading and Latching ToD in 8A3xxxx Devices
  - This Application Note describes the methods for Loading and Latching ToD counters using GPIO signals.

Chassis-Based Systems for Class A or B Compliance

Chassis-based routers and switches implementing Telecom Boundary Clock (T-BC) functionality have historically had an architecture as shown in Figure 1. This architecture was good enough for implementation of ITU-T G.8273.2 Class A or Class B compliant systems. Each line card supported a single clock trace for a master clock (usually SyncE) from each of a master and a slave timing card and a recovered clock trace from each line card to each of the master and slave timing cards. Master and slave timing cards would have traces between them to exchange their respective master clock signals to maintain alignment when an activity switch from master to slave occurred. There was also a data bus (not shown) used to control each card that could be used to exchange ToD information.

In this diagram, the line card PLL is shown generating the clocks for the PHY device's high-speed serializer / deserializer (SerDes) circuits. These are low-jitter clocks used to generate the physical layer signals on the line-side of the PHY chip. These clocks are separate reference clocks than those clocking the time-stamp units within the same PHY chips. The SerDes clocks need to be have very low phase noise, but do not need tight phase alignment. This contrasts to the TSU clocks being discussed in this family of application notes, which need tight phase alignment, but do not usually need low phase noise. This diagram shows the SerDes clocks being generated locally by the Line Card PLL running in a synthesizer mode, however they could also be generated from some other system clock by using the Line Card PLL in jitter attenuator mode.

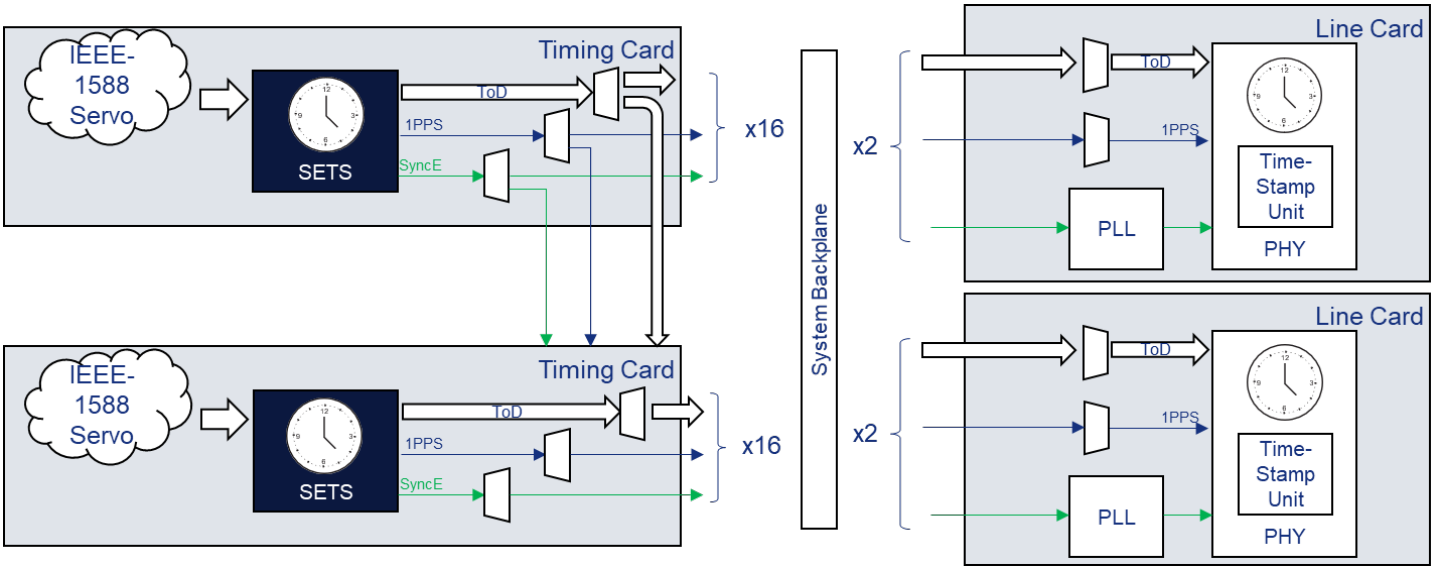
Figure 1. System Clock Infrastructure Diagram for Class A or B Compliance



Additional Signals Needed for Class C or D Compliance

In AN-1032, a system connection diagram was shown for a chassis-based system's ToD alignment infrastructure to meet the tighter requirements of Class C and Class D compliance. Figure 2 repeats this here, illustrating the signals to be transported between cards in a system that transfers ToD data precisely from timing cards to line cards.

Figure 2. System ToD Infrastructure Diagram for Class C or D Compliance



As can be seen in Figure 2, there needs to be a data bus running from the active timing card, where the master ToD resides, to each peripheral ToD (including the backup timing card). With proper addressing schemes, this could be a shared data bus. However, it must run fast enough to transport as many 88-bit ToD values as are needed for each update, within one period of the Synchronization Pulse clock, as discussed earlier. Depending on the system distribution scheme, it can be necessary to send different ToD values to each peripheral ToD or the system can use a broadcast scheme whereby the same ToD is sent to all.

There also need to be paths for the Synchronization Pulses and for the Master System Clock to each peripheral ToD. It may be possible to use a single, multi-drop signal to distribute the master clock to all destinations since the phase is not important, but in practice most systems use a point-point arrangement. The synchronization pulses are phase-critical though, so these must be point-point to avoid unpredictable delays introduced in a multi-drop signal as loads are added or subtracted by cards being added or removed from the system.

In addition, most systems will support redundant timing cards, requiring duplicate paths for all the above from the backup timing card.

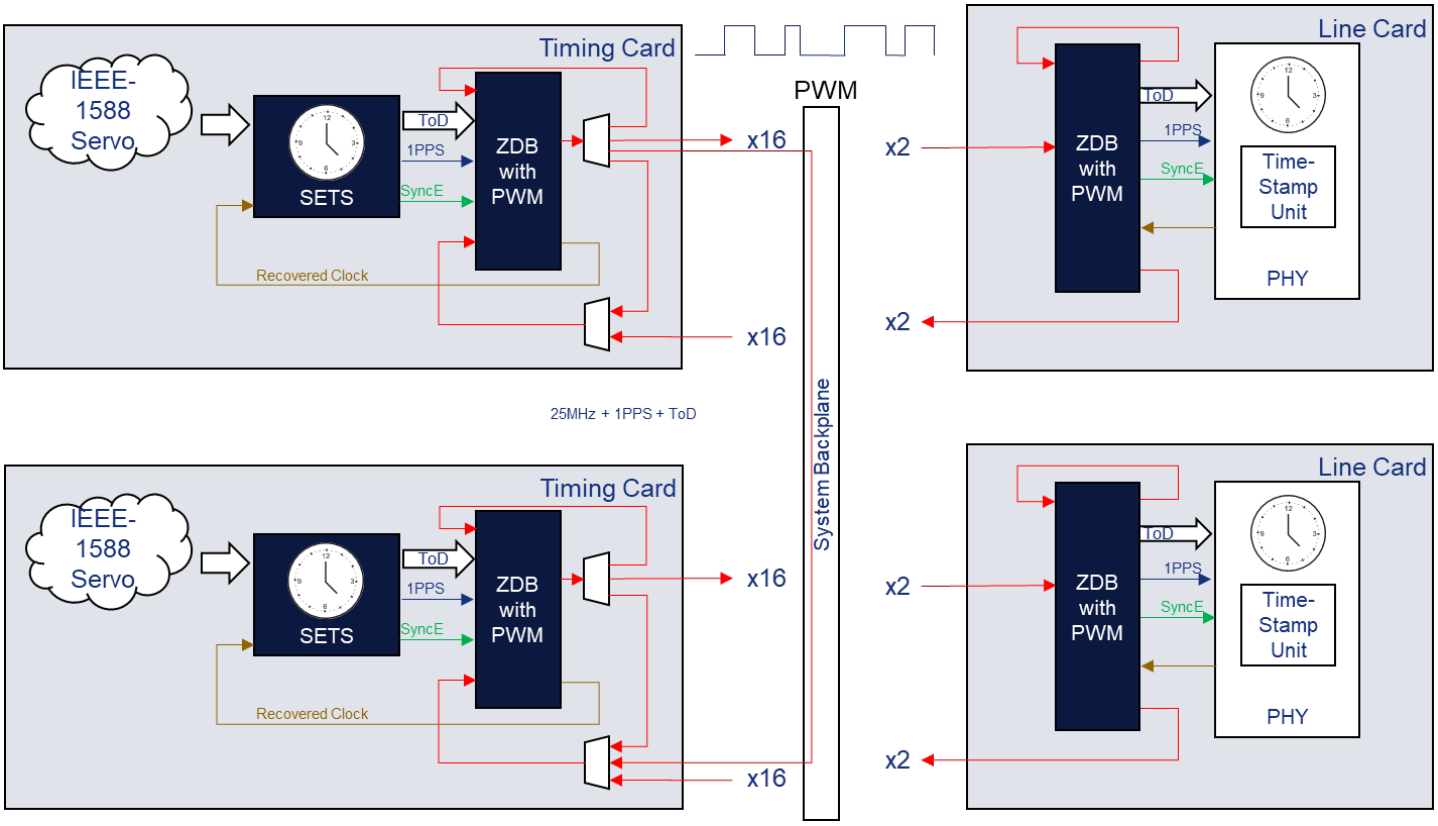
How to Support Additional Signals Without Backplane Changes

IDT's ClockMatrix family of devices addresses this issue by using PWM to encode both an asynchronous clock and a data bus onto a single clock signal to each destination. A high-speed carrier signal is used on the physical clock trace. That physical clock conveys one of the required clocks to the destination, usually the master system clock. Then PWM encoding is used to carry information about the relationship of the second clock signal, the Synchronization Pulse, to the first clock signal across to the destination, where it is reconstructed by the receiving PLL into a 2nd physical clock. Also, the ToD data can be PWM encoded onto the same carrier and recovered into a FIFO on the receiving PLL.

Note that the carrier clock must be a high-speed clock to ensure that the ToD data can be conveyed fast enough and that enough clock data is provided to accurately reconstruct the PWM-encoded clock on the receiving PLL. Slow PWM clock rates will result in significant error in reconstruction, reducing the accuracy of the peripheral ToD alignment.

This is shown in Figure 3. Often this PWM encoding technique can allow existing system backplanes to be re-used to accommodate line and timing cards that support the low-cTE applications.

Figure 3. System ToD Infrastructure Using PWM Encoding



In AN-1033, there were several feedback paths for the RTT delay method introduced to the above diagram. In addition, most wireless infrastructure nodes also support transport of a recovered clock from each line card to each of the redundant pair of timing cards. This allows any line card to be the source of the master clock, which is traceable to the master time source in the network. This recovered clock is often a SyncE clock representing the exact desired frequency reference.

Fortunately, PWM can also help here, allowing both the recovered clock and the feedback path of the RTT method to share a single backplane signal path. The recovered clock (brown) is encoded with the RTT feedback on the line card and decoded on the timing card. The PLL on the timing card will extract the recovered clock information and create a physical clock on the timing card that is routed to the SETS device. Despite the multiplexing used on the recovered clock / RTT path, a continuous recovered clock is still provided to the SETS device by the PLL doing the reconstruction of the signal. The rate at which the mux is switched will be high enough to allow changes in the recovered clock's frequency to be transmitted to the SETS within response time targets for various standards such as ITU-T G.8262.1.

Summary

Most chassis-based systems in routers and switches support backplane traces that run point-point from each of the master and slave timing cards and traces running back from each line card to both the master and slave timing cards. A trace running in each direction between master and slave timing cards are also usually available. By use of PWM encoding on those signal traces, the extra signals needed to implement the tighter alignment of Class C or D don't require any changes to system backplanes. This allows for a much smoother and easier transition of an existing chassis-based system to the more recent alignment targets.

Glossary of Terms

Table 1. Glossary of Terms

1PPS	One Pulse-pre-Second – common synchronization clock used within networking systems. Aligns with the 1 second roll-over of the ToD timer that generates it. This is a 1Hz periodic signal but can be referenced to the rising or falling edge of each pulse. A 1PPS pulse is not required to have a 50% / 50% duty cycle.
3GPP	3rd Generation Protocol Partnership – international standards body that defines specifications for wireless communications.
5G	5th Generation Wireless Networking family of protocols. This is an imprecisely defined term that is loosely understood to refer to the IMT-2020 series of standards being defined by 3GPP.
CP	Charge Pump – sub-circuit within an analog PLL that converts the time-related pulse width from a Phase Detector into a control voltage that can be applied to the VCO.
cTE	Constant Time Error – error in time introduced by a single network node as it receives and transmits time / phase information. This is specifically the error introduced by fixed functions that cannot be accounted for or compensated for.
DCO	Digitally-Controlled Oscillator - sub-circuit within a PLL that contains an oscillator generating the master frequency reference within the PLL. The frequency of oscillation can be adjusted by applying different digital control values. These values are often called Frequency Control Words.
dTE	Dynamic Time Error – error in time introduced by a single network node as it receives and transmits time / phase information. This is specifically the error introduced by periodically varying factors that cannot be accounted for or compensated for.
FIFO	First-In / First-Out – a circuit that queues up pieces of information and maintains them in the order they were received.
FOM	Fiber-Optic Module
FPGA	Field-Programmable Gate Array – often used by board designers to implement complex circuits. Due to their flexible nature, FPGAs are ideal for implementation of circuits that can need changing to fully achieve the desired functionality. Unfortunately, that flexibility also leads in many cases to large uncertainty in signal propagation delays.
FR4	Fire Retardant 4 – material used in Printed Circuit Board manufacturing. FR4 is one of the cheaper options and is widely used in PCBs that don't require tightly controlled impedances, low parameter variation or support multi-GHz frequencies.
GM	Telecom Grand Master – common time reference source for a wireless infrastructure (or other) network. Capable of transmitting its reference using the IEEE 1588 protocols to other network nodes. Usually only one GM is active in any network, although one or more backups can be available to take over in case of disqualification of the active GM.
GNSS	Global Navigation Satellite System – generic term used for any of several satellite constellations used to transmit time information used to establish position on the globe or used as a common time reference. The protocols used require at least 4 satellites to be visible to any receiver to achieve the time/phase alignments discussed in these Application Notes.
IDT	Integrated Device Technology – a semiconductor designer and supplier with a leading market position for timing and synchronization integrated circuits, including the ClockMatrix family.
IoT	Internet-of-Things – term used to include any device of any kind connected to the Internet. Recently there has been an exponential increase in the number of such devices as simpler devices are now able to cheaply connect to the Internet over wireless networks.

ITU	International Telecommunications Union – a standards body that defines internationally recognized specifications for the interaction of telecommunications and networking equipment.
LF	Loop Filter – sub-circuit within a PLL that takes the digital words or analog control voltages from the PD and CP sub-circuits over a period of time and filters them to ensure the VCO responds smoothly to the requested changes. This is usually a low-pass filter, although more complex digital filters can be used.
PD	Phase Detector – component within a PLL device that detects the difference in time between the rising (or falling in some cases) edges of the two input signals. The output can be a voltage or pulse that is proportional to the time difference in analog PDs or a digital word in the case of digital PDs (sometimes also called TDCs).
PHY	Physical layer protocol translation device. In the context of these Application Notes, these are assumed to include a Time-of-Day counter used to time-stamp IEEE 1588 packets for minimum inaccuracy in the transfer of time/phase information.
PLL	Phase-Locked Loop
PTP	Precision Time Protocol – any protocol used across a communications network for transferring time information. In the context of these Application Notes, it refers specifically to IEEE 1588.
PWM	Pulse-Width Modulation – a way of encoding extra information onto a periodic signal such as a clock.
RTT	Round-Trip Time – elapsed time from when a signal is transmitted until it is looped back and received at the source.
SerDes	Serializer / Deserializer – circuit within a PHY device that generates the signals on the line side of the PHY with very high speed. Reference clocks for the SerDes usually need to meet low phase noise targets to maintain low bit-error rates on the line (clean eye pattern).
SETS	Synchronous Equipment Timing Source – function within a telecommunications system that establishes and communications the master time sources for the node.
SyncE	Synchronous Ethernet protocol – defined by ITU-T G.8261. Carries data in similar packet formats as regular Ethernet, but also includes a frequency reference that can be used by all nodes in the network. Requires an unbroken path to the active GM of the network across synchronous networking protocols.
T-BC	Telecom Boundary Clock – one of several profiles within the IEEE 1588 family of standards. Defined in ITU-T 8273.2.
TDC	Time-to-Digital Converter – digital circuit that measures and reports time differences (phase errors) between the rising edge of two signals supplied to its input terminals. The output is a time measurement that can be used to drive a phase-locked loop or read by external software for use in compensation calculations. Some TDCs require periodic signals to achieve a desired accuracy whereas others can make one-shot measurements.
ToD	Time-of-Day – in the context of these Application Notes, this does not refer to a universal time standard, but rather to the time representation used in a specific wireless infrastructure network.
UTC	Universal Time Content – internationally recognized accurate time standard and format for representing it.
VCO	Voltage-Controlled Oscillator – sub-circuit within a PLL that contains an oscillator generating the master frequency reference within the PLL. The frequency of oscillation can be adjusted by applying different control voltage values.
ZDB	Zero-Delay Buffer – an application of a PLL to create multiple copies of an incoming clock signal, potentially at different output frequencies, but with minimal delay from input-output. Despite the name, delays from input-output are not zero, but are much smaller than a normal PLL implementation. A ZDB usually uses an external PCB trace to implement its feedback path. This PCB trace acts as a delay function of one period of the clock being fed back.

Revision History

Revision Date	Description of Change
February 8, 2019	Initial release of the application note.

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