Reference Design

6 W Isolated auxiliary power supply for SiC-MOSFET gate driver

WÜRTH ELEKTRONIK

RD001 // Eleazar Falco / Emil Nierges

1 Overview

This reference design presents an extremely compact auxiliary power supply, providing two isolated output rails of +15 V and -4 V with a combined total output power of 6 W. It aims at optimally driving Silicon Carbide (SiC) MOSFETs in high-performance applications in a variety of industry fields.

Key Features

- Extremely compact and lightweight (3.5 g)
- 4 kV primary-secondary Isolation
- Only 7.5 pF typ. interwinding capacitance
- PSR Flyback topology with LT8302 (AD/LT)
- Very tight load/line regulation of 5% typ.
- Up to 86% peak efficiency (83% at 6 W)
- AEC-Q component qualification

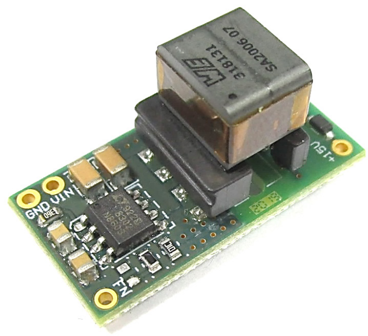

Figure 1: Board Image

Typical Applications

- Automotive powertrain: Traction motor inverter
- On-board and off-board battery chargers
- Industrial drives: AC motor inverter
- Renewable energy: Solar inverters
- Power factor corrector (PFC) stage
- Switch-mode power supplies with SiC MOSFETs

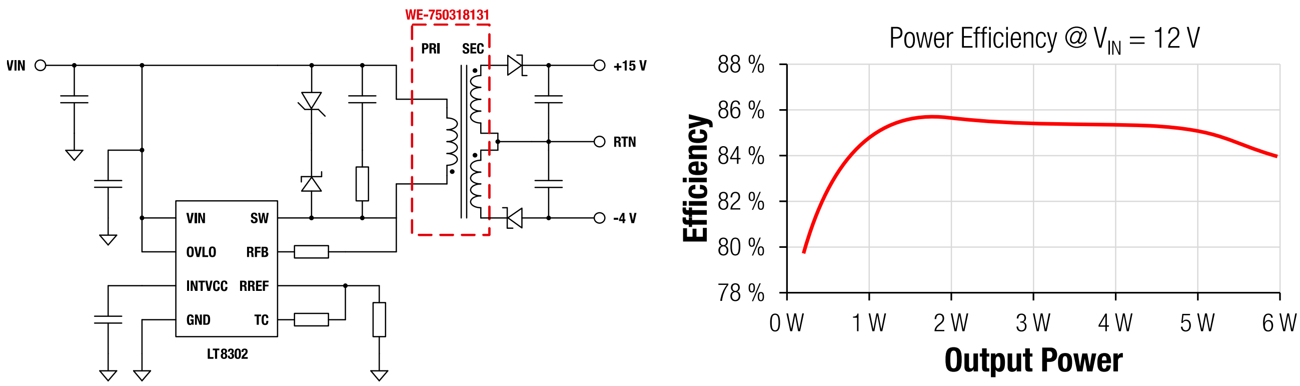

Figure 2: Simplified circuit topology and efficiency at V_{in} (nom) = 12 V

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2 Technology and System Design Considerations

Silicon Carbide (SiC) technology is enjoying growing popularity in medium and high voltage power switching applications (typically above 300 V). The extremely fast switching speed of SiC-MOSFETs, their low ON-resistance and excellent thermal performance (conductivity and stability) are some of the key advantages against its Silicon-based counterparts. SiC devices are thus starting to replace IGBT (Insulated Gate Bipolar Transistor) in many applications in industries as diverse as E-mobility, industrial and renewable energy.

The voltage required across the gate-source terminals of a SiC-MOSFET for optimal turn-on and turn-off of the device are typically found in the range of 14 to 20 V for full turn-on and -2 to -5 V for robust turn-off. Note that this negative voltage is required for a faster turn-off transition as well as to keep the device off reliably, preventing spurious Miller-effect turn-on in hard-switched half-bridge applications (see 2.2 section), due to the very high dv/dt generated across the device terminals during the switching transition.

2.1 Gate Driver, SiC-MOSFET and Auxiliary Power Supply System

A low-power isolated auxiliary supply, typically a flyback, push-pull or half-bridge topology, provides the positive and negative output rails in addition to the required galvanic isolation between the high-voltage and low-voltage sides. This is a requirement not only to meet relevant safety standards, but also to reduce electrical noise as well as to improve EMI and gate driver control robustness. The transformer in the auxiliary supply fulfils this primary task.

Regarding the gate driver stage, an isolated gate driver IC commonly using an integrated totem-pole transistor configuration is used to drive the gate-source of the SiC device based on a control signal from the controller system. The system connection is shown below:

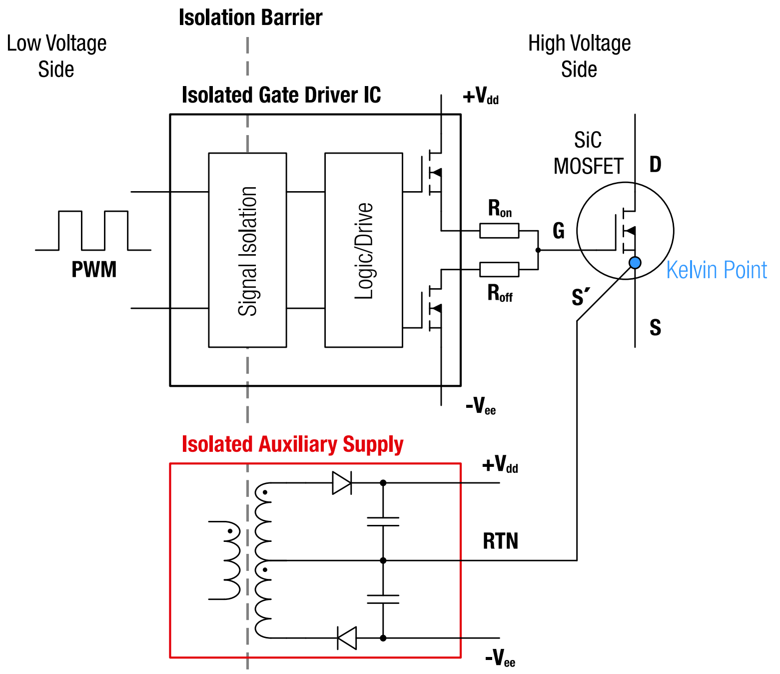

Figure 3: Connection of auxiliary supply with gate driver and SiC-MOSFET

Please note that some SiC devices feature an additional source pin S' (Kelvin connection) as shown above. This provides a low-inductance gate current return path which further increases turn-off robustness.

2.2 Why a negative voltage for turn-off of SiC-MOSFETs

A half-bridge SiC-MOSFET configuration is the building block of many power switching applications, with a high-side device and a low-side device switching alternately, and each with its own auxiliary power supply and gate driver circuit:

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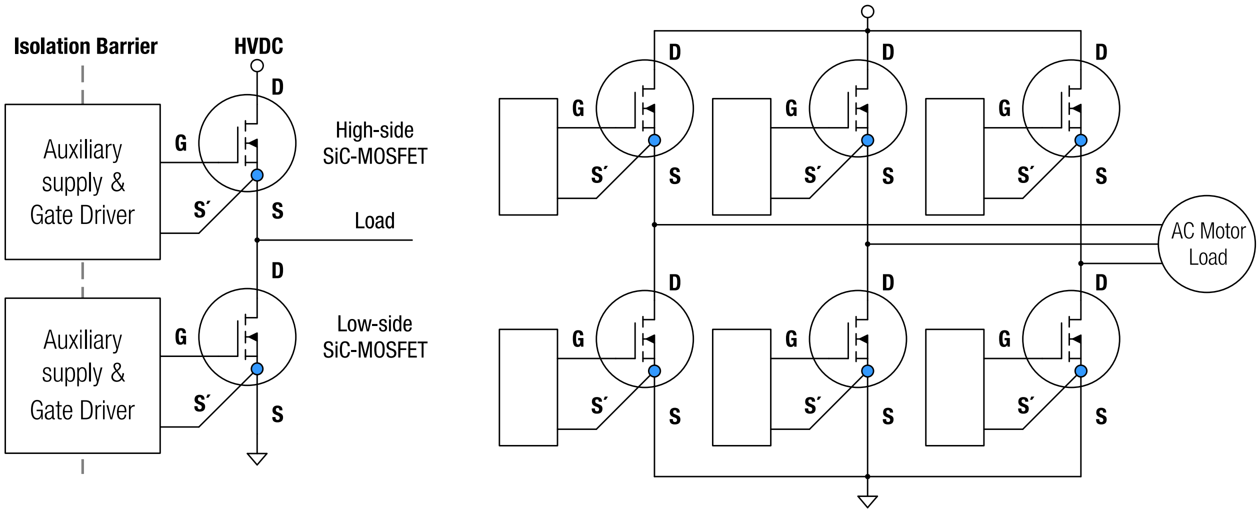

Figure 4: SiC-MOSFET half-bridge configuration (left) and 3-phase inverter application example (right)

When any of the SiC devices in the half-bridge leg (high-side or low-side) is turned on, the complementary device is already off as deadtime is used to prevent shoot-through or cross-conduction (i.e. both devices on at the same time). However, the very fast switching speed coupled with the typically high application voltage causes a very high dV/dt to appear across the terminals of the complementary device. This dV/dt in turn causes an instantaneous current to flow across the gate-drain capacitance (Figure 5) into the gate of the device. The gate-source impedance (Z_{gs}) is approximated by a parallel combination of the gate-source capacitance (C_{gs}) with the sum of the total turn-off gate resistance (R_g) and the gate loop inductance (L_p). If Z_{gs} is higher or comparable to C_{gd} impedance, then the voltage bump/glitch may turn the complementary device on, causing shoot-through. This is known as Miller-effect turn-on and its consequences are typically a considerable drop in efficiency, higher operating temperature, lower reliability and in extreme cases even damage of the devices.

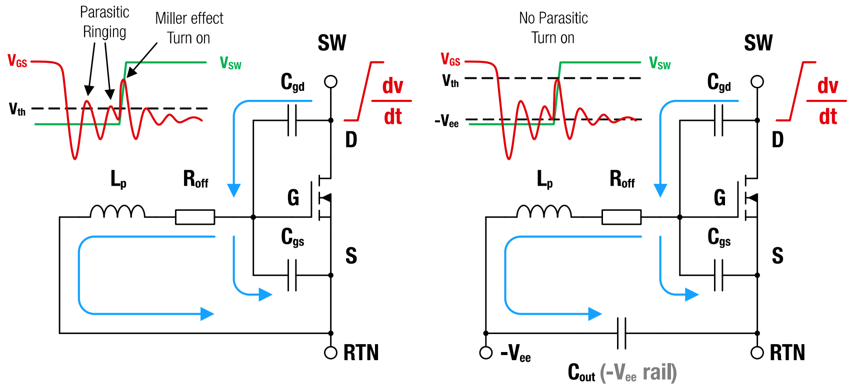

Figure 5: SiC-MOSFET Turn-off transient. Parasitic turn-on without $-V_{ee}$ rail connection due to Miller effect and gate resonant ringing (left) and with $-V_{ee}$ rail connection (right).

In Figure 5, an example of the Miller effect is shown for the low-side switch when the high-side switch turns-on. Using a negative voltage for turn-off provides extended margin to the SiC-MOSFET ON threshold voltage (V_{th}). This helps the system to tolerate higher dv/dt and di/dt and thus higher switching speeds, which is the main advantage of SiC devices. There are some particular cases, like in soft-switching applications (zero voltage switching ZVS), or when using a gate driver IC with an active Miller clamp, where a negative voltage may not be at first essential. However, even in these cases a negative voltage is still recommended for extended reliability.

2.3 Auxiliary supply: Output power requirement

The auxiliary power supply needs to provide for the power loss in the gate driver circuit during the switching transitions. This power is dissipated in the total resistance of the gate current loop to the SiC device (Figure 6), and depends on the gate voltage, switching frequency and total gate charge of the SiC-MOSFET, as follows:

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$$P = Q_g \cdot f_{sw} \cdot \Delta V_{gs}$$

Where:

Q_g: Total gate charge of SiC device for ΔV_{gs} (see Q_g vs V_{gs} curve in SiC device datasheet)

f_{sw}: Switching frequency of SiC device

ΔV_{gs}: Gate-to-source voltage (full-swing) (e.g. for V_{dd} = +15 V and V_{ee} = -4 V, then ΔV_{gs} = 19 V)

Some gate driver ICs also take some power from the auxiliary power supply rails (i.e. V_{dd}, -V_{ee}) to supply internal circuitry, this needs to be considered in addition to the previously calculated value, although this power is normally much lower than the SiC-MOSFET gate loop driving losses.

During turn-on, the +V_{dd} rail provides the required charge (Q_g) to the gate capacitance (C_g), and during turn-off, C_g discharges via the –V_{ee} rail (see Figure 6). Note that there is the same amount of charge flow to and from the gate capacitance (Cg) on turn on and off transition leading to the same average current on each rail.

In this reference design, V_{dd} = +15 V and V_{ee} = -4 V and up to 6 W of output power is provided, meaning that each rail sources an average current of around 320 mA. The power contribution of each rail to the total 6 W is different: 4.8 W for the +15 V rail and 1.2 W for the -4 V rail.

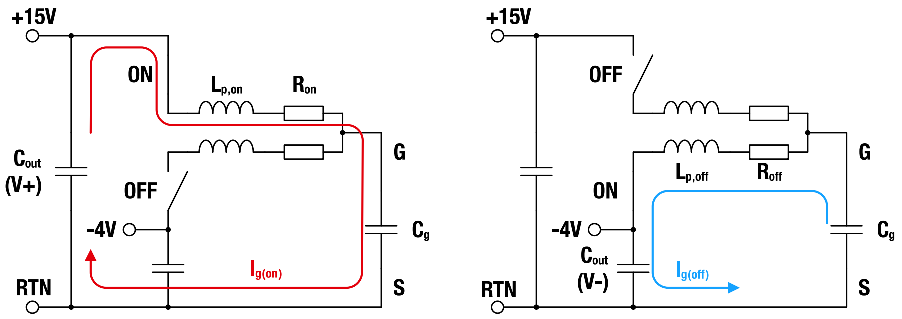

Figure 6: SiC-MOSFET main gate current loops from auxiliary supply output rails for turn-on (left) and turn-off (right)

Please note that R_{on} and R_{off} have no effect on the power requirement calculation. They limit the gate current peak (I_g) during turn-on and turn-off transition respectively and in turn, adjust the switching speed of the SiC device. Care should be taken to ensure that they can withstand the high instantaneous peak power during the switching transitions. In order to increase the switching speed, R_g should be minimized together with the respective loop parasitic inductance ($L_{p,on}$ and $L_{p,off}$).

Regarding system integration, it is critical to place the auxiliary supply and in particular, the output capacitors, very close to the gate driver and SiC device gate terminal in order to minimize the gate current loop and with it the parasitic inductance L_p. Multi-layer Ceramic Capacitors (MLCC) like the CSGP series from Wurth Elektronik are also recommended, due to their extremely low package lead inductance L_c and ESR. The paralleling of several capacitors further allows for a higher di/dt due to significant reduction of total L_c and ESR. The final value and configuration of the auxiliary supply output rail capacitors can be adjusted by the designer to set the desired maximum voltage ripple, switching speed and transient response required by the application.

2.4 A critical parameter for SiC gate driver systems: CMTI

CMTI is the acronym for 'Common-mode Transient Immunity', and it is measured in kV/µs or V/ns. It is an indication of the maximum dv/dt which can be applied across the isolation barrier of the gate driver system before erratic behavior or loss of control occurs, due to excessive distortion of the logic control signals.

The CMTI rating of the system is the maximum dv/dt which can be tolerated across the isolation barrier for reliable operation, which in turn depends directly on the dv/dt applied across the SiC-MOSFET terminals during its switching transition. A higher CMTI rating of the driver system allows for a faster switching speed of the SiC-MOSFET, enabling the SiC device to unleash its top performance.

The different isolated gate driver ICs in the market use different techniques to transfer the control signal information across the isolation barrier (i.e. capacitive coupling, magnetic coupling, optocoupler, etc). In the auxiliary power supply, the supply energy is transferred via the magnetic field using a transformer. In both cases, a parasitic capacitance exists across the isolation barrier. The high dv/dt appearing across this capacitance (C_{pt}) will generate a displacement current (i_d(t)), as follows.

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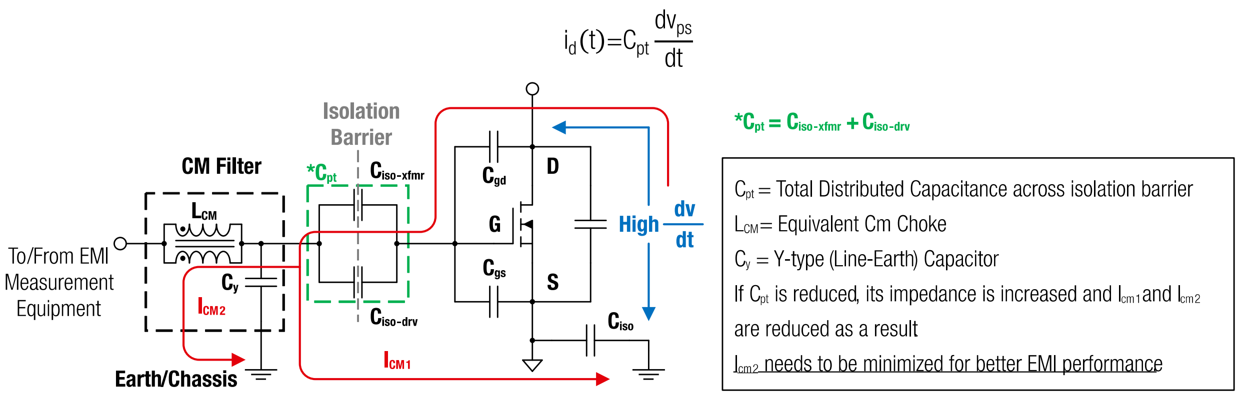

Figure 7: Simplified example of common-mode noise current coupling path for EMI considerations

A too high displacement current may cause several issues in the system, ending with the distortion of the drive logic control signals and loss of control of the SiC device. But in addition to the functional problems, EMC performance may also be compromised, since the very high dv/dt during the switching transitions generates common-mode currents across the isolation barrier parasitic capacitance.

It can be noted how as the total parasitic capacitance across the isolation barrier C_{pt} is reduced, a higher dv/dt can be tolerated for the same displacement current. So the parasitic capacitance across the isolation barrier (both for auxiliary supply and isolated driver IC) should be minimized in order to achieve a high CMTI rating.

In addition to this, it is important to note that the high dv/dt is not only applied with respect to system ground (GND), but also with reference to earth potential via the parasitic capacitance between the high speed dv/dt metallic nodes in the circuit board and earth (to which the product chassis might be connected). The lower the parasitic capacitance C_{pt} across the isolation barrier, the higher the impedance presented to any common-mode noise currents generated in the HV side trying to couple to the LV side capacitively across the isolation barrier (see Figure 7).

Improved EMI performance (especially in radiated emissions frequency spectrum) and lower attenuation requirement for the common mode input EMI filter are as a result expected.

The WE-AGDT Transformer series from Würth Elektronik feature an extremely low interwinding capacitance of only 6.8 pF, helping the full gate driver system to achieve CMTI ratings of above 100 kV/µs as required by many state-of-the-art SiC applications.

For further information on SiC gate driver system considerations, please also refer to the Application note ANP082 on www.we-online.com.

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3 Electrical Specification

	Minimum	Nominal	Maximum	Units
Input Voltage	9	12	18	(V)
Output Voltage (+)	14.8	14.9	15.6 (*)	(V)
Output Voltage (-)	-4.1	-3.85	-3.75	(V)
Output Current (per rail)	3		330	(mA)
Output Power			6	(W)
Switching Frequency (**)	80		360	(kHz)

Table 1. Electrical specification table

NOTE: Specification at 25 °C ambient temperature

(*) When using minimum load clamping zener (PLZ16BHG3H).

(**) Switching frequency varies with load current and input voltage.

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4 Schematic

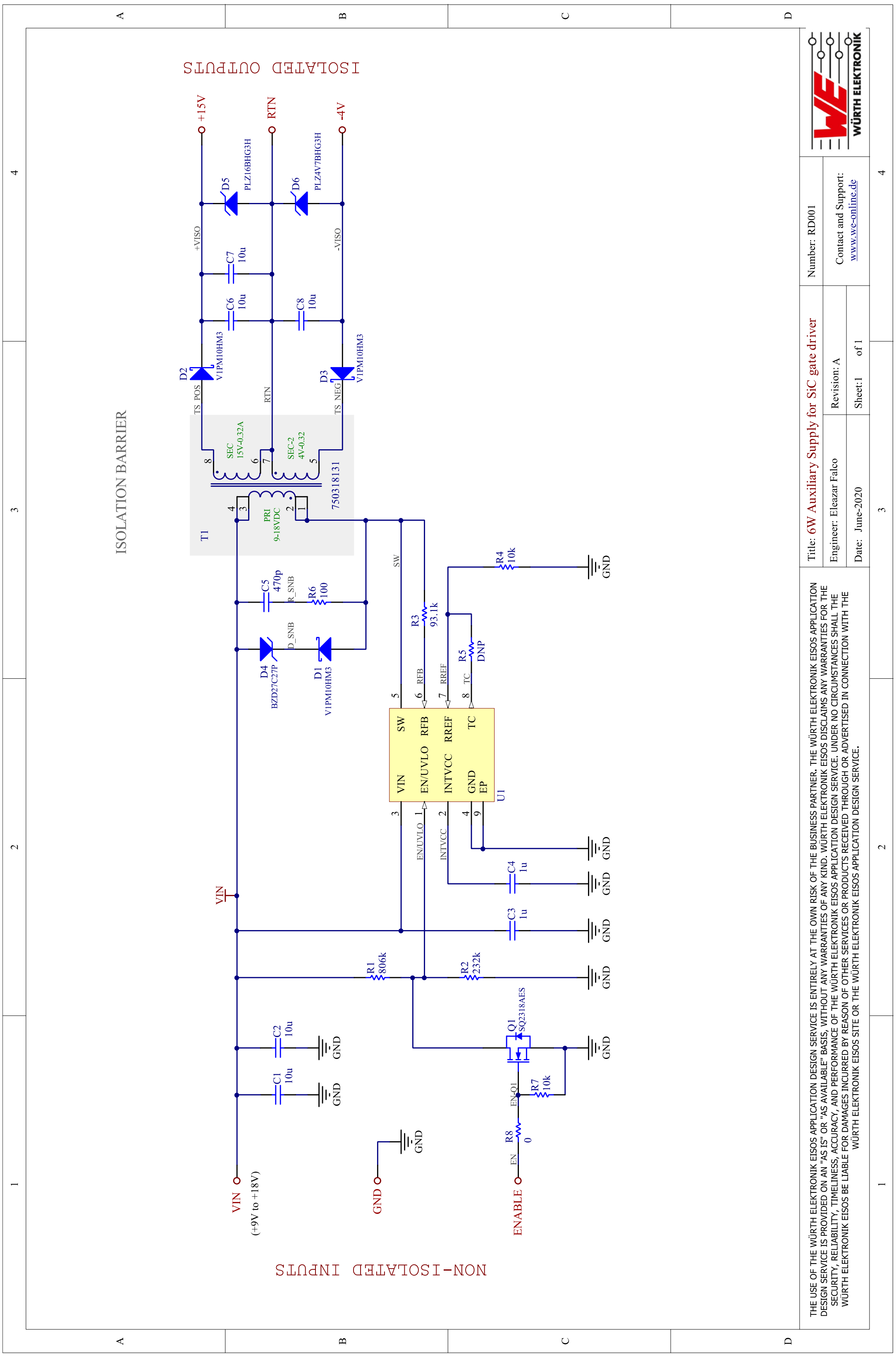

Figure 8: Schematic

5 WE-750318131 transformer characteristics

Würth Elektronik has designed a new transformer with optimal characteristics to be used in this PSR Flyback converter reference design to drive high-performance SiC-MOSFET devices.

Finding an optimal converter operating condition to achieve the smallest transformer size and at the same time high efficiency, good thermal performance and compliance with relevant safety standards were the key design objectives. The WE-AGDT 750318131 transformer uses a very compact EP7 assembly, 4 kV isolation voltage, overvoltage category II, pollution degree 2, fully insulated wire (FIW) and creepage/clearance distances according to standards IEC62368-1 and IEC61558-2-16. Additionally, it counts with AEC-Q200 qualification.

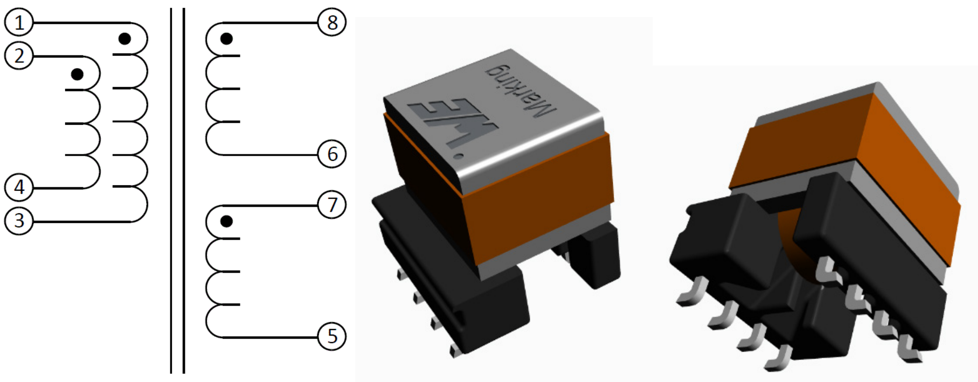

Figure 10: WE-750318131 Transformer details

Parameter	Test conditions	Value
DC resistance – primary	tie(1+2, 3+4), +20 °C	0.047 Ω ± 15%
DC resistance – Sec.1	8-6, +20 °C	0.205 Ω ± 15%
DC resistance – Sec.2	7-5, +20 °C	0.071 Ω ± 15%
Magnetizing inductance	10 kHz, 100 mV	7.00 µH ± 10%
Saturation current	20% roll-off of L_{mag}	4.5 A (min.)
Leakage inductance	100 kHz, 100 mV	270 nH (typ.)
Interwinding capacitance	100 kHz, 10mVAC	7.5 pF (typ.)
Dielectric	4000 VAC, 1 second	4000 VAC, 1 minute
Partial discharge	1000 V_{pk}, 5 sec. 800 V_{pk} 15sec.	10 pC
Turns ratio	(1-3):(2:4)	1:1 (±1%)
Turns ratio	(8-6):(1:3)	1.55:1 (±1%)
Turns ratio	(1-3):(7:5)	2.2:1 (±1%)
Temperature range		-40 °C / +130 °C

Table 2: WE-750318131 transformer characteristics

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6 Board layout variants

This reference design is provided in two layout variants: a two-layer single-sided and a four-layer double-sided solution, as well as with two component assembly options: Standard and with AEC-Q qualified components.

6.1 Board layout variant A: Double-sided design

This variant is a four-layer design with all-SMD (surface mount) component assembly on top and bottom sides.

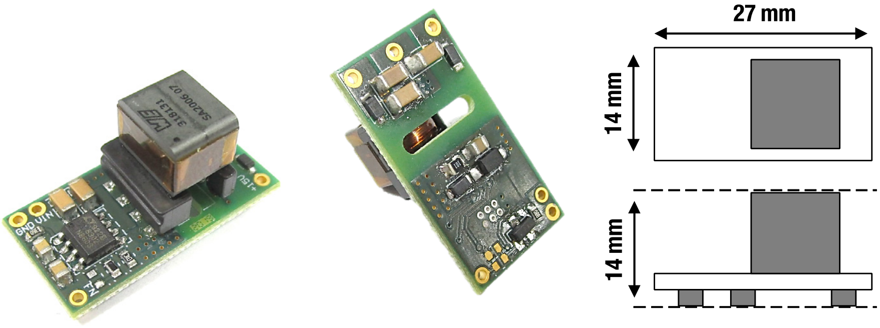

Figure 11: Board variant-A (a) top view (b) bottom view (c) dimensions

6.2 Board layout variant B: Single-sided design

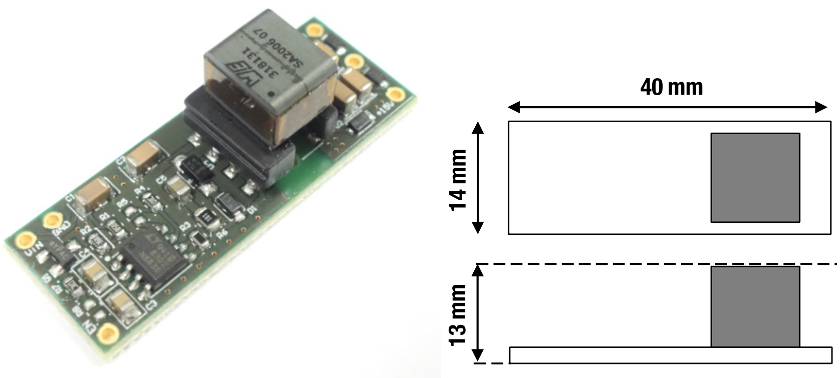

Figure 12: Board variant-B detail and dimensions overview

NOTE: No appreciable performance difference has been observed or can be expected between the two board layout variants, be this functional, thermal or regarding EMC behaviour. The selection of the variant to use can therefore be made based only on the mechanical design constraints of the application. The compact layout also lends itself optimally to integration onto a larger board together with the full gate driver system.

The PCB Layout design files are available (Altium Designer) on www.we-online.com.

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7 Experimental results

7.1 Experimental test setup

The power supply has been tested separately for functional performance using two electronic loads configured in constant-current (CC) mode. Alternatively, resistive-mode of electronic load or discrete power resistors drawing balanced current on both rails can also be used. Tests are carried out at 25 °C ambient temperature.

7.1.1 List of equipment required (used in this case)

- 1 x Laboratory power supply (min. 25 V/1.5 A) (used EA-PSI 9040-40 T)
- 4 x 4-digit precision multimeter (it was used instead a Yokogawa WT3000E precision power analyzer)
- 2 x electronic loads (25 V/1 A min.) (used EA-EL 9080-45 T)
- 1 x oscilloscope (4 channel, 350 MHz or higher) (used Keysight InfiniiVision DSO-X-3034T)

NOTE: A precision power analyzer (min. 3-channel) can be used as an alternative to the four multimeters for highly-accurate voltage and current measurements.

7.1.2 System setup

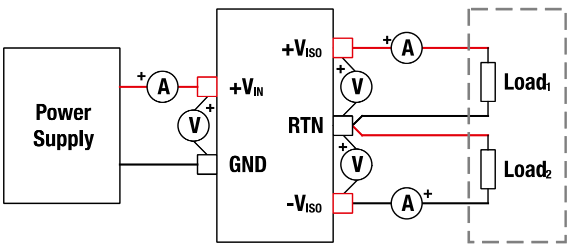

Figure 13: Example of test setup configuration

NOTE: When testing the power supply as described here, both channels must be loaded with the same average current (balanced load). This current represents the charge flow per second between the gate capacitance of the SiC-MOSFET and the respective output rail when switching (+15 V rail for charging and -4 V for discharging). This average current will increase with switching frequency and SiC-MOSFET total gate charge (i.e. capacitance), with a maximum considered in this design of up to 350 mA per rail (over 6 W total).

7.2 Load and line regulation

The output power can reach up to 6 W for this reference design. In addition, the input voltage range is 9 V to 18 V. The line and load regulation results show how each output voltage rail varies with variations in the input voltage and output power, respectively.

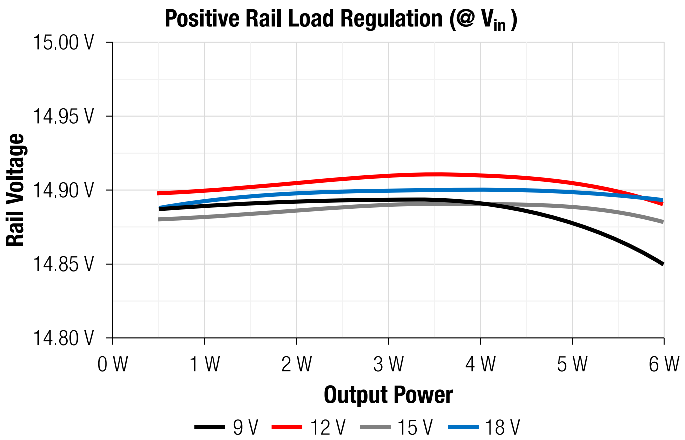

Figure 14: Load and line regulation of output positive rail

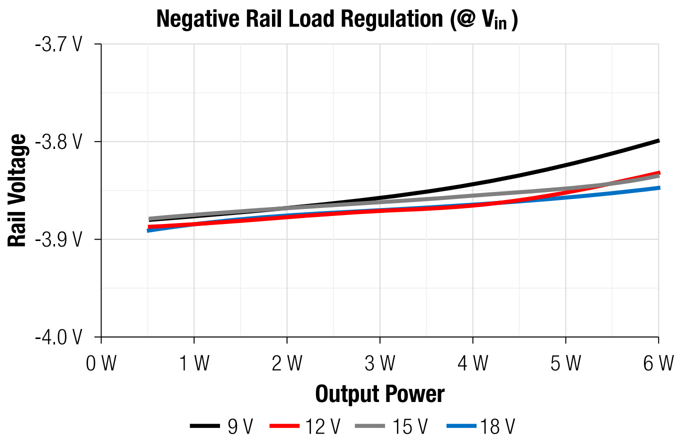

Figure 15: Load and line regulation of output negative rail

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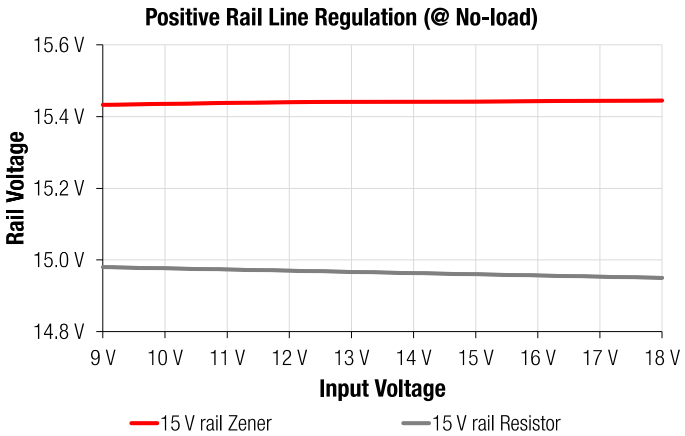
7.3 Minimum-load line regulation

The LT8302 IC controller requires a minimum load in order to keep the output voltage regulated. This minimum load current requirement can be met by using resistors or alternatively clamping Zener diodes. Minimum load resistors will provide more accurate voltage level but lower efficiency against Zener diodes. Please note that clamping Zener diodes are used in any case for overvoltage protection and are the preferred option, but the designer can also use the minimum load resistors if desired.



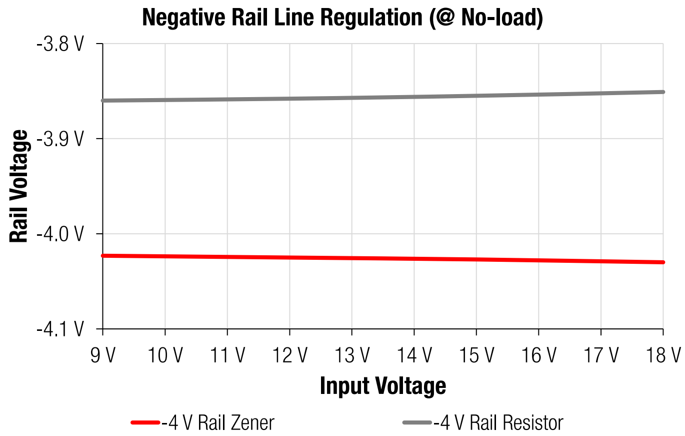


Figure 16: Minimum load line regulation on positive rail (left) and on negative rail (right)

7.4 Power efficiency vs input voltage

Nearly 86% peak efficiency and 84% efficiency at 6 W (full-load) at nominal input voltage is observed.

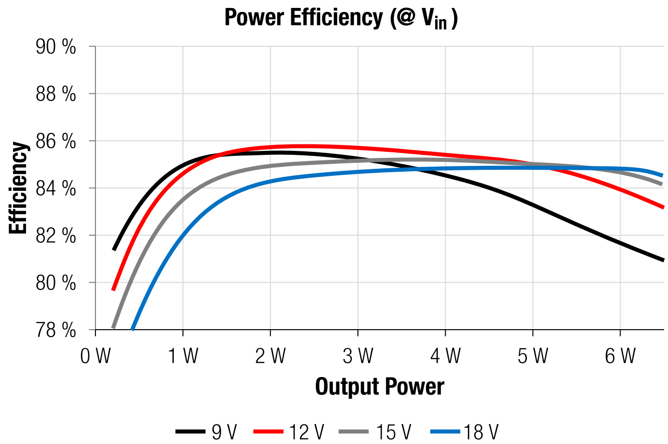


Figure 17: Power efficiency curves

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8 Main waveforms, oscilloscope captures

8.1 Start-up and shut-down (@ full-load)

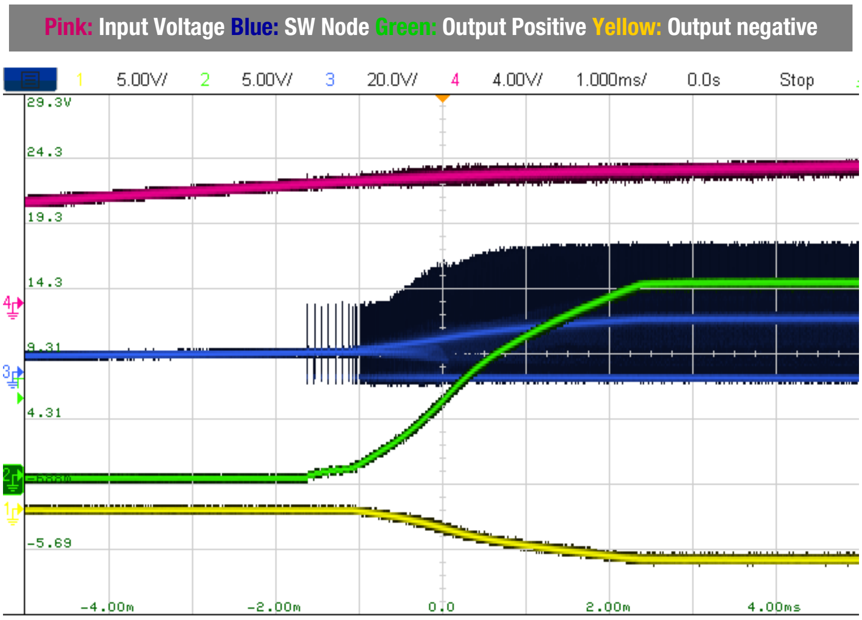

Figure 18: Start-up at full-load

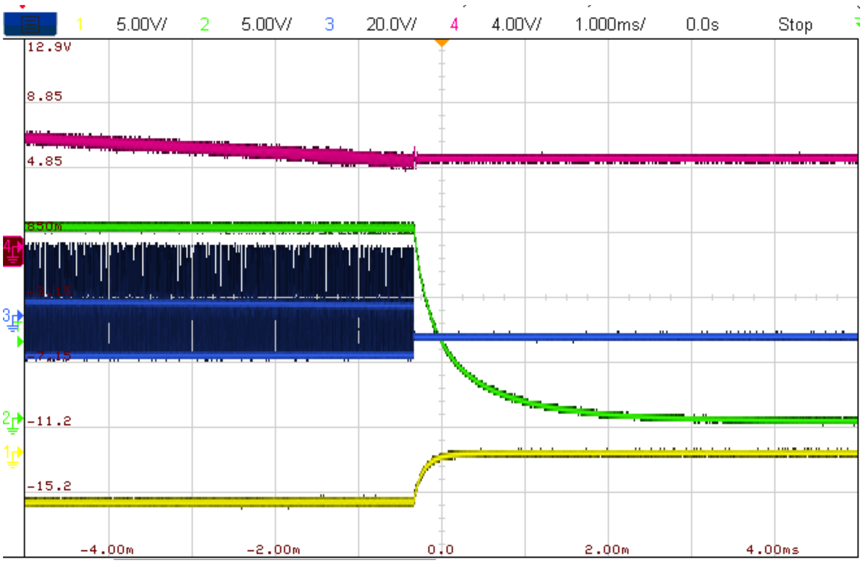

Figure 19: Shut-down at full-load

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8.2 Steady-state operation

8.2.1 Operation mode with load power

Below transformer primary current and SW node characteristic for 1 W and 6 W loads.

Pink: Transfomer Primary Current Blue: SW Node

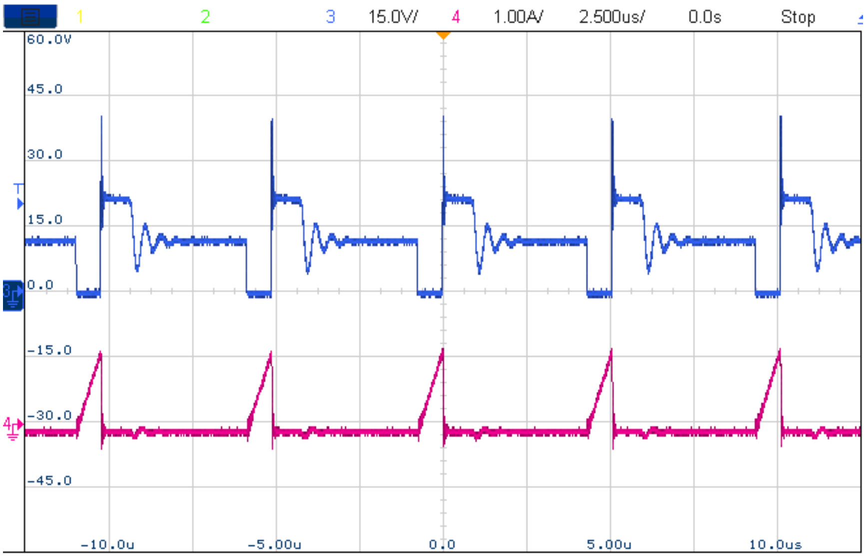

Figure 20: 1 W load (DCM operation)

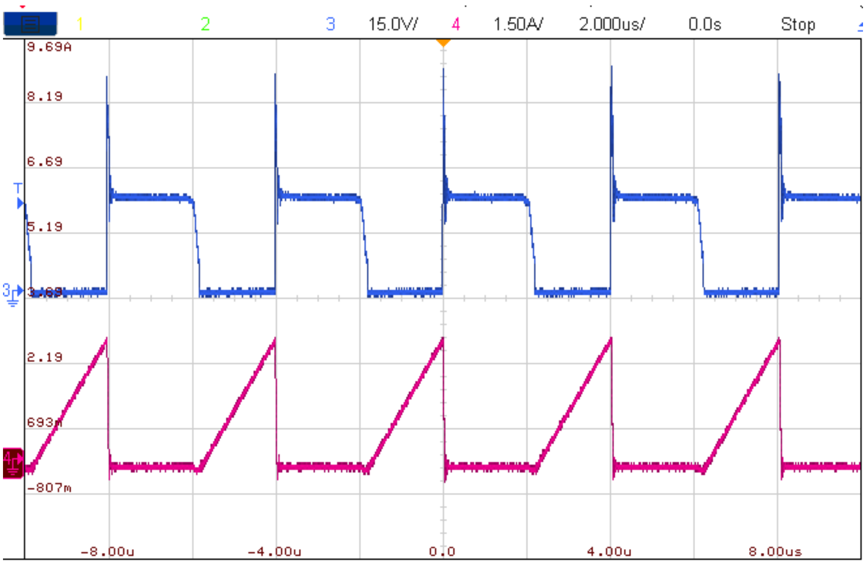

Figure 21: Full load (6 W) (BCM operation)

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8.2.2 SW node clamping and damping snubbers

The SW node voltage must be kept under 65 V (IC integrated MOSFET rating) and any ringing appearing after switch turn-off must be fully damped before 250 ns to correctly sample and regulate the output voltage. Minimum input voltage represents the worst-case scenario in steady-state operation. Oscilloscope captures below under an overload of 6.5 W show maximum SW node voltage of 57.7 V and ringing fully damped before 200 ns, which meets the requirements with margin for tolerance and temperature variations.

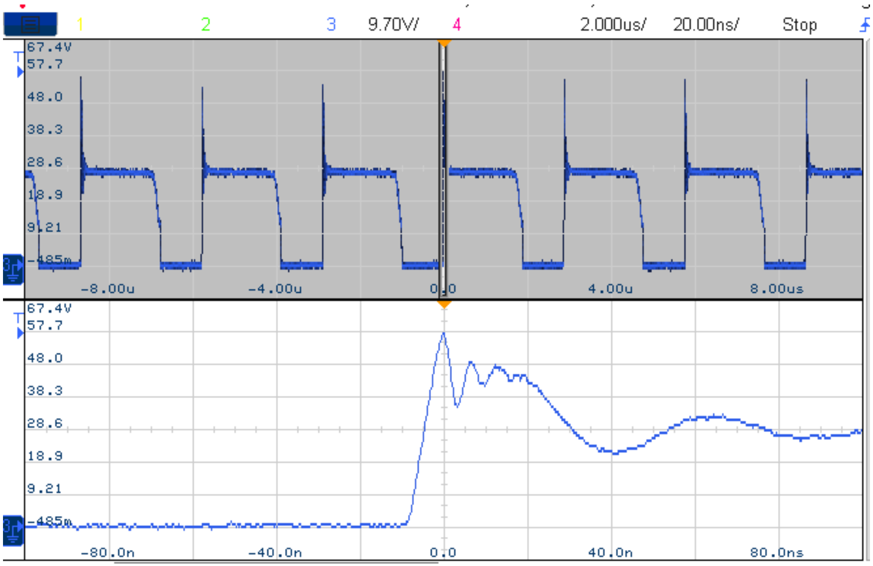

Figure 22: SW Node voltage clamping

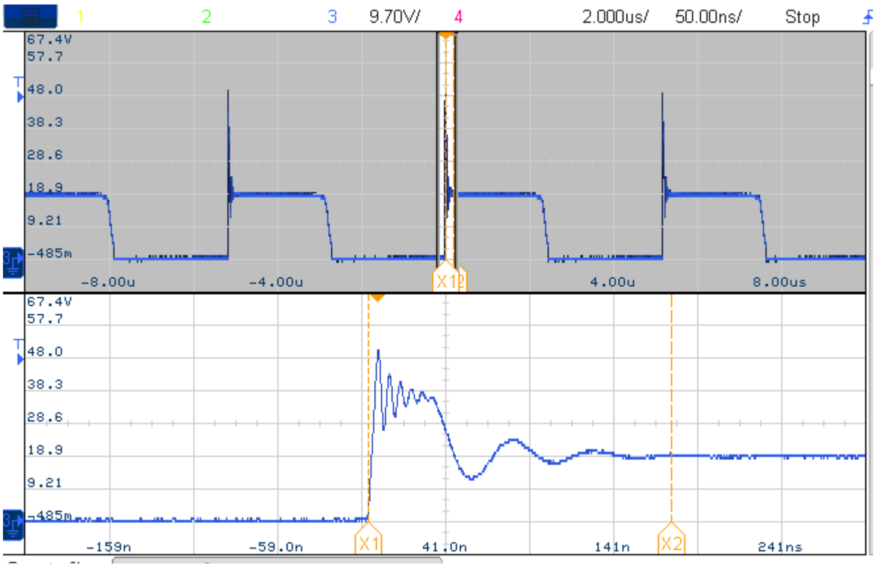

Figure 23: SW Node ringing damping

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8.2.3 Output voltage ripple (at full load)

Experimental results below show how output voltage ripple values at nominal V_{in} = 12 V and full load condition are 250 mVpp for the positive rail (under 2%) and 180 mVpp for negative rail (under 5%). A very cost-effective solution using the same input and output components has been selected. As mentioned in 2.3, this can be modified by the designer as desired, adding more capacitance to further reduce the voltage ripple if required.

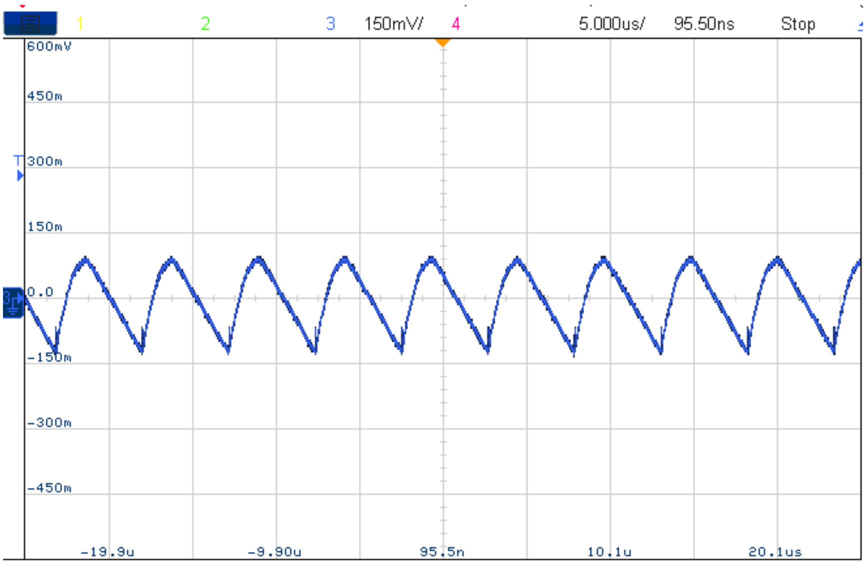

Figure 24: ΔVout. Positive rail (12 V_{in}, 6 W)

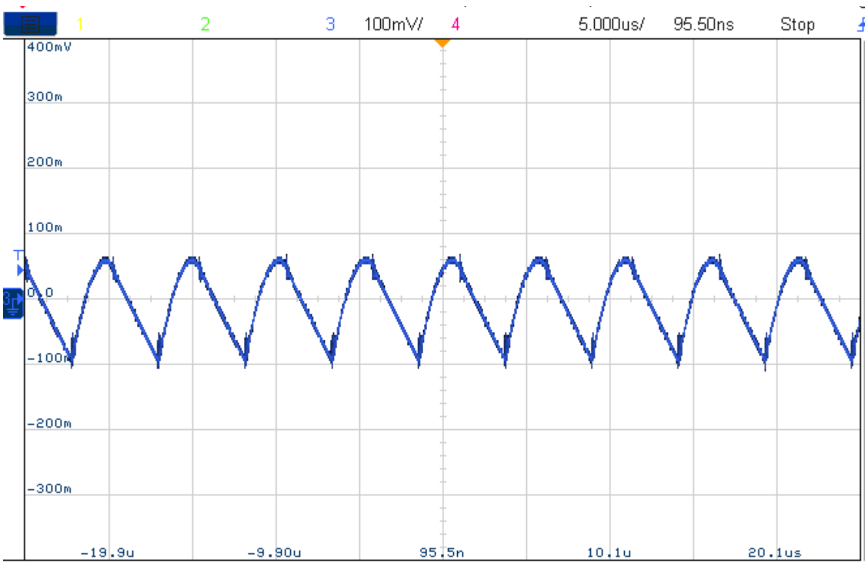

Figure 25: ΔVout. Negative rail (12 V_{in}, 6 W)

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8.2.4 Load short-circuit protection

A load short-circuit condition would represent a scenario of a fault in the system, which can be caused, for instance, by the gate driver transistors or by the SiC-MOSFET having failed short-circuit between gate and source, thus presenting a short-circuit across the auxiliary supply output rails.

In this situation, the LT8302 controller will enter hiccup short-circuit protection mode, limiting maximum peak currents. Worst-case SW node voltage is found at V_{in} = 18 V under this fault scenario. Maximum peak current is 4.65 A (LT8302 limit), and maximum switch voltage around 62 V, both within ratings of WE-AGDT transformer and integrated switch, improving reliability and robustness of the power supply.

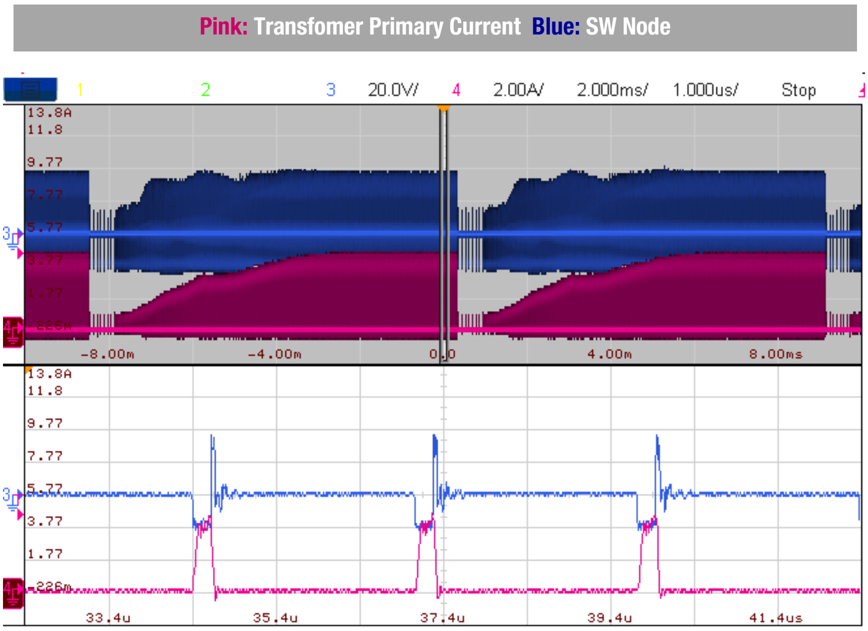


Figure 26: Short-circuit protection at V_{in} = 9 V

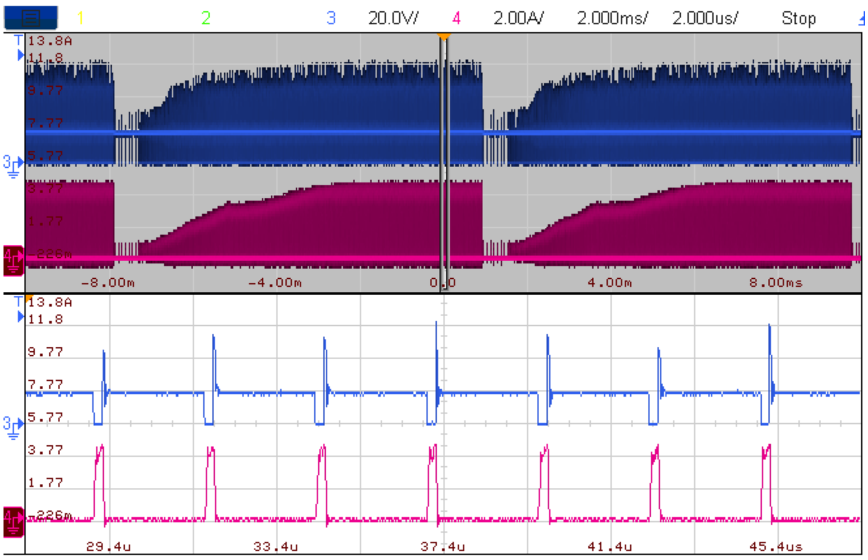


Figure 27: Short-circuit protection at V_{in} = 18 V

9 Thermal performance

Thermal performance results over the full-load range (0.1 to 6 W) at minimum input voltage (V_{in} = 9 V) are exposed in this section. The results correspond to layout Variant-B board, but the thermal performance of Variant-A shows no appreciable difference.

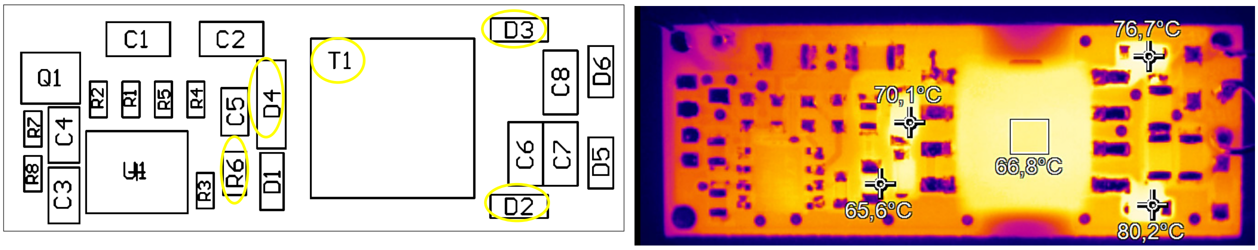


Figure 28: Board components temperature at V_{in} (min) = 9 V (worst-case) and 25 °C ambient

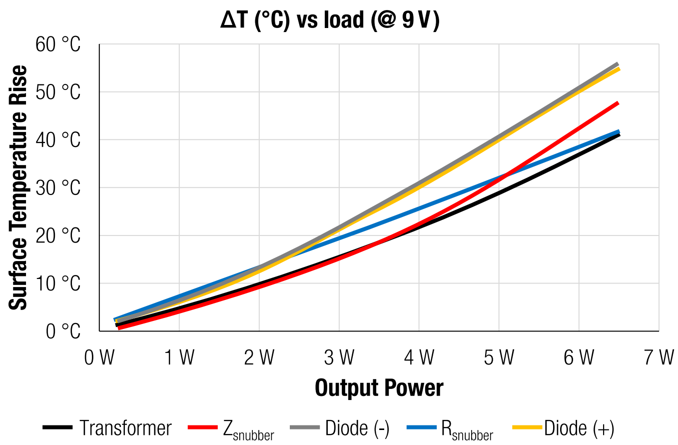


Figure 29: Temperature rise at V_{in} (min) = 9 V (worst-case)

Based on the above results, in order to keep internal/junction component temperatures within maximum ratings, it is recommended not to exceed a maximum ambient temperature of 80 °C (max) under operation for longer lifetime and higher reliability of the application.

If this ambient temperature is exceeded, the output power must be reduced (de-rated) accordingly.

Reference Design

6 W Isolated auxiliary power supply for SiC-MOSFET gate driver

10 EMC performance

EMC test results based on CISPR32-Class B limits are shown below for board variant-A. An input LC filter and a 10 cm x 10 cm copper plane connected to input GND equivalent to chassis as detailed below were added to pass the test. Operating conditions are V_{in} = 12 V with 6 W output resistive load (330 mA current draw per rail).

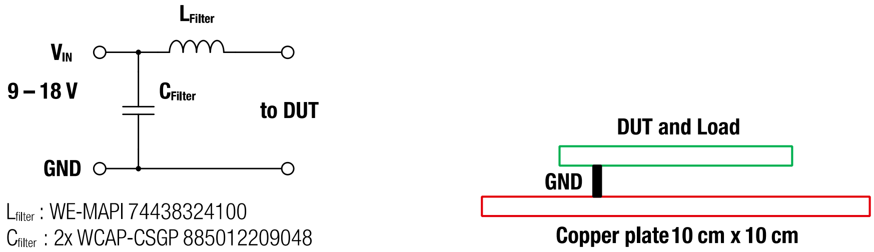


Figure 30: LC filter and copper plane added to pass CE and RE CISPR-32B EMC tests

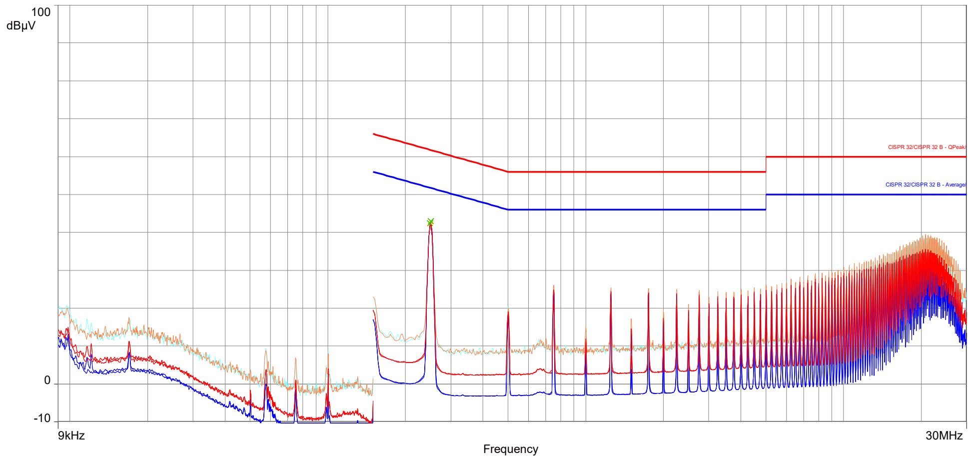


Figure 31: Conducted emissions results (CISPR32 class B limits)

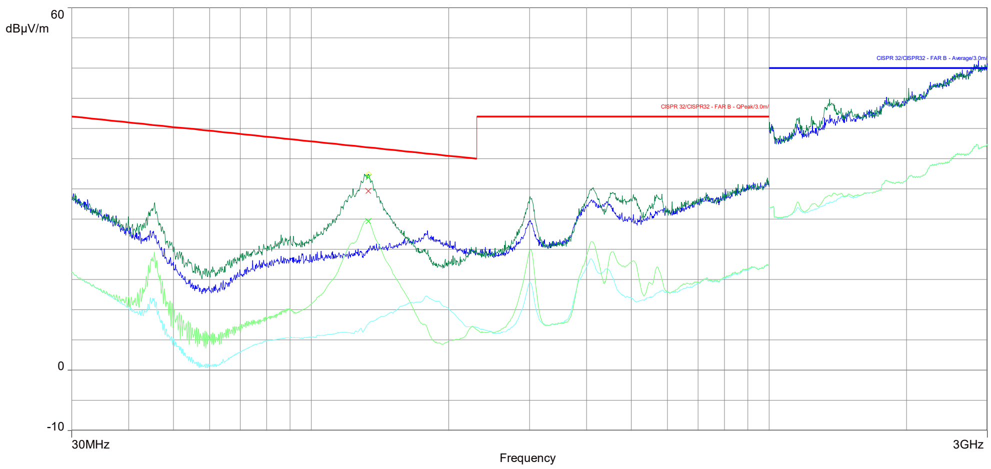


Figure 32: Radiated emissions results (CISPR32 class B limits) (30 cm length input cables)

Reference Design

6 W Isolated auxiliary power supply for SiC-MOSFET gate driver

11 Bill-of-Materials (BoM) Option 1: Standard

Reference designator	Description	Package	Manufacturer	MPN
C1, C2, C6, C7, C8	MLCC 10uF 50V X5R 10%	1206	Würth Elektronik	885012108022
C3, C4	MLCC 1uF 50V X7R 10%	0805	Würth Elektronik	885012207103
C5	MLCC 470nF 50V X7R 10%	0805	Würth Elektronik	885012207102
D1, D2, D3	Barrier Rectifier 1 A, 100 V AEC-Q101	µSMP	Vishay	V1PM10HM3
D4	Zener 27 V, 0.5 W, AEC-Q101	µSMF	Vishay	BZD27C27P
D5	Zener 16 V, 0.5 W, AEC-Q101	µSMF	Vishay	PLZ16BHG3H
D6	Zener 4.8 V, 0.5 W, AEC-Q101	µSMF	Vishay	PLZ4V7BHG3H
R1	Thick Film, 806k, 0.1 W, 1 %, AEC-Q101	0603	Yageo	AC0603FR-07806KL
R2	Thick Film, 232k, 0.1 W, 1 %, AEC-Q101	0603	Yageo	AC0603FR-07232KL
R3	Thin Film, 93.1k, 0.1 W, 0.1 %, AEC-Q200	0603	Panasonic	ERA-3AEB9312V
R4, R7	Thick Film, 10k, 0.1 W, 1 %, AEC-Q101	0603	Yageo	AC0603FR-0710KL
R5 (DNP)	N/A	0603	N/A	N/A
R6	Thick Film, 100, 0.5 W, 5 %, AEC-Q200	0805	Vishay	CRCW0805100RJNEAHP
Q1	MOSFET N-channel, 40 V, AEC-Q101	SOT23-3	Vishay	SQ2318AES-T1_GE3
U1	PSR Flyback Controller 65V 4.5A AEC-Q200	SO-8	ADI / LT	LT8302-HS8E
T1	Transformer dual-output 7uH, 4.5A, 7.5pF AEC-Q200	EP-7	Würth Elektronik	750318131

Table 3. Bill-of-Materials (BoM) Option 1: Standard

Reference Design

6 W Isolated auxiliary power supply for SiC-MOSFET gate driver

WÜRTH ELEKTRONIK

12 Bill-of-Materials (BoM) Option 2: AEC-Q qualified components

Reference designator	Description	Package	Manufacturer	MPN
C1, C2, C6, C7, C8	MLCC 10uF 50V X5R 10% AEC-Q200	1206	Murata	GRT31CR61H106KE01L
C3, C4	MLCC 1uF 50V CGJ 10% AEC-Q200	0805	TDK	CGJ4J3X7R1H105K125AB
C5	MLCC 470nF 50V X7R 10% AEC-Q200	0603	TDK	CGA3E3X7R1H474K080AE
D1, D2, D3	Barrier Rectifier 1 A, 100 V AEC-Q101	µSMP	Vishay	V1PM10HM3
D4	Zener 27 V, 0.5 W, AEC-Q101	µSMF	Vishay	BZD27C27P
D5	Zener 16 V, 0.5 W, AEC-Q101	µSMF	Vishay	PLZ16BHG3H
D6	Zener 4.8 V, 0.5 W, AEC-Q101	µSMF	Vishay	PLZ4V7BHG3H
R1	Thick Film, 806k, 0.1 W, 1 %, AEC-Q101	0603	Yageo	AC0603FR-07806KL
R2	Thick Film, 232k, 0.1 W, 1 %, AEC-Q101	0603	Yageo	AC0603FR-07232KL
R3	Thin Film, 93.1k, 0.1 W, 0.1 %, AEC-Q200	0603	Panasonic	ERA-3AEB9312V
R4, R7	Thick Film, 10k, 0.1 W, 1 %, AEC-Q101	0603	Yageo	AC0603FR-0710KL
R5 (DNP)	N/A	0603	N/A	N/A
R6	Thick Film, 100, 0.5 W, 5 %, AEC-Q200	0805	Vishay	CRCW0805100RJNEAHP
Q1	MOSFET N-channel, 40 V, AEC-Q101	SOT23-3	Vishay	SQ2318AES-T1_GE3
U1	PSR Flyback Controller 65V 4.5A AEC-Q200	SO-8	ADI / LT	LT8302-HS8E
T1	Transformer dual-output 7uH, 4.5A, 7.5pF AEC-Q200	EP-7	Würth Elektronik	750318131

Table 4: Bill-of-Materials (BoM), option 2: AEC-Q qualified components

Reference Design

6 W Isolated auxiliary power supply for SiC-MOSFET gate driver

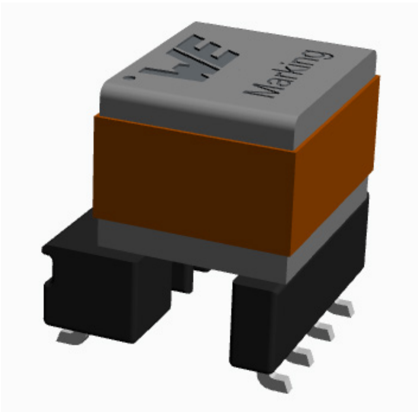
WÜRTH ELEKTRONIK

13 WE-AGDT series

The WE-AGDT (Auxiliary Gate Drive Transformer) series from Würth Elektronik include six transformers, all using a compact EP7 assembly and each optimized for its corresponding reference design. They provide bipolar (+15 V; -4 V) as well as unipolar (15 to 20 V; 0 V) options, with input voltage ranging from 9 to 36 V and maximum output power of 3 to 6 W. They are optimized for SiC applications, but they are also suitable for driving IGBT and power MOSFETs alike, and even high-voltage GaN-FETs with the correct output regulation stage.

Characteristics

- Interwinding capacitance as low as 6.8 pF typical
- Flyback with primary side regulation
- High efficiency and very compact. Surface mount EP7
- Common control voltages for SiC MOSFET
- Wide range input voltages 9 to 36 V
- Safety: IEC62368-1 /IEC61558-2-16
- Basic insulation
- Dielectric insulation up to 4 kV
- Temperature class B
- Reference designs with TI and ADI



Applications

Industrial drives, AC motor inverters, electric vehicle powertrain, battery chargers, solar inverters, data centers, uninterruptible power supplies, active power factor correction, switching power supplies with SiC-MOSFETs.

Order code	V_{in} range (V)	V_{out1} (V)	V_{out2} (V)	C_{w_w} (pF)	Frequency max (kHz)	IC Reference Design	Power (W)
750317893	9 – 18	15 – 20	-	6.8	350	LM5180	3
750317894	9 – 18	15	-4	7.5			
750318207	18 – 36	15 – 20	-	8.2			5
750318208	18 – 36	15	-4	7.0			
750318114	9 – 18	15 – 20	-	6.8		LT8302	6
750318131	9 – 18	15	-4	6.8			

Table 5: WE-AGDT transformer series

Reference Design

6 W Isolated auxiliary power supply for SiC-MOSFET gate driver

WÜRTH ELEKTRONIK

IMPORTANT NOTICE

USEFUL LINKS

Application Notes
www.we-online.com/app-notes

REDEXPERT Design Tool
www.we-online.com/redexpert

Toolbox
www.we-online.com/toolbox

Produkt Katalog
www.we-online.com/products

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