QuickLogic EOS S3 Interrupt Document

Intr Num	NVIC Intr	**Address**	**Exception**	**Priority**	**Comments**
0		0x0	Main SP	NA	M4 Core internal
1		0x4	Reset	-3 (highest)	M4 Core internal
2		0x8	NMI	-2	M4 Core internal
3		0xC	Hard Fault	-1	M4 Core internal
4		0x10	Mem Manage Fault	0-7 (programmable)	M4 Core internal
5		0x14	Bus Fault	0-7 (programmable)	M4 Core internal
6		0x18	Usage Fault	0-7 (programmable)	M4 Core internal
7		0x1C	Reserved	0-7 (programmable)	M4 Core internal
8		0x20	Reserved	0-7 (programmable)	M4 Core internal
9		0x24	Reserved	0-7 (programmable)	M4 Core internal
10		0x28	Reserved	0-7 (programmable)	M4 Core internal
11		0x2C	SVC	0-7 (programmable)	M4 Core internal
12		0x30	Debug Monitor	0-7 (programmable)	M4 Core internal
13		0x34	Reserved	0-7 (programmable)	M4 Core internal
14		0x38	Pend SV	0-7 (programmable)	M4 Core internal
15		0x3C	SysTick	0-7 (programmable)	M4 Core internal
16	0	0x40	Software Interrupt 2	0-7 (programmable)	SoC WIC interrupts
17	1	0x44	Software Interrupt 1	0-7 (programmable)	SoC WIC interrupts
18	2	0x48	Reserved	0-7 (programmable)	SoC WIC interrupts
19	3	0x4C	FFE0 Message	0-7 (programmable)	SoC WIC interrupts
20	4	0x50	Fabric Message	0-7 (programmable)	SoC WIC interrupts
21	5	0x54	Sensor/GPIO	0-7 (programmable)	SoC WIC interrupts
22	6	0x58	M4 SRAM Sleep	0-7 (programmable)	SoC WIC interrupts
23	7	0x5C	UART	0-7 (programmable)	SoC WIC interrupts
24	8	0x60	TIMER	0-7 (programmable)	SoC WIC interrupts
25	9	0x64	CPU WDOG_INTR	0-7 (programmable)	SoC WIC interrupts
26	10	0x68	CPU WDOG_RST	0-7 (programmable)	SoC WIC interrupts
27	11	0x6C	Bus Timeout	0-7 (programmable)	SoC WIC interrupts
28	12	0x70	FPU	0-7 (programmable)	SoC WIC interrupts
29	13	0x74	PKFB	0-7 (programmable)	SoC WIC interrupts
30	14	0x78	I2S	0-7 (programmable)	SoC WIC interrupts
31	15	0x7C	Audio	0-7 (programmable)	SoC WIC interrupts
32	16	0x80	SPI_MS	0-7 (programmable)	SoC WIC interrupts
33	17	0x84	CFG_DMA	0-7 (programmable)	SoC WIC interrupts

34	18	0x88	PMU Timer	0-7 (programmable)	SoC WIC interrupts
35	19	0x8C	ADC Done	0-7 (programmable)	SoC WIC interrupts
36	20	0x90	RTC Alarm	0-7 (programmable)	SoC WIC interrupts
37	21	0x94	Reset Interrupt	0-7 (programmable)	SoC WIC interrupts
38	22	0x98	FFE0 Combined	0-7 (programmable)	SoC WIC interrupts
39	23	0x9C	FFE WDT	0-7 (programmable)	SoC WIC interrupts
40	24	0xA0	AP Boot	0-7 (programmable)	SoC WIC interrupts
41	25	0xA4	LDO30 PG INTR	0-7 (programmable)	SoC WIC interrupts
42	26	0xA8	LDO50 PG INTR	0-7 (programmable)	SoC WIC interrupts
43	27	0xAC	128KB SRAM TIMEOUT	0-7 (programmable)	SoC WIC interrupts
44	28	0xB0	LPSD Voice Det	0-7 (programmable)	SoC WIC interrupts
45	29	0xB4	DMIC Voice Det	0-7 (programmable)	SoC WIC interrupts
46	30	0xB8	*Reserved*	0-7 (programmable)	SoC WIC interrupts
47	31	0xBC	**SDMA_DONE[11:1]*	0-7 (programmable)	SoC WIC interrupts
48	32	0xC0		0-7 (programmable)	SoC WIC interrupts
49	33	0xC4		0-7 (programmable)	SoC WIC interrupts
50	34	0xC8		0-7 (programmable)	SoC WIC interrupts
51	35	0xCC		0-7 (programmable)	SoC WIC interrupts
52	36	0xD0		0-7 (programmable)	SoC WIC interrupts
53	37	0xD4		0-7 (programmable)	SoC WIC interrupts
54	38	0xD8		0-7 (programmable)	SoC WIC interrupts
55	39	0xDC		0-7 (programmable)	SoC WIC interrupts
56	40	0xE0		0-7 (programmable)	SoC WIC interrupts
57	41	0xE4		0-7 (programmable)	SoC WIC interrupts
58	42	0xE8	*AP_PDM_CLK_ON*	0-7 (programmable)	SoC non-WIC interrupts
59	43	0xEC	*AP_PDM_CLK_OFF*	0-7 (programmable)	SoC non-WIC interrupts
60	44	0xF0	*DMAC0_BLK_DONE*	0-7 (programmable)	SoC non-WIC interrupts
61	45	0xF4	*DMAC0_BUF_DONE*	0-7 (programmable)	SoC non-WIC interrupts
62	46	0xF8	*DMAC1_BLK_DONE*	0-7 (programmable)	SoC non-WIC interrupts
63	47	0xFC	*DMAC1_BUF_DONE*	0-7 (programmable)	SoC non-WIC interrupts
64	48	0x100	*SDMA_DONE[0]*	0-7 (programmable)	SoC non-WIC interrupts
65	49	0x104	*SDMA_ERR*	0-7 (programmable)	SoC non-WIC interrupts
66	50	0x108	*I2SSLV_M4_tx_or_intr*	0-7 (programmable)	SoC non-WIC interrupts
67	51	0x10C	*LPSD_VOICE_OFF*	0-7 (programmable)	SoC non-WIC interrupts
68	52	0x110	*DMIC_VOICE_OFF*	0-7 (programmable)	SoC non-WIC interrupts
69	53	0x114	*Reserved*	0-7 (programmable)	SoC non-WIC interrupts
70	54	0x118	*Reserved*	0-7 (programmable)	SoC non-WIC interrupts
71	55	0x11C	*Reserved*	0-7 (programmable)	SoC non-WIC interrupts
…					
255		0x3FF	*Reserved*	0-7 (programmable)	

All interrupts to M4 will be connected to M4's NVIC. There are 2 levels of interrupt masking and clearing. One will be at the source of interrupts, and the other at the top level interrupt controller.

*Note: SDMA_DONE is a one dma_clk pulse interrupt. They can be used as wake up interrupt source to M4. They are not latched, and thus there is no need for ISR to clear/service them.

External CPU Interrupts

- Floating Point Unit (FPU) Interrupts
  There are 6 different FPU interrupts generated by the M4, but they are not necessarily always an interrupt source. All 6 interrupts are individually masked so each can be enabled as needed, and a combined interrupt is created with its own mask is connected to the NVIC of the M4. The status can be read and cleared (0x4000_4830[6]), and can be masked (0x4000_4834[6] for Host), and (0x4000_4838[6] for M4).
  Below are the individual interrupt sources.
  i. FPIXC
  ii. FPOFC
  iii. FPUFC
  iv. FPIOC
  v. FPDZC
  vi. FPIDC

- Bus Timeout
  There are different timeouts on the bus/bridge, each individually masked with a combined interrupt to NVIC. The status can be read and cleared (0x4000_4830[5]), and can be masked (0x4000_4834[5] for Host), and (0x4000_4838[5] for M4).
  Below are the individual interrupt sources.
  i. ExtRegM4
  ii. Fabric
  iii. FFE
  iv. M4 SRAM 1
  v. M4 SRAM 2
  vi. M4 SRAM 3

- UART
  These interrupts are triggered from ARM's PL011 UART. The status can be read and cleared (0x4000_4830[1]), and can be masked (0x4000_4834[1] for Host), and (0x4000_4838[1] for M4).
  Below are the individual interrupt sources.
  i. UARTOEINTR
  ii. UARTBEINTR
  iii. UARTPEINTR
  iv. UARTFEINTR

- Timer
  Interrupt triggered when a timer counts down to 0. The status can be read and cleared (0x4000_4830[2]), and can be masked (0x4000_4834[2] for Host), and (0x4000_4838[2] for M4).
  Below are the individual interrupt sources.

- Watchdog
  Software can enable the watchdog timer, and upon counting down to 0, an interrupt will be triggered. If the interrupt is not cleared, a reset will be triggered. The status can be read and cleared (0x4000_4830[4:3]), and can be masked (0x4000_4834[4:3] for Host), and (0x4000_4838[4:3] for M4).
  Below are the individual interrupt sources.
  i. WDT_INTR
  ii. WDT_RST

- M4 SRAM Low Power Interrupt
  Interrupt triggered when any segment of the 32KB (12 instances) M4 memory is accessed when the memory is in lower power state (deep sleep or shut down). The status can be read and cleared (0x4000_4830[0]), and can be masked (0x4000_4834[0] for Host), and (0x4000_4838[0] for M4).

INTR_CTRL Registers

Base Address: 0x40004800

Offset	Register Name	Default
0x<000	GPIO_INTR	
0x004	GPIO_INTR_RAW	
0x008	GPIO_INTR_TYPE	
0x00C	GPIO_INTR_POL	
0x010	GPIO_INTR_EN_AP	
0x014	GPIO_INTR_EN_M4	
0x018	GPIO_INTR_EN_FFE0	
0x01C	GPIO_INTR_EN_FFE1	
0x030	OTHER_INTR	
0x034	OTHER_INTR_EN_AP	
0x038	OTHER_INTR_EN_M4	
0x040	SOFTWARE_INTR_1	
0x044	SOFTWARE_INTR_1_EN_AP	
0x048	SOFTWARE_INTR_1_EN_M4	
0x050	SOFTWARE_INTR_2	
0x054	SOFTWARE_INTR_2_EN_AP	
0x058	SOFTWARE_INTR_2_EN_M4	
0x060	FFE_INTR	
0x064	FFE_INTR_EN_AP	
0x068	FFE_INTR_EN_M4	
0x070	FFE1_FB_INTR	
0x074	FFE1_FB_INTR_EN_AP	
0x078	FFE1_FB_INTR_EN_M4	
0x0080	FB_INTR	
0x0084	FB_INTR_RAW	

0x088	FB_INTR_TYPE	
0x08C	FB_INTR_POL	
0x090	FB_INTR_EN_AP	
0x094	FB_INTR_EN_M4	

INTR_CTRL.GPIO_INTR

Base Address: 0x40004800 Offset Address: 0x000 Default Value:

Register Description:

Field	Bits	Type	Default	Description
GPIO_7_INTR	7	RW1C	0x0	Active high edge interrupt detected for GPIO_7. When interrupt type is selected as edge detect, this register will return high when triggered, write 1 to clear.
GPIO_6_INTR	6	RW1C	0x0	Active high edge interrupt detected for GPIO_6. When interrupt type is selected as edge detect, this register will return high when triggered, write 1 to clear.
GPIO_5_INTR	5	RW1C	0x0	Active high edge interrupt detected for GPIO_5. When interrupt type is selected as edge detect, this register will return high when triggered, write 1 to clear.
GPIO_4_INTR	4	RW1C	0x0	Active high edge interrupt detected for GPIO_4. When interrupt type is selected as edge detect, this register will return high when triggered, write 1 to clear.
GPIO_3_INTR	3	RW1C	0x0	Active high edge interrupt detected for GPIO_3. When interrupt type is selected as edge detect, this register will return high when triggered, write 1 to clear.
GPIO_2_INTR	2	RW1C	0x0	Active high edge interrupt detected for GPIO_2. When interrupt type is selected as edge detect, this register will return high when triggered, write 1 to clear.
GPIO_1_INTR	1	RW1C	0x0	Active high edge interrupt detected for GPIO_1. When interrupt type is selected as edge detect, this register will return high when triggered, write 1 to clear.
GPIO_0_INTR	0	RW1C	0x0	Active high edge interrupt detected for GPIO_0. When interrupt type is selected as edge detect, this register will return high when triggered, write 1 to clear.

INTR_CTRL.GPIO_INTR_RAW

Base Address: 0x40004800 Offset Address: 0x004 Default Value:

Register Description:

Field	Bits	Type	Default	Description
GPIO_7_INTR_RAW	7	RO	0x0	Raw interrupt for GPIO_7. This register will reflect the value of the IO regardless of the type/polarity
GPIO_6_INTR_RAW	6	RO	0x0	Raw interrupt for GPIO_6. This register will reflect the value of the IO regardless of the type/polarity

GPIO_5_INTR_RAW	5	RO	0x0	Raw interrupt for GPIO_5. This register will reflect the value of the IO regardless of the type/polarity
GPIO_4_INTR_RAW	4	RO	0x0	Raw interrupt for GPIO_4. This register will reflect the value of the IO regardless of the type/polarity
GPIO_3_INTR_RAW	3	RO	0x0	Raw interrupt for GPIO_3. This register will reflect the value of the IO regardless of the type/polarity
GPIO_2_INTR_RAW	2	RO	0x0	Raw interrupt for GPIO_2. This register will reflect the value of the IO regardless of the type/polarity
GPIO_1_INTR_RAW	1	RO	0x0	Raw interrupt for GPIO_1. This register will reflect the value of the IO regardless of the type/polarity
GPIO_0_INTR_RAW	0	RO	0x0	Raw interrupt for GPIO_0. This register will reflect the value of the IO regardless of the type/polarity

INTR_CTRL.GPIO_INTR_TYPE

Base Address: 0x40004800 Offset Address: 0x008 Default Value:

Register Description:

Field	Bits	Type	Default	Description
GPIO_7_INTR_TYPE	7	RW	0x0	GPIO_7 interrupt type 0: level 1: edge
GPIO_6_INTR_TYPE	6	RW	0x0	GPIO_6 interrupt type 0: level 1: edge
GPIO_5_INTR_TYPE	5	RW	0x0	GPIO_5 interrupt type 0: level 1: edge
GPIO_4_INTR_TYPE	4	RW	0x0	GPIO_4 interrupt type 0: level 1: edge
GPIO_3_INTR_TYPE	3	RW	0x0	GPIO_3 interrupt type 0: level 1: edge
GPIO_2_INTR_TYPE	2	RW	0x0	GPIO_2 interrupt type 0: level 1: edge
GPIO_1_INTR_TYPE	1	RW	0x0	GPIO_1 interrupt type 0: level 1: edge
GPIO_0_INTR_TYPE	0	RW	0x0	GPIO_0 interrupt type 0: level 1: edge

INTR_CTRL.GPIO_INTR_POL

Base Address: 0x40004800 Offset Address: 0x00C Default Value:

Register Description:

Field	Bits	Type	Default	Description
GPIO_7_INTR_POL	7	RW	0x0	GPIO_7 interrupt POL (depends on interrupt type) 0x008 = 0 0:low 1:hi 0x008 = 1

				0:fall 1:rise
GPIO_6_INTR_POL	6	RW	0x0	GPIO_6 interrupt POL (depends on interrupt type) 0x008 = 0 0:low 1:hi 0x008 = 1 0:fall 1:rise
GPIO_5_INTR_POL	5	RW	0x0	GPIO_5 interrupt POL (depends on interrupt type) 0x008 = 0 0:low 1:hi 0x008 = 1 0:fall 1:rise
GPIO_4_INTR_POL	4	RW	0x0	GPIO_4 interrupt POL (depends on interrupt type) 0x008 = 0 0:low 1:hi 0x008 = 1 0:fall 1:rise
GPIO_3_INTR_POL	3	RW	0x0	GPIO_3 interrupt POL (depends on interrupt type) 0x008 = 0 0:low 1:hi 0x008 = 1 0:fall 1:rise
GPIO_2_INTR_POL	2	RW	0x0	GPIO_2 interrupt POL (depends on interrupt type) 0x008 = 0 0:low 1:hi 0x008 = 1 0:fall 1:rise
GPIO_1_INTR_POL	1	RW	0x0	GPIO_1 interrupt POL (depends on interrupt type) 0x008 = 0 0:low 1:hi 0x008 = 1 0:fall 1:rise
GPIO_0_INTR_POL	0	RW	0x0	GPIO_0 interrupt POL (depends on interrupt type) 0x008 = 0 0:low 1:hi 0x008 = 1 0:fall 1:rise

INTR_CTRL.GPIO_INTR_EN_AP

Base Address: 0x40004800 Offset Address: 0x010 Default Value:

Register Description:

Field	Bits	Type	Default	Description
GPIO_7_INTR_EN_AP	7	RW	0x0	GPIO_7 interrupt enable for AP 0: disable 1: enable
GPIO_6_INTR_EN_AP	6	RW	0x0	GPIO_6 interrupt enable for AP 0: disable 1: enable
GPIO_5_INTR_EN_AP	5	RW	0x0	GPIO_5 interrupt enable for AP 0: disable 1: enable
GPIO_4_INTR_EN_AP	4	RW	0x0	GPIO_4 interrupt enable for AP 0: disable 1: enable

GPIO_3_INTR_EN_AP	3	RW	0x0	GPIO_3 interrupt enable for AP 0: disable 1: enable
GPIO_2_INTR_EN_AP	2	RW	0x0	GPIO_2 interrupt enable for AP 0: disable 1: enable
GPIO_1_INTR_EN_AP	1	RW	0x0	GPIO_1 interrupt enable for AP 0: disable 1: enable
GPIO_0_INTR_EN_AP	0	RW	0x0	GPIO_0 interrupt enable for AP 0: disable 1: enable

INTR_CTRL.GPIO_INTR_EN_M4

Base Address: 0x40004800 Offset Address: 0x014 Default Value:

Register Description:

Field	Bits	Type	Default	Description
GPIO_7_INTR_EN_M4	7	RW	0x0	GPIO_7 interrupt enable for M4 0: disable 1: enable
GPIO_6_INTR_EN_M4	6	RW	0x0	GPIO_6 interrupt enable for M4 0: disable 1: enable
GPIO_5_INTR_EN_M4	5	RW	0x0	GPIO_5 interrupt enable for M4 0: disable 1: enable
GPIO_4_INTR_EN_M4	4	RW	0x0	GPIO_4 interrupt enable for M4 0: disable 1: enable
GPIO_3_INTR_EN_M4	3	RW	0x0	GPIO_3 interrupt enable for M4 0: disable 1: enable
GPIO_2_INTR_EN_M4	2	RW	0x0	GPIO_2 interrupt enable for M4 0: disable 1: enable
GPIO_1_INTR_EN_M4	1	RW	0x0	GPIO_1 interrupt enable for M4 0: disable 1: enable
GPIO_0_INTR_EN_M4	0	RW	0x0	GPIO_0 interrupt enable for M4 0: disable 1: enable

INTR_CTRL.GPIO_INTR_EN_FFE0

Base Address: 0x40004800 Offset Address: 0x018 Default Value:

Register Description:

Field	Bits	Type	Default	Description
GPIO_7_INTR_EN_FFE0	7	RW	0x0	GPIO_7 interrupt enable for FFE0 0: disable 1: enable

GPIO_6_INTR_EN_FFE0	6	RW	0x0	GPIO_6 interrupt enable for FFE0 0: disable 1: enable
GPIO_5_INTR_EN_FFE0	5	RW	0x0	GPIO_5 interrupt enable for FFE0 0: disable 1: enable
GPIO_4_INTR_EN_FFE0	4	RW	0x0	GPIO_4 interrupt enable for FFE0 0: disable 1: enable
GPIO_3_INTR_EN_FFE0	3	RW	0x0	GPIO_3 interrupt enable for FFE0 0: disable 1: enable
GPIO_2_INTR_EN_FFE0	2	RW	0x0	GPIO_2 interrupt enable for FFE0 0: disable 1: enable
GPIO_1_INTR_EN_FFE0	1	RW	0x0	GPIO_1 interrupt enable for FFE0 0: disable 1: enable
GPIO_0_INTR_EN_FFE0	0	RW	0x0	GPIO_0 interrupt enable for FFE0 0: disable 1: enable

INTR_CTRL.GPIO_INTR_EN_FFE1

Base Address: 0x40004800 Offset Address: 0x01C Default Value:

Register Description:

Field	Bits	Type	Default	Description
GPIO_7_INTR_EN_FFE1	7	RW	0x0	GPIO_7 interrupt enable for FFE1 0: disable 1: enable
GPIO_6_INTR_EN_FFE1	6	RW	0x0	GPIO_6 interrupt enable for FFE1 0: disable 1: enable
GPIO_5_INTR_EN_FFE1	5	RW	0x0	GPIO_5 interrupt enable for FFE1 0: disable 1: enable
GPIO_4_INTR_EN_FFE1	4	RW	0x0	GPIO_4 interrupt enable for FFE1 0: disable 1: enable
GPIO_3_INTR_EN_FFE1	3	RW	0x0	GPIO_3 interrupt enable for FFE1 0: disable 1: enable
GPIO_2_INTR_EN_FFE1	2	RW	0x0	GPIO_2 interrupt enable for FFE1 0: disable 1: enable
GPIO_1_INTR_EN_FFE1	1	RW	0x0	GPIO_1 interrupt enable for FFE1 0: disable 1: enable
GPIO_0_INTR_EN_FFE1	0	RW	0x0	GPIO_0 interrupt enable for FFE1 0: disable 1: enable

INTR_CTRL.OTHER_INTR

Base Address: 0x40004800 Offset Address: 0x030 Default Value:

Register Description:

Field	Bits	Type	Default	Description
WDT FFE	17	RW1C	0x0	Interrupt detected for WDT FFE
FFE0_INTR_OTHERS	16	RW1C	0x0	Interrupt detected for FFE0 other interrupts
RST_INTR	15	RW1C	0x0	Interrupt detected for Reset
RTC_INTR	14	RW1C	0x0	Interrupt detected for RTC
ADC_INTR	13	RW1C	0x0	Interrupt detected for ADC
PMU_TMR_INTR	12	RW1C	0x0	Interrupt detected for PMU Timer
CFG_DMA_DONE	11	RW1C	0x0	Interrupt detected for Config DMA
SPI_MS_INTR	10	RW1C	0x0	Interrupt detected for SPI Master
AUD_INTR	9	RW1C	0x0	Interrupt detected for Audio
I2S_INTR	8	RW1C	0x0	Interrupt detected for I2S
PKFB_INTR	7	RW1C	0x0	Interrupt detected for Packet FIFO Bank
FPU_INTR	6	RW1C	0x0	Interrupt detected for M4 FPU
TIMEOUT_INTR	5	RW1C	0x0	Interrupt detected for bus timeout
WDOG_RST	4	RW1C	0x0	Interrupt detected for WDT M4 Reset
WDOG_INTR	3	RW1C	0x0	Interrupt detected for WDT M4
TIMER_INTR	2	RW1C	0x0	Interrupt detected for timer
UART_INTR	1	RW1C	0x0	Interrupt detected for UART
M4_SRAM_INTR	0	RW1C	0x0	Interrupt detected for M4 SRAM (acccess during low power)

INTR_CTRL.OTHER_INTR_EN_AP

Base Address: 0x40004800 Offset Address: 0x034 Default Value:

Register Description:

Field	Bits	Type	Default	Description
WDT FFE_EN_AP	17	RW	0x0	WDT FFE interrupt enable for AP 0: disable 1: enable
FFE0_INTR_OTHERS_EN_AP	16	RW	0x0	FFE0 Other interrupt enable for AP 0: disable 1: enable
RST_INTR_EN_AP	15	RW	0x0	Reset interrupt enable for AP 0: disable 1: enable
RTC_INTR_EN_AP	14	RW	0x0	RTC interrupt enable for AP 0: disable 1: enable
ADC_INTR_EN_AP	13	RW	0x0	ADC interrupt enable for AP 0: disable 1: enable
PMU_TMR_INTR_EN_AP	12	RW	0x0	PMU Timer interrupt enable for AP 0: disable 1: enable
CFG_DMA_DONE_EN_AP	11	RW	0x0	Config DMA interrupt enable for AP 0: disable 1: enable
SPI_MS_INTR_EN_AP	10	RW	0x0	SPI Master interrupt enable for AP

				0: disable 1: enable
AUD_INTR_EN_AP	9	RW	0x0	Audio interrupt enable for AP 0: disable 1: enable
I2S_INTR_EN_AP	8	RW	0x0	I2S interrupt enable for AP 0: disable 1: enable
PKFB_INTR_EN_AP	7	RW	0x0	PKFB interrupt enable for AP 0: disable 1: enable
FPU_INTR_EN_AP	6	RW	0x0	FPU interrupt enable for AP 0: disable 1: enable
TIMEOUT_INTR_EN_AP	5	RW	0x0	Bus Timeout interrupt enable for AP 0: disable 1: enable
WDOG_RST_EN_AP	4	RW	0x0	Watchdog Reset enable for AP 0: disable 1: enable
WDOG_INTR_EN_AP	3	RW	0x0	WDT M4 interrupt enable for AP 0: disable 1: enable
TIMER_INTR_EN_AP	2	RW	0x0	Timer interrupt enable for AP 0: disable 1: enable
UART_INTR_EN_AP	1	RW	0x0	UART interrupt enable for AP 0: disable 1: enable
M4_SRAM_INTR_EN_AP	0	RW	0x0	M4 SRAM interrupt enable for AP 0: disable 1: enable

INTR_CTRL.OTHER_INTR_EN_M4

Base Address: 0x40004800 Offset Address: 0x038 Default Value:

Register Description:

Field	Bits	Type	Default	Description
WDT FFE_EN_M4	17	RW	0x0	WDT FFE interrupt enable for M4 0: disable 1: enable
FFE0_INTR_OTHERS_EN_M4	16	RW	0x0	FFE0 Other interrupt enable for M4 0: disable 1: enable
RST_INTR_EN_M4	15	RW	0x0	Reset interrupt enable for M4 0: disable 1: enable
RTC_INTR_EN_M4	14	RW	0x0	RTC interrupt enable for M4 0: disable 1: enable
ADC_INTR_EN_M4	13	RW	0x0	ADC interrupt enable for M4 0: disable 1: enable

PMU_TMR_INTR_EN_M4	12	RW	0x0	PMU Timer interrupt enable for M4 0: disable 1: enable
CFG_DMA_DONE_EN_M4	11	RW	0x0	Config DMA interrupt enable for M4 0: disable 1: enable
SPI_MS_INTR_EN_M4	10	RW	0x0	SPI Master interrupt enable for M4 0: disable 1: enable
AUD_INTR_EN_M4	9	RW	0x0	Audio interrupt enable for M4 0: disable 1: enable
I2S_INTR_EN_M4	8	RW	0x0	I2S interrupt enable for M4 0: disable 1: enable
PKFB_INTR_EN_M4	7	RW	0x0	PKFB interrupt enable for M4 0: disable 1: enable
FPU_INTR_EN_M4	6	RW	0x0	FPU interrupt enable for M4 0: disable 1: enable
TIMEOUT_INTR_EN_M4	5	RW	0x0	Bus Timeout interrupt enable for M4 0: disable 1: enable
WDOG_RST_EN_M4	4	RW	0x0	Watchdog Reset enable for M4 0: disable 1: enable
WDOG_INTR_EN_M4	3	RW	0x0	WDT M4 interrupt enable for M4 0: disable 1: enable
TIMER_INTR_EN_M4	2	RW	0x0	Timer interrupt enable for M4 0: disable 1: enable
UART_INTR_EN_M4	1	RW	0x0	UART interrupt enable for M4 0: disable 1: enable
M4_SRAM_INTR_EN_M4	0	RW	0x0	M4 SRAM interrupt enable for M4 0: disable 1: enable

INTR_CTRL.SOFTWARE_INTR_1

Base Address: 0x40004800 Offset Address: 0x040 Default Value:
Register Description:

Field	Bits	Type	Default	Description
SW_INTR_1	0	RW	0x0	General purpose interrupt (can be used for AP-M4 interrupt)

INTR_CTRL.SOFTWARE_INTR_1_EN_AP

Base Address: 0x40004800 Offset Address: 0x044 Default Value:
Register Description:

Field	Bits	Type	Default	Description
SW_INTR_1_EN_AP	0	RW	0x0	General purpose interrupt (can be used for AP-M4 interrupt)

INTR_CTRL.SOFTWARE_INTR_1_EN_M4

Base Address: 0x40004800 Offset Address: 0x048 Default Value:

Register Description:

Field	Bits	Type	Default	Description
SW_INTR_1_EN_M4	0	RW	0x0	General purpose interrupt (can be used for AP-M4 interrupt)

INTR_CTRL.SOFTWARE_INTR_2

Base Address: 0x40004800 Offset Address: 0x050 Default Value:

Register Description:

Field	Bits	Type	Default	Description
SW_INTR_2	0	RW	0x0	General purpose interrupt (can be used for AP-M4 interrupt)

INTR_CTRL.SOFTWARE_INTR_2_EN_AP

Base Address: 0x40004800 Offset Address: 0x054 Default Value:

Register Description:

Field	Bits	Type	Default	Description
SW_INTR_2_EN_AP	0	RW	0x0	General purpose interrupt (can be used for AP-M4 interrupt)

INTR_CTRL.SOFTWARE_INTR_2_EN_M4

Base Address: 0x40004800 Offset Address: 0x058 Default Value:

Register Description:

Field	Bits	Type	Default	Description
SW_INTR_2_EN_M4	0	RW	0x0	General purpose interrupt (can be used for AP-M4 interrupt)

INTR_CTRL.FFE_INTR

Base Address: 0x40004800 Offset Address: 0x060 Default Value:

Register Description:

Field	Bits	Type	Default	Description
FFE0_7_INTR	7	RW1C	0x0	Interrupt detected for FFE0_7
FFE0_6_INTR	6	RW1C	0x0	Interrupt detected for FFE0_6
FFE0_5_INTR	5	RW1C	0x0	Interrupt detected for FFE0_5
FFE0_4_INTR	4	RW1C	0x0	Interrupt detected for FFE0_4
FFE0_3_INTR	3	RW1C	0x0	Interrupt detected for FFE0_3
FFE0_2_INTR	2	RW1C	0x0	Interrupt detected for FFE0_2
FFE0_1_INTR	1	RW1C	0x0	Interrupt detected for FFE0_1
FFE0_0_INTR	0	RW1C	0x0	Interrupt detected for FFE0_0

INTR_CTRL.FFE_INTR_EN_AP

Base Address: 0x40004800 Offset Address: 0x064 Default Value:

Register Description:

Field	Bits	Type	Default	Description
FFE0_7_INTR_EN_AP	7	RW	0x0	FFE0_7 interrupt enable for AP 0: disable 1: enable
FFE0_6_INTR_EN_AP	6	RW	0x0	FFE0_6 interrupt enable for AP 0: disable 1: enable
FFE0_5_INTR_EN_AP	5	RW	0x0	FFE0_5 interrupt enable for AP 0: disable 1: enable
FFE0_4_INTR_EN_AP	4	RW	0x0	FFE0_4 interrupt enable for AP 0: disable 1: enable
FFE0_3_INTR_EN_AP	3	RW	0x0	FFE0_3 interrupt enable for AP 0: disable 1: enable
FFE0_2_INTR_EN_AP	2	RW	0x0	FFE0_2 interrupt enable for AP 0: disable 1: enable
FFE0_1_INTR_EN_AP	1	RW	0x0	FFE0_1 interrupt enable for AP 0: disable 1: enable
FFE0_0_INTR_EN_AP	0	RW	0x0	FFE0_0 interrupt enable for AP 0: disable 1: enable

INTR_CTRL.FFE_INTR_EN_M4

Base Address: 0x40004800 Offset Address: 0x068 Default Value:

Register Description:

Field	Bits	Type	Default	Description
FFE0_7_INTR_EN_M4	7	RW	0x0	FFE0_7 interrupt enable for M4 0: disable 1: enable
FFE0_6_INTR_EN_M4	6	RW	0x0	FFE0_6 interrupt enable for M4 0: disable 1: enable
FFE0_5_INTR_EN_M4	5	RW	0x0	FFE0_5 interrupt enable for M4 0: disable 1: enable
FFE0_4_INTR_EN_M4	4	RW	0x0	FFE0_4 interrupt enable for M4 0: disable 1: enable
FFE0_3_INTR_EN_M4	3	RW	0x0	FFE0_3 interrupt enable for M4 0: disable 1: enable
FFE0_2_INTR_EN_M4	2	RW	0x0	FFE0_2 interrupt enable for M4

				0: disable 1: enable
FFE0_1_INTR_EN_M4	1	RW	0x0	FFE0_1 interrupt enable for M4 0: disable 1: enable
FFE0_0_INTR_EN_M4	0	RW	0x0	FFE0_0 interrupt enable for M4 0: disable 1: enable

INTR_CTRL.FFE1_FB_INTR

Base Address: 0x40004800 Offset Address: 0x070 Default Value:

Register Description:

Field	Bits	Type	Default	Description
FFE1_7_INTR	7	RW1C	0x0	Interrupt detected for FFE1_7
FFE1_6_INTR	6	RW1C	0x0	Interrupt detected for FFE1_6
FFE1_5_INTR	5	RW1C	0x0	Interrupt detected for FFE1_5
FFE1_4_INTR	4	RW1C	0x0	Interrupt detected for FFE1_4
FFE1_3_INTR	3	RW1C	0x0	Interrupt detected for FFE1_3
FFE1_2_INTR	2	RW1C	0x0	Interrupt detected for FFE1_2
FFE1_1_INTR	1	RW1C	0x0	Interrupt detected for FFE1_1
FFE1_0_INTR	0	RW1C	0x0	Interrupt detected for FFE1_0

INTR_CTRL.FFE1_FB_INTR_EN_AP

Base Address: 0x40004800 Offset Address: 0x074 Default Value:

Register Description:

Field	Bits	Type	Default	Description
FFE1_7_INTR_EN_AP	7	RW	0x0	FFE1_7 interrupt enable for AP 0: disable 1: enable
FFE1_6_INTR_EN_AP	6	RW	0x0	FFE1_6 interrupt enable for AP 0: disable 1: enable
FFE1_5_INTR_EN_AP	5	RW	0x0	FFE1_5 interrupt enable for AP 0: disable 1: enable
FFE1_4_INTR_EN_AP	4	RW	0x0	FFE1_4 interrupt enable for AP 0: disable 1: enable
FFE1_3_INTR_EN_AP	3	RW	0x0	FFE1_3 interrupt enable for AP 0: disable 1: enable
FFE1_2_INTR_EN_AP	2	RW	0x0	FFE1_2 interrupt enable for AP 0: disable 1: enable
FFE1_1_INTR_EN_AP	1	RW	0x0	FFE1_1 interrupt enable for AP 0: disable 1: enable
FFE1_0_INTR_EN_AP	0	RW	0x0	FFE1_0 interrupt enable for AP 0: disable 1: enable

INTR_CTRL.FFE1_FB_INTR_EN_M4

Base Address: 0x40004800 Offset Address: 0x078 Default Value:

Register Description:

Field	Bits	Type	Default	Description
FFE1_7_INTR_EN_M4	7	RW	0x0	FFE1_7 interrupt enable for M4 0: disable 1: enable
FFE1_6_INTR_EN_M4	6	RW	0x0	FFE1_6 interrupt enable for M4 0: disable 1: enable
FFE1_5_INTR_EN_M4	5	RW	0x0	FFE1_5 interrupt enable for M4 0: disable 1: enable
FFE1_4_INTR_EN_M4	4	RW	0x0	FFE1_4 interrupt enable for M4 0: disable 1: enable
FFE1_3_INTR_EN_M4	3	RW	0x0	FFE1_3 interrupt enable for M4 0: disable 1: enable
FFE1_2_INTR_EN_M4	2	RW	0x0	FFE1_2 interrupt enable for M4 0: disable 1: enable
FFE1_1_INTR_EN_M4	1	RW	0x0	FFE1_1 interrupt enable for M4 0: disable 1: enable
FFE1_0_INTR_EN_M4	0	RW	0x0	FFE1_0 interrupt enable for M4 0: disable 1: enable

INTR_CTRL.FB_INTR

Base Address: 0x40004800 Offset Address: 0x0080 Default Value:

Register Description:

Field	Bits	Type	Default	Description
FB_3_INTR	3	RW1C	0x0	Active high edge interrupt detected for Fabric. When interrupt type is selected as edge detect, this register will return high when triggered, write 1 to clear.
FB_2_INTR	2	RW1C	0x0	Active high edge interrupt detected for Fabric. When interrupt type is selected as edge detect, this register will return high when triggered, write 1 to clear.
FB_1_INTR	1	RW1C	0x0	Active high edge interrupt detected for Fabric. When interrupt type is selected as edge detect, this register will return high when triggered, write 1 to clear.
FB_0_INTR	0	RW1C	0x0	Active high edge interrupt detected for Fabric. When interrupt type is selected as edge detect, this register will return high when triggered, write 1 to clear.

INTR_CTRL.FB_INTR_RAW

Base Address: 0x40004800 Offset Address: 0x0084 Default Value:

Register Description:

Field	Bits	Type	Default	Description
FB_3_INTR_RAW	3	RO	0x0	Raw interrupt for Fabric. This register will reflect the value of the Fabric regardless of the type/polarity
FB_2_INTR_RAW	2	RO	0x0	Raw interrupt for Fabric. This register will reflect the value of the Fabric regardless of the type/polarity
FB_1_INTR_RAW	1	RO	0x0	Raw interrupt for Fabric. This register will reflect the value of the Fabric regardless of the type/polarity
FB_0_INTR_RAW	0	RO	0x0	Raw interrupt for Fabric. This register will reflect the value of the Fabric regardless of the type/polarity

INTR_CTRL.FB_INTR_TYPE

Base Address: 0x40004800 Offset Address: 0x088 Default Value:

Register Description:

Field	Bits	Type	Default	Description
FB_3_INTR_TYPE	3	RW	0x0	FB_3 interrupt type 0: level 1: edge
FB_2_INTR_TYPE	2	RW	0x0	FB_2 interrupt type 0: level 1: edge
FB_1_INTR_TYPE	1	RW	0x0	FB_1 interrupt type 0: level 1: edge
FB_0_INTR_TYPE	0	RW	0x0	FB_0 interrupt type 0: level 1: edge

INTR_CTRL.FB_INTR_POL

Base Address: 0x40004800 Offset Address: 0x08C Default Value:

Register Description:

Field	Bits	Type	Default	Description
FB_3_INTR_POL	3	RW	0x0	FB_3 interrupt POL (depends on interrupt type) 0x08c = 0 0:low 1:hi 0x08c = 1 0:fall 1:rise
FB_2_INTR_POL	2	RW	0x0	FB_2 interrupt POL (depends on interrupt type) 0x08c = 0 0:low 1:hi 0x08c = 1 0:fall 1:rise
FB_1_INTR_POL	1	RW	0x0	FB_1 interrupt POL (depends on interrupt type) 0x08c = 0 0:low 1:hi 0x08c = 1 0:fall 1:rise
FB_0_INTR_POL	0	RW	0x0	FB_0 interrupt POL (depends on interrupt type) 0x08c = 0 0:low 1:hi

				0x08c = 1 0:fall 1:rise

INTR_CTRL.FB_INTR_EN_AP

Base Address: 0x40004800 Offset Address: 0x090 Default Value:

Register Description:

Field	Bits	Type	Default	Description
FB_3_INTR_EN_AP	3	RW	0x0	FB_3 interrupt enable for AP 0: disable 1: enable
FB_2_INTR_EN_AP	2	RW	0x0	FB_2 interrupt enable for AP 0: disable 1: enable
FB_1_INTR_EN_AP	1	RW	0x0	FB_1 interrupt enable for AP 0: disable 1: enable
FB_0_INTR_EN_AP	0	RW	0x0	FB_0 interrupt enable for AP 0: disable 1: enable

INTR_CTRL.FB_INTR_EN_M4

Base Address: 0x40004800 Offset Address: 0x094 Default Value:

Register Description:

Field	Bits	Type	Default	Description
FB_3_INTR_EN_M4	3	RW	0x0	FB_3 interrupt enable for M4 0: disable 1: enable
FB_2_INTR_EN_M4	2	RW	0x0	FB_2 interrupt enable for M4 0: disable 1: enable
FB_1_INTR_EN_M4	1	RW	0x0	FB_1 interrupt enable for M4 0: disable 1: enable
FB_0_INTR_EN_M4	0	RW	0x0	FB_0 interrupt enable for M4 0: disable 1: enable