LC29H Series
Reference Design

GNSS Module Series

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Status: Released

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About the Document

Document Information	
Title	**LC29H Series Reference Design**
Subtitle	GNSS Module Series
Document Type	Reference Design
Document Status	Released

Revision History

Version	Date	Description
-	2022-03-21	Creation of the document
1.0	2022-06-10	First official release
1.1	2022-09-02	Reserved pins 2 and 4 for LC29H (DA) and LC29H (EA)*.
1.2	2023-01-18	1. Added the applicable variant: LC29H (BS). 2. Updated pins 5, 6, 15 and 16 from RESERVED to D_SEL1, D_SEL2, TXD2 and RXD2, respectively 3. Added the SPI* and the reference circuit. 4. Updated the pin 17 of LC29H (BA) and LC29H (CA) from RESERVED to WI*. 5. Updated the block diagram (Sheet 1). 6. Updated the module interfaces and deleted 1PPS indication circuit (Sheet 5). 7. Added the band-pass filter in the active and passive antennas (Sheet 6). 8. Added the SCH and PCB design checklists.

Contents

1 Reference Design

1.1. Introduction

This document provides the reference design of Quectel LC29H GNSS module, including the design of block diagram, 3.3 V MCU and UART circuits, power supply, I2C and SPI circuits, module interfaces and antenna interface.

The LC29H series includes six variants: LC29H (AA), LC29H (BA), LC29H (CA), LC29H (DA), LC29H (EA)* and LC29H (BS).

1.1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	The asterisk (*) after a model indicates that the sample of the model is currently unavailable.

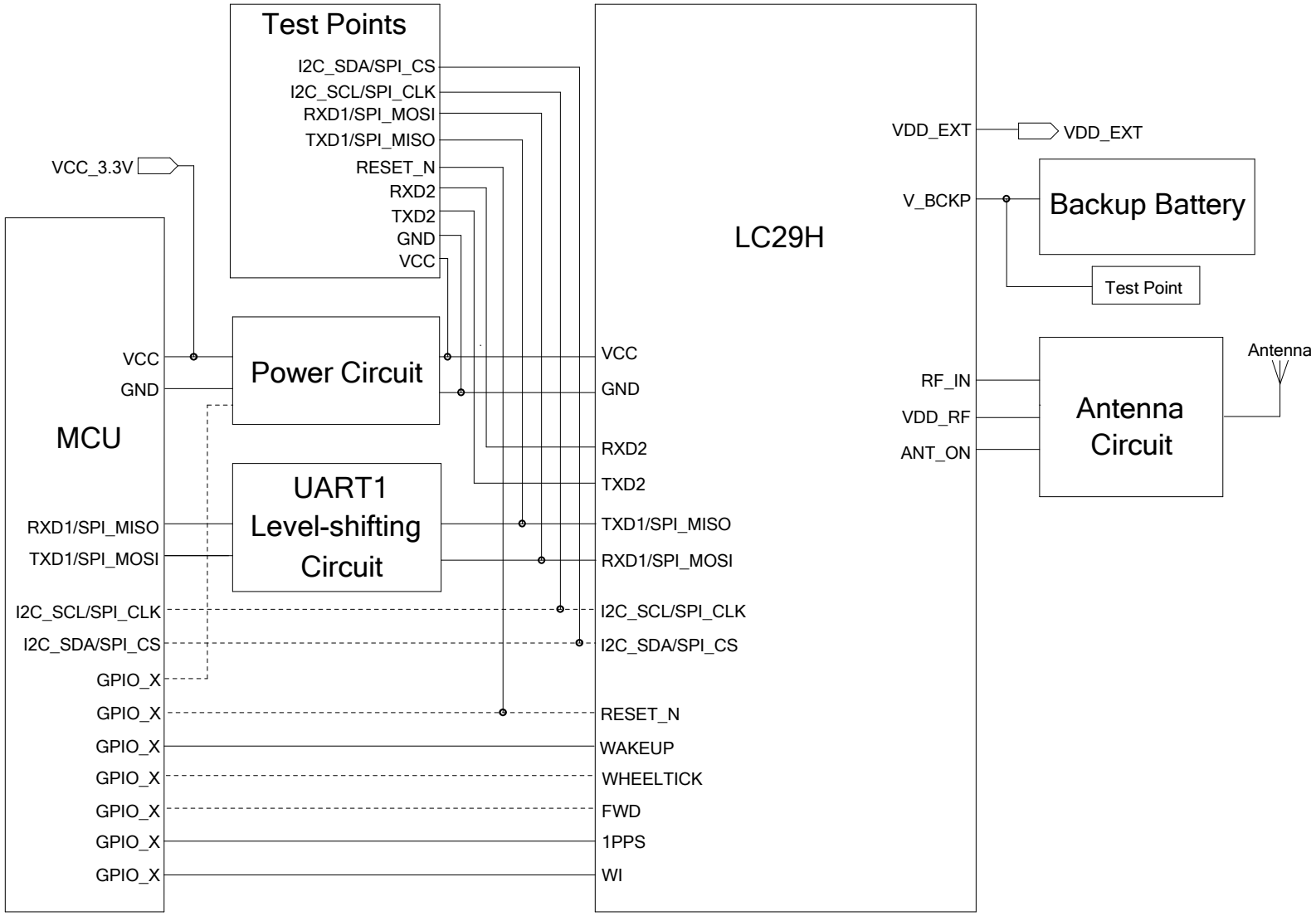
1.2. Reference Schematics and Design Checklists

The schematics and design checklists are provided for your reference only.

NOTE

Quectel also provides design review services. It is strongly recommended that you submit your schematics and PCB designs to Quectel Technical Support for a formal review.

Block Diagram



NOTE:

1. FWD, WHEELTICK and WI are supported by LC29H (BA) and LC29H (CA).
2. The I/O voltage of UART2 interface is 1.8 V.

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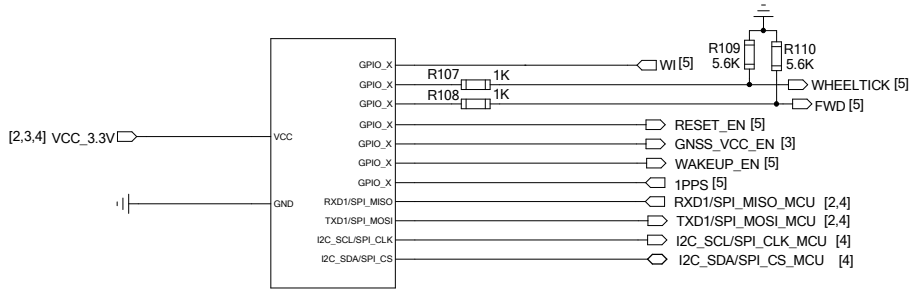
3.3 V MCU and UART Circuits

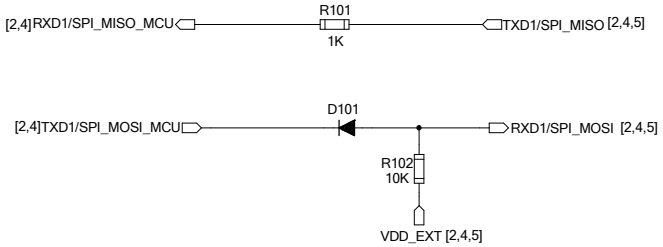
MCU Circuit



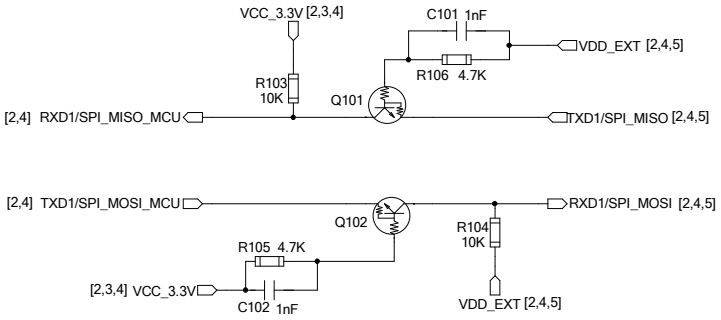
NOTE:

The MCU voltage is VCC_3.3V and the I/O voltage of the module is 2.8 V, while the I/O voltage of TXD2, RXD2, D_SEL1 and D_SEL2 is 1.8 V.

UART1 Level-shifting Circuit - Diode Solution



UART1 Level-shifting Circuit - Transistor Solution



NOTE:

Refer to the above level-shifting circuit when the I/O voltage of MCU does not match that of the module.

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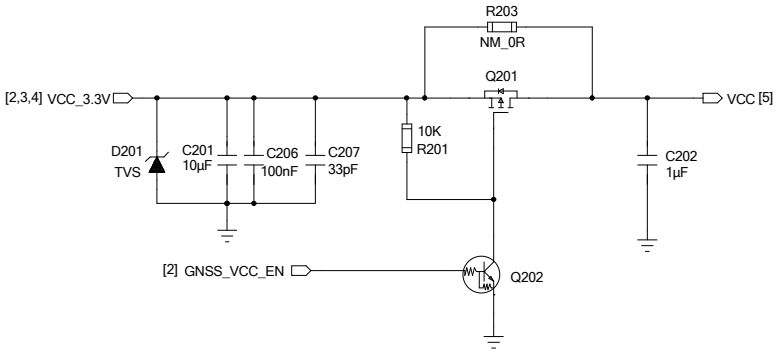
Power Supply

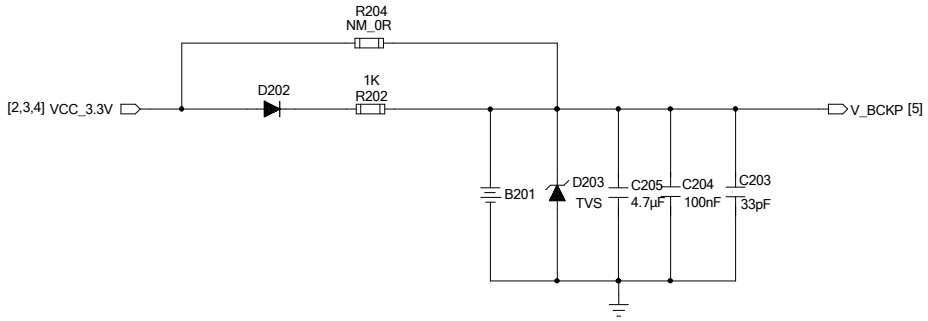
VCC Power Supply Control Circuit



NOTE:

1. This circuit can control the power supply of the module through MCU.
2. The power supply design must meet the sequence requirements in hardware design. For more information, see *Quectel_LC29H_Series_Hardware_Design.*

V_BCKP Circuit



NOTE:

1. V_BCKP must be powered simultaneously with VCC or before it.
2. The V_BCKP pin should always be powered if hot (warm) start is needed.
3. A suitable resistor (R202) should be selected according to the charging current value of the battery.

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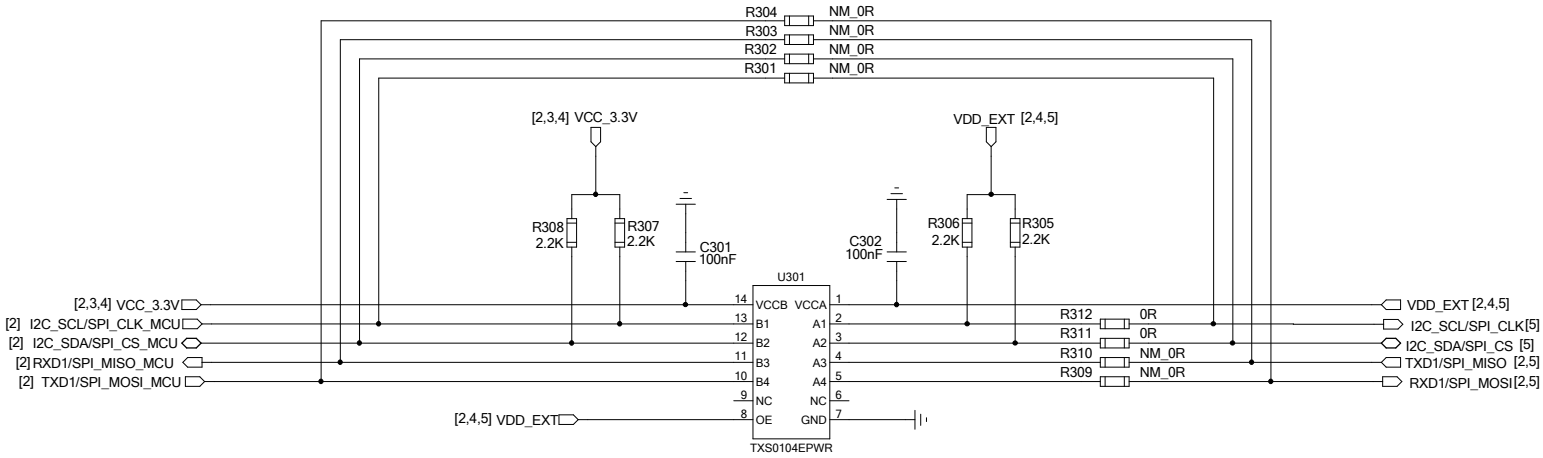
I2C and SPI Circuits



	R305	R306	R307	R308	R309	R310	R311	R312
SPI	NM	NM	NM	NM	0 Ω	0 Ω	0 Ω	0 Ω
I2C	2.2 kΩ	2.2 kΩ	2.2 kΩ	2.2 kΩ	NM	NM	0 Ω	0 Ω

(NM: Not Mounted)

NOTE:

1. Generally, the level converter IC solution requires VCCA ≤ VCCB. Please pay attention to the voltage relation before using the above circuit.
2. The I2C circuit requires externally pull-up resistors.
3. SPI cannot be used simultaneously with either I2C or UART1.

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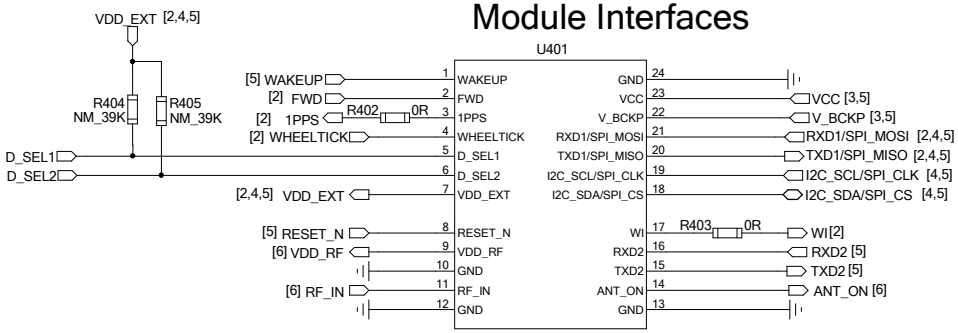
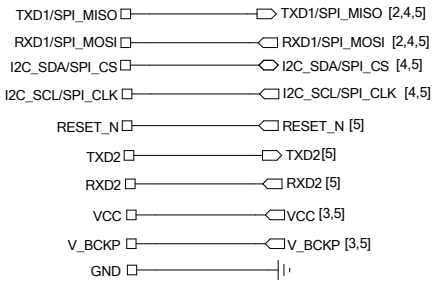
Module Interfaces

Module Interfaces



Test Points

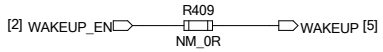


NOTE:

1. The UART1 interface is used for standard NMEA message output, RTCM message output, binary data input/output, PAIR/PQTM message input/output and firmware upgrade. For LC29H (BA), LC29H (DA) and LC29H (EA), it can also be used for RTCM message input.
2. The UART2 interface is used for outputting system debugging data and power domain of the interface is 1.8 V.
3. The module works normally only if both VCC and V_BCKP pins are powered.
4. If the I/O voltage of MCU is not matched with that of the module, a level-shifting circuit must be selected.
5. D_SEL1 and D_SEL2 are pulled down internally with 75 kΩ resistors by default and the power domain is 1.8 V. Pull one or both of them up externally to high logical level to switch the interface for communication and downloading. The requirements for different interface selection are listed in the table on the right.
   1) When R404 and R405 are not mounted, UART1 and I2C can be selected. The UART1 can be used for communication and downloading; the I2C can only be used for communication.
   2) When R404 is not mounted while R405 is mounted, no interface can be selected.
   3) When R404 is mounted while R405 is not mounted, the SPI can be selected for communication.
   4) When R404 and R405 are mounted, UART1 and I2C can be selected. The UART1 can only be used for communication; the I2C can be used for communication and downloading.

Interface Selection	R404	R405	Remarks
D_SEL1 = 0, D_SEL2 = 0	NM	NM	UART1/I2C
D_SEL1 = 0, D_SEL2 = 1	NM	39 kΩ	-
D_SEL1 = 1, D_SEL2 = 0	39 kΩ	NM	SPI
D_SEL1 = 1, D_SEL2 = 1	39 kΩ	39 kΩ	I2C/UART1

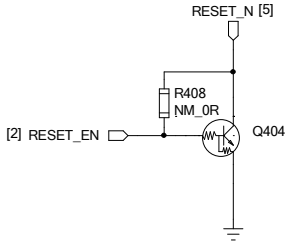
WAKEUP Circuit



NOTE:

1. Use a GPIO that supports push-pull output as WAKEUP_EN.
2. Restore VCC and pull the WAKEUP pin high for at least 10 ms to exit the Backup mode.

RESET_N Circuit



NOTE:

RESET_N must be connected so that it can be used to reset the module if the module enters an abnormal state.

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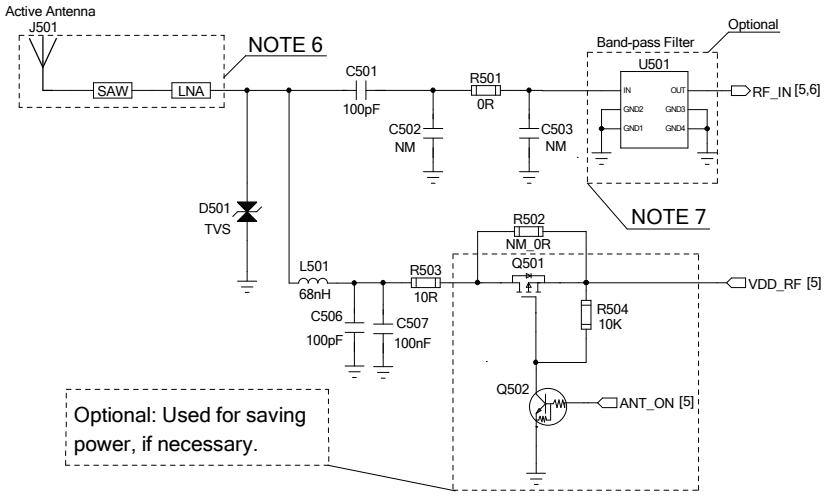
Antenna Interface

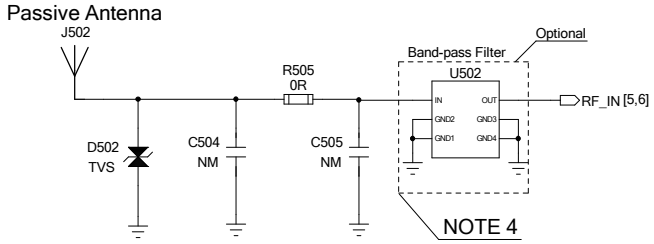
Active Antenna



NOTE:

1. D501 is an electrostatic discharge (ESD) protection device to protect the RF signal input from the potential damage caused by ESD.
2. L501 is used for preventing the RF signal from leaking into the VDD_RF and preventing noise propagation from the VDD_RF to the antenna. L501 routes the bias voltage to the active antenna without losses.
3. The resistor R503 is used for protecting the module in case the active antenna is short-circuited to the ground plane.
4. R501, C502 and C503 form a π matching circuit for antenna impedance modification. By default, R501 is 0 Ω, C502 and C503 are not mounted.
5. The impedance of the RF trace line on the main PCB should be controlled to 50 Ω and the trace length should be kept as short as possible.
6. When selecting the active antenna, it is recommended to choose one of which the SAW filter is placed in front of the LNA in the internal framework. That can be used to further reduce the impact of out-of-band signals on the GNSS module when there is a complex electromagnetic environment around the module.
7. In a complex electromagnetic environment, a band-pass filter circuit is optional and recommended to be added to further reduce the impact of out-of-band signals on the GNSS module. It should be placed closed to the RF_IN pin during PCB design.
8. For more information, see *Quectel_LC29H_Series_Hardware_Design.*

Passive Antenna



NOTE:

1. D502 is an electrostatic discharge (ESD) protection device to protect the RF signal input from the potential damage caused by ESD.
2. R505, C504 and C505 form a π matching circuit for antenna impedance modification. By default, R505 is 0 Ω, C504 and C505 are not mounted.
3. The impedance of the RF trace line on the main PCB should be controlled to 50 Ω and the trace length should be kept as short as possible.
4. In a complex electromagnetic environment, a band-pass filter circuit is optional and recommended to be added to further reduce the impact of out-of-band signals on the GNSS module. It should be placed closed to the RF_IN pin during PCB design.
5. For more information, see *Quectel_LC29H_Series_Hardware_Design.*

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Table 1: SCH Design Checklist

Pin No.	Pin Name	Checklist	Result			Comment
			Pass	Fail	N/A	
1	WAKEUP	If Backup mode is used, the pin must be connected to the GPIO of the MCU in series with a 0 Ω resistor, and the GPIO should support push-pull output.				
2	FWD /RESERVED	1. Connect the FWD pin (supported only by LC29H (BA) and LC29H (CA)) to the GPIO of the MCU in series with a 0 Ω resistor when the I/O voltage of MCU and that of the module are the same, or design a level-shifting circuit when the I/O voltage of MCU does not match that of the module. 2. Note that the level of this pin is 2.8 V input. If unused, leave the pin N/C.				
3	1PPS	Connect to the GPIO of the MCU in series with a 0 Ω resistor. If unused, leave the pin N/C.				
4	WHEELTICK/ RESERVED	1. Connect the WHEELTICK pin (supported only by LC29H (BA) and LC29H (CA)) to the GPIO of the MCU in series with a 0 Ω resistor when the I/O voltage of MCU and that of the module are the same, or design a suitable level-shifting circuit when the I/O voltage of MCU does not match that of the module. 2. Note that the level of this pin is 2.8 V input. If unused, leave the pin N/C.				
5	D_SEL1	1. By default, D_SEL1 and D_SEL2 are pulled down internally to GND with 75 kΩ resistors. Pull one or both of them up externally to high logical level to switch the interface for communication and downloading. Connect them to VDD_EXT with 39 kΩ pull-up resistor respectively. 2. Note that the I/O voltage domain of D_SEL1 and D_SEL2 is 1.8 V. If unused, leave the pin N/C.				
6	D_SEL2					
7	VDD_EXT	The power output is 2.8 V, and the maximum output current capability is 100 mA. If unused, leave the pin N/C.				
8	RESET_N	Using OC drive circuit to control the module reset and the control pin must be connected to the MCU. Reserve a test point.				

Pin No.	Pin Name	Checklist	Result			Comment
			Pass	Fail	N/A	
9	VDD_RF	Used to supply power for the external active antenna.				
10	GND	Reference ground of the module. The GND pin must be connected to ground.				
11	RF_IN	1. π matching circuit must be added for impedance modification. 2. In a complex electromagnetic environment, a band-pass filter circuit must be added to reduce the impact of out-of-band signals interference. 3. It is recommended to select an ESD protection device with junction capacitance lower than 0.6 pF. 4. The inductor used in the power supply circuit of the active antenna is at least 68 nH and that the inductor is placed so that its pad is part of the RF line.				
12	GND	Reference ground of the module. The GND pin must be connected to ground.				
13	GND	Reference ground of the module. The GND pin must be connected to ground.				
14	ANT_ON	ANT_ON is connected to the transistor's base to control the power supply of VDD_RF for active antenna.				
15	TXD2	The UART2 is used for outputting system debugging data. Reserve test points. Note that the I/O voltage domain is 1.8 V.				
16	RXD2					
17	WI /RESERVED	Connect the WI pin (supported only by LC29H (BA) and LC29H (CA)) to the GPIO of the MCU in series with a 0 Ω resistor.				
18	I2C_SDA/ SPI_CS	1. Connect them to MCU with level shifting circuit. Reserve test points. 2. I2C_SDA and I2C_SCL need to be pulled up externally to 2.8 V with a 2.2 kΩ resistor respectively.				
19	I2C_SCL/ SPI_CLK					

Pin No.	Pin Name	Checklist	Result			Comment
			Pass	Fail	N/A	
20	TXD1/ SPI_MISO	Connect them to MCU with level shifting circuit. Reserve test points.				
21	RXD1/ SPI_MOSI					
22	V_BCKP	1. It is recommended to place a TVS, and a combination of a 4.7 μF, a 100 nF and a 33 pF decoupling capacitor near the V_BCKP pin. 2. Ensure that V_BCKP can be controlled by MCU. 3. Reserve a test point. 4. V_BCKP must be connected to power supply for startup, and it should always be powered if hot (warm) start is needed.				
23	VCC	1. It is recommended to place a TVS and a combination of a 10 μF, a 100 nF and a 33 pF decoupling capacitor near the VCC pin. 2. Ensure that VCC can be controlled by MCU. 3. Reserve a test point.				
24	GND	Reference ground of the module. The GND pin must be connected to ground.				

NOTE

1. All GND pins must be connected to ground and reserved a GND test point; all RESERVED pins must be left floating.
2. Quectel also provides design review services. It is strongly recommended that you submit your schematics and PCB designs to Quectel Technical Support for a formal review.

Table 2: PCB Design Checklist

Pin No.	Pin Name	Checklist	Result			Comment
			Pass	Fail	N/A	
1	WAKEUP	1. Surround the signal trace with ground. 2. Avoid routing near strong interference signals; avoid acute angles and right angles in trace routing.				
2	FWD /RESERVED	1. Surround the signal trace with ground. 2. Avoid routing near strong interference signals; avoid acute angles and right angles in trace routing.				
3	1PPS	1. Surround the signal trace with ground. 2. Avoid routing near strong interference signals; avoid acute angles and right angles in trace routing.				
4	WHEELTICK/ RESERVED	1. Surround the signal trace with ground. 2. Avoid routing near strong interference signals; avoid acute angles and right angles in trace routing.				
5	D_SEL1	1. Surround the signal traces with ground. 2. Place the pull-up resistor close to the pins.				
6	D_SEL2					
7	VDD_EXT	Power routing should be surrounded by GND and avoid being parallel with other line(s).				
8	RESET_N	Surround the RESET_N signal trace with ground, and avoid routing near the strong interference signals.				
9	VDD_RF	Power routing should be surrounded by GND and avoid being parallel with other line(s).				
10	GND	1. Confirm that there are no isolated shapes in the ground layer. 2. Module GND pads must be completely covered by the ground plane.				
11	RF_IN	1. The characteristic impedance of the RF signal line(s) is kept at 50 Ω, and the RF trace is as short and straight as possible, with smooth lines (without bumps, with consistent geometry–it would be ideal for the footprints to be blended into the RF trace, with curved rather than sharp angles). 2. Ensure that there are no vias in the RF signal path. 3. Ensure that RF signal path is surround by ground.				

Pin No.	Pin Name	Checklist	Result			Comment
			Pass	Fail	N/A	
		4. RF signal line(s) and GNSS antenna are kept away from noise sources such as MCU(s), crystal(s) and other RF antenna(s).				
12	GND	1. Confirm that there are no isolated shapes in the ground layer. 2. Module GND pads must be completely covered by the ground plane.				
13	GND	1. Confirm that there are no isolated shapes in the ground layer. 2. Module GND pads must be completely covered by the ground plane.				
14	ANT_ON	1. Surround the signal trace with ground. 2. Avoid routing near strong interference signals; avoid acute angles and right angles in trace routing.				
15	TXD2	Surround the signal traces with ground. Keep the routing short and away from interference source.				
16	RXD2					
17	WI /RESERVED	1. Surround the signal trace with ground. 2. Avoid routing near strong interference signals; avoid acute angles and right angles in trace routing.				
18	I2C_SDA/ SPI_CS	Surround the signal traces with ground. Keep the routing short and away from interference source.				
19	I2C_SCL/ SPI_CLK					
20	TXD1/ SPI_MISO	Surround the signal traces with ground. Keep the routing short and away from interference source.				
21	RXD1/ SPI_MOSI					
22	V_BCKP	1. The power supply first passes through the TVS, and then through the subsequent components.				

Pin No.	Pin Name	Checklist	Result			Comment
			Pass	Fail	N/A	
		2. The capacitors are placed near the power supply pin in descending order of capacitance. At least one GND via must be placed near the grounded end of the capacitor. If needed, there should be more than one GND via to meet the requirements. 3. The routing width of the power supply is at least 1 mm per ampere The longer the routing, the wider it should be. The power routing and sensitive signal routings (with Clock, USB, MIPI, RF, etc.) must be isolated.				
23	VCC	1. The power supply first passes through the TVS, and then through the subsequent components. 2. The capacitors are placed near the power supply pin in descending order of capacitance. At least one GND via must be placed near the grounded end of the capacitor. If needed, there should be more than one GND via to meet the requirements. 3. The routing width of the power supply is at least 1 mm per ampere. The longer the routing, the wider it should be. The power routing and sensitive signal routings (with Clock, USB, MIPI, RF, etc.) must be isolated.				
24	GND	1. Confirm that there are no isolated shapes in the ground layer. 2. Module GND pads must be completely covered by the ground plane.				

NOTE

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