Thermoelectric Cooler Optimization

for Deployment in Electronics Thermal Management

Thermoelectric coolers (TEC) are solid state refrigeration devices which use DC current to generate cooling or heating. Unlike traditional vapor-compression refrigeration system, thermoelectric cooling has no moving parts and circulating fluid. Its simple structure and small size makes it a good choice for a thermal management device in electronics. However, the low coefficient of performance (COP) of a TEC hampers its wide deployment.

As illustrated in Figure 1, a typical thermoelectric module is manufactured using two thin ceramic wafers with a series of P and N doped bismuth-telluride semiconductor material sandwiched between them. The ceramic wafer on both sides of the module adds rigidity and the necessary electrical insulation.

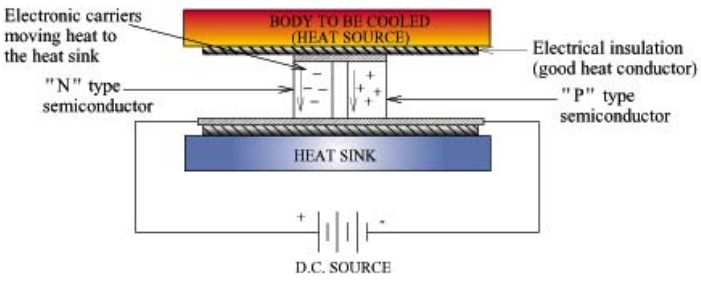


Figure 1. Illustration of a Thermoelectric Module [1]

When a DC current is applied to a TEC, the TEC can work as a cooler or heater depending on the direction of current. When working as a cooler, the TEC maintains a low temperature at the cold side by transferring heat from the cold side to the hot side against the temperature gradient. When working as a heater, the TEC transfers heat from the hot side of the device to the cold side.

For electronics thermal management, a TEC is generally used as cooler to maintain or lower the chip's junction temperature. Despite poor thermal performance, TEC modules can be a good and reliable solution for the applications that require temperature stability, sub-ambient operating conditions, or devices with a special design to accommodate TECs.

This paper discusses an optimization process for using a TEC model to maintain a high-power electronic component's junction temperature inside an air-cooled chassis at certain level. Figure 2 illustrates the application. A chip (J1) is a 40X40 mm device located on the back of the PCB and it dissipates a maximum of 50 Watts. For the stable operation of a chip, its junction temperature has to be maintained below 25°C. The junction-to-case thermal resistance of the chip is 0.1°C/W. The ambient temperature is 25°C at the chassis inlet and 30°C in front of the chip. For the sake of simplicity, all the interfacial and contact resistances are ignored.

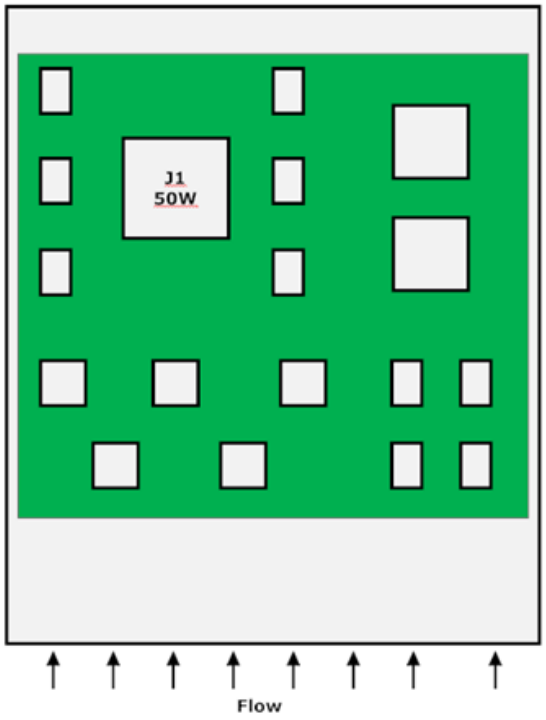


Figure 2. Chip and Board Layout

1. Regular TEC Cooling Method

To keep the chip junction temperature below 25°C, a cooling method has to be applied. The regular method is putting a heat sink with an integrated TEC module on top of the heat sink. Figure 3 shows the concept. A TEC module is sandwiched between the chip and the air-cooled heat sink.

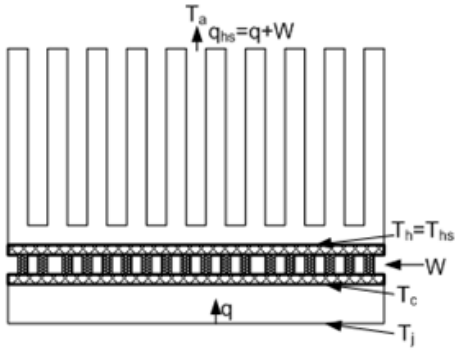


Figure 3. Schematic of a Heat Sink with TEC

Cooled by the TEC, the junction temperature of the chip is,

$$T_j = T_c + (R_{jc} + R_{TIM})q \quad (1)$$

where T_c is the TEC cold side temperature, and R_{jc} is the thermal resistance of chip from junction to case, and R_{TIM} is the thermal resistance of thermal interface material used both between TEC and chip and between TEC and heat sink.

The COP of the TEC for cooling is defined as,

$$COP = \frac{q}{W} \quad (2)$$

where q is the heat removed from the cold side by TEC and W is the electric energy consumed by TEC.

The heat sink temperature is,

$$T_{hs} = T_h = T_a + (R_{hs} + R_{TIM})(q + W) \quad (3)$$

Where T_h is the TEC hot side temperature, T_a is the local air temperature, and R_{hs} is thermal resistance of heat sink from base to ambient.

Equation 3 can be written as,

$$T_h = T_a + (R_{hs} + R_{TIM})(1 + \frac{1}{COP})q \quad (4)$$

Let,

$$\Delta T_{TEC} = T_h - T_c \quad (5)$$

The junction temperature of device becomes,

$$T_j = T_a + (R_{jc} + R_{TIM})q + (R_{hs} + R_{TIM})(1 + \frac{1}{COP})q - \Delta T_{TEC} \quad (6)$$

For the TEC, the value of ΔT_{TEC} is directly proportional to the voltage applied on the TEC module. Generally the larger the ΔT_{TEC} is, the larger the voltage applied and energy consumed by TEC module are.

Assuming the thermal resistance of the heat sink is 0.2°C/W, which is reasonable for a high performance heat sink with forced air cooling and the thermal resistance of thermal interface material (grease) is 0.01°C/W, Equation 6 becomes,

$$25 = 30 + (0.1 + 0.01) \times 50 + (0.2 + 0.01)(1 + \frac{1}{COP})50 - \Delta T_{TEC} \quad (7)$$

The ΔT_{TEC} required is,

$$\Delta T_{TEC} = 21 + \frac{10.5}{COP} \quad (8)$$

2. Optimized TEC Cooling Method

An optimized TEC cooling method that can minimize the required ΔT_{TEC} is shown in Figure 4. A copper block with integrated heat pipes is mounted on the top of the chip. The heat pipes transfer the heat dissipated by the chip to the heat sink module located at the front of the chassis. This design has two distinct advantages:

1. The air temperature at inlet is lower than that of the air in front of the chip
2. The heat sink can have a larger size and more complicated design, its thermal performance also improves with uniform inlet flow

The junction temperature of the chip is as follows,

$$T_j = T_a + (R_{jc} + R_{TIM} + R_{hp})q + (R_{hs} + R_{TIM})(1 + \frac{1}{COP})q - \Delta T_{TEC} \quad (9)$$

Where R_{hp} is the thermal resistance of the heat pipe.

In the optimized case, the ambient temperature is 25°C, the thermal resistance of the heat sink can be as low as 0.1°C/W, and the thermal resistance of the heat pipe can be in the order of 0.01°C/W.

Equation 9 becomes:

$$25 = 25 + (0.1 \times 0.01 + 0.01) \times 50 + (0.1 + 0.01)(1 + \frac{1}{COP})50 - \Delta T_{TEC} \quad (10)$$

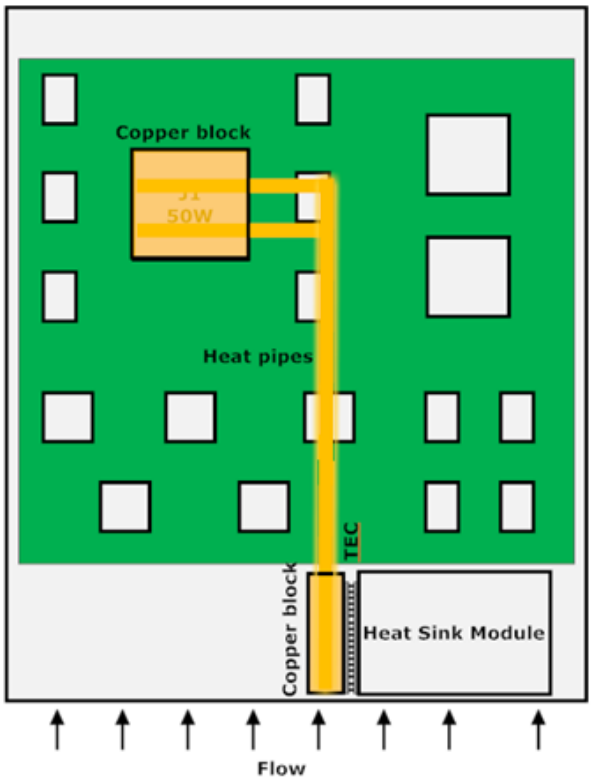


Figure 4. Optimized Heat Sink with TEC Module

$$\Delta T_{TEC} = 11.5 + \frac{5.5}{COP} \quad (11)$$

To evaluate the two TEC cooling methods, a TEC (RC12-8) from Marlow industries [2] is selected for the calculation. The image of the RC12-8 is shown in Figure 5. The specifications of the RC12-8 are shown in Table 1.

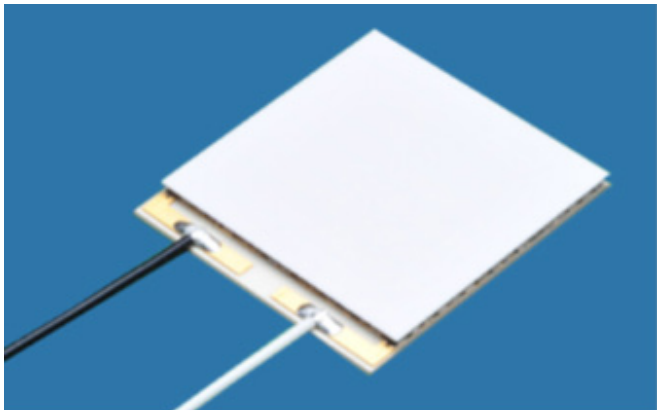


Figure 5. Marlow RC12-8 TEC [2]

	RC12-8 (40mm x 40mm x 3.6mm)	
Hot Side Temperature	27	50
ΔT_{max} (°C)	66	74
q_{max} (watts)	71	78
I_{max} (amps)	7.4	7.4
V_{max} (vdc)	14.7	16.4

Table 1. Marlow RC12-8 TEC Specifications [2]

The performance curves of RC12-8 at 50°C hot side temperature are shown in Figure 6.

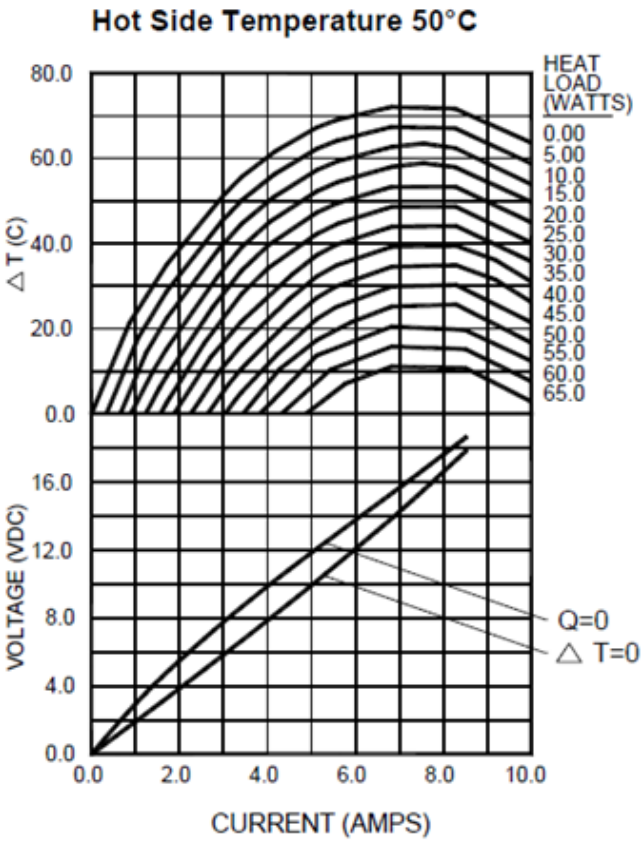


Figure 6. Marlow RC12-8 TEC Performance Curves [2]

Working at 50°C hot side temperature and transferring 50 Watts heat load, the maximum ΔT_{TEC} that RC12-8 can generate is 25°C, see Figure 6. At this operating condition, the voltage applied on the TEC is 15V and the current consumed by the TEC is 7A.

So the COP of the TEC is,

$$COP = \frac{50}{15x7} = 0.476 \quad (12)$$

For the regular TEC solution,

$$\Delta T_{TEC\_required} = 21 + \frac{10.5}{0.476} = 43°C > 25°C \quad (13)$$

The $\Delta T_{TEC\_required}$ is larger than the maximum ΔT_{TEC} that RC12-8 can generate, which means the solution does not work.

For the optimized TEC solution,

$$\Delta T_{TEC\_required} = 11.5 + \frac{5.5}{0.476} = 23°C < 25°C \quad (14)$$

The $\Delta T_{TEC\_required}$ is smaller than the maximum ΔT_{TEC} that RC12-8 can generate. The estimated hot side temperature of the TEC is 42°C and the cold side is 19°C. So the optimized solution works and the chip junction temperature can be maintained lower than 25°C even at 50 Watts maximum power.

The electrical and thermal performance of current TEC's is still low compared with other refrigeration methods. However, this paper shows that TEC cooling is feasible for high-power chips by laying out the heat sink cleverly and utilizing heat pipe. The keys for successfully using the TEC for electronic cooling applications are optimizing the design to decrease ΔT_{TEC} to reach better COP and using high performance heat sinks.

References:

1. http://www.melcor.com/tec_intro.html

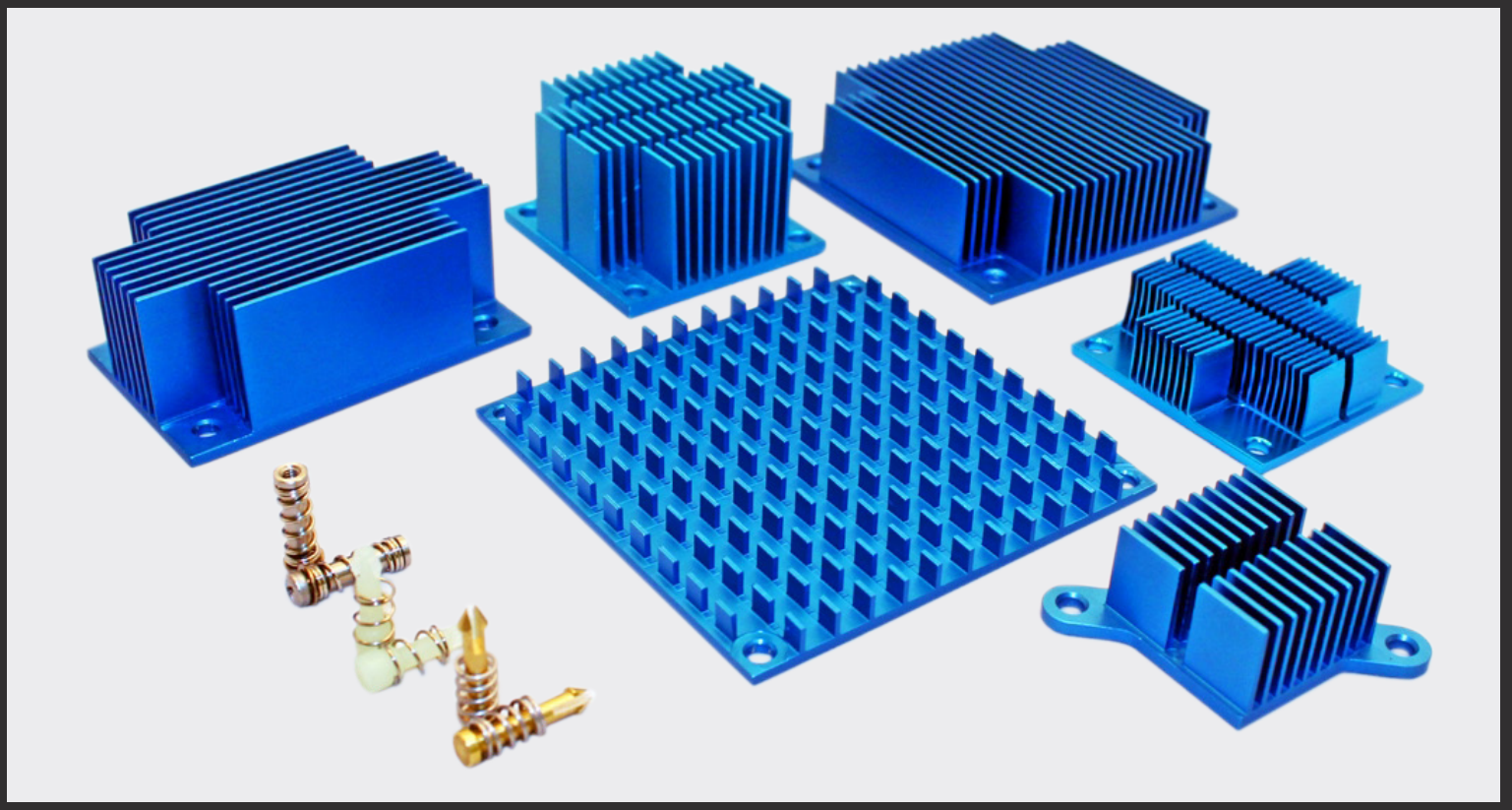
2. http://www.marlow.com/

112
fine + superfine
fin pitch designs

98
course
fin pitch
designs

21
compression
spring types

128
straight fin designs



82
cross-cut
designs

18
maxiFLOW™
designs

30
push pin
options

108,000
push pin heat sink configurations available

ATS ADVANCED THERMAL SOLUTIONS, INC.
Innovations in Thermal Management®
www.qats.com

pushPIN™