Evaluation Board PCB Information

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	RO4003	8.00mil	3.66	
5	Signal Layer 1	Copper	1.40mil		
6	Dielectric 3	FR-4	42.00mil	4.26	
7	Signal Layer 2	Copper	1.40mil		
8	Dielectric 2	FR-4	8.00mil	4.26	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

TOTAL THICKNESS: .062+/- 10%

Evaluation Board
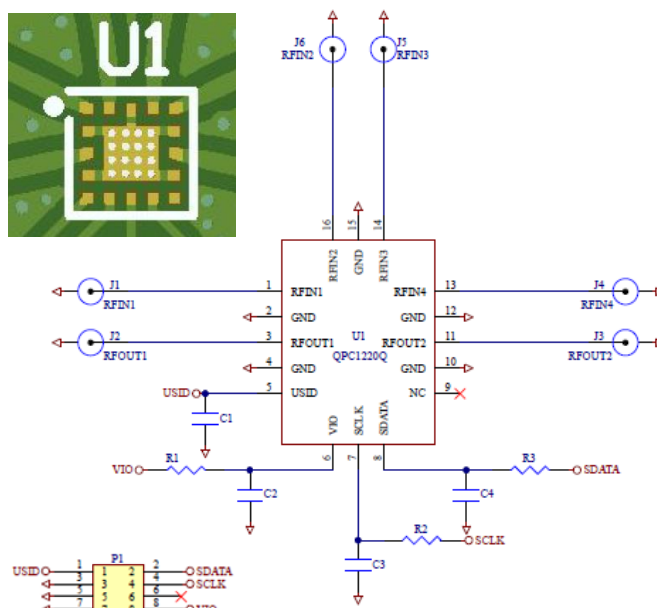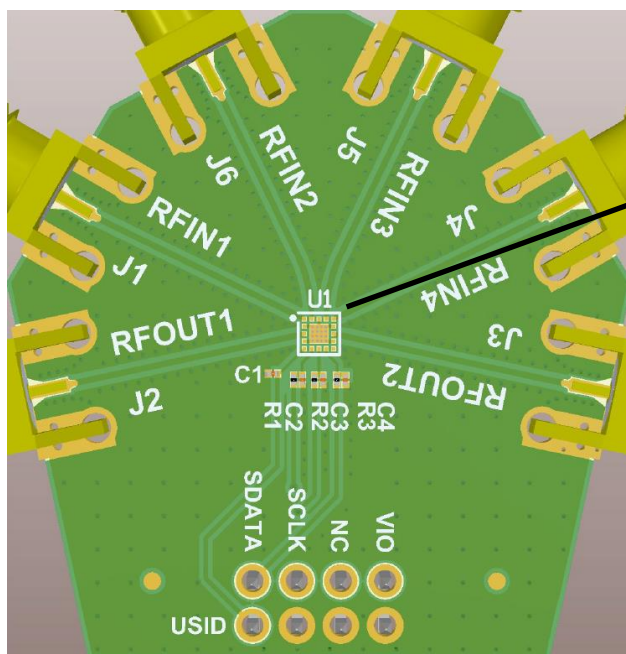
Additional Application Notes:

DC blocking caps are typically not required.   If external voltage is applied to RF pins then an external DC block should be added in series.

Bypass capacitors should be placed as close to the DUT as possible. The bypass caps should be less than 0.3 inches away from edge of DUT. VIO requires a bypass cap.

Mulitple 6 to 8 mil diameter drilled vias are to be placed under the DUT in the GND pad, recommend at least 5 vias. The vias serve to dissipate heat as well as provide an RF common ground.

Unused RF pins should be terminated in 50 ohms.

Evaluation Board BOM

Item No	Material#	Rev	Qty	Ref Des	Description
130	291026	A	1		PCB, QPC1220Q
110	287325	A	2	C1,C2	CAP, 0.01uF, 10%, 16V, X7R, 0201
20	21253		3	R1, R2, R3	RES, 0 OHM, 5%, 1/20W, 0201
50	262452		6	J1, J2, J3, J4, J5, J6	CONN, SMA, EL MINI FLT 0.068" SPE-000303
40	274947	A	1	P1	CONN, HDR, SHRD, RT-ANG, 2x4, 0.100"
60	4XXX1		2	C3, C4	NOT POPULATED ITEM-1

## Application for Ultra High Band(UHB) Operation

In order to improve performance from 3 to 6GHz, a matching circuit can be implemented.
Test results indicate the lowest IL path is RFIN1 to RFOUT2.
The lowest IL paths for antenna swapping are RFIN1 or RFIN4 for UHB operation.
Recommend high-Q SMDs in 01005 or 0201 package size.
Unused RF ports should be terminated in 50 ohms.
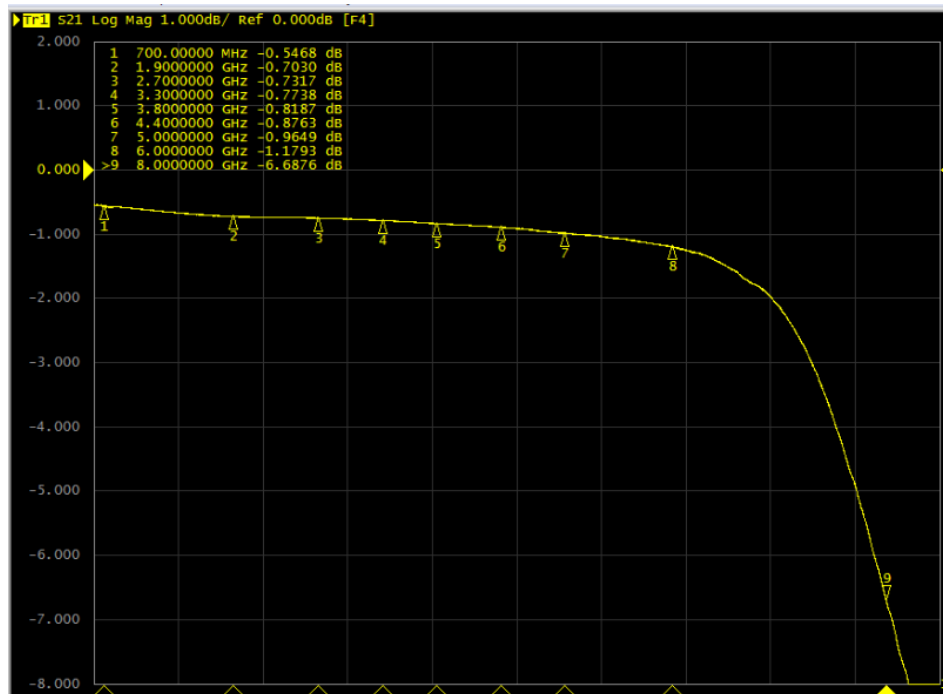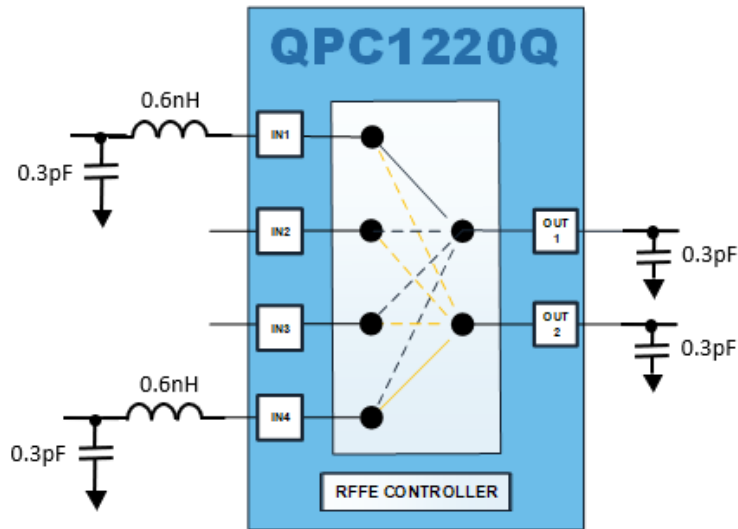
Register Configuration

Register 0x0000 — Output_Cross_CTRL

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/WM
7:1	SPARE	Reserved for future use	0x00	No	0	R/WM
0	Output_Cross	Enable DPDT output Switch to cross mode, 0x0: DPDT Direct operating mode 0x1: DPDT output cross operating mode	0x0	No	0	R/WM
		Note 1: See Truth Table for example of operation *Note 2: Use Trigger[0] along with Triggers[1] and/or [2]*				

Register 0x0001 — SW_CTRL

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/WM
7:6	SPARE	Reserved for future use	0x0	No	0	R/WM
5:4	SW_Connect_Ind[1:0]	Indicate switch connect sequence from bit0 to bit 3 00: one port connect to output1,ouput2 isolation 01: Lower bit in bit0 to bit3 connect to output1 10: Higher bit in bit0 to bit3 connect to output1 11: one port connect to output2,ouput1 isolation	0x0	No	0	R/WM
3:0	Input_Sel[3:0]	Input Ports Select Enables DP4T input Port. Each bit is a dedicated input port. Bit0 <->input1 Bit1 <->input2 Bit2 <->input3 Bit3 <->input4 0000: Isolation 0001: Input 1 Select 0010: Input 2 Select 0100: Input 3 Select 1000: Input 4 Select	0x0	No	0	R/WM
		Note 1: See Truth Table for example of operation *Note 2: Use Trigger[0] along with Triggers[1] and/or [2]*				

Register 0x001A — RFFE_STATUS

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit reads as 0.*	0	No	No	W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

Register 0x001B — GSID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x001C — PM_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	PWR_MODE[1]	0: Normal Operation 1: Low Power - Antenna in isolation	1	B/G	No	R/W
6	PWR_MODE[0]	0: ACTIVE 1: STARTUP - Reset all registers to default settings *Note: Setting PWR_MODE to STARTUP is identical to a hardware reset initiated by the VIO signal.*	0	B/G	No	R/W
5:3	TriggerMask[2:0]	Setting bit TriggerMask[N] disables Trigger[N] TriggerMask[N] updates <u>before</u> Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register.* *If a register is associated with multiple triggers, then <u>all associated triggers</u> must be disabled to allow direct writes to the associated register.*	0b000	No	No	R/W
2:0	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note 1: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. <u>All triggers</u> are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.* *Note 2: Use Trigger[0] along with Triggers[1] and/or [2]*	0b000	B/G	No	W

Register 0x001D — PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[7:0]	Lower eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x1E	No	No	R

Register 0x001E — MANUFACTURER_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	MFG_ID[7:0]	Lower eight bits of MIPI Manufacturer ID *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0xC6	No	No	R

Register 0x001F — MAN_USID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	MFG_ID[11:8]	Upper four bits of MIPI Manufacturer ID *Note: This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.6.2 for details.*	0x3	No	No	R
3:0	USID[3:0]	Programmable Unique Slave ID The default value at reset is selected via pin SID0. SID0 | USID 0 | 0x6 1 | 0x7 *Note: USID is only writeable using a special programming sequence. See MIPI 6.6.2 for details.*	0x6	No	No	R/W

Register 0x0020 — EXT_PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[15:8]	Upper eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x00	No	No	R

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	MAJOR_REV[1:0]	Major Revisions - all layer	0b00	No	No	R
5:4	MINOR_REV[1:0]	Minor Revisions - metal only	0b00	No	No	R
3:0	MISC_REV[3:0]	Misc Revisions - mask variants	0b0001	No	No	R

Note: The REVISION_ID register contains this product's revision number which is set by Qorvo according to manufacture date. The value may change throughout the product life cycle.

Register 0x0022 — GSID0-1

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x0023 — UDR_RST

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	B/G	No	W
6:0	RESERVED		0x00	No	No	R

Register 0x0024 — ERR_SUM

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	SPARE	Reserved for future use	0	No	No	R/W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

Register 0x002C — TEST_PATT

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	TEST_PATT[7:0]	Test Pattern	0xD2	No	No	R

Register 0x002D — EXT_TRIG_MASK

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	TriggerMask[10:3]	Setting bit TriggerMask[N] disables Trigger[N] If using an Extended Write to update both TriggerMask and Trigger, than TriggerMask[N] updates <u>before</u> Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register.* *If a register is associated with multiple triggers, then <u>all associated triggers</u> must be disabled to allow direct writes to the associated register.*	0x00	No	No	R/W

Register 0x002E — EXT_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	Trigger[10:3]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. <u>All triggers</u> are processed immediately and simultaneously and then cleared. Trigger[10 - 3] will always read as 0.*	0x00	B/G	No	W

Truth Table

Reg_00	Reg_01						RFOUT1	RFOUT2
0	5	4	3	2	1	0		
0	0	0	0	0	0	0	Isolation	Isolation
0	0	0	0	0	0	1	RFIN1	Isolation
0	0	0	0	0	1	0	RFIN2	Isolation
0	0	0	0	1	0	0	RFIN3	Isolation
0	0	0	1	0	0	0	RFIN4	Isolation
0	0	1	0	0	1	1	RFIN1	RFIN2
0	0	1	0	1	0	1	RFIN1	RFIN3
0	0	1	0	1	1	0	RFIN2	RFIN3
0	0	1	1	0	0	1	RFIN1	RFIN4
0	0	1	1	0	1	0	RFIN2	RFIN4
0	0	1	1	1	0	0	RFIN3	RFIN4
0	1	0	0	0	1	1	RFIN2	RFIN1
0	1	0	0	1	0	1	RFIN3	RFIN1
0	1	0	0	1	1	0	RFIN3	RFIN2
0	1	0	1	0	0	1	RFIN4	RFIN1
0	1	0	1	0	1	0	RFIN4	RFIN2
0	1	0	1	1	0	0	RFIN4	RFIN3
0	1	1	0	0	0	1	Isolation	RFIN1
0	1	1	0	0	1	0	Isolation	RFIN2
0	1	1	0	1	0	0	Isolation	RFIN3
0	1	1	1	0	0	0	Isolation	RFIN4

Reg_00	Reg_01						RFOUT1	RFOUT2
0	5	4	3	2	1	0		
1	0	0	0	0	0	0	Isolation	Isolation
1	0	0	0	0	0	1	Isolation	RFIN1
1	0	0	0	0	1	0	Isolation	RFIN2
1	0	0	0	1	0	0	Isolation	RFIN3
1	0	0	1	0	0	0	Isolation	RFIN4
1	0	1	0	0	1	1	RFIN2	RFIN1
1	0	1	0	1	0	1	RFIN3	RFIN1
1	0	1	0	1	1	0	RFIN3	RFIN2
1	0	1	1	0	0	1	RFIN4	RFIN1
1	0	1	1	0	1	0	RFIN4	RFIN2
1	0	1	1	1	0	0	RFIN4	RFIN3
1	1	0	0	0	1	1	RFIN1	RFIN2
1	1	0	0	1	0	1	RFIN1	RFIN3
1	1	0	0	1	1	0	RFIN2	RFIN3
1	1	0	1	0	0	1	RFIN1	RFIN4
1	1	0	1	0	1	0	RFIN2	RFIN4
1	1	0	1	1	0	0	RFIN3	RFIN4
1	1	1	0	0	0	1	RFIN1	Isolation
1	1	1	0	0	1	0	RFIN2	Isolation
1	1	1	0	1	0	0	RFIN3	Isolation
1	1	1	1	0	0	0	RFIN4	Isolation

Power On and Off Sequence

It is very important that the user adheres to the correct timing sequences in order to avoid damaging the device. Figures are NOT drawn to scale.

1. Once VIO is powered down to 0V, wait a minimum of 10 μs to reapply power to VIO. (see Figure: Digital Supply Detail)
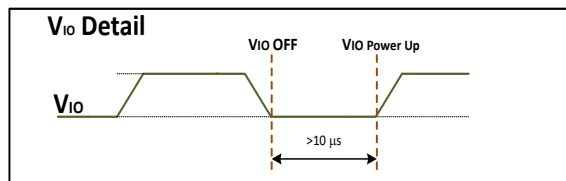

Figure: Digital Supply Detail

2. VIO must be applied for a minimum of 120 ns before sending SDATA/SCLK to ensure correct data transmission. (see Figure: RF Power-Up Detail)
3. VIO must be applied for a minimum of 15 μs before applying RF power. (see Figure: Digital Signal / RF Power-On Detail)
4. Wait a minimum of 6.5 μs after RFFE bus is idle to apply an RF signal. (see Figure: RF Power-Up Detail)
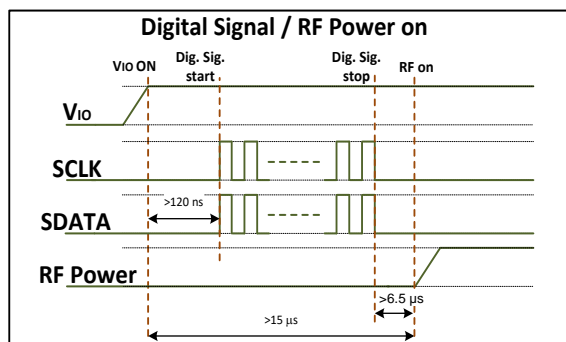

Figure: Digital Signal / RF Power-On Detail

5. RF power must not be applied during switching events. To ensure this, remove RF power before completing a register write that will change the switch mode. (see Figure: Switch Event Timing)
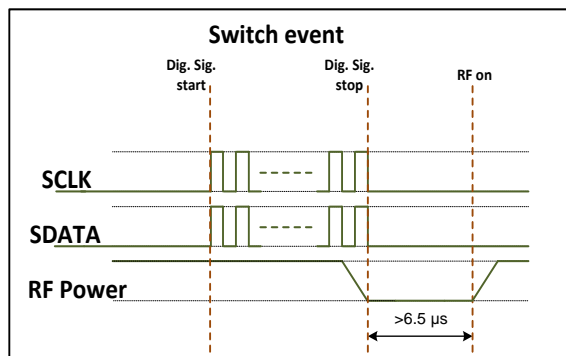

Figure: Switch Event Timing

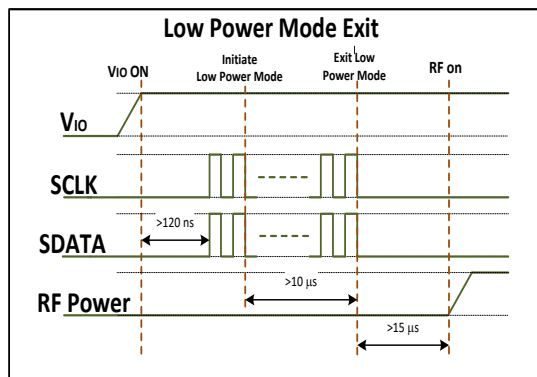6. If "Low Power Mode" is utilized, there must be a delay of 10 μs before exiting "Low Power Mode". (see Figure: Low-Power Mode Exit Timimg)

Figure: Low-Power Mode Exit Timing