Product Specification | Rev. 2.0 | 2025

IMM2G72D4SOD8AG (Die Revision B)
16GByte (2G x 72Bit)

16GB DDR4 ECC Unbuffered SODIMM
RoHS Compliant Product

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Features

- 260-Pin Unbuffered Small Outline Dual-In-Line Memory Module
- JEDEC-Standard
- Capacity: 16GB
- 72Bit Data Bus Width with ECC
- Programmable CAS Latency (CL):
  - DDR4-3200: 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 22, 24
  - DDR4-2933: 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22
  - DDR4-2666: 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20
  - DDR4-2400: 10, 11, 12, 13, 14, 15, 16, 17, 18
- Programmable CAS Write Latency (CWL):
  - DDR4-3200: 9, 10, 11, 12, 14, 16, 18, 20
  - DDR4-2933: 9, 10, 11, 12, 14, 16, 18, 20
  - DDR4-2666: 9, 10, 11, 12, 14, 16, 18
  - DDR4-2400: 9, 10, 11, 12, 14, 16
- Power Supply: V_{DD}, V_{DDQ} = 1.2V ± 0.06V
- DRAM Activating Power Supply: V_{PP} = 2.5V (2.375V – 2.75V)
- SPD Power Supply: V_{DDSPD} = 2.5V or 3.3V
- Bi-directional Differential Data-Strobe
- 8192 Refresh Cycle / 64ms
- Refresh Mode: Auto, Self
- Low Power Auto Self Refresh Mode
- Burst Length: 8, 4
- On-Die Termination (ODT)
- ZQ Calibration
- Asynchronous Reset
- On-board I2C Temperature Sensor with Integrated Serial Presence Detect (SPD) EEPROM
- Golde Edge Contacts
- 100% RoHS Compliant
- Standard Module Height: 30.00mm (1.18inch)

Table 1 - Ordering Information for RoHS Compliant Product

Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM2G72D4SOD8AG-Bzzzy(:qqq)	16GB	2Gx72	2	DDR4 ECC Unbuffered SODIMM

Note:

y:	Temperature Grade	(refer to Table 2)
zzz:	Speed Grade	(refer to Table 3)
qqq:	IM Reference Code	Blank or Reserved

Table 2 - Temperature Grade

Part Number	Temperature Grade	T_{CASE}
Blank	Commercial Temperature	0°C to 95°C
I	Industrial Temperature	-40°C to 95°C

Note: T_{CASE} is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to be double when 85°C < T_{CASE} ≤ 95°C

Table 3 - Speed Grade

Part Number	Speed Grade	Max. Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
062	DDR4-3200	1600MHz (0.625ns @ CL22)
068	DDR4-2933	1467MHz (0.682ns @ CL21)
075	DDR4-2666	1333MHz (0.750ns @ CL19)
083	DDR4-2400	1200MHz (0.833ns @ CL17)

Table 4 - Memory Chip Information

Part Number	Base Device Brand	Base Device	Voltage	Type	Chip Packing
IMM2G72D4SOD8AG-Bzzzy(:qqq)	IM	IM8G08D4GBBG	1.2V	1Gx8	Lead Free

Part Number Decoder

IM M 2G72 D4 SO D 8 A G - B 062 (I) (:qqq)

IM Module

DRAM Brand
M = IM

Module Configuration
2G72 = 2Gx72 (16GB)

Memory Type
D4 = DDR4

Module Form Factor
SO = Unbuffered SODIMM (SODIMM)

Number of Rank
D = Dual Rank

IM Reference code
Blank or Reserved

Temperature Grade
Blank = Commercial Temperature
(0℃ to +95℃ T_{CASE})
I = Industrial Temperature
(-40℃ to +95℃ T_{CASE})
***Note**: The refresh rate must be doubled when the operating temperature TCASE exceeds +85℃*

Speed Grade
062 = DDR4-3200 CL22
068 = DDR4-2933 CL21
075 = DDR4-2666 CL19
083 = DDR4-2400 CL17

DRAM Revision
B = Revision B

Green Nature
G = RoHS Compliance

Module PCB Revision
A = Revision A

DRAM Bit Width
8 = using x8 components

Table 5 - Addressing

Parameter	16GB
Bank Group	4 BG[1:0]
Bank Address	4 BA[1:0]
Row Address	64K A[15:0]
Column Address	1K A[9:0]
Device Configuration	8Gb (1Gx8)
Module Rank Address	2 CS[1:0]_n
Number of Devices	18

Table 6 – Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	2	V_{SS}	131	A3	132	A2
3	D5	4	D4	133	A1	134	EVENT_n
5	V_{SS}	6	V_{SS}	135	V_{DD}	136	V_{DD}
7	D1	8	D0	137	CK0_t	138	CK1_t
9	V_{SS}	10	V_{SS}	139	CK0_c	140	CK1_c
11	DQS0_c	12	DM0_n, DBI0_n	141	V_{DD}	142	V_{DD}
13	DQS0_t	14	V_{SS}	143	PARITY	144	A0
15	V_{SS}	16	D6	145	BA1	146	A10, AP
17	D7	18	V_{SS}	147	V_{DD}	148	V_{DD}
19	V_{SS}	20	D2	149	CS0_n	150	BA0
21	D3	22	V_{SS}	151	A14, WE_n	152	A16, RAS_n
23	V_{SS}	24	D12	153	V_{DD}	154	V_{DD}
25	D13	26	V_{SS}	155	ODT0	156	A15, CAS_n
27	V_{SS}	28	D8	157	CS1_n	158	A13
29	D9	30	V_{SS}	159	V_{DD}	160	V_{DD}
31	V_{SS}	32	DQS1_c	161	ODT1	162	NC
33	DM1_n, DBI1_n	34	DQS1_t	163	V_{DD}	164	V_{REFCA}
35	V_{SS}	36	V_{SS}	165	NC	166	SA2
37	D15	38	D14	167	V_{SS}	168	V_{SS}
39	V_{SS}	40	V_{SS}	169	D37	170	D36
41	D10	42	D11	171	V_{SS}	172	V_{SS}
43	V_{SS}	44	V_{SS}	173	D33	174	D32
45	D21	46	D20	175	V_{SS}	176	V_{SS}
47	V_{SS}	48	V_{SS}	177	DQS4_c	178	DM4_n, DBI4_n
49	D17	50	D16	179	DQS4_t	180	V_{SS}
51	V_{SS}	52	V_{SS}	181	V_{SS}	182	D39
53	DQS2_c	54	DM2_n, DBI2_n	183	D38	184	V_{SS}
55	DQS2_t	56	V_{SS}	185	V_{SS}	186	D35
57	V_{SS}	58	D22	187	D34	188	V_{SS}
59	D23	60	V_{SS}	189	V_{SS}	190	D45
61	V_{SS}	62	D18	191	D44	192	V_{SS}
63	D19	64	V_{SS}	193	V_{SS}	194	D41
65	V_{SS}	66	D28	195	D40	196	V_{SS}
67	D29	68	V_{SS}	197	V_{SS}	198	DQS5_c
69	V_{SS}	70	D24	199	DM5_n, DBI5_n	200	DQS5_t
71	D25	72	V_{SS}	201	V_{SS}	202	V_{SS}
73	V_{SS}	74	DQS3_c	203	D46	204	D47
75	DM3_n, DBI3_n	76	DQS3_t	205	V_{SS}	206	V_{SS}
77	V_{SS}	78	V_{SS}	207	D42	208	D43
79	D30	80	D31	209	V_{SS}	210	V_{SS}
81	V_{SS}	82	V_{SS}	211	D52	212	D53
83	D26	84	D27	213	V_{SS}	214	V_{SS}
85	V_{SS}	86	V_{SS}	215	D49	216	D48
87	CB5	88	CB4	217	V_{SS}	218	V_{SS}
89	V_{SS}	90	V_{SS}	219	DQS6_c	220	DM6_n, DBI6_n
91	CB1	92	CB0	221	DQS6_t	222	V_{SS}

Pin	Name	Pin	Name	Pin	Name	Pin	Name
93	V_{SS}	94	V_{SS}	223	V_{SS}	224	D54
95	DQS8_c	96	DM8_n, DBI8_n	225	D55	226	V_{SS}
97	DQS8_t	98	V_{SS}	227	V_{SS}	228	D50
99	V_{SS}	100	CB6	229	D51	230	V_{SS}
101	CB2	102	V_{SS}	231	V_{SS}	232	D60
103	V_{SS}	104	CB7	233	D61	234	V_{SS}
105	CB3	106	V_{SS}	235	V_{SS}	236	D57
107	V_{SS}	108	RESET_n	237	D56	238	V_{SS}
109	CKE0	110	CKE1	239	V_{SS}	240	DQS7_c
111	V_{DD}	112	V_{DD}	241	DM7_n, DBI7_n	242	DQS7_t
113	BG1	114	ACT_n	243	V_{SS}	244	V_{SS}
115	BG0	116	ALERT_n	245	D62	246	D63
117	V_{DD}	118	V_{DD}	247	V_{SS}	248	V_{SS}
119	A12	120	A11	249	D58	250	D59
121	A9	122	A7	251	V_{SS}	252	V_{SS}
123	V_{DD}	124	V_{DD}	253	SCL	254	SDA
125	A8	126	A5	255	V_{DDSPD}	256	SA0
127	A6	128	A4	257	V_{PP}	258	V_{TT}
129	V_{DD}	130	V_{DD}	259	V_{PP}	260	SA1

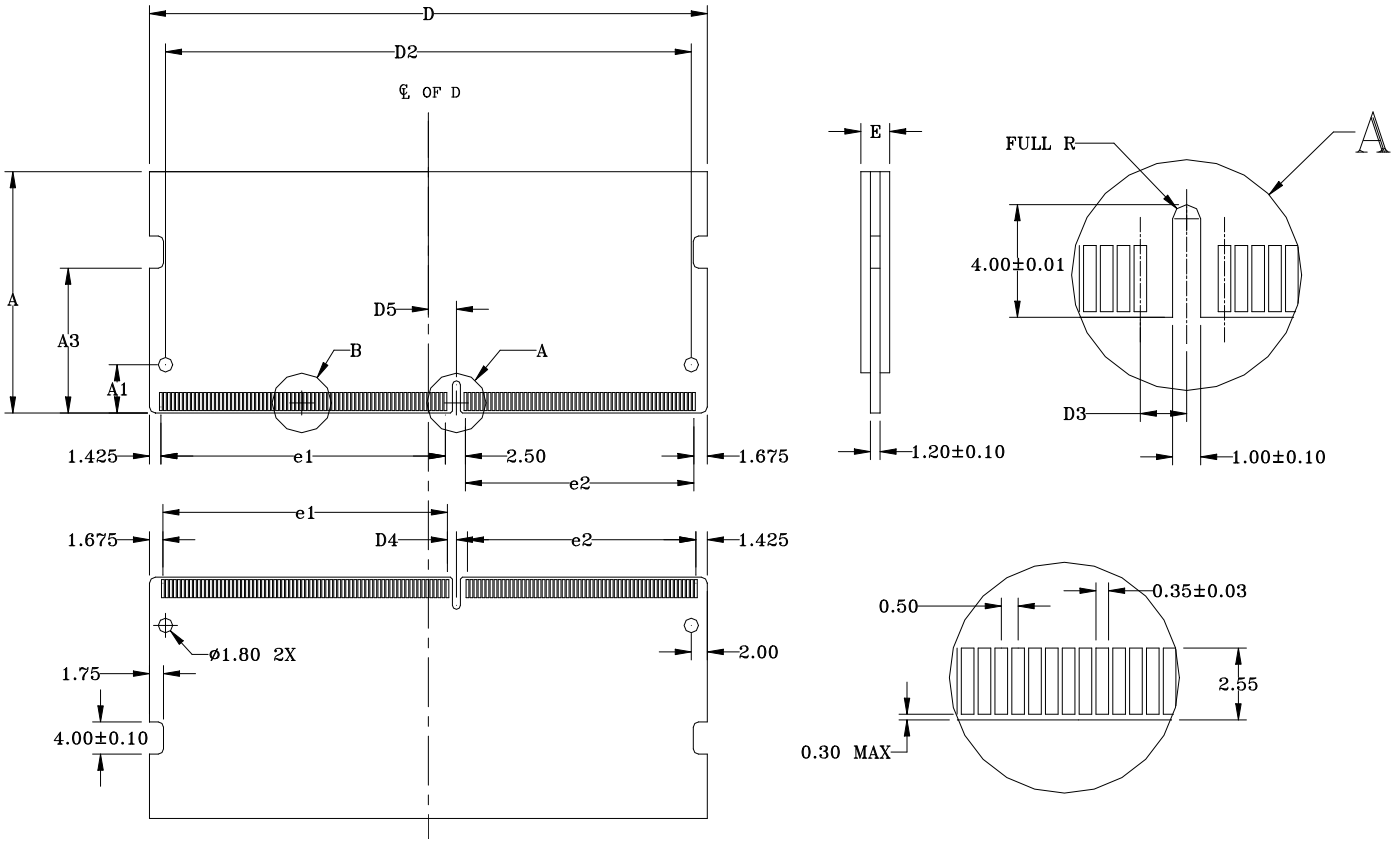
Note:
1. Pin 110, 157 and 161 are defined as NC for single rank module.

Table 7 - Pin Description

Pin Name	Description	Pin Name	Description
V_{DD}	SDRAM I/O & Core Power Supply	V_{PP}	SDRAM Activating Power Supply
V_{REFCA}	SDRAM Command/Address Reference Supply	V_{TT}	SDRAM I/O Termination Supply
V_{SS}	Power Supply Return (Ground)	BG[1:0]	SDRAM Bank Group Select
BA[1:0]	SDRAM Bank Select	A[16:0]	SDRAM Address Bus
CS[1:0]_n	Rank Select Line	ODT[1:0]	SDRAM On-Die Termination Contorl Line
CKE[1:0]	SDRAM Clock Enable Line	RAS_n	SDRAM Row Address Strobe
CAS_n	SDRAM Column Address Strobe	WE_n	SDRAM Write Enable
ACT_n	SDRAM Activate	PARITY	SDRAM Parity Input
CK[1:0]_t	SDRAM Clock (Positive line of Differential pair)	CK[1:0]_c	SDRAM Clock (Negative line of Differential pair)
DQS[8:0]_t	SDRAM Data Strobe (Positive line of Differential pair)	DQS[8:0]_c	SDRAM Data Strobe (Negative line of Differential pair)
D[63:0]	DIMM Memory Data Bus	CB[7:0]	DIMM ECC Check Bit
DM[8:0]_n	SDRAM Data Mask	DBI[8:0]_n	SDRAM Data Bus Inversion
ALERT_n	SDRAM /ALERT	RESET_n	Set SDRAMs to a Known State
V_{DDSPD}	SPD Positive Power Supply	SA[2:0]	EEPROM Address Input
SCL	EEPROM Bus Clock	SDA	EEPROM Data Line
EVENT_n	Thermal Event	NC	Spare Pin (No Connect)

Module Dimension

Figure 1 – 260 Pin DDR4 Unbuffered SODIMM



Symbol	MIN	NOM	MAX
A	29.85	30.00	30.15
A1		6.00 BASIC	
A3	17.85	18.00	18.15
D	69.45	69.60	69.75
D2		65.60 BASIC	
D3		1.375 BASIC	
D4		1.125 BASIC	
D5		3.50 BASIC	
e1		35.50 BASIC	
e2		28.50 BASIC	
E			3.70

Notes:
1. All dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. Tolerance on all dimensions is ±0.15 unless otherwise specified.
3. All dimensions are in millimeter.

Revision History

Revision	Descriptions	Release Date
0.1	Preliminary release	May, 2022
1.0	Initial release	Nov, 2023
2.0	Add “DDR4-2933” and “DDR4-3200” into supported speed	Jul, 2025