Product Specification | Rev. 1.0 | 2025

IMM2G64D4DUD8BG (Die Revision B)

16GByte (2G x 64Bit)

16GB DDR4 Unbuffered DIMM
RoHS Compliant Product

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Features

- 288-Pin Unbuffered Dual-In-Line Memory Module
- JEDEC-Standard
- Capacity: 16GB
- 64Bit Data Bus Width without ECC
- Programmable CAS Latency (CL):
  - DDR4-3200: 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 22, 24
  - DDR4-2933: 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22
  - DDR4-2666: 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20
  - DDR4-2400: 10, 11, 12, 13, 14, 15, 16, 17, 18
- Programmable CAS Write Latency (CWL):
  - DDR4-3200: 9, 10, 11, 12, 14, 16, 18, 20
  - DDR4-2933: 9, 10, 11, 12, 14, 16, 18, 20
  - DDR4-2666: 9, 10, 11, 12, 14, 16, 18
  - DDR4-2400: 9, 10, 11, 12, 14, 16
- Power Supply: V_{DD}, V_{DDQ} = 1.2V ± 0.06V
- DRAM Activating Power Supply: V_{PP} = 2.5V (2.375V – 2.75V)
- SPD Power Supply: V_{DDSPD} = 2.5V or 3.3V
- Bi-directional Differential Data-Strobe
- 8192 Refresh Cycle / 64ms
- Refresh Mode: Auto, Self
- Low Power Auto Self Refresh Mode
- Burst Length: 8, 4
- On-Die Termination (ODT)
- ZQ Calibration
- Asynchronous Reset
- Serial Presence Detect (SPD) EEPROM
- Golde Edge Contacts
- 100% RoHS Compliant
- Standard Module Height: 31.25mm (1.23inch)

Table 1 - Ordering Information for RoHS Compliant Product

Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM2G64D4DUD8BG-Bzzzy(:qqq)	16GB	2Gx64	2	DDR4 Unbuffered DIMM

Note:

y:	Temperature Grade	(refer to Table 2)
zzz:	Speed Grade	(refer to Table 3)
qqq:	IM Reference Code	Blank or Reserved

Table 2 - Temperature Grade

Part Number	Temperature Grade	T_{CASE}
Blank	Commercial Temperature	0°C to 95°C
I	Industrial Temperature	-40°C to 95°C

Note: T_{CASE} is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to be double when 85°C < T_{CASE} ≤ 95°C

Table 3 - Speed Grade

Part Number	Speed Grade	Max. Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
062	DDR4-3200	1600MHz (0.625ns @ CL22)
068	DDR4-2933	1467MHz (0.682ns @ CL21)
075	DDR4-2666	1333MHz (0.750ns @ CL19)
083	DDR4-2400	1200MHz (0.833ns @ CL17)

Table 4 - Memory Chip Information

Part Number	Base Device Brand	Base Device	Voltage	Type	Chip Packing
IMM2G64D4DUD8BG-Bzzzy(:qqq)	IM	IM8G08D4GBBG	1.2V	1Gx8	Lead Free

Part Number Decoder

IM M 2G64 D4 DU D 8 B G - B 062 (I) (:qqq)

IM Module

DRAM Brand
M = IM

Module Configuration
2G64 = 2Gx72 (16GB)

Memory Type
D4 = DDR4

Module Form Factor
DU = Unbuffered DIMM (UDIMM)

Number of Rank
D = Dual Rank

IM Reference code
Blank or Reserved

Temperature Grade
Blank = Commercial Temperature
(0℃ to +95℃ T_{CASE})
I = Industrial Temperature
(-40℃ to +95℃ T_{CASE})
***Note**: The refresh rate must be doubled when the operating temperature TCASE exceeds +85℃*

Speed Grade
062 = DDR4-3200 CL22
068 = DDR4-2933 CL21
075 = DDR4-2666 CL19
083 = DDR4-2400 CL17

DRAM Revision
B = Revision B

Green Nature
G = RoHS Compliance

Module PCB Revision
B = Revision B

DRAM Bit Width
8 = using x8 components

Table 5 - Addressing

Parameter	16GB
Bank Group	4 BG[1:0]
Bank Address	4 BA[1:0]
Row Address	64K A[15:0]
Column Address	1K A[9:0]
Device Configuration	8Gb (1Gx8)
Module Rank Address	2 CS[1:0]_n
Number of Devices	16

Table 6 – Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	NC	145	NC	73	V_{DD}	217	V_{DD}
2	V_{SS}	146	V_{REFCA}	74	CK0_t	218	CK1_t
3	D4	147	V_{SS}	75	CK0_c	219	CK1_c
4	V_{SS}	148	D5	76	V_{DD}	220	V_{DD}
5	D0	149	V_{SS}	77	V_{TT}	221	V_{TT}
6	V_{SS}	150	D1	78	EVENT_n	222	PARITY
7	DM0_n, DBI0_n	151	V_{SS}	79	A0	223	V_{DD}
8	NC	152	DQS0_c	80	V_{DD}	224	BA1
9	V_{SS}	153	DQS0_t	81	BA0	225	A10, AP
10	D6	154	V_{SS}	82	A16, RAS_n	226	V_{DD}
11	V_{SS}	155	D7	83	V_{DD}	227	NC
12	D2	156	V_{SS}	84	CS0_n	228	A14, WE_n
13	V_{SS}	157	D3	85	V_{DD}	229	V_{DD}
14	D12	158	V_{SS}	86	A15, CAS_n	230	NC
15	V_{SS}	159	D13	87	ODT0	231	V_{DD}
16	D8	160	V_{SS}	88	V_{DD}	232	A13
17	V_{SS}	161	D9	89	CS1_n	233	V_{DD}
18	DM1_n, DBI1_n	162	V_{SS}	90	V_{DD}	234	NC
19	NC	163	DQS1_c	91	ODT1	235	NC
20	V_{SS}	164	DQS1_t	92	V_{DD}	236	V_{DD}
21	D14	165	V_{SS}	93	NC	237	NC
22	V_{SS}	166	D15	94	V_{SS}	238	SA2
23	D10	167	V_{SS}	95	D36	239	V_{SS}
24	V_{SS}	168	D11	96	V_{SS}	240	D37
25	D20	169	V_{SS}	97	D32	241	V_{SS}
26	V_{SS}	170	D21	98	V_{SS}	242	D33
27	D16	171	V_{SS}	99	DM4_n, DBI4_n	243	V_{SS}
28	V_{SS}	172	D17	100	NC	244	DQS4_c
29	DM2_n, DBI2_n	173	V_{SS}	101	V_{SS}	245	DQS4_t
30	NC	174	DQS2_c	102	D38	246	V_{SS}
31	V_{SS}	175	DQS2_t	103	V_{SS}	247	D39
32	D22	176	V_{SS}	104	D34	248	V_{SS}
33	V_{SS}	177	D23	105	V_{SS}	249	D35
34	D18	178	V_{SS}	106	D44	250	V_{SS}
35	V_{SS}	179	D19	107	V_{SS}	251	D45
36	D28	180	V_{SS}	108	D40	252	V_{SS}
37	V_{SS}	181	D29	109	V_{SS}	253	D41
38	D24	182	V_{SS}	110	DM5_n, DBI5_n	254	V_{SS}
39	V_{SS}	183	D25	111	NC	255	DQS5_c
40	DM3_n, DBI3_n	184	V_{SS}	112	V_{SS}	256	DQS5_t
41	NC	185	DQS3_c	113	D46	257	V_{SS}
42	V_{SS}	186	DQS3_t	114	V_{SS}	258	D47
43	D30	187	V_{SS}	115	D42	259	V_{SS}
44	V_{SS}	188	D31	116	V_{SS}	260	D43
45	D26	189	V_{SS}	117	D52	261	V_{SS}
46	V_{SS}	190	D27	118	V_{SS}	262	D53
47	NC	191	V_{SS}	119	D48	263	V_{SS}

Pin	Name	Pin	Name	Pin	Name	Pin	Name
48	V_{SS}	192	NC	120	V_{SS}	264	D49
49	NC	193	V_{SS}	121	DM6_n, DBI6_n	265	V_{SS}
50	V_{SS}	194	NC	122	NC	266	DQS6_c
51	NC	195	V_{SS}	123	V_{SS}	267	DQS6_t
52	NC	196	NC	124	D54	268	V_{SS}
53	V_{SS}	197	NC	125	V_{SS}	269	D55
54	NC	198	V_{SS}	126	D50	270	V_{SS}
55	V_{SS}	199	NC	127	V_{SS}	271	D51
56	NC	200	V_{SS}	128	D60	272	V_{SS}
57	V_{SS}	201	NC	129	V_{SS}	273	D61
58	RESET_n	202	V_{SS}	130	D56	274	V_{SS}
59	V_{DD}	203	CKE1	131	V_{SS}	275	D57
60	CKE0	204	V_{DD}	132	DM7_n, DBI7_n	276	V_{SS}
61	V_{DD}	205	NC	133	NC	277	DQS7_c
62	ACT_n	206	V_{DD}	134	V_{SS}	278	DQS7_t
63	BG0	207	BG1	135	D62	279	V_{SS}
64	V_{DD}	208	ALERT_n	136	V_{SS}	280	D63
65	A12, BC_n	209	V_{DD}	137	D58	281	V_{SS}
66	A9	210	A11	138	V_{SS}	282	D59
67	V_{DD}	211	A7	139	SA0	283	V_{SS}
68	A8	212	V_{DD}	140	SA1	284	V_{DDSPD}
69	A6	213	A5	141	SCL	285	SDA
70	V_{DD}	214	A4	142	V_{PP}	286	V_{PP}
71	A3	215	V_{DD}	143	V_{PP}	287	V_{PP}
72	A1	216	A2	144	NC	288	V_{PP}

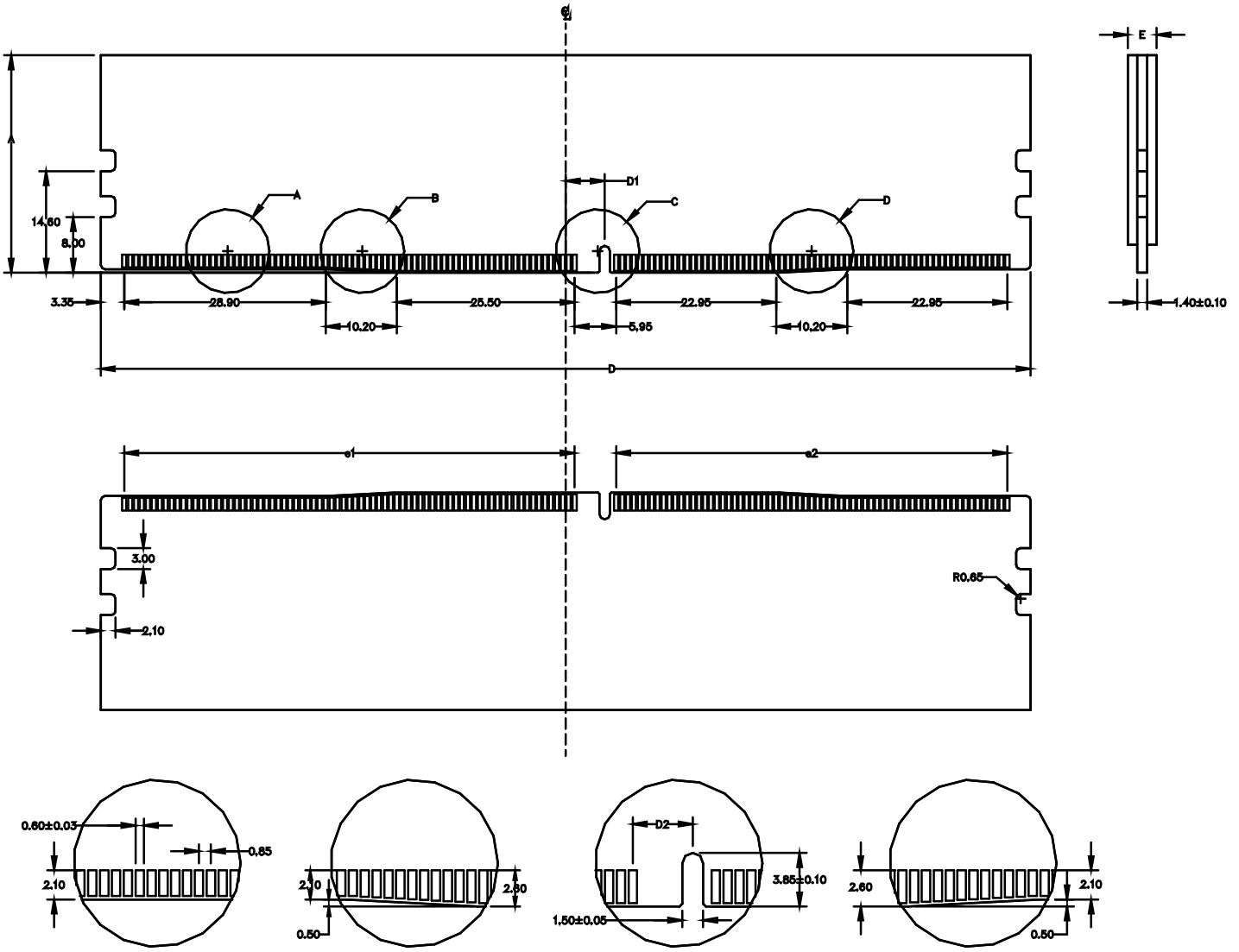
Note:
1. Pin 89, 91 and 203 are defined as NC for single rank module.
2. Pin 207 is defined as NC for x16 based module.

Table 7 - Pin Description

Pin Name	Description	Pin Name	Description
V_{DD}	SDRAM I/O & Core Power Supply	V_{PP}	SDRAM Activating Power Supply
V_{REFCA}	SDRAM Command/Address Reference Supply	V_{TT}	SDRAM I/O Termination Supply
V_{SS}	Power Supply Return (Ground)	BG[1:0]	SDRAM Bank Group Select
BA[1:0]	SDRAM Bank Select	A[16:0]	SDRAM Address Bus
CS[1:0]_n	Rank Select Line	ODT[1:0]	SDRAM On-Die Termination Control Line
CKE[1:0]	SDRAM Clock Enable Line	RAS_n	SDRAM Row Address Strobe
CAS_n	SDRAM Column Address Strobe	WE_n	SDRAM Write Enable
ACT_n	SDRAM Activate	PARITY	SDRAM Parity Input
CK[1:0]_t	SDRAM Clock (Positive line of Differential pair)	CK[1:0]_c	SDRAM Clokc (Negative line of Differential pair)
DQS[7:0]_t	SDRAM Data Strobe (Positive line of Differential pair)	DQS[7:0]_c	SDRAM Data Strobe (Negative line of Differential pair)
D[63:0]	DIMM Memory Data Bus	DM[7:0]_n	SDRAM Data Mask
DBI[7:0]_n	SDRAM Data Bus Inversion	RESET_n	Set SDRAMs to a Known State
ALERT_n	SDRAM ALERT_n	V_{DDSPD}	SPD Positive Power Supply
SA[2:0]	EEPROM Address Select	SCL	EEPROM Clock
SDA	EEPROM Data Line	NC	No Connection

Module Dimension

Figure 1 – 288 Pin DDR4 Unbuffered DIMM



Symbol	MIN	NOM	MAX
A	31.05	31.25	31.40
D	133.20	133.35	133.50
D1		5.575 BASIC	
D2		4.30 BASIC	
e1		64.60 BASIC	
e2		56.10 BASIC	
E			4.10

Notes:
1. All dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. Tolerance on all dimensions is ±0.15 unless otherwise specified.
3. All dimensions are in millimeter.

Revision History

Revision	Descriptions	Release Date
1.0	Initial release	Jul, 2025