

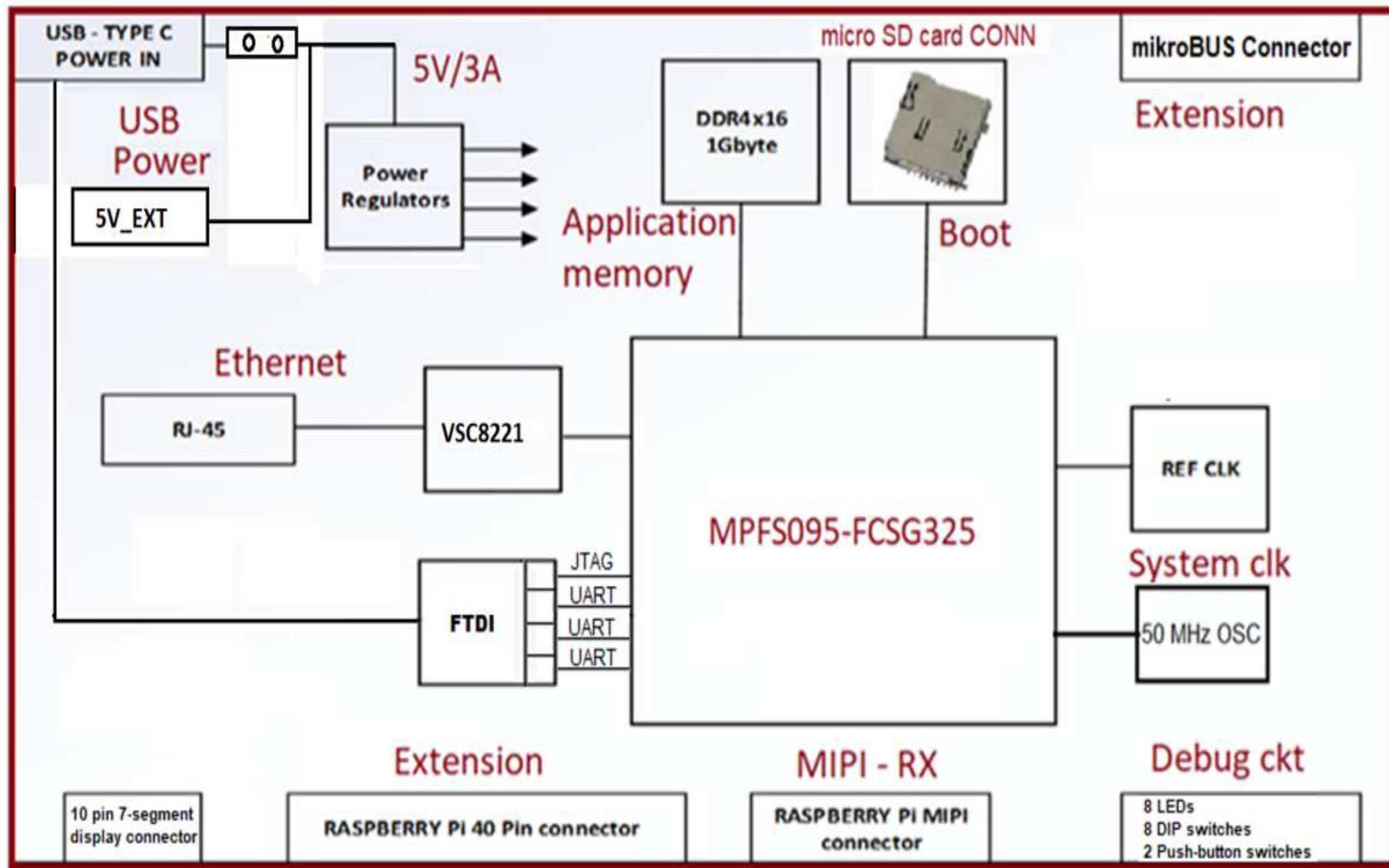
PolarFire SoC Discovery Kit

Part Number: MPFS-DISCO-KIT

PAGE NO	TITLE	PAGE NO	TITLE
01	TITLE PAGE	18	
02	Block Diagram	19	
03	MSS_DDR4X16_Connection	20	
04	BANK4 & uSD Card Connection	21	
05	VSC8221 MAC Connection	22	
06	VSC8221 G5 Interface Connection	23	
07	Bank0,1,2 Connection	24	
08	Peripheral Connection	25	
09	Programming Connection	26	
10	FT4232H Connection	27	
11	Power & GND Connection	28	
12	Decoupling Capacitor Connection	29	
13	5V Supply	30	
14	Power Regulator Connection		
15			
16			
17			

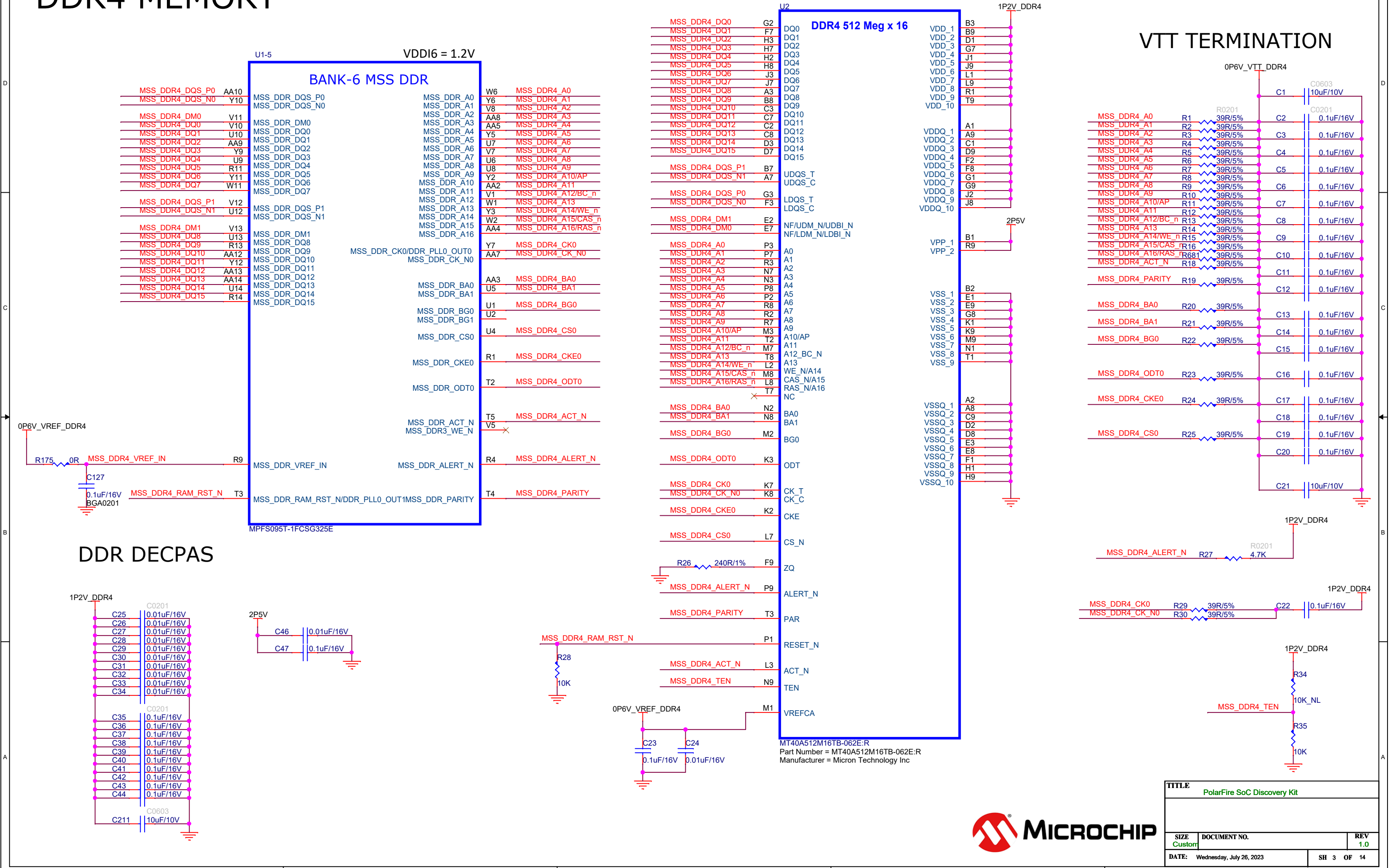


Project Name:			PolarFire SoC Discovery Kit		
Rev	Part Number:	DVP-100-000578-002		PACTRON:	
1.0					
Originator:					
Size	Date:	Wednesday, July 26, 2023			Sheet
B				1	of 14



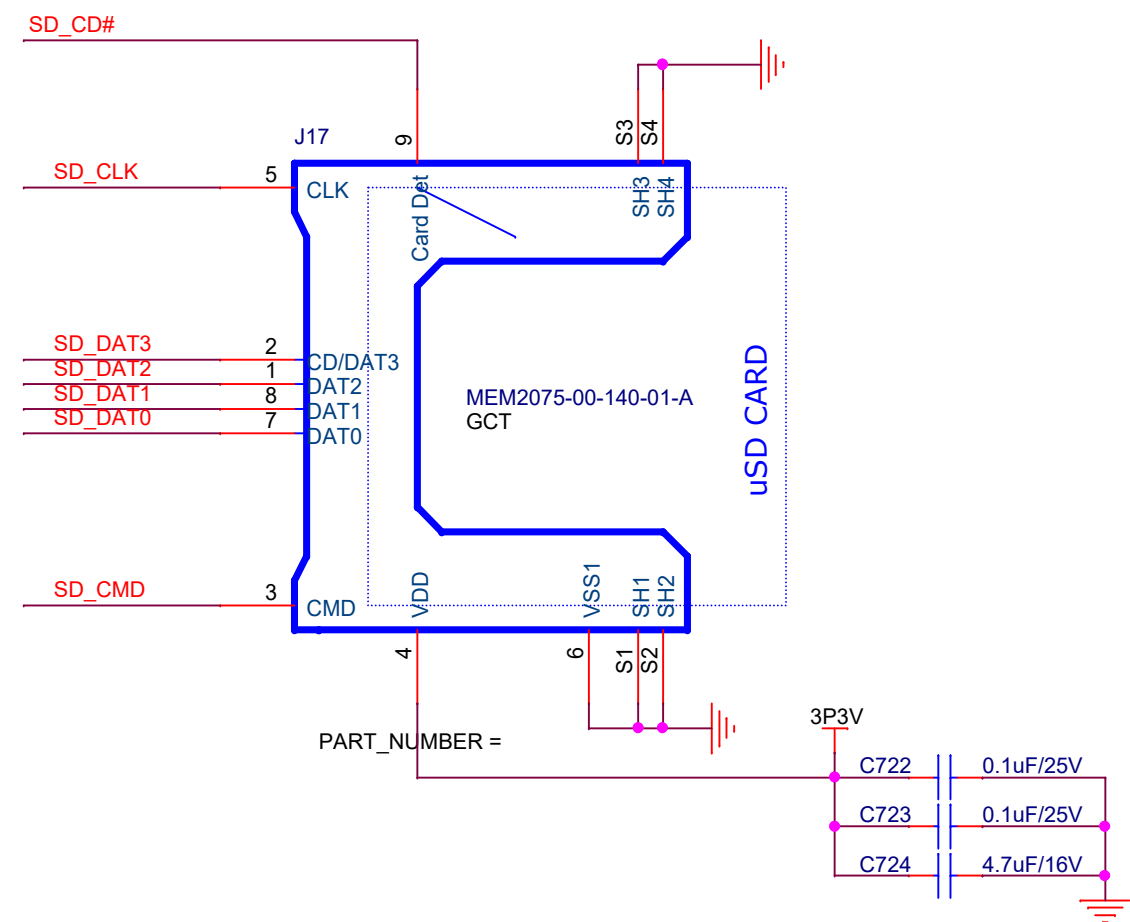
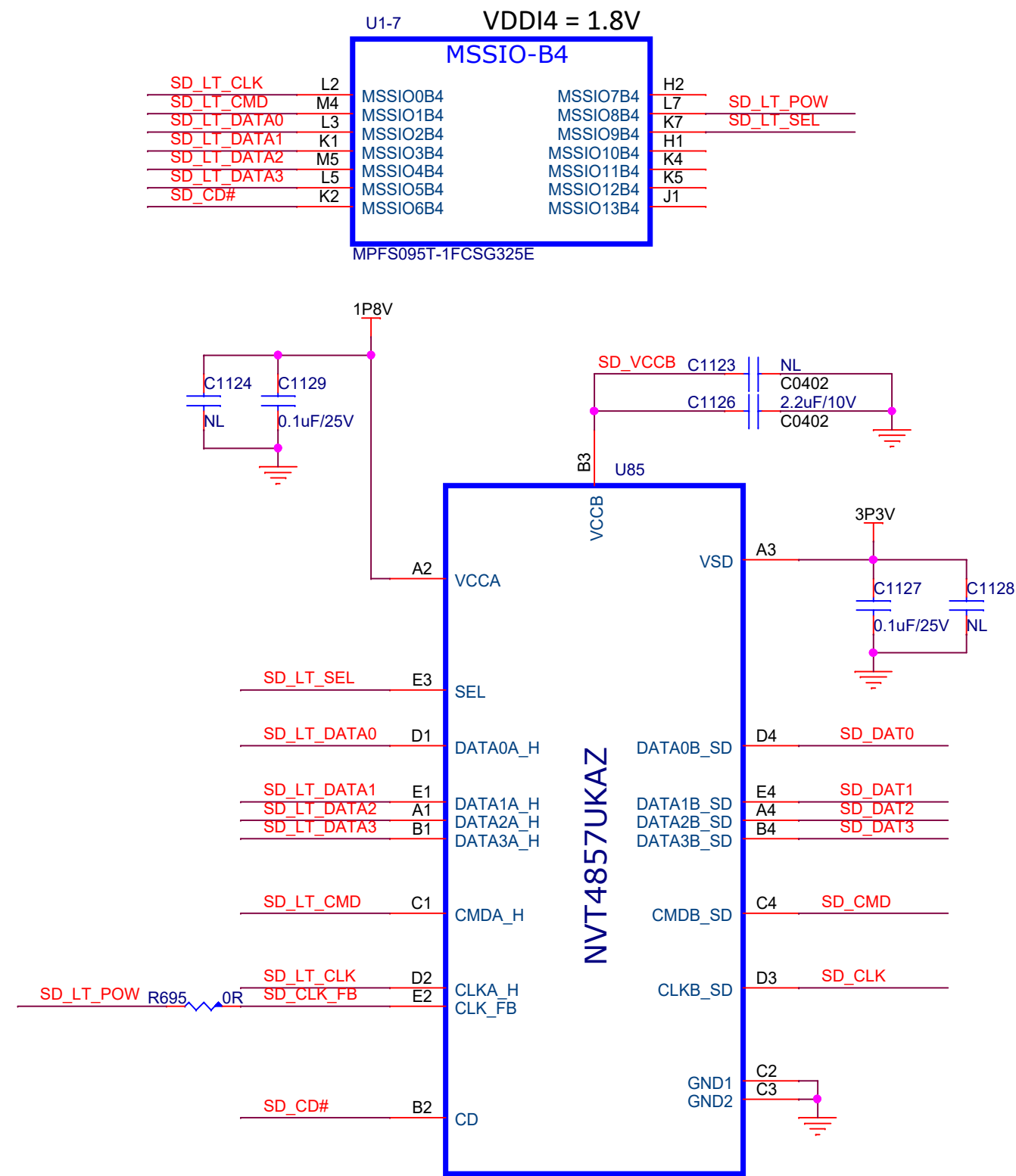
TITLE		
PolarFire SoC Discovery Kit		
SIZE	DOCUMENT NO.	REV
B		1.0
DATE:	Wednesday, July 26, 2023	SH 2 OF 14

DDR4 MEMORY



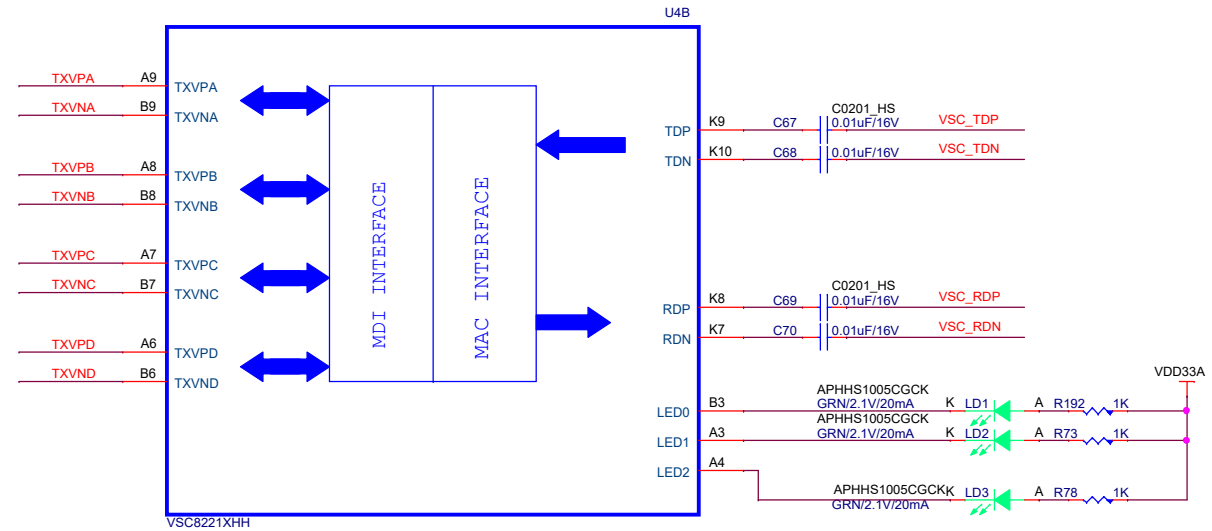
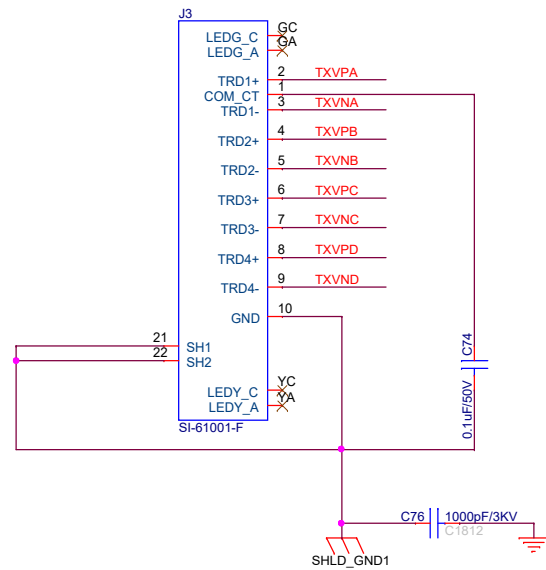
TITLE		
PolarFire SoC Discovery Kit		
SIZE	DOCUMENT NO.	REV
Custom		1.0
DATE: Wednesday, July 26, 2023		SH 3 OF 14

BANK4- uSD Conneciton

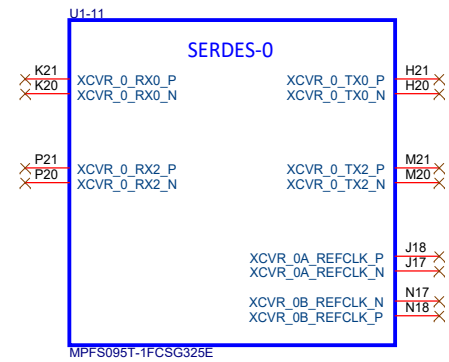
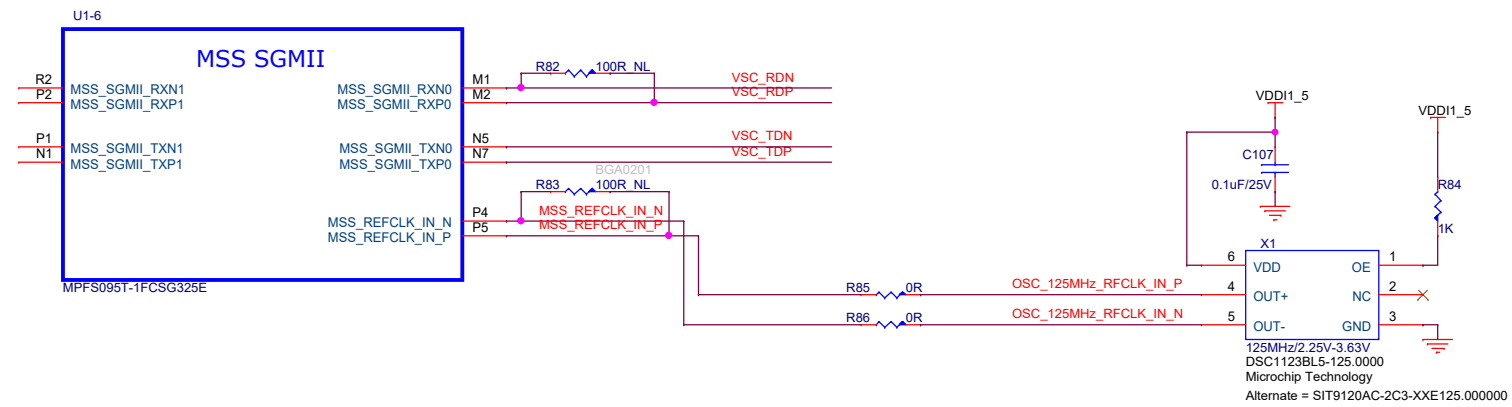
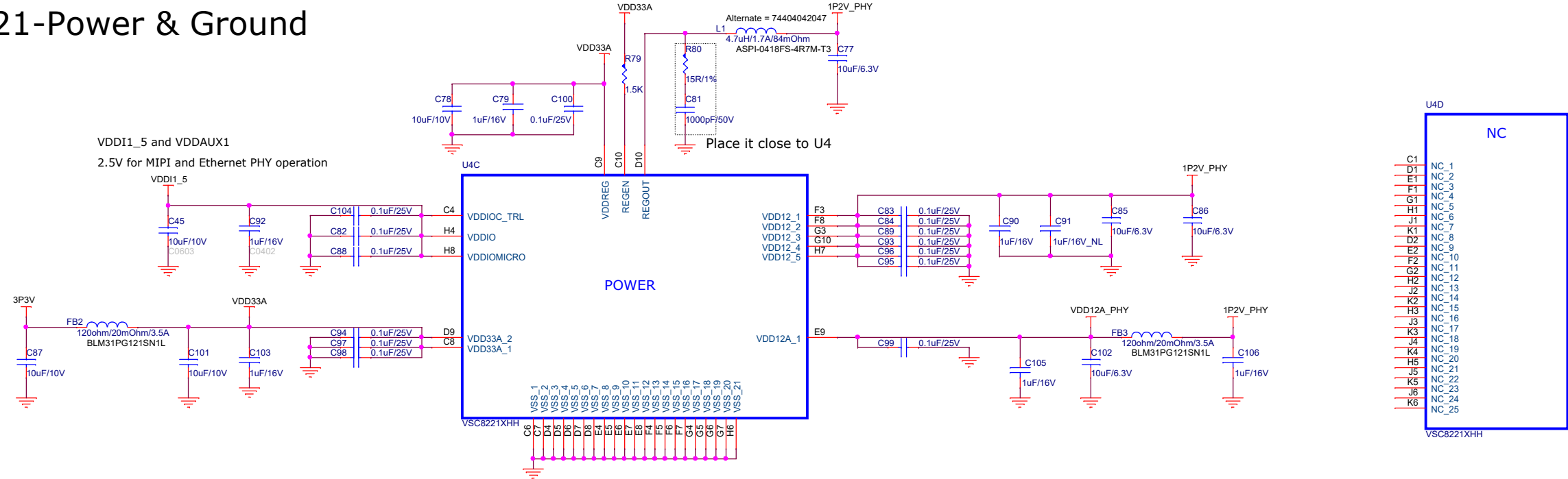


TITLE		
PolarFire SoC Discovery Kit		
SIZE	DOCUMENT NO.	REV
Custom		1.0
DATE:	Wednesday, July 26, 2023	SH 4 OF 14

VSC8221 - SGMII Interface

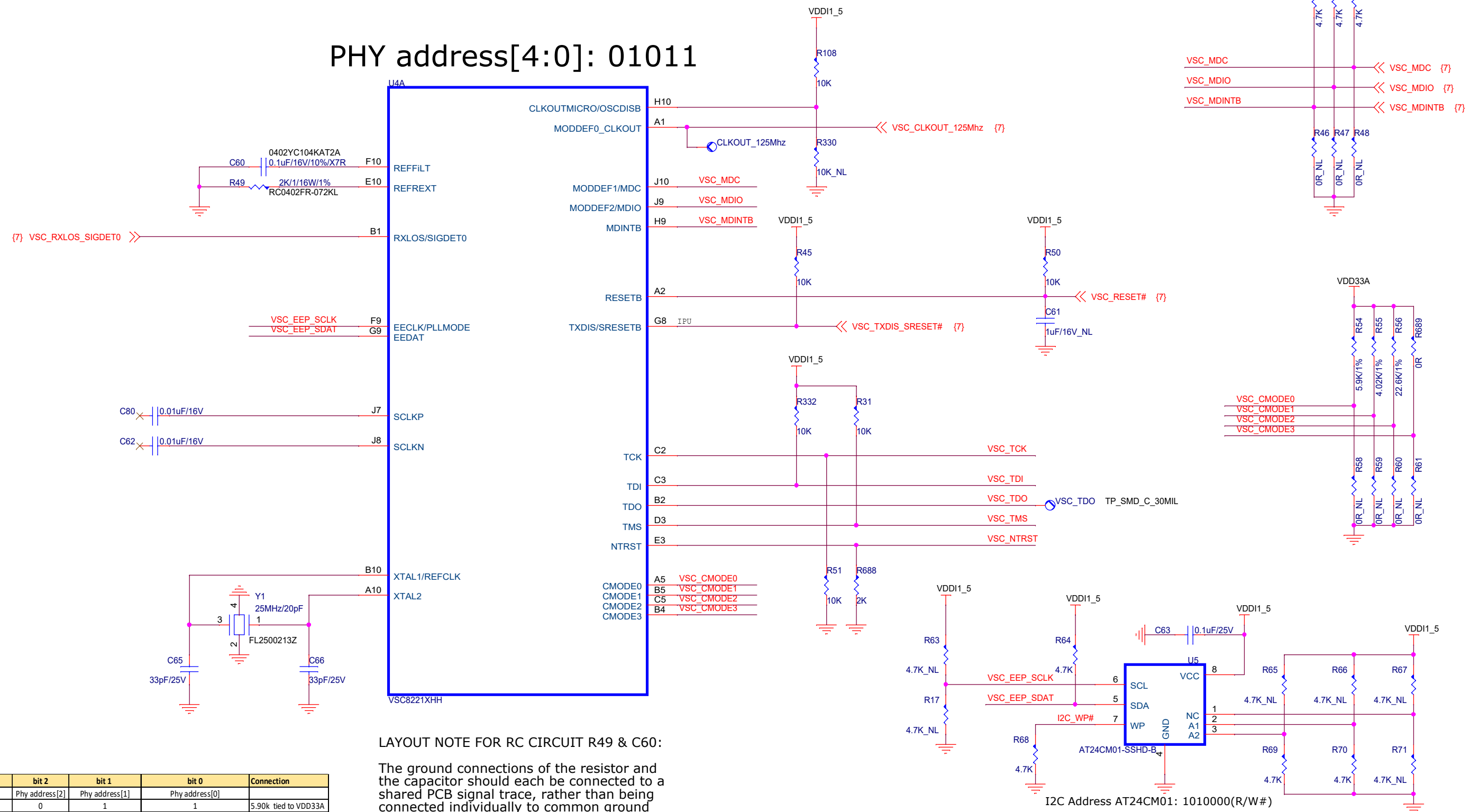


VSC8221-Power & Ground



VSC8221 - Connection

PHY address[4:0]: 01011



	bit 3	bit 2	bit 1	bit 0	Connection
CMODE 0	Phy address[3]	Phy address[2]	Phy address[1]	Phy address[0]	
	1	0	1	1	5.90k tied to VDD33A
CMODE1	SFP Mode Disable	PHY Address[4]	SIGDET pin direction	SerDes Line impedance	
	1	0	1	0	4.02k tied to VDD33A
CMODE 2	PHY Operating Mode[3]	PHY Operating Mode[2]	PHY Operating Mode[1]	PHY Operating Mode[0]	
	1	1	1	1	22.6k tied to VDD33A
CMODE3	LED Control[1]	SQE Enable	Reserved	Auto-negotiation Advertisement Control[1]	
	1	0	0	0	0k tied to VDD33A
	LED[2:0] = {Link/Activty, Link/Activty, Fault}			10/100/1000BASE-T HDX, FDX	

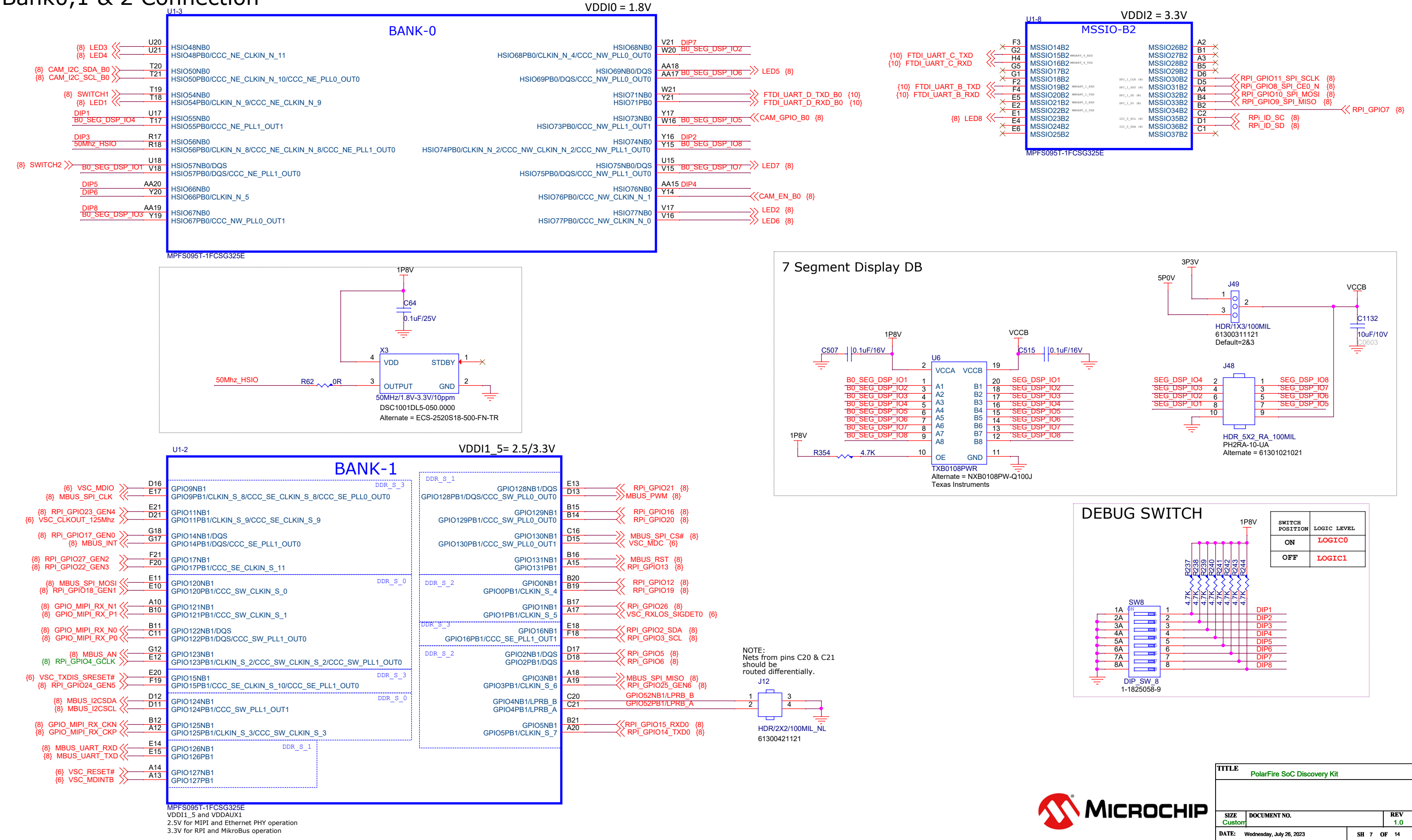
LAYOUT NOTE FOR RC CIRCUIT R49 & C60:

The ground connections of the resistor and the capacitor should each be connected to a shared PCB signal trace, rather than being connected individually to common ground plane. This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitor and resistor should be placed as close as possible to the VSC8221

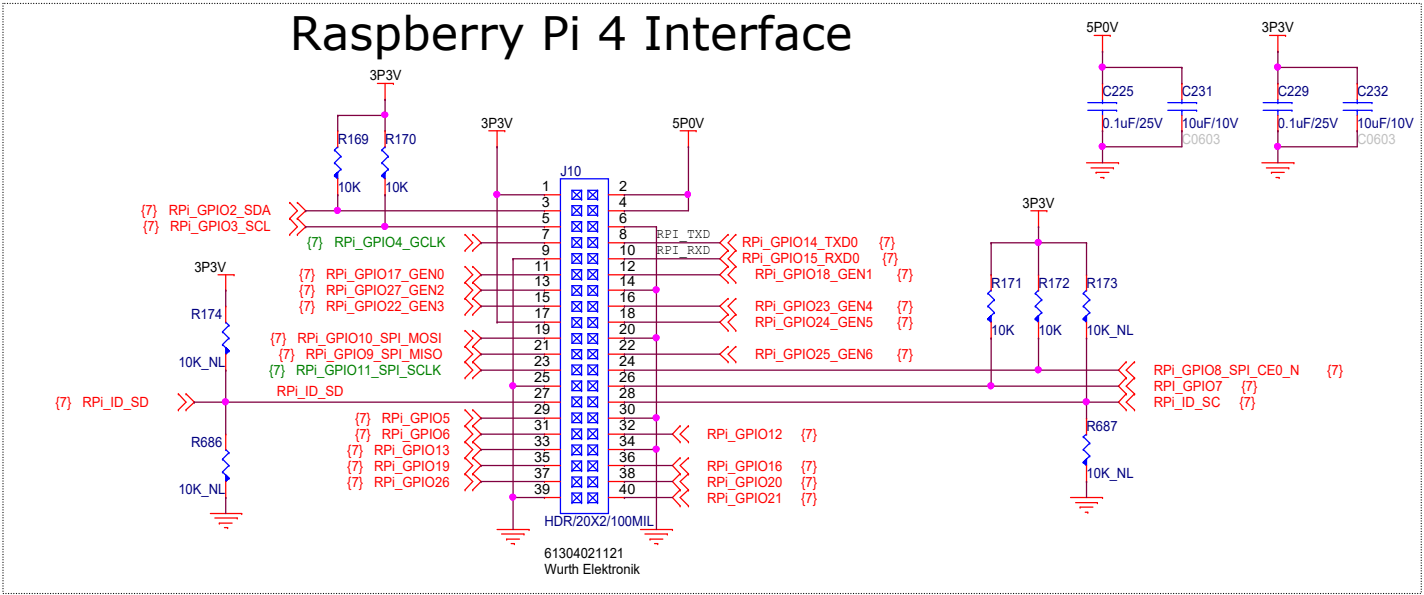
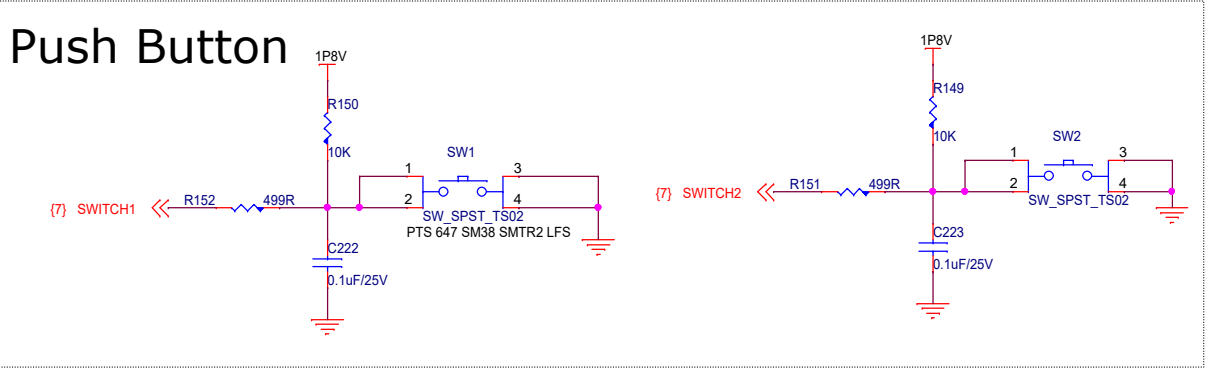
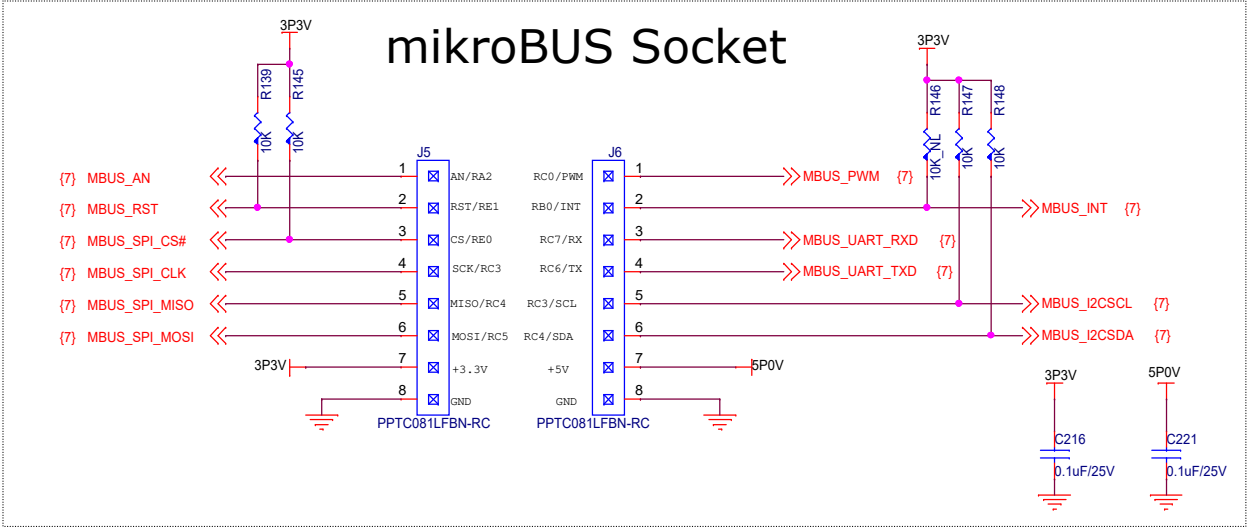


TITLE			
PolarFire SoC Discovery Kit			
SIZE	DOCUMENT NO.		REV
Custom			1.0
DATE: Wednesday, July 26, 2023			SH 6 OF 14

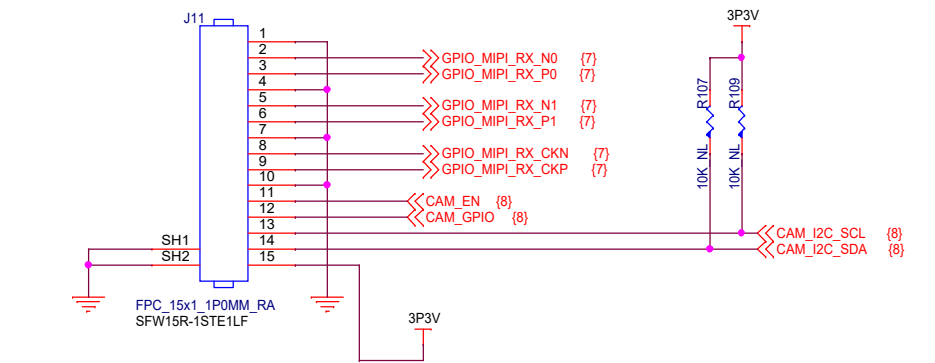
Bank0,1 & 2 Connection



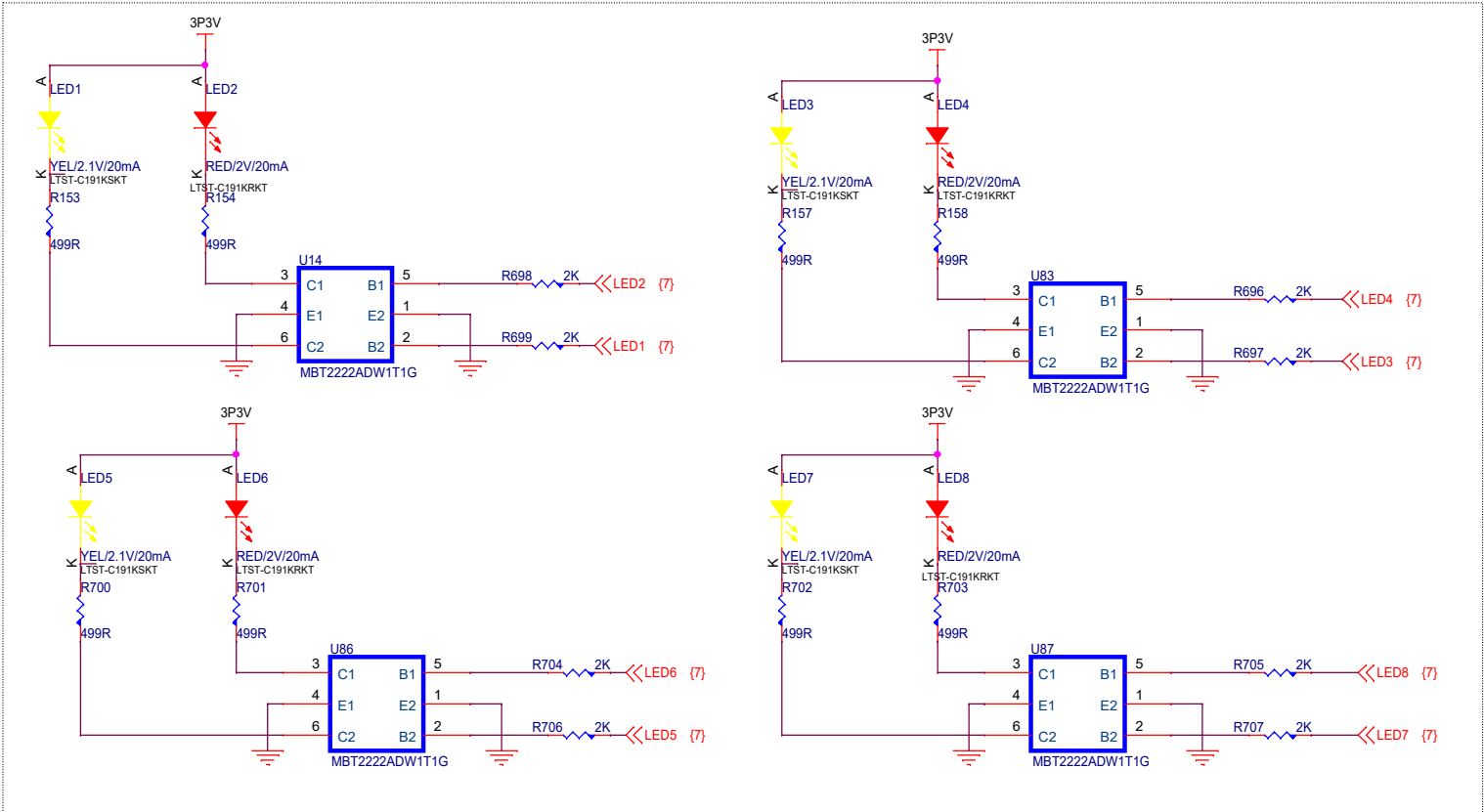
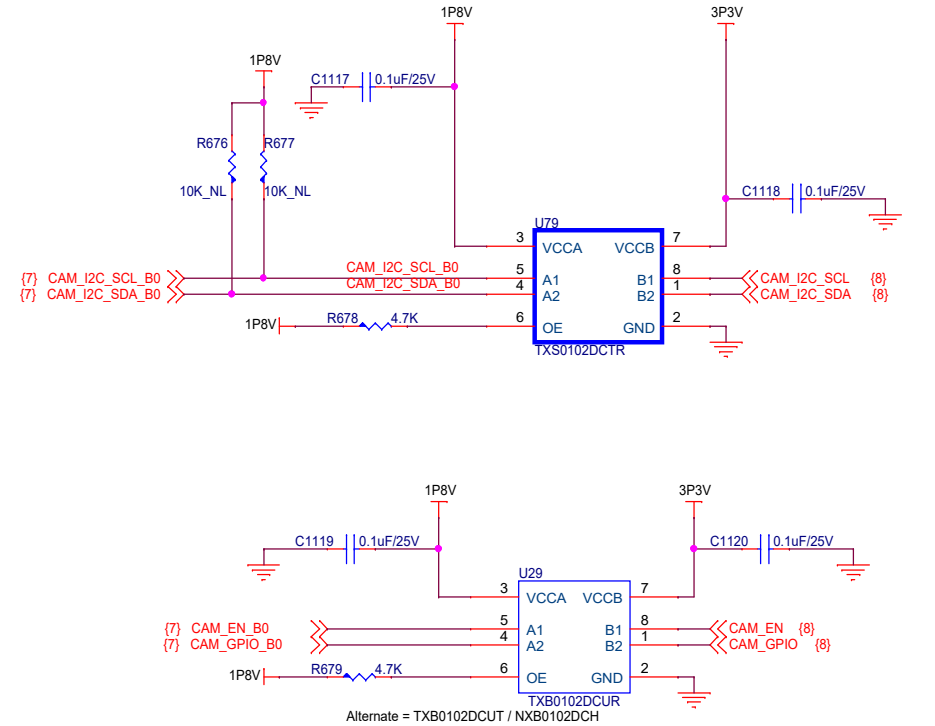
TITLE		
PolarFire SoC Discovery Kit		
SIZE	DOCUMENT NO.	REV
Custom		1.0
DATE:	Wednesday, July 26, 2023	SH 7 OF 14



Raspberry Pi MIPI RX Connector

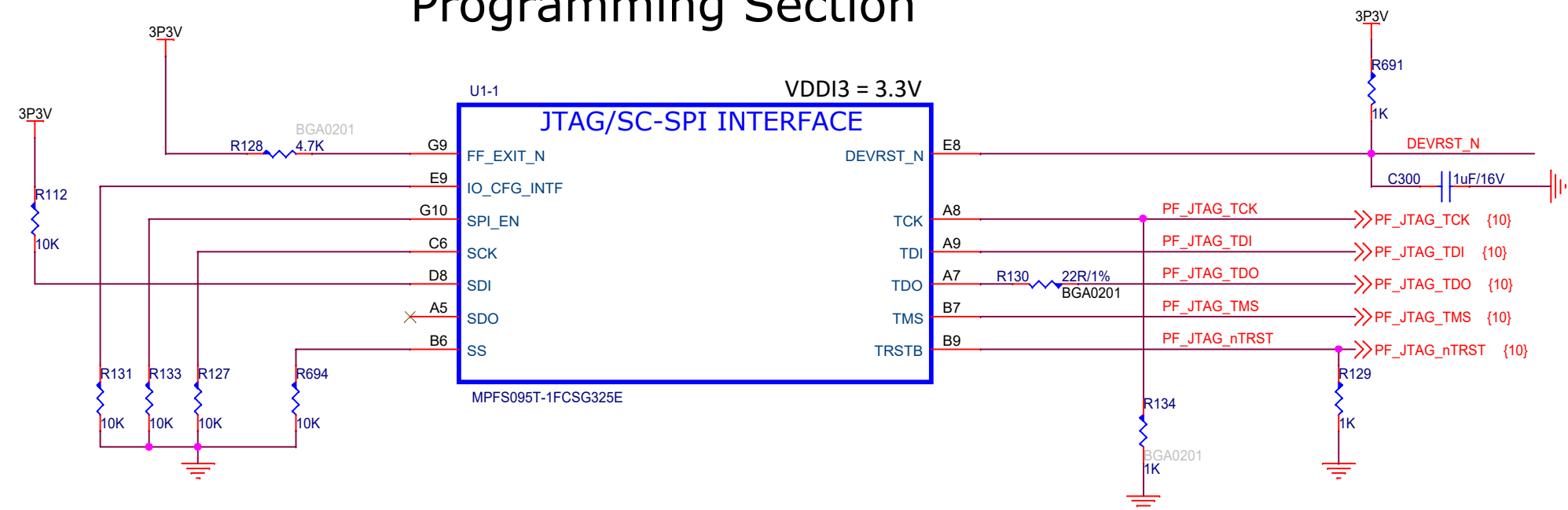


Cable to cable mating, Raspberry Camera module V2 board/Camera HQ
Cable Part Supplied with Camera Module - Opposite Sided Contacts

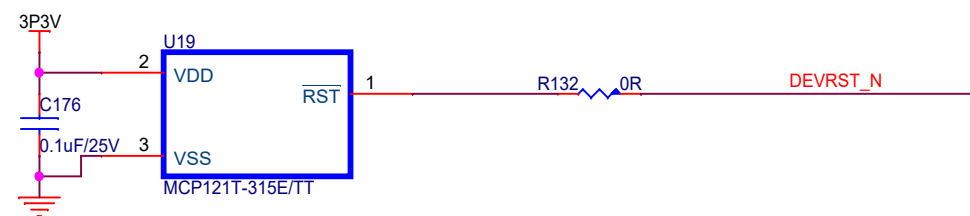


TITLE		
PolarFire SoC Discovery Kit		
SIZE	DOCUMENT NO.	REV
Custom		1.0
DATE:	Wednesday, July 26, 2023	SH 8 OF 14

Programming Section

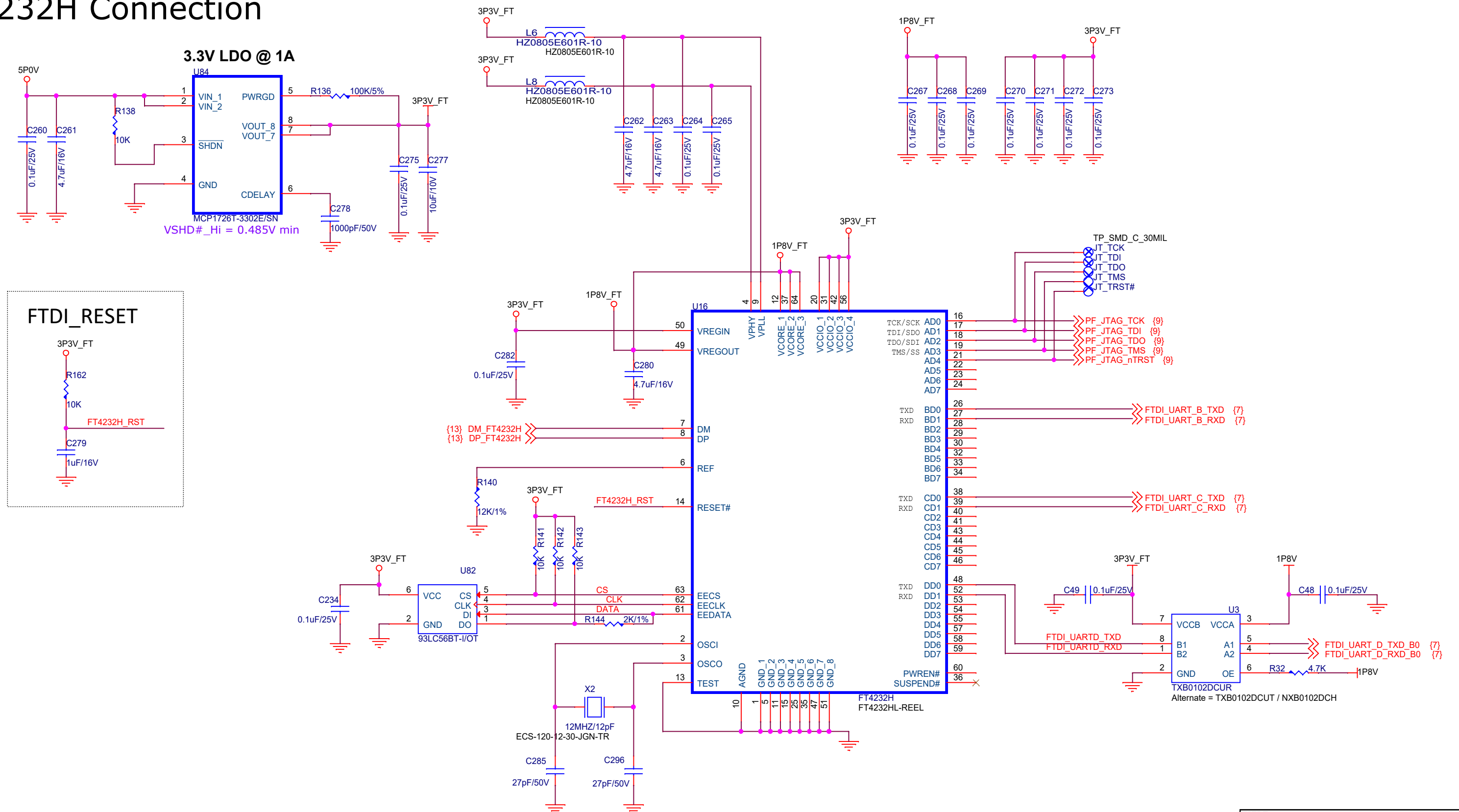


Device Reset



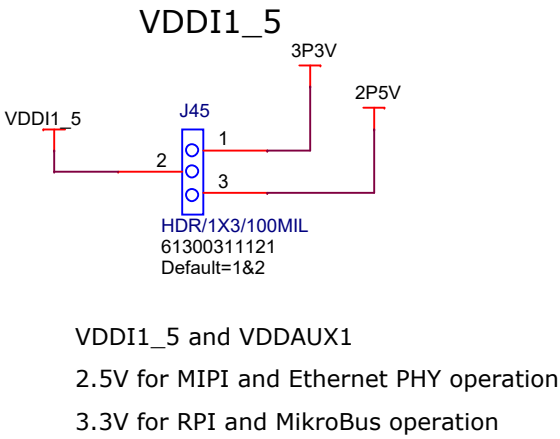
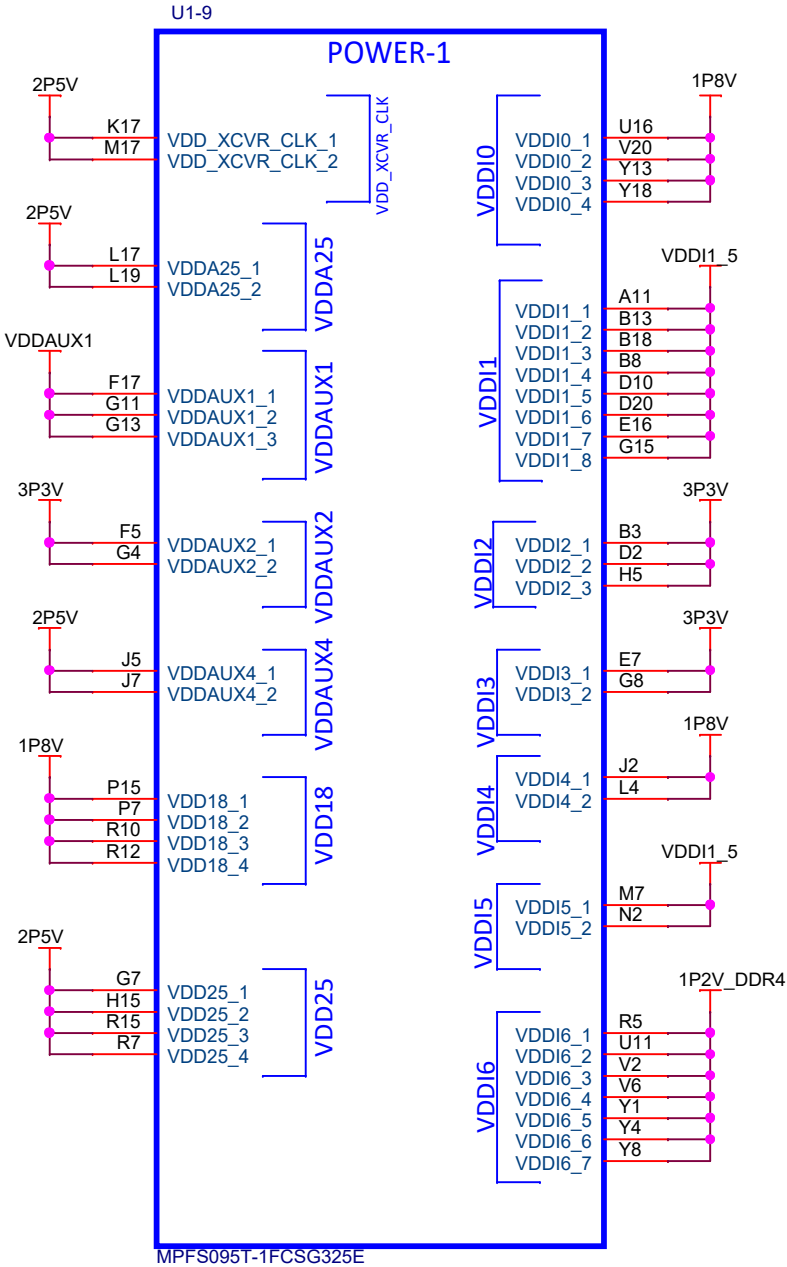
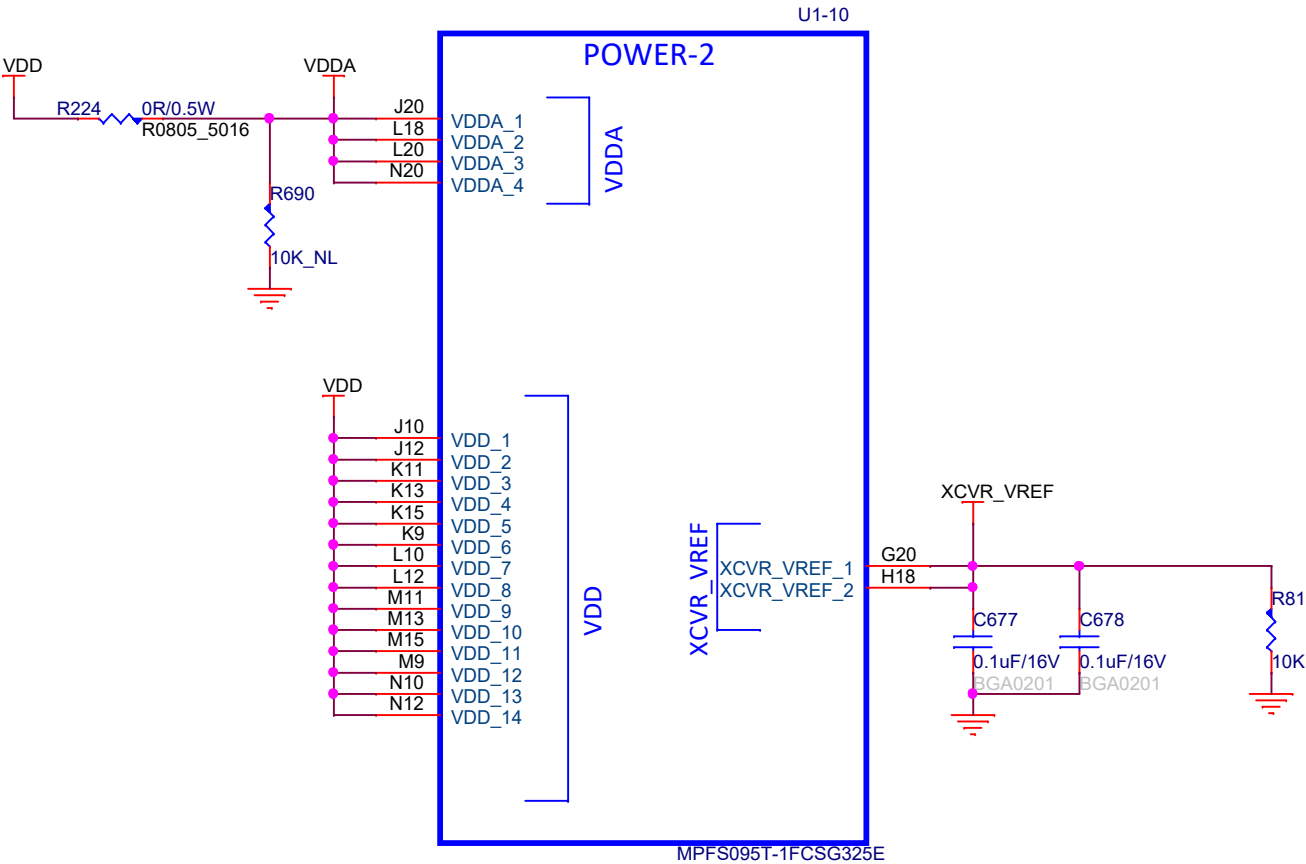
TITLE		
PolarFire SoC Discovery Kit		
SIZE	DOCUMENT NO.	REV
Custom		1.0
DATE: Wednesday, July 26, 2023		SH 9 OF 14

FT4232H Connection



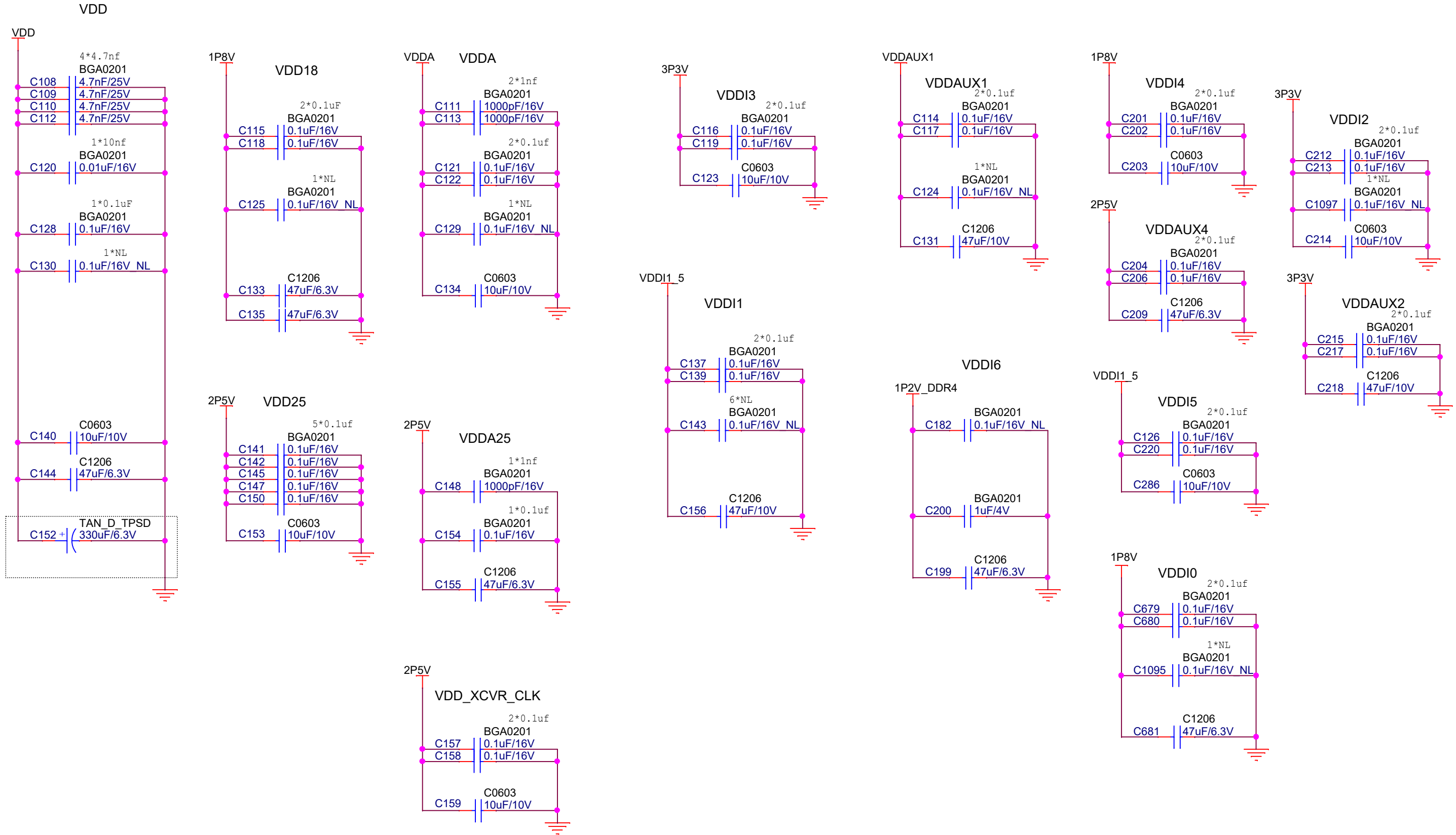
TITLE PolarFire SoC Discovery Kit			
SIZE Custom	DOCUMENT NO. 		REV 1.0
DATE: Wednesday, July 26, 2023		SH 10 OF 14	

Power & GND Connection



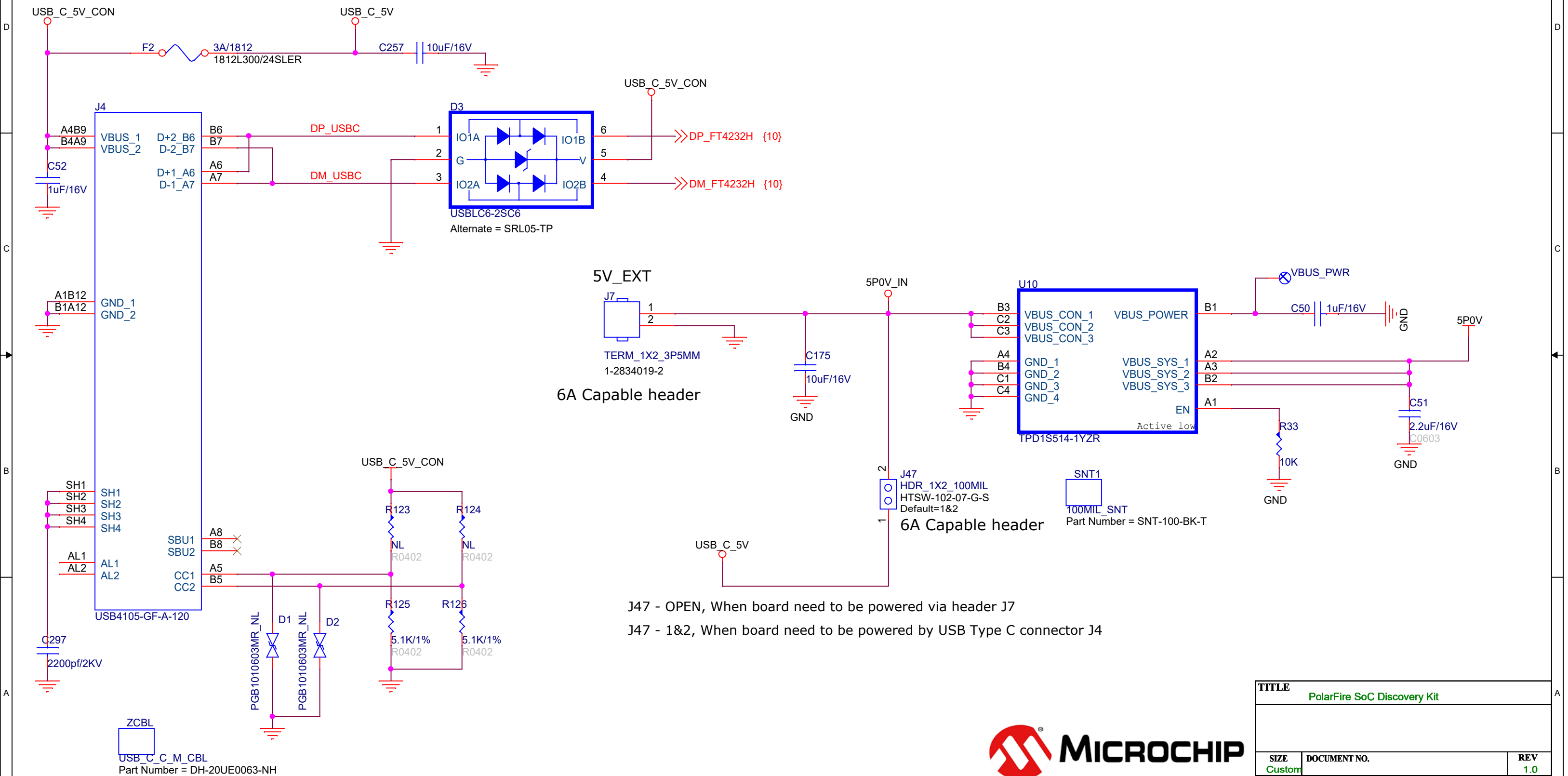
TITLE		
PolarFire SoC Discovery Kit		
SIZE	DOCUMENT NO.	REV
B		1.0
DATE:	Wednesday, July 26, 2023	SH 11 OF 14

Decoupling Capacitors



TITLE		
PolarFire SoC Discovery Kit		
SIZE	DOCUMENT NO.	REV
Custom		1.0
DATE:		SH 12 OF 14
Wednesday, July 26, 2023		

5V DC Supply



TITLE PolarFire SoC Discovery Kit			
SIZE Custom	DOCUMENT NO.		REV 1.0
DATE: Wednesday, July 26, 2023			SH 13 OF 14

