PolarFire DisplayPort Rx Solution with Video Output Application Note

AN4684

Introduction (Ask a Question)

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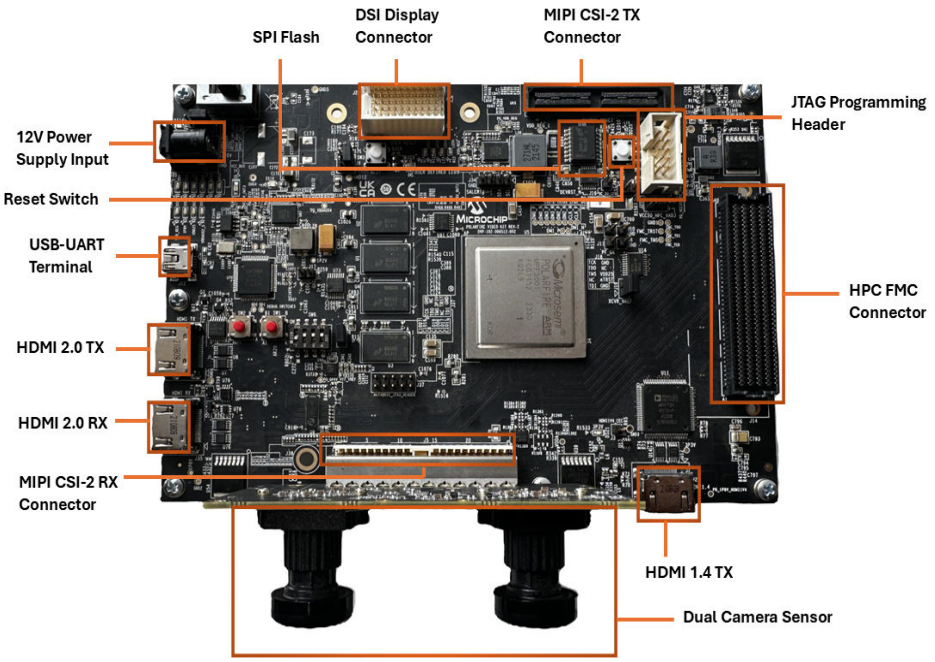
Important: This application note is no longer maintained. The latest documentation, design files and updates are available at: PolarFire FPGA DisplayPort Passthrough Reference Design. This PDF remains available as the final published version and will not receive any further updates.

The DisplayPort Rx IP is designed to receive video signals from DisplayPort Rx sources, making it ideal for PolarFire® FPGA applications. This IP core adheres to the Video Electronics Standards Association (VESA) DisplayPort Standard 1.4 protocol. For detailed information on the VESA protocol, see the official VESA documentation. It supports standard data rates of 1.62 Gbps, 2.7 Gbps, 5.4 Gbps, and 8.1 Gbps for display applications.

This application note demonstrates the usage and running of the imaging and video demo using the PolarFire Video kit, with a Host PC and a DisplayPort Rx (for more information about DisplayPort Receiver IP, see DisplayPort Rx IP User Guide). The demo design showcases a fully integrated solution developed using Microchip's Libero® System-on-Chip (SoC) software, enabling customers to evaluate PolarFire FPGA for smart embedded vision applications and rapidly build prototypes.

The following figure highlights the features of the PolarFire Video kit.

Figure 1. Board Callout



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Summary (Ask a Question)

The following table provides a summary of the DisplayPort Receiver IP characteristics.

Table 1. DisplayPort Receiver IP Characteristics

Core Version	This document applies to DisplayPort Receiver v2.1
Supported Device Families	• PolarFire® SoC • PolarFire
Licensing	The core is license-locked for clear text RTL. It supports the generation of Encrypted RTL for the Verilog version of the core with no license.

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Table of Contents

Introduction....1
Summary....3
1. Demo Requirements....5
2. Demo Prerequisites....6
2.1. Libero License....6
3. Design Description....7
3.1. Hardware Implementation....8
4. Setting Up the Hardware....13
5. Appendix: Running the Tcl Script—Reference Design....16
5.1. Test Setup....16
5.2. Test Setup Prerequisites....16
5.3. Programming the PolarFire Device using FlashPro Express....17
5.4. Running the Demo....18
6. Revision History....20
Microchip FPGA Support....21
Microchip Information....22
Trademarks....22
Legal Notice....22
Microchip Devices Code Protection Feature....22

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1. Demo Requirements (Ask a Question)

The following table lists the hardware and software required to run the demo.

Table 1-1. Demo Requirements

Requirement	Description
Hardware	
PolarFire® Video Kit	MPF300-VIDEO-KIT-NS Kit Contents: • PolarFire Video and Imaging board with MPF300T-1FCG1152E Device • HDMI cable • 12V power pack/AC adapter • USB 2.0 A male to mini-B
DisplayPort FMC card	VIDEO-DC-DP
DisplayPort cable	DisplayPort A Male-to-Male cable
HDMI monitor	1920×1080 (60 Hz) resolution
Host PC with USB port	—
Software	
`Program_Debug_vxx.x_win.exe`	This executable file installs FlashPro Express used to program FPGA.

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2. Demo Prerequisites (Ask a Question)

Before you begin, perform the following steps.

- Download the design files from the following link: www.microchip.com/en-us/application-notes/AN4684
- Download and install Libero® SoC Design Suite from Libero SoC Software Downloads.

2.1. Libero License (Ask a Question)

To generate the design, Libero® silver license is required. To get silver license, see www.microchipdirect.com/fpga-software-products.

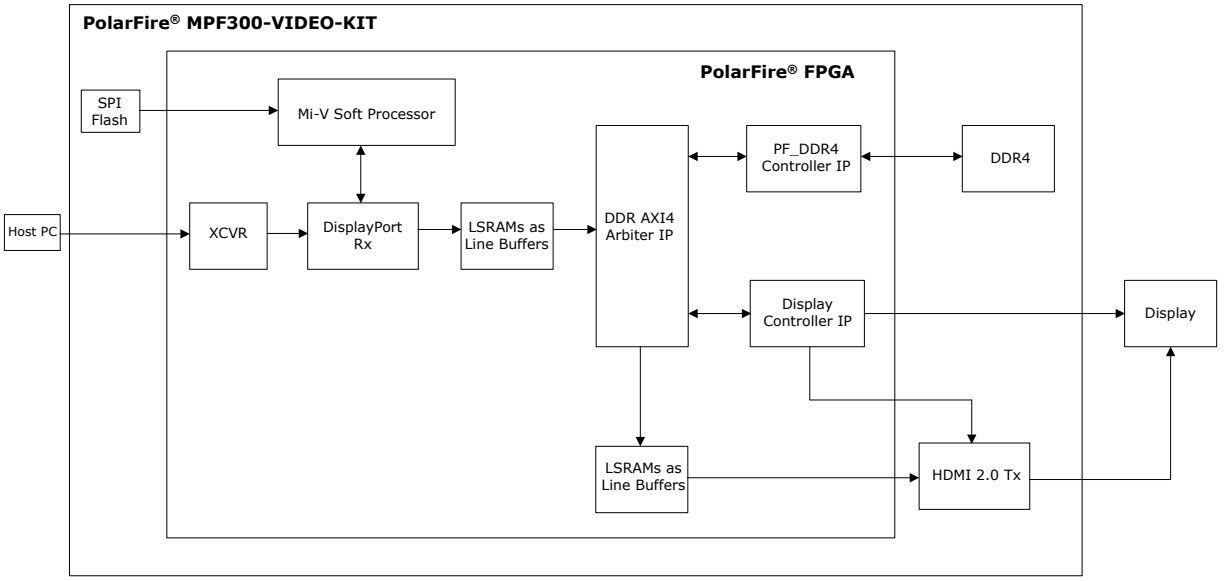
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3. Design Description (Ask a Question)

In this design, The XCVR block manages high-speed serial data reception from the host PC, converting it into parallel data for processing. This parallel data is then received and decoded by the DisplayPort Rx block, which initially stores the frame data in LSRAM line buffers. Due to the significant memory required to store an entire video frame, the frame data is transferred to DDR4 memory. This transfer is efficiently managed using a DDR AXI4 Arbiter IP block and a DDR4 controller. Once stored, the video frame data is read from DDR4 memory and processed by the onboard HDMI 2.0 IP. Finally, the HDMI IP outputs the video to the connected HDMI monitor, ensuring smooth and reliable display of the video content.

The following figure shows a high-level block diagram of the design.

Figure 3-1. Block Diagram

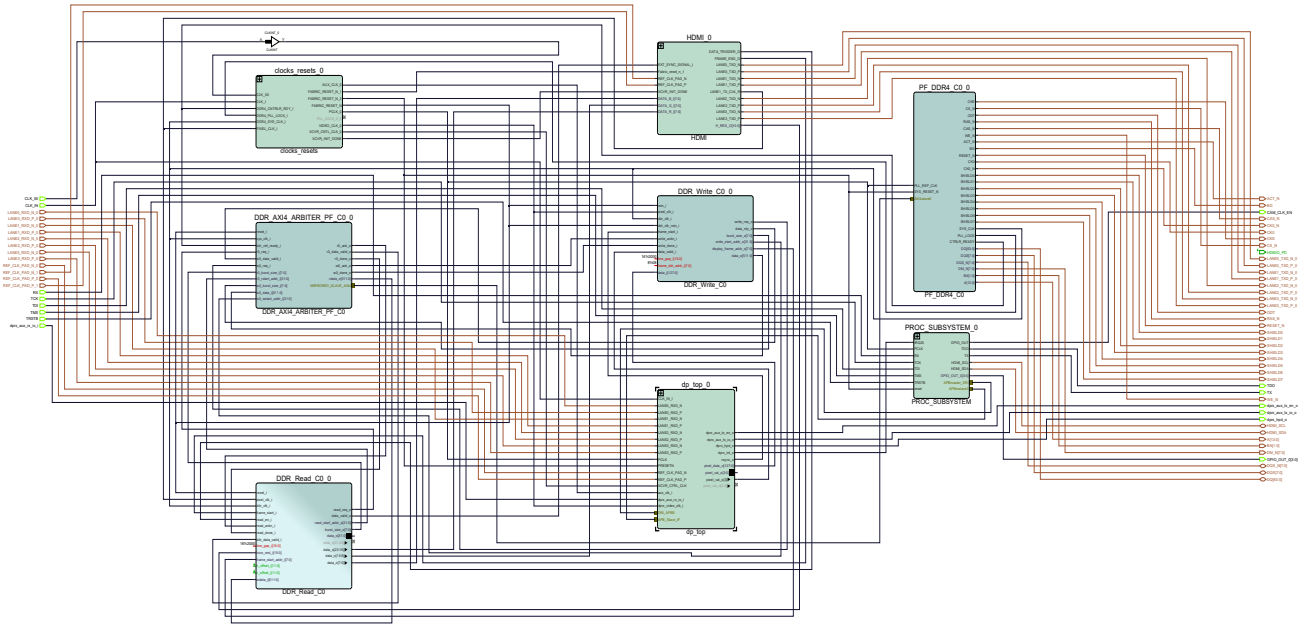


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3.1. Hardware Implementation (Ask a Question)

The following figure shows the Libero SoC implementation of the top-level SmartDesign.

Figure 3-2. High-Level DisplayPort Rx Design



The DisplayPort Rx design includes the following key blocks:

- DisplayPort Rx Configuration
- XCVR Configuration
- Display Controller Configuration
- HDMI TX IP Configuration

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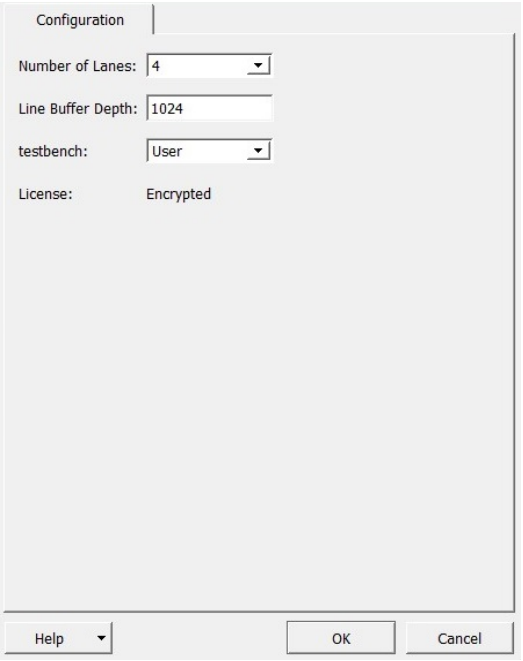
3.1.1. DisplayPort Receiver Configuration (Ask a Question)

The DisplayPort Receiver is configured with the following settings:

- 4 Lanes
- Line Buffer Depth of "1024"

The following figure shows DisplayPort Receiver configuration.

Figure 3-3. DisplayPort Receiver Configuration



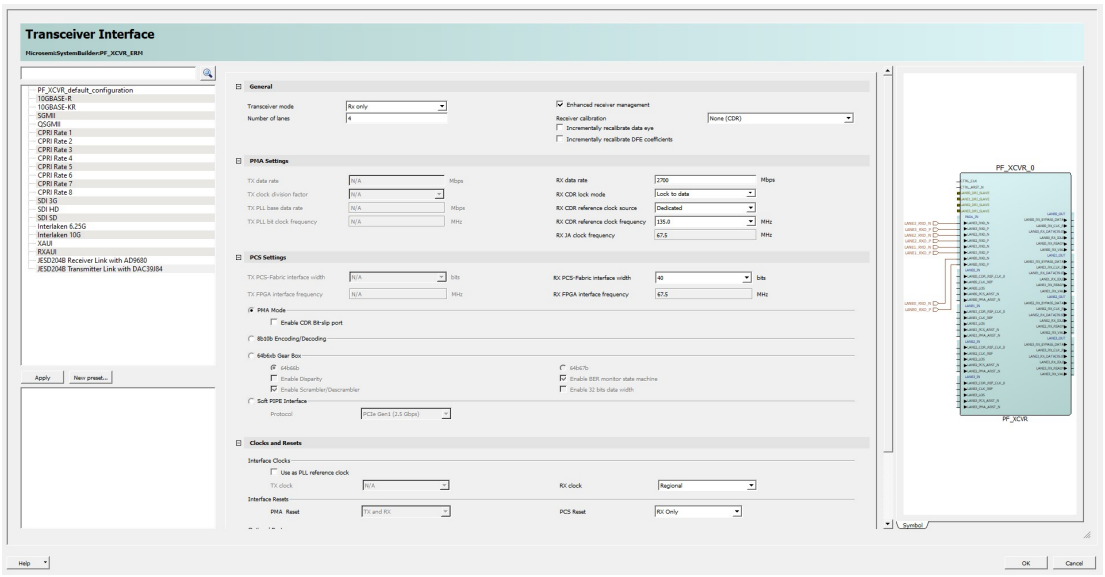
Important: For more information, see DisplayPort Rx IP User Guide.

3.1.2. XCVR Configuration (Ask a Question)

The transceiver configuration for the DisplayPort Rx implementation is shown in the following figure. The transceiver is configured in Rx only mode in a 4 Lane configuration. The Lanes 0,1, 2, and 3 carry DisplayPort Receiver output data.

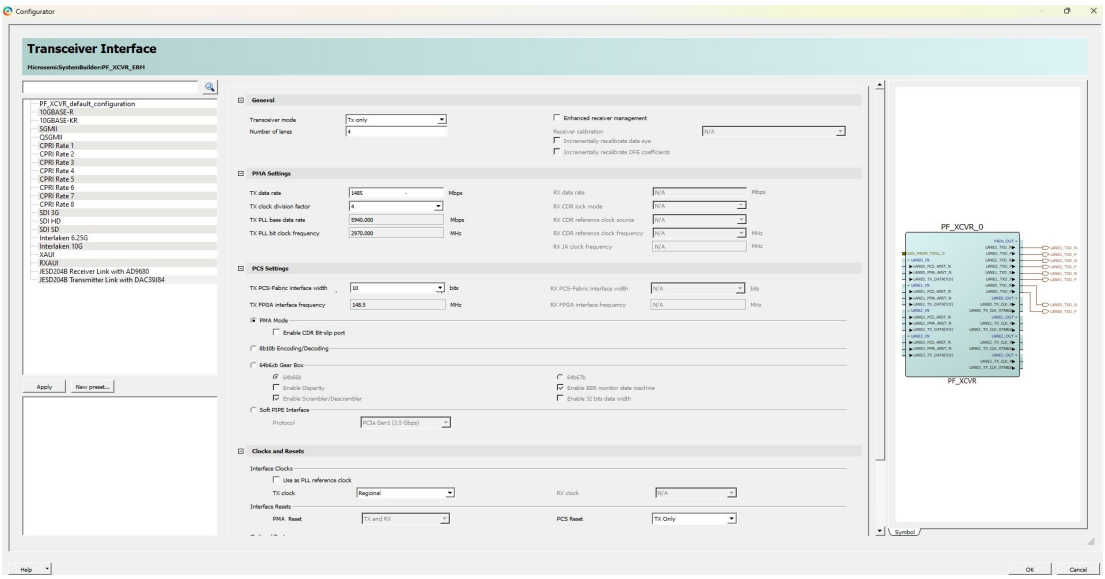
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Figure 3-4. Transceiver Interface Configuration—Instance 1



The transceiver configuration for the HDMI TX implementation is shown in the following figure. The transceiver is configured in Tx only mode in a 4 Lane configuration. The clock signal is carried by LANE0, while Lanes 1, 2, and 3 carry DisplayPort Transmitter output data.

Figure 3-5. Transceiver Interface Configuration—Instance 2



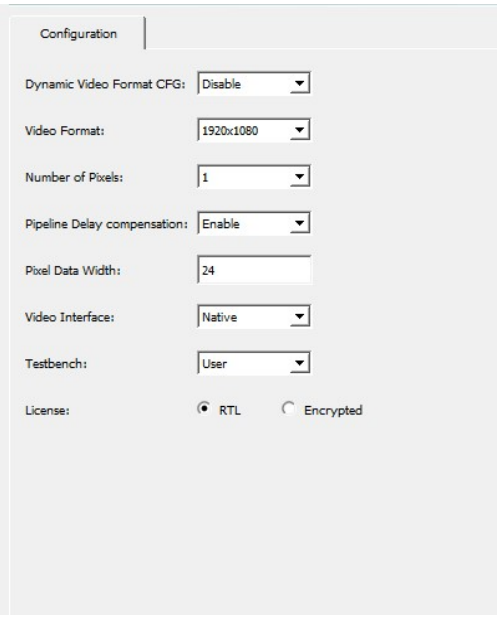
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3.1.3. Display Controller Configuration (Ask a Question)

The VESA standard defines the timing signals required for interfacing with displays such as monitors. The display controller generates synchronization signals based on the VESA standard for various display resolutions. It generates horizontal and vertical sync signals, horizontal and vertical active signals, as well as frame end and data enable signals. The timing parameters for standard resolutions are predefined in the IP, and the desired resolutions are selected from the configuration options.

The following figure shows the display controller configuration, with the resolution set to 1920x1080.

Figure 3-6. Display Controller Configuration



Important: For more information, see Display Controller IP User Guide.

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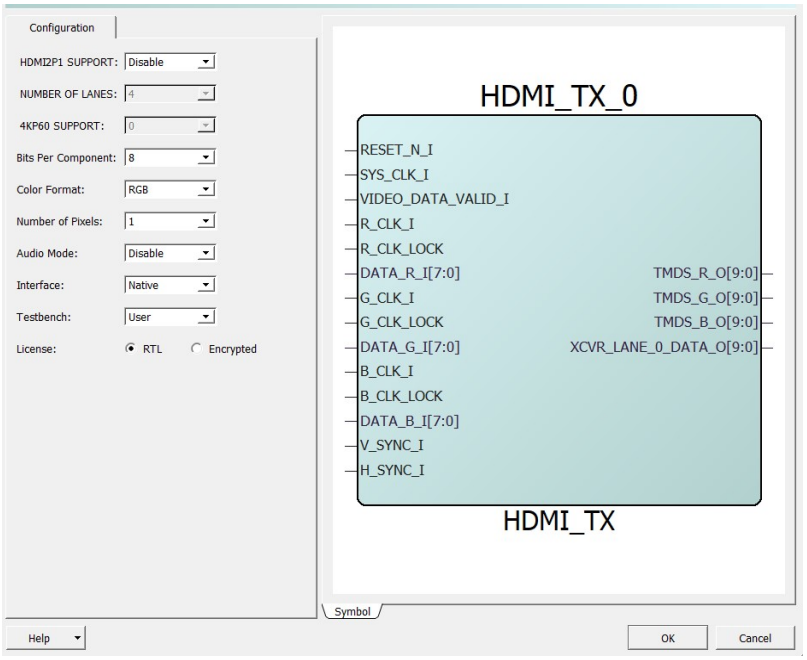
3.1.4. HDMI TX Configuration (Ask a Question)

The HDMI TX IP is implemented based on the VESA standards. In this design, the HDMI TX IP is configured with the following settings:

- Number of Bits Per Component: 8
- Number of Pixels Per Clock: 1
- Color Format: RGB
- Audio Mode: Disabled
- Interface: Native

The following figure shows the HDMI TX IP configuration.

Figure 3-7. HDMI TX IP Configuration



Important: For more information, see HDMI TX IP User Guide.

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4. Setting Up the Hardware (Ask a Question)

Setting up the hardware involves verifying the jumper settings and interfacing the DisplayPort FMC (VIDEO-DC-DP) card with the PolarFire Video kit. For more information, see

The following figures shows the DisplayPort daughter card.

Figure 4-1. DisplayPort Daughter (FMC) Card—Front Side Image

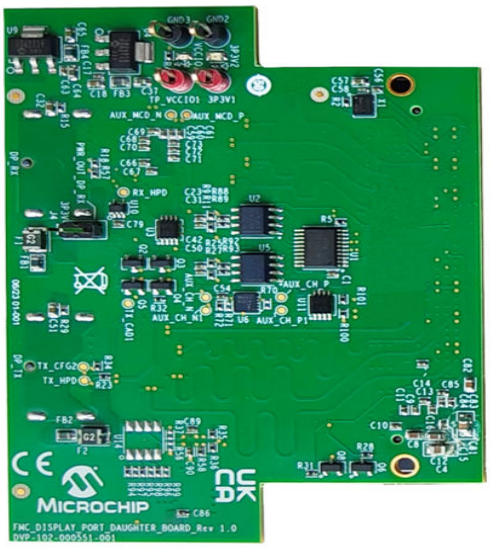
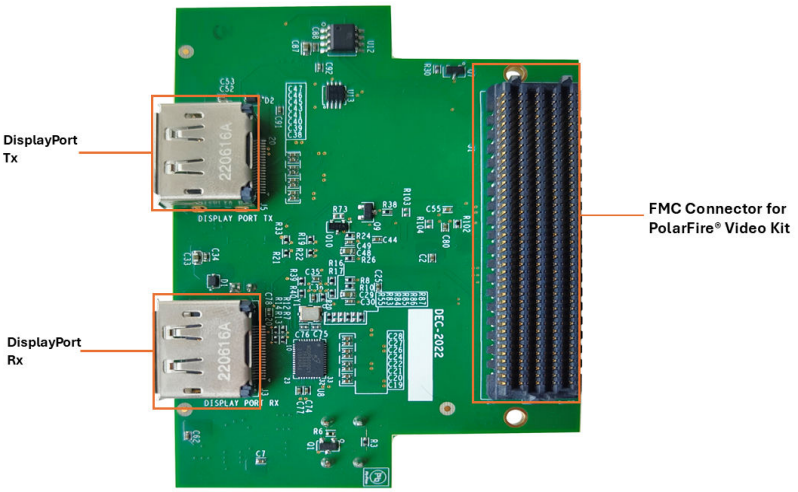


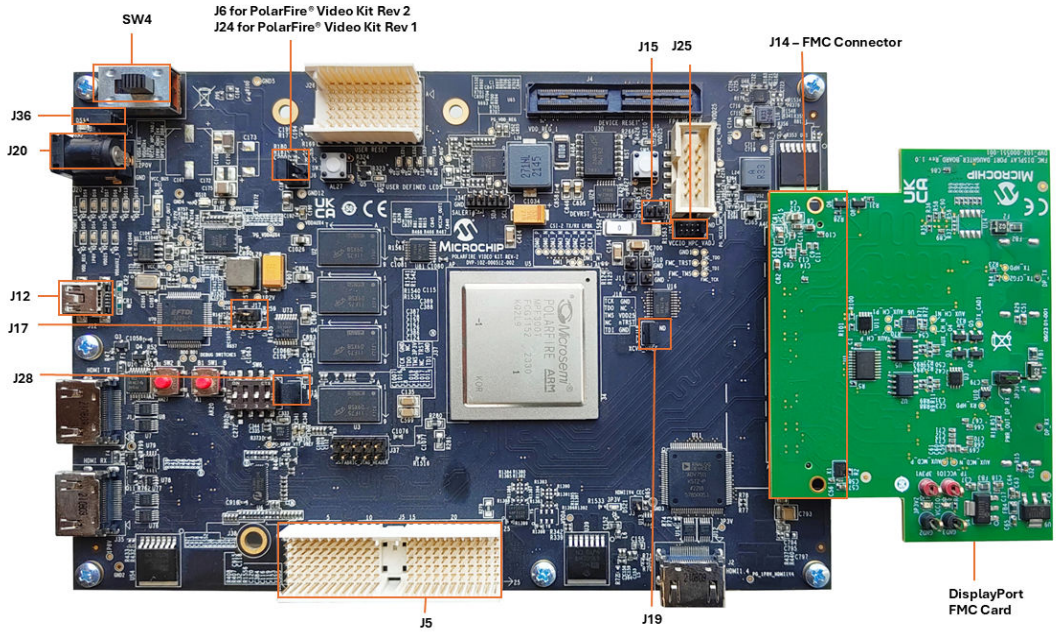
Figure 4-2. DisplayPort Daughter (FMC) Card—Back Side Image



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The following figure shows the hardware setup of the DisplayPort FMC with the PolarFire Video kit.

Figure 4-3. Setting up the Hardware



The following table lists the jumper and switch settings of PolarFire Video kit.

Table 4-1. Jumper and Switch Settings of PolarFire Video kit

Jumper and Switch	Position	Description
J15	Open (default)	SPI Target and Initiator mode selection. By default, select SPI Initiator.
J14	DisplayPort FMC	DisplayPort FMC to be connected
J17	Open	100K PD for TRSTn
J19	Pin 1 and 2 (default)	Default: XCVR_VREF is connected to ground.
J28	Pin 1 and 2 (default)	Default: Programming through the FTDI.
J24 (For Video Kit Rev1) J6 (For Video Kit Rev2)	Pin 1 and 3	Default: VDDAUX4 voltage is set to 2.5V.
J25	Pin 5 and 6	Bank4 voltage which is set to 1.8V.
J36	Pin 1 and 2 (default)	Default: Board power-up through the SW4.
SW4	OFF or ON	Power On or Off slide switch
SW6	OFF	User slide switch. Default position: Off.
J20	12 Volts Input	12V input to the board
J12	USB-UART	USB-UART mini cable

To set up the hardware, perform the following steps:

1. Connect the DisplayPort daughter card to **J14** of the FMC connector on the PolarFire Video kit.
2. Connect the DisplayPort cable to the DisplayPort Rx on the DisplayPort FMC daughter card.
3. Connect the Host PC and the video kit using the USB mini cable through the **J12** on the video kit .
4. Connect the HDMI cable from the monitor to the **J1** (HDMI TX) port on the video kit.
5. Connect the 12V power supply cable to the **J20** onboard DC jack on the video kit.
6. Ensure that the jumper settings on the video kit are correctly configured according to the preceding table.

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7. Power-up the board using the **SW4** slide switch.
8. After the powering up, program the PolarFire Video kit device. For more information, see Programming the PolarFire Device using FlashPro Express section.
9. Once the PolarFire device is programmed, the test pattern generator will start streaming the video data.

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5. Appendix: Running the Tcl Script—Reference Design (Ask a Question)

Tcl scripts are provided in https://www.microchip.com/en-us/application-notes/an4684.

To run Tcl, perform the following steps:

1. Launch the Libero® software.
2. From the menu bar, click **ProjectExecute Script**.
3. In the downloaded directory `mpf_an4684_v20xxpx_df`, locate and select the `script.tcl` file.
4. To execute the selected Tcl script, click **Run**.

Upon successful execution, the Libero project is created within the top directory of `mpf_an4684_v20xxpx_df`. You can verify the process by reviewing the log file, see `mpf_an4684_v20xxpx_df_log`.

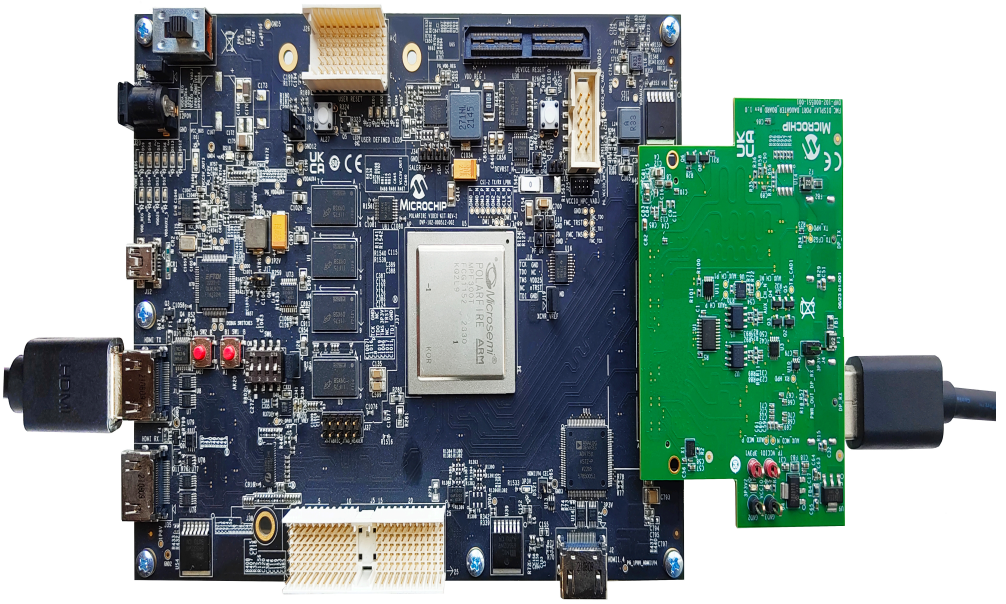
To understand the folder structure and details of the Tcl scripts and commands, see `TCL_Scripts_readme.txt` file and the Tcl Commands Reference Guide. For any queries about running the Tcl script, contact Technical Support.

5.1. Test Setup (Ask a Question)

The PolarFire DisplayPort Receiver design is demonstrated using a PolarFire Video kit, a DisplayPort FMC card, and a DisplayPort cable.

The following figure shows the setting up the hardware.

Figure 5-1. Setting up the Hardware—PolarFire Video Kit with DisplayPort FMC



5.2. Test Setup Prerequisites (Ask a Question)

Before you begin, ensure to download the following files from AN4684: PolarFire DisplayPort Rx Solution with Video Output.

- `mpf_an4684_v20xxpx_jb` - Job file to test on PolarFire® Video kit.

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5.3. Programming the PolarFire Device using FlashPro Express (Ask a Question)

This section describes how to program the PolarFire Video kit with the `.job` file using FlashPro Express. The `.job` file `mpf_an4684_v20xxpx_jb` to test on PolarFire Video kit is provided in the Test Setup Prerequisites section.

To program the PolarFire device, perform the following steps:

1. On the host PC, start the **FlashPro Express** software from its installation directory.
2. To create a new job project on the **Project** menu, click **New** or **New Job Project from FlashPro Express Job**.
3. In the **New Job Project from FlashPro Express Job** dialog box, perform the following steps:
   a. **Programming job file**: Click **Browse** and navigate to the location where the job file is located and select the file. The default location is `mpf_an4686_v20xxpx_jb`
   b. **FlashPro Express job project location**: Select **Browse** and navigate to the location where you want to save the project.
4. Click **OK**. The required programming file is selected and ready to be programmed in the device. The FlashPro Express window appears.
5. Verify that a programmer number appears in the **Programmer** box. If it does not, verify the board connections and click **Refresh/Rescan Programmers**.
6. To program the device, click **RUN**. When the device is programmed successfully, a **RUN PASSED** status is displayed.
7. To close FlashPro Express, click **Project** > **Exit**.
8. Close **FlashPro Express** or in the **Project** tab, click **Exit**.

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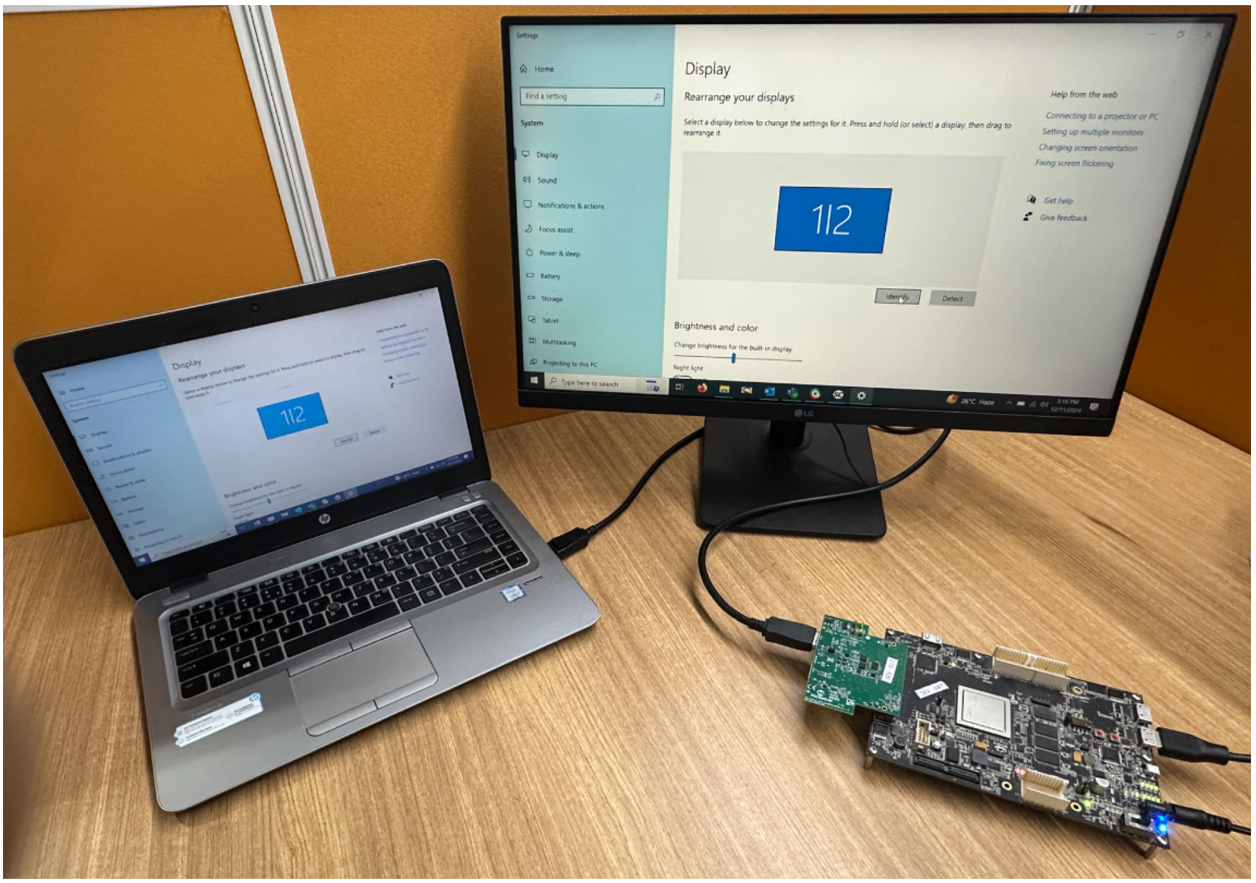
5.4. Running the Demo (Ask a Question)

The demonstration highlights the capability of DisplayPort Rx IP to receive video data from the host PC through the transceiver (XCVR) block. The video frames received are stored in the DDR and then sent to the HDMI 2.0 TX IP. The transfer follows the timing parameters set by the display controller, ensuring seamless video output. The HDMI TX IP displays the video on the full HD monitor, providing a clear and enhanced display.

Once the FPGA board is programmed and powered on, with all necessary connections properly configured, the video data streamed from the host PC is successfully displayed on the HDMI monitor. This setup effectively demonstrates the data flow from DisplayPort Rx to HDMI TX, highlighting the seamless integration of the IP cores and their functionality.

The following figure illustrates the demo setup and its components, including the host PC, FPGA board, and HDMI monitor.

Figure 5-2. HDMI TX Displaying the Laptop Data from DisplayPort Rx



This concludes the demo.

The PolarFire DisplayPort Rx solution has been tested with the following sources, at a 1080 resolution of 60 fps:

- HP® Elite Tower 800 G9 Desktop PC
- HP® EliteBook 840 G4

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Important: For the DisplayPort Rx demonstration, it is not recommended to use a docking station to transmit the DisplayPort signal.

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6. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 6-1. Revision History

Revision	Date	Description
E	10/2026	Added a note about application note and design file migration in Introduction section.
D	07/2025	The following is the list of changes in revision D of the document: • Updated the `.job` filepath and TCL script filepath throughout the document. • Updated the Running the Demo section to add a note and information about the sources used for PolarFire DisplayPort Rx solution testing.
C	12/2024	The following is the list of changes in revision C of the document: • Updated Introduction section. • Updated Hardware Implementation as follows: – Updated Figure 3-2. – Added DisplayPort Receiver Configuration, XCVR Configuration , Display Controller Configuration and HDMI TX Configuration sections. • Added Libero License section. • Updated Figure 4-1, Figure 4-2, and Figure 4-3 in the Setting Up the Hardware section. • Added Appendix: Running the Tcl Script—Reference Design section.
B	07/2023	The following is the list of changes in revision B of the document: • The document is updated for Libero v2023.1. • Added Figure 5-2 to display the data from host PC on the monitor. • Added Appendix: Running the Tcl Script—Reference Design section for running the Tcl scripts.
A	07/2022	Initial Revision

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