Test Systems for High Speed Data Streaming Applications

Breakthrough bandwidth
with PXI Express

Use Case

Test Systems for High Speed Data Streaming Application

Electronic systems, both analog and digital, are processing and managing increasing amounts of information at continually increasing data rates. The information age continues to increase demands on developers of high accuracy and reliability systems and subsystems. A major challenge to researchers and systems developers lies in testing, debugging and servicing systems. Continuous data acquisition of high speed and high resolution signals, both analog and digital, is widely sought after for application in popular analytical techniques such as video analytics. Capturing a large continuous and coherent information/data stream is vital in establishing reliability and accuracy, and critical in identifying design flaws and problems thereby reducing development costs and time-to-market, while reducing field recalls and costly redesign of deployed systems.

Applications requiring high accuracy and long sampling times, include spectral monitoring, signal intelligence, LIDAR testing, optical fiber testing, radar and satellite signal acquisition, and software defined radios present unique engineering challenges to meet demands for high throughput. ADLINK shares our specific expertise in devising systems that capture high-bandwidth applications flawlessly, satisfying considerations including onboard digitizer/waveform generation memory, bus interface, PCIe routing in PXI Express chassis, system memory and OS, and storage devices.

Customers gain the benefits of a flexible general purpose PXI Express System, maximizing throughput and post-signal processing.

Introduction

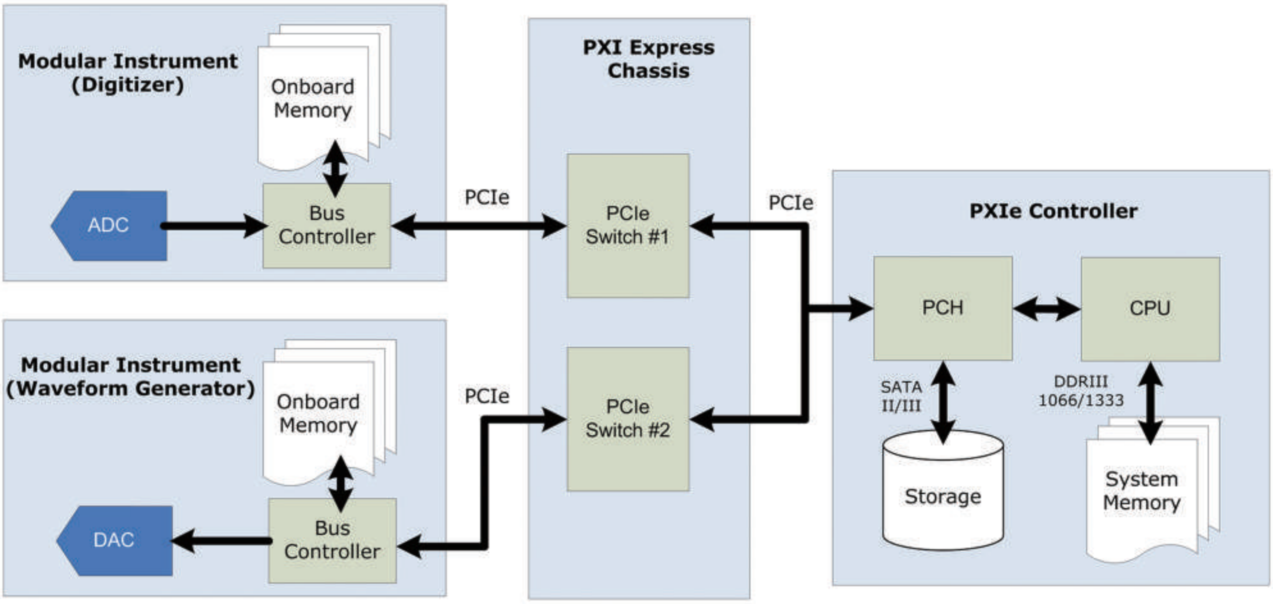
Communication interfaces employed in conventional standalone instrument are normally GPIB, RS-232, or LAN ports. While easy to use, they can be ineffective when transferring excessive amounts of high speed data. Data length for these instruments is limited by internal memory size, especially when data is to be continuously acquired. Popularly used high end instrumentation such as oscilloscopes, waveform generators, and logic analyzers, utilize internal x86 computers to process massive amounts of data. Synchronization of such instruments, especially in combination, is difficult and provided acquisition features and processing functions are limited.

Since initial release of the specification in 1998, PXI platforms and modules have found placement in a wide variety of applications, including military, electronics manufacturing, and research testing. Based on the high speed parallel PCI bus in the first release of the PXI specification, recent evolutions have resulted in the PCI Express bus, featuring low latency, high bandwidth and peer-to-peer communication, and unique trigger and timing synchronization capabilities, making PXI platforms and PXI module data streaming faster than ever.

When deployed in a test system for high-speed streaming, PXI Express leverages high parallel bus speed, delivering low latency, high bandwidth and peer-to-peer communication features, and unique trigger and timing synchronization. Data streaming continuously transports data from/to instrument to/ from host system continuously, either streaming to/ from memory or to/from storage. Configuration and evaluation of streaming systems according to different requirements will be discussed.

Data Streaming Architecture and Considerations

Data flow in a PXI Express Platform is shown. Using a high speed digitizer as an example, data generated by ADC is moved to onboard memory for temporary storage, after which it is transferred to system memory on the host controller via the PCI Express interface for post-processing. If the final destination is a storage disk, data is moved to disk without any processing. On the PXIe backplane, PCIe switches enable system interconnection and I/O expansion. Since different PXIe chassis may have different slot types, PCIe switch routing is commensurately different and may impact data throughput for each slot. In modular instruments like arbitrary waveform generators, data flow is in the opposite direction. Each stage of the data streaming flow and respective effects on bandwidth are discussed.

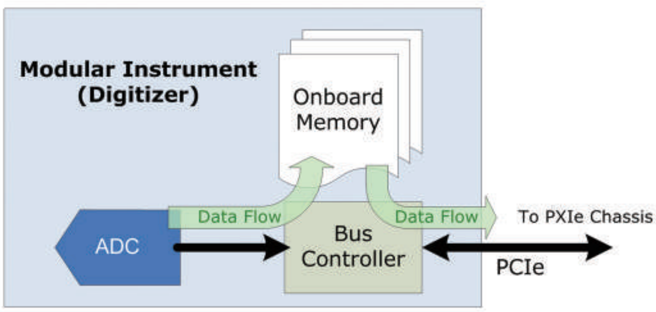


* Figure 1 – Simplified block diagram of data flow in a PXI Express platform with modular instruments

Onboard Memory of Modular Instruments

As recently as 10 years ago, high speed PCI digitizers required large onboard memory to store data from high speed ADCs, since the PCI bus provides only 132 MB/sec throughput, but often only 80MB/sec can be achieved. PCI Bus Bandwidth is often inadequate for 8-bit 1 GS/s or 14-bit 200 MS/s digitizers. To increase recording time, 512 MB, 1 GB, 4 GB, or more of memory was required. Currently, although the high speed PCIe bus provides faster data throughput, it is still preferable to have large scale (100 MB+) memory onboard to provide adequate data buffering when the CPU/DMA controller is engaged. For example, a 1-CH 8-bit 500 MS/s digitizer with 512 MB memory can record up to 1 sec without transferring back to system memory, and with 2 GB, up to 4 sec.

Another key factor when choosing a digitizer for data streaming applications is onboard memory controller bandwidth. As the bridge between ADC and system memory, the memory controller requires twice the bandwidth of the data throughput, since it must not only move data from ADC to onboard memory, but also simultaneously manage data from onboard memory to the PCIe interface. If memory controller bandwidth is less than twice the data throughput, data queues in onboard memory and ultimately overflows, resulting in information loss



* Figure 2 – Block diagram of data flow within a digitizer

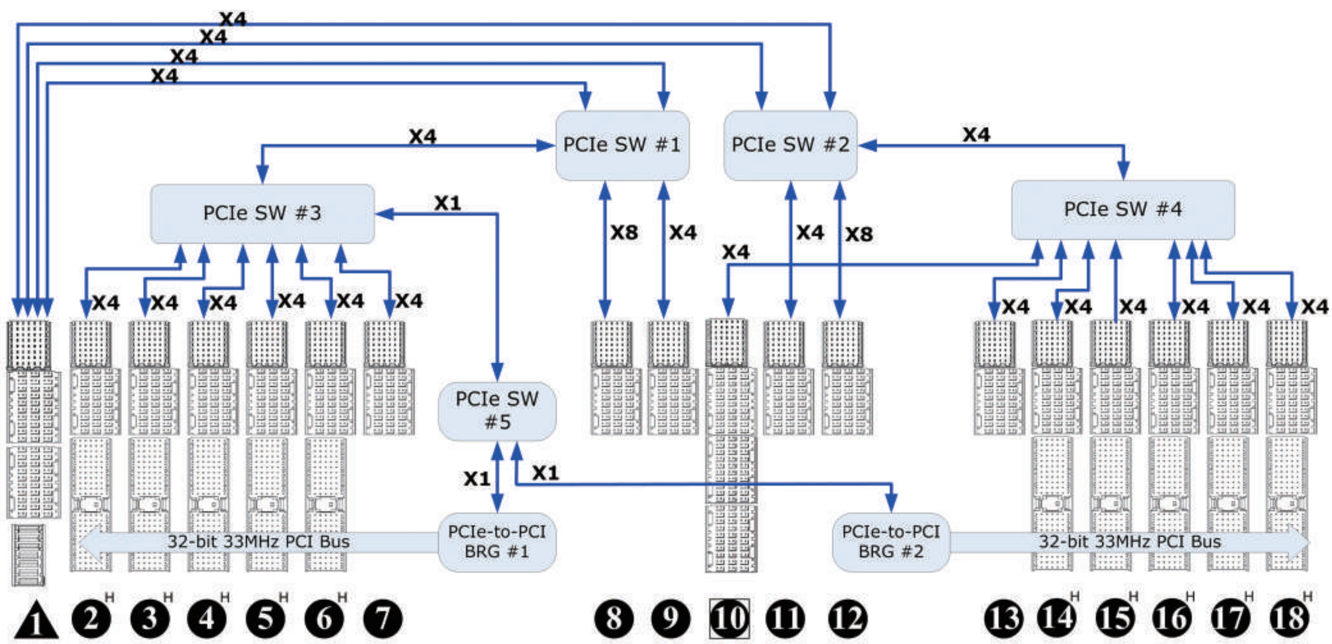
Modular Instrumentation Bus Interface

As is shown, PCI Express provides maximizes advantages as a modular instrumentation bus interface. Unlike the PCI bus, which, being parallel, offers only 132 MB/s (32-bit 33 MHz) to all devices on the same bus, PCI Express' point-to-point serial connection delivers 250 MB/s per link, per direction. To increase total bandwidth, multiple links can be grouped into X1, X4, X8 and X16 lanes. In 2003, PCI-SIG introduced PCIe 1.0a with a per-lane data rate of 250 MB/s. In 2007, PCI-SIG announced the PCIe 2.0 standard, doubling throughput to 500 MB/s. In November 2010, PCIe 3.0 was released, with upgraded encoding and enhanced signaling and data integrity, doubling the PCIe 2.0 bandwidth. For high speed data streaming applications, modular instrumentation equipped with PCI Express interface is required. For low speed and low cost data streaming applications (< 80 MB/s), while the PCI bus may be sufficient, care should be taken, since, as a parallel bus, it shares bandwidth with other devices.

	PCIe Gen 1	PCIe Gen 2	PCIe Gen 3
Lane	Bandwidth, per direction & lane	Bandwidth, per direction & lane	Bandwidth, per direction & lane
X 1	250 MB/s	500 MB/s	1 GB/s
X 4	1 GB/s	2 GB/s	4 GB/s
X 16	4 GB/s	8 GB/s	16 GB/s

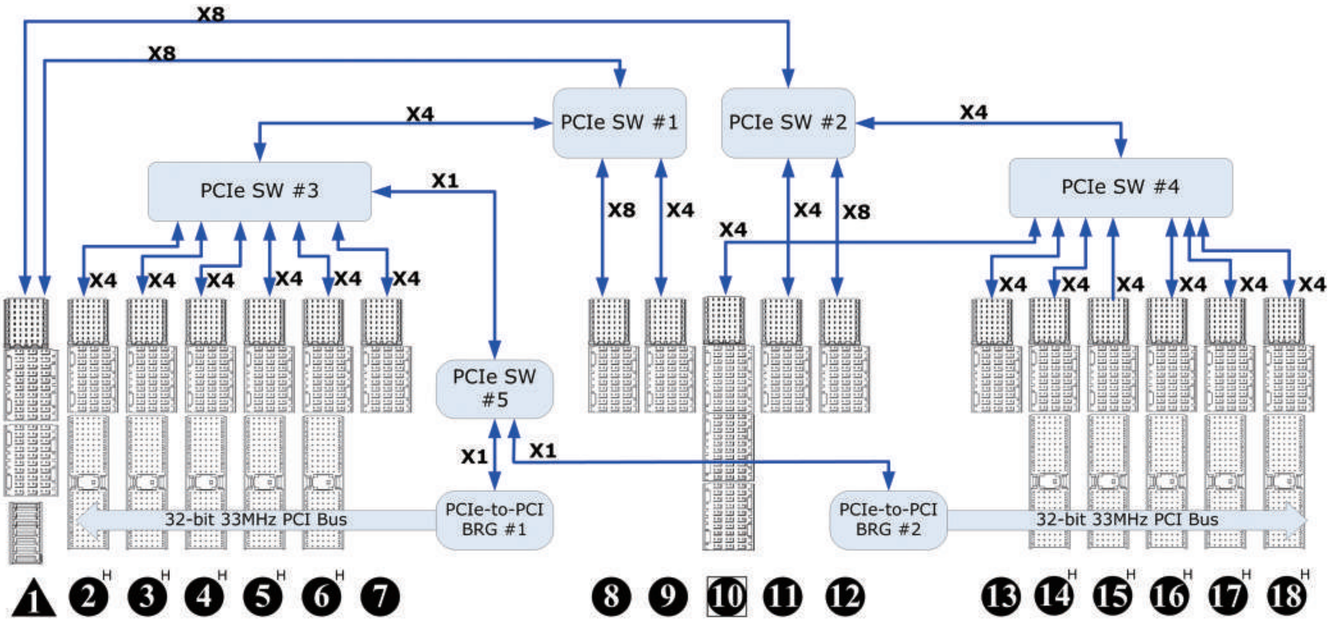
PCIe Routing in PXIe Chassis

To increase peripheral slot count and configuration flexibility, the PXI Express chassis offers both 4-Link and 2-Link configuration routing schemes for the system slot. 4 lanes per link are provided in 4-Link configuration, and in 2-Link configuration, one link can be up to eight lanes and the other up to 16. For maximum throughput, the specific routing scheme of the PXI Express chassis must be considered. Using the ADLINK PXES-2780 as an example, an 18-slot PXI Express chassis, one system slot, one system timing slot, six PCIe peripheral slots, and ten hybrid peripheral slots are provided. Configuration as 4-Link by 4 lanes in the system slot delivers maximum balance throughput for each slot. Based on PXIe Gen 2 signaling technology, the chassis provides 8 GB/s system bandwidth and up to 4 GB/s bandwidth in slots 8 & 12 or 2 GB/s bandwidth for the remaining PXIe peripheral slots. The 4-Link PCIe routing scheme is as shown.



* Figure 3 – Example of 4-Link configuration of ADLINK PXES-2780

However, with the PCIe X8 interface, 2-Link configuration is preferable for higher throughput. The ADLINK PXES-2780 can be configured as 2-Link by 8 by software interface, with PCIe routing topology as follows. In this configuration, slots 8 and 12 can provide X8 dedicated throughput.



* Figure 4 – Example of 2-Link configuration of ADLINK PXES-2780

Familiarity with PXIe chassis topology can enable modular instrumentation deployment for optimum throughput.

System Memory and Operating System

Large scale memory in the host controller benefits data streaming, extending total recording time. However, memory limitations vary with operating system. For general 32-bit OS, memory address space tops out at 4 GB, while 64-bit OS can accommodate as much as 512 GB or even 1TB.

Storage

To write data to storage, device selection is critical. Hard disk drives' (HDD) one or more rapidly rotating discs with magnetic heads arranged on a moving actuator arm read and write data to disc surfaces. Read/write throughput is limited, however, by movement of the magnetic heads. To increase data throughput, several HDDs are often combined into one large virtual device, referred to as RAID (redundant array of independent disks) systems. Recently less expensive Solid-State Disks (SSD) are increasingly popular, with no magnetic head activity delivering significantly improved read/write performance over HDDs. For optimal performance in data streaming, SSDs provide a clear storage advantage.

Application Example 1: Streaming Data to Memory

High speed data recorder for material structure testing

Solution Requirement

Vibration of material must be simultaneously monitored by multiple sensors, at rates from 1 MS/s (megasamples per second) to 50 MS/s. Data can only be stored in system memory for post-processing rather than streamed to disk, and a minimum of 5-10 seconds is to be recorded for each channel, but the time may vary. Limitation at different sample rates and the memory size required to determine location of the bottleneck are determined as follows.

Diagnostic

The following system configuration demonstrates consideration of the high-speed data streaming system.

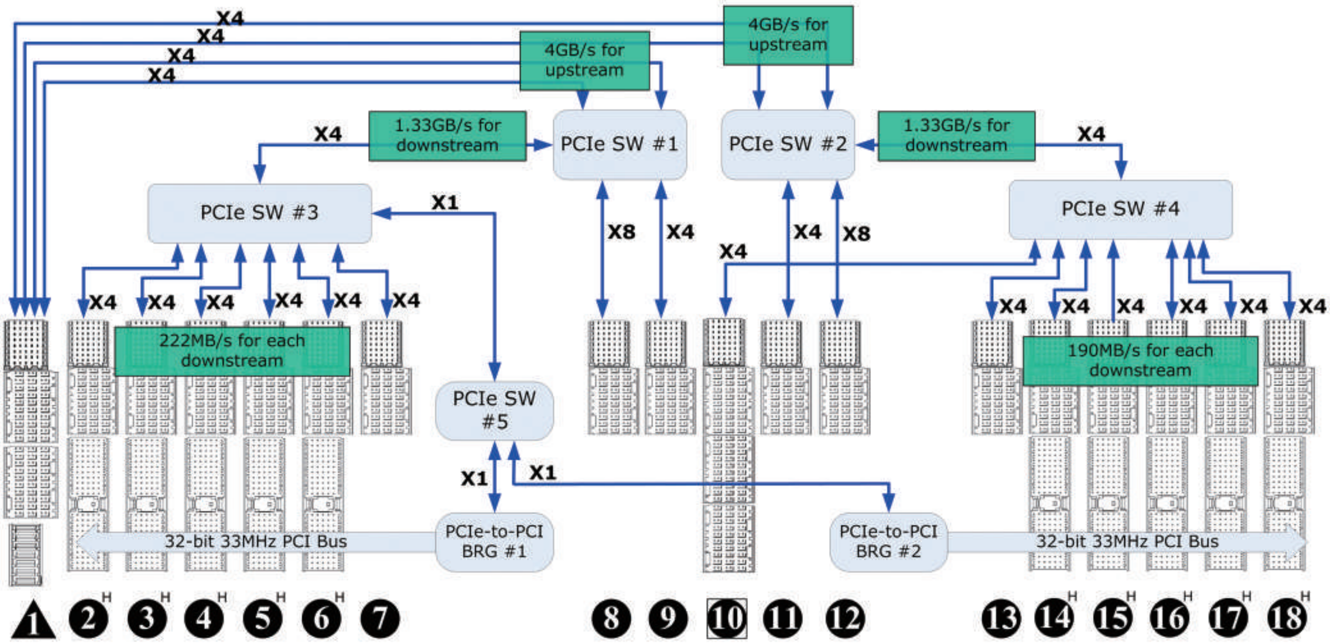
- **PXIe Chassis: ADLINK PXES-2780, the 18-slot PXIe chassis**
- **Digitizer: ADLINK PXIe-9848, 100MS/s 8-CH 14-bit PXIe Digitizer**

Evaluation of memory required vs. sampling rate with a single digitizer in the PXIe system is shown

Single PXIe-9848 in PXIe Chassis				System Memory Required for Specified Time in MB				
SR MS/ s	Data Width, Byte	No of CH	Data Rate, MB/s	1/2 sec	1 sec	2 sec	5 sec	10 sec
5	2	8	80	40	80	160	400	800
10	2	8	160	80	160	320	800	1600
20	2	8	320	160	320	640	1600	3200
50	2	8	800	400	800	1600	4000	8000
100	2	8	1600	800	1600	3200	8000	16000

With a single PXIe-9848 sampling at 100 MS/s for 8-CH, total data throughput is 1.6 GB/s. Since the PXIe-9848 interface is Gen One PCIe X4, however, data rate cannot exceed 1 GB/s if data is to be streamed from digitizer to system memory directly and continuously. If the sampling rate is lowered to 50 MS/s, the PXIe-9848 can deliver 800 MB/s data rate. The PCIe interconnection in the PXIe chassis, with Gen 2 PCIe X4 in each slot, is also capable of delivering 800 MB/s. A further limitation is the host system memory size, whereby if up to 10 sec is to be recorded under 50 MS/s, required system memory is 8 GB. Consequently, limitation of the specific PXI controller in use must be determined. If the controller cannot support more than 8GB memory, recording time must shortened or sampling rate lowered. Installation of multiple digitizers in the PXIe system is next considered. In an example, if PXIe-9848 digitizers are installed into all peripheral slots (17 cards) to maximize recording channels, not only must the system throughput of the PXIe controller but also the PCIe routing in the PXIe chassis be considered.

Observing the PCIe routing in the PXES-2780 PXIe chassis, it is shown that PCIe switch #1 has two X4 Link in the upstream port and three X4 Link in the downstream ports. Thus, each downstream port can share approximately 1.33 GB/s (4 GB/s / 3 ports) bandwidth from its upstream ports. The same calculation can be applied to PCIe switch #2. For PCIe switches #3 and 4, each respective downstream port can share about 222 MB/s (1.33 GB / 6 ports) and 190 MB/s (1.33GB/s / 7 ports), respectively. Accordingly, if digitizers are to sample at the same rate, the bandwidth bottleneck occurs at modules plugged into slots 10 and 13 to 18.



* Figure 5 – Block diagram of PCIe x4 link configuration and throughput estimation

Based on the backplane limitations of slots 10, 13-18, system memory required versus digitizer sampling rate can be evaluated as follows.

Configuration of single PXIe-9848 module					System memory (MB) required for specified time with 17 PXIe-9848 modules deployed in PXIe platform				
SR MS/ s	Data Width, Byte	No of CH	Data Rate, MB/s	Slot BW Bottle-neck, MB/s	1/2 sec	1 sec	2 sec	5 sec	10 sec
5	2	8	80	190	680	1,360	2,720	6,800	13,600
8.33	2	8	133.28	190	1,133	2,266	4,532	11,329	22,658
10	2	8	160	190	1,360	2,720	5,440	13,600	27,200

Accordingly, 6.8 GB system memory is required for 17 PXIe-9848 modules to stream data at 5 MS/s for each channel. If sampling rate is increased to 10 MS/s, recording time for 17 modules is reduced to 2 seconds (5.44 GB memory required). With data amounts of this size, digitizers which can support onboard storage memory for extra buffering will be able to extend acquisition for required durations.

Application Example 2: Streaming Data to Disk

High speed photo-diode signals in laser monitoring

Solution Requirement

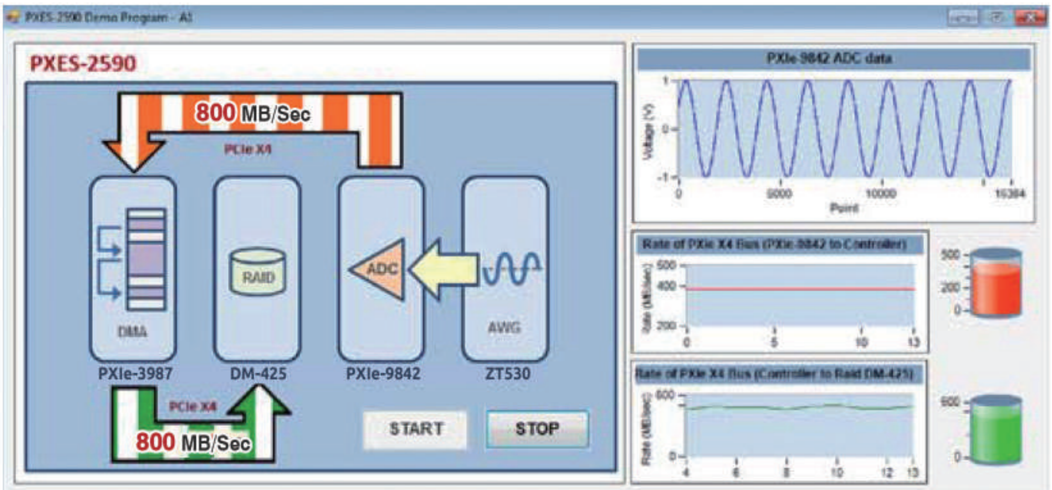
Acquisition of high speed signals is desired from a photo-diode in a laser monitoring application used with a portable system. Only one channel of signal acquisition is required, but with sampling rates up to 200 MS/s.

Solution

Using a 200 MS/s digitizer as an example with the ADLINK PXIe-9852 and the PXIe chassis PXES-2590 deployed, total data throughput can reach 800MB/s (200MS/s x 2 Byte x 2 CH). Stream of this high data rate to PXIe controller storage is difficult even with SSD, since the PXIe controller conventionally supports only a single SATA II or SATA III interface. Up to 400 MB/s throughput to storage requires RAID storage. The RAID module discussed earlier provides 4 SATA III SSDs with PCI Express interface.

Configuration

- **PXIe Controller: ADLINK PXIe-3987, 3U PXI Intel Core i7-7820EQ processor with 16GB memory & 240GB SSD**
- **PXIe Chassis: ADLINK PXES-2590, 9-slot PXIe chassis**
- **Digitizer: ADLINK PXIe-9852, 200MS/s 14 bit 2 CH high speed digitizer**
- **Storage: Conduant DM-425**



* Figure 6 – PXIe-9852 stream-to-disk program display

Summary

Test system configuration for data streaming applications via PXIe platform requires consideration of not only modular instrumentation itself, but also platform system throughput. Here, configuration and limitations incurred when configuring the PXIe platform for streaming systems are examined and discussed, with two exemplary systems presented.

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