APPLICATION NOTE

PMBus Commands and Advanced Control Functions for MLX/SLX Series Modules

Applicable to MLX160, MLX120, MLX080, MLX040, SLX 160 and SLX040

The MLX/SLX series of Digital DLynxIII™ power module provide basic and advanced PMBus commands to adjust the performance of the modules and provide access to advanced features which can be used to configure modules for atypical applications. These modules use an advanced PID based adjustable digital control loop which ensures loop stability, provides fast transient response and reduces amount of required output capacitance. This document also explain the settings necessary to configure satellite based phase modules either in parallel to form a high current common rail or a second stand-alone bus.

Digital Power Insight (DPI)

ABB offers a software tool that helps users evaluate and simulate the PMBus performance of the MLX series modules without the need to write software. The software can be downloaded for free at abbpowerconversion.com.

An ABB USB to I2C adapter and associated cable set are required for proper functioning of the software suite. For first time users, we recommend using the ABB's DPI Evaluation Kit, which can be purchase from any of the leading distributors. Please ensure the ABB USB to I2C adapter being used/ purchased is Version 2.2 or higher.

Technical Specifications

Detailed Description of Supported PMBus Commands

Each command will have the following basic information.

Command Name [Code]

Definition

Data format

Factory default

Additional information may be provided if necessary.

PAGE [0x00]

Definition: Allows, control, monitoring of each loop/output of the Master + Satellite module through a single PMBus address. Each output is assigned a specific page value. Once the Page Register is set for a particular output, all subsequent commands are directed to the set output. Page register setting has to be changed to be able to communicate with the other output.

Format	**8-bit unsigned (bit field)**							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	L2	L1
Default Value	X	X	X	X	X	X	0	0

Page Command Setting options

L2	**L1**	**Results**
0	0	All commands address Output 1(Loop1)
0	1	All commands address Output 2 (Loop 2)
		All commands address both Outputs (Loop 1 and 2) – Write commands only—Setting Below

Both Outputs	1	1	1	1	1	1	1	1

OPERATION [0x01]

Definition: Changes output state of the module, sets V_{OUT} margins and margin's fault response.

Setting options

Format	**8-bit unsigned (bit field)**							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Immediate OFF (No sequencing)	0	0	X	X	X	X	X	X
Soft OFF(With Sequencing)	0	1	X	X	X	X	X	X
ON without VOUT_COMMAND (DEFAULT)	1	0	0	0	X	X	0	X
Margin Low (Ignore Fault)	1	0	0	1	0	1	X	X
Margin Low (Act Fault)	1	0	0	1	1	0	X	X
Margin High (Ignore Fault)	1	0	1	0	0	1	X	X
Margin High (Act Fault)	1	0	1	0	1	0	X	X

Attempting to set the command to any setting no listed in Table above will result in an invalid data CML fault. (STATUS_BYTE, STATUS_CML, SMBALERT# could be affected)

Technical Specifications (continued)

ON_OFF_CONFIG [0x02]

Definition: Configures the interpretation and coordination of the OPERATION command and the ON/OFF pin state.

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not used			pu	cmd	cpr	pol	cpa
Default Value	0	0	0	1	1	1	0	0

Bit 4 Coordinates the response to the OPERATION command and ON/OFF pin state

0 Module is always on

1 Module does not power up until commanded by the ON/OFF pin and the OPERATION command.

Bit 3 Set the response to the OPERATION command

0 Ignores on/off portion of the OPERATION command

1 Responds to on/off portion of the OPERATION command according to the setting of Bit 2.

Bit 2 Set the response to the ON/OFF pin state

0 Ignores ON/OFF pin (on/off controlled by the OPERATION command only)

1 Requires the ON/OFF pin to be asserted to start the module. May also require OPERATION command depending on Bit 4.

Bit 1 ON/OFF pin polarity

0 Active Low

1 Active high

Bit 0 ON/OFF pin action when turning the module off

0 Use the configured ramp-down settings (“soft-off”)

1 Turn off immediately

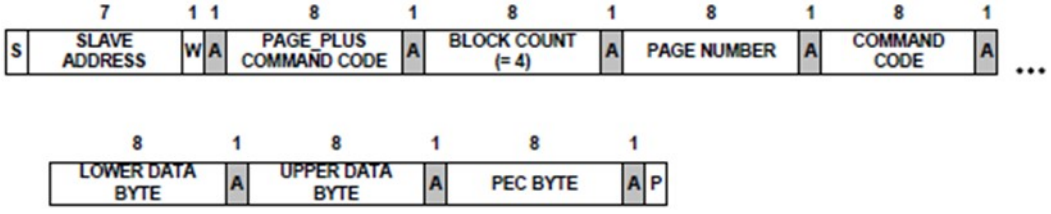
Attempting to set the command to any setting no listed in Table above will result in an invalid data CML fault. (STATUS_BYTE, STATUS_CML, SMBALERT# could be affected)

CLEAR_FAULTS [0x03]

Definition: Clear any fault bits that may have been set and releases the SMBALERT# signal if it has been asserted. If the fault condition still exists, the fault bits will be reasserted immediately. This command will not restart the module if it has shut down in response to a fault.

PAGE_PLUS_WRITE [0x05]

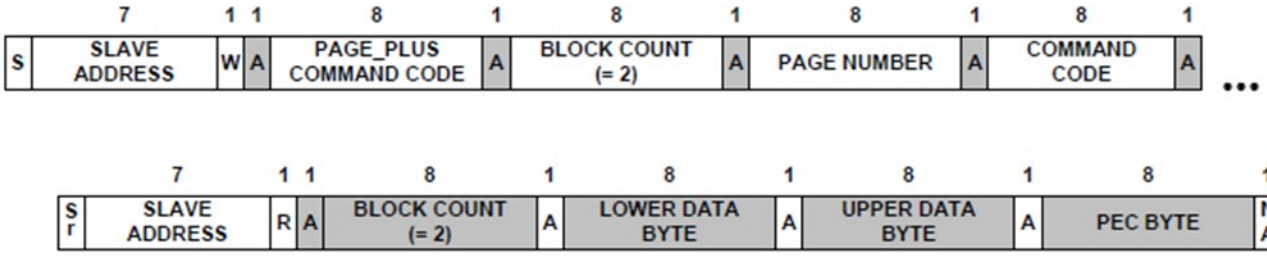
Definition: This command is used to set a page within a device and send the command and data for the command in one packet using the Block Write protocol. An example of this command that has 2 data bytes to be written and a PEC byte is as shown



Technical Specifications (continued)

PAGE_PLUS_READ [0x06]

Definition: This command is used to set a page within a device and send the command and read the data returned by the command in one packet using the Block Read protocol. An example of this command that has 2 data bytes and a PEC byte is as shown



WRITE_PROTECT [0x10]

Definition: This command is used to prevent accidental changes to the PMBus settings. Command still have their settings read when WRITE protected. This command does not protect against writing controller registers via the I^2C bus. To prevent writing controller registers through I^2C bus, the I^2C bus can be disabled by setting the I^2C address to 0

Setting options

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Disables all writes except to the WRITE_PROTECT command	1	0	0	0	0	0	0	0
Disables all writes except to the WRITE_PROTECT, and OPERATION commands	0	1	0	0	0	0	0	0
Disables all writes except to the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG and VOUT_COMMAND commands	0	0	1	0	0	0	0	0
ENABLE ALL WRITES (Default)	0	0	0	0	0	0	0	0

RESTORE_DEFAULT_ALL [0x12]

Definition: Restores the settings from the nonvolatile USER store memory into operating memory. Function of this command is identical to RESTORE_USER_ALL. The module will be unresponsive for 40µs while storing values. This command should not be used while module is delivering power

STORE_USER_ALL [0x15] - Can Use only 24 times.

Definition: Stores all current values from the operating memory into nonvolatile USER store memory. The duration depends on the number of "1" bits in the registers as it takes approximately 51µs per "1" bit.

RESTORE_USER_ALL [0x16]

Definition: Restores the settings from the nonvolatile USER store memory into operating memory. Function of this command is identical to RESTORE_DEFAULT_ALL. The module will be unresponsive for 50µs while storing values. This command should not be used while module is delivering power

Technical Specifications (continued)

CAPABILITY [0x19]

Definition: Reports some of module's communications capabilities and limits.

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	PEC	SPD		ALRT	Numeric / AVSBUS		Not used	
Default Value	1	0	1	1	0	0	0	0

Bit 7 Packet error checking

1 Supported

Bits 6:5 Maximum bus speed

01 400kHz

11 Not used

Bit 4 SMBALLERT#

1 Module supports SMBus alert response protocol

Bit 3 Numeric format

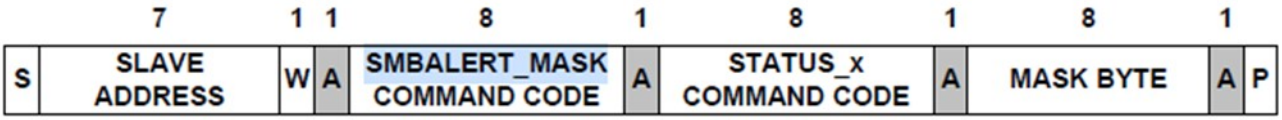
0 Numeric data in LINEAR or DIRECT format

Bit 2 AVSBus supported

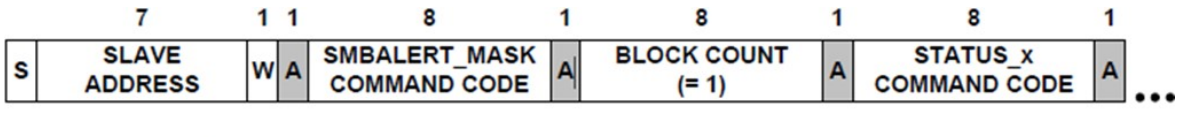
0 AVSBus is not supported

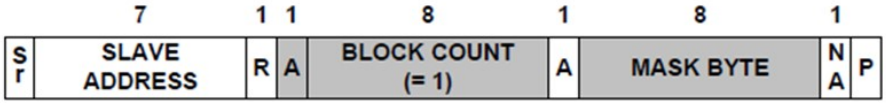
SMBALERT_MASK [0x1B]

Definition: The SMBALERT_MASK is used to mask warning or fault conditions from asserting the SMBALERT signal. For example, a VOUT_OV_WARN_LIMIT warning would set bit 6 in the STATUS_VOUT register. If we want to mask the SMBALERT when this occurs we would use the SMBALERT_MASK to set the command cod for STATUS_VOUT (7A) and the bit for OV warn (40h). In this case, an overvoltage warning condition on VOUT would not assert SMBALERT. However OV fault would do it. If both the fault and warning on VOUT needs to be masked, we would set bits 7 and 6 (C0h) in the SMBALERT_MASK of STATUS_VOUT. The STATUS_X command is sent in the low byte and the bits to be masked sent with the high byte



Command for retrieving the SMBALERT_MASK Setting for a Given Status Register





Technical Specifications (continued)

VOUT_MODE [0x20]

Definition: Reports the V_{OUT} mode and provides the exponent used in calculation of several V_{OUT} settings.

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	Mode (linear)			2's complement exponent				
Default Value	0	0	0	1	1	0	0	0

Mode 000 Linear mode
Exponent 11000 - 8 (decimal) default, -9 (decimal) and –12 (decimal) are other options

VOUT_COMMAND [0x21]

Definition: Sets or reports the target output voltage. 2 databytes in 16-bit linear format and exponent is as per VOUT_MODE

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1

Equation: $V_{OUT} = VOUT\_COMMAND \times 2^{-8}$
Range: 0.45V to V_{OUT_MAX}
Units: V

VOUT_TRIM [0x22]

Definition: Applies a fixed trim voltage to the output voltage command value. Module will accept write command, however REGISTER VALUES CANNOT BE TRANSFERRED TO NVM USING STORE_USER_ALL. Some VOUT_TRIM values may trigger VOUT_MIN_MAX_WARNING bit in STATUS_VOUT(7A) command. USE CLEAR_FAULTS to clear Warning bit.

Format	16-bit signed															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Equation: $V_{OUT\_TRIM} = VOUT\_TRIM \times 2^{-8}$
Range: -5 to 5V, VOUT_MODE **Default value: 0V**
Units: V

VOUT_MAX [0x24]

Definition: Sets the upper limit of the output voltage of the module regardless of any other commands or combinations. If an output voltage value higher than the limit her is attempted, the module will set the value equal to the value here and a warning will be recorded in STATUS_BYTE/WORD/VOUT registers and SMBALERT will be pulled down

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	0	0	1	0	0	0	0	0	0	0	0	1	1	0	1	0

Equation: $V_{OUT\_MAX} = VOUT\_MAX \times 2^{-8}$
Range: 0000 to FFFF, VOUT_MODE **Default value: 2.102V**
Units: V

Technical Specifications (continued)

VOUT_MARGIN_HIGH [0x25]

Definition: Sets the value of V_{OUT} during margin high. The command loads the module with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”.

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Equation: $V_{OUT\_MARGIN\_HIGH} = VOUT\_MARGIN\_HIGH \times 2^{-8}$

Range: 0 to VOUT_MAX, VOUT_MODE Units: V

VOUT_MARGIN_LOW [0x26]

Definition: Sets the value of V_{OUT} during margin low. The command loads the module with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”.

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Equation: $V_{OUT\_MARGIN\_LOW} = VOUT\_MARGIN\_LOW \times 2^{-8}$

Range: 0 to VOUT_MAX, VOUT_MODE Units: V

VOUT_TRANSITION_RATE [0x27]

Definition: Sets the rate at which the output voltage should change when the module receives an OPERATION command that requires output voltage change. If a value outside of the acceptable range is written to this command, the module will ignore the value and fault will be recorded in STATUS_BYTE/CML. registers and SMBALERT will be pulled down

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed exponent					Signed mantissa										
Default Value	1	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0

Equation: $VOUT\_TRANSITION\_RATE = Y \times 2^{-3}$

Range: 0 to 127.875mv/µsec **Default value: 1mV/µs**

Resolution 0.125mV/µsec

Technical Specifications (continued)

VOUT_DROOP [0x28]

Definition: Sets the adaptive voltage positioning.

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Resolution is 5/256 mΩ per bit. A value of 0033(h) or 51 decimal sets the loadline to 1mΩ

Default value is 0

Range is 0 to about 10mohms which is equivalent to 0mV/A to 9.98mV/A in increments of 19.53uV/A

VOUT_MIN [0x2B]

Definition: Sets the minimum limit of the output voltage of the module to act as a safeguard against a user accidentally setting voltage at a possibly destructive level. If an attempt to program module below this limit, the module will set the value equal to the lower limit and a warning will be recorded in STATUS_BYTE/WORD/VOUT registers and SMBALERT will be pulled down

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	0	0	1	0	0	0	0	0	0	0	0	1	1	0	1	0

Equation: V_{OUT_MAX} = VOUT_MAX x 2^{-8}

Range: 0000 to FFFF, VOUT_MODE **Default value: 0.25V**

Units: V

FREQUENCY_SWITCH [0x33]

Definition: Sets the switching frequency of the module. Users should not change the value.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed exponent							Signed mantissa								
Default Value	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0

Equation: FREQUENCY_SWITCH = Y x 2°

Default value: 580 kHz

Units: kHz

Technical Specifications (continued)

POWER_MODE [0x34]

Definition: Sets power state of the Module

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Max Efficiency (automatically enables Diode emulation when current drops below threshold)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Max Power – Max configured phases operate (Default)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Power State1- Commands phases to drop to 1 or 2 phases	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Power State2- Commands phases to drop to 1 phase diode emulation mode	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

If an invalid value is attempted, the module will ignore the value and fault will be recorded in STATUS_BYTE/CML. registers and SMBALERT will be pulled down

VIN_ON [0x35]

Definition: Sets the value of the Input Voltage at which the device is enabled to start power conversion

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed exponent						Signed mantissa									
Default Value	1	1	1	1	0	0	0	0	0	0	0	1	1	0	0	1

Equation: $V_{IN\_ON} = VIN\_ON \times 2^{-2}$

Range: 0 to 15.75 **Default value: 6.25V. Do not go below this as it will cause damage to device**

Units: V

If a change of exponent, negative value or greater than 15.75V is attempted, the module will ignore the value and fault will be recorded in STATUS_BYTE/CML. registers and SMBALERT will be pulled down

Technical Specifications (continued)

VIN_OFF [0x36]

Definition: Sets the value of the Input Voltage at which the device is disabled to stop power conversion

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed exponent					Signed mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	1	0	1	1	1

If a change of exponent, negative value or greater than 15.75V is attempted, the module will ignore the value and fault will be recorded in STATUS_BYTE/CML. registers and SMBALERT will be pulled down

Equation: $V_{IN\_ON} = VIN\_ON \times 2^{-2}$

Range: 0 to 15.75 **Default value: 5.75V. Do not go below this as it will cause damage to device**

Units: V

IOUT_CAL_GAIN [0x38]

Definition: Sets the effective impedance across the current sense circuit for use in the calculating output current at

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed exponent					Signed mantissa										
Default Value	1	1	0	0	1	X	X	X	X	X	X	X	X	X	X	X

Equation: IOUT_CAL_GAIN = Y x 2^N where N=-7

Range: -25% to 24.2187% **Resolution 0.78125%** Units: Percent

IOUT_CAL_OFFSET [0x39]

Definition: Adjusts the offset in the output current sensing circuit. (Also used to compensate for delayed measurement of current ramp due to the current sensing blanking time

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed exponent					Signed mantissa										
Default Value	1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X

Equation: IOUT_CAL_OFFSET = Y x 2^N where N=-2

Range: -16A to 15.75A **Resolution: 0.25A** Units: A

Technical Specifications (continued)

VOUT_OV_FAULT_LIMIT [0x40]

Definition: Sets the V_{OUT} overvoltage fault threshold. This command is ignored when module is disabled and when output voltage is ramping from OFF to target voltage. There are 8 settings above VOUT that the fault limit can be set, ranging from 50mV to 400mV in 50mV increments. The fault threshold will be the value set in the register rounded down to the nearest lower setting. For example, if VOUT is set to 1V and VOUT_OV_FAULT_LIMIT is set to 1.23V, then the actual fault limit will be 1.2V. Any setting greater than 400mV above VOUT will result in a fault limit of VOUT + 400mV

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1

Equation: $V_{OUT\_OV\_FAULT\_LIMIT} = VOUT\_OV\_FAULT\_LIMIT \times 2^{-8}$

Range: 0 to 2.102 Default Value: 1.05 Units: V

VOUT_OV_FAULT_RESPONSE [0x41]

Definition: Configures the V_{OUT} overvoltage fault response. Module supports two responses, ignore and shutdown as per table below.

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value - Shutdown	1	0	0	0	0	0	0	0
Ignore	0	0	0	0	0	0	0	0

The module also Sets the Fault bits in STATUS_BYTE, STATUS_WORD and STATUS_VOUT

VOUT_OV_WARN_LIMIT [0x42]

Definition: Sets the V_{OUT} overvoltage warning threshold. VOUT_OV_WARN_LIMIT must be set below the VOUT_OV_FAULT_LIMIT for fault responses.

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Equation: $V_{OUT\_OV\_WARNING\_LIMIT} = VOUT\_OV\_WARN\_LIMIT \times 2^{-8}$

Range: 0 to 2.102 Default Value 2V Units: V

The module also Sets the Fault bits in STATUS_BYTE, STATUS_WORD and STATUS_VOUT

Technical Specifications (continued)

VOUT_UV_WARN_LIMIT [0x43]

Definition: Sets the V_{OUT} undervoltage warning threshold.

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1

Equation: $V_{OUT\_UV\_WARNING\_LIMIT}$ = VOUT_UV_WARN_LIMIT x 2^{-8}

Range: 0 to 2.102, Default value 0.449V Units: V

The module also Sets the Fault bits in STATUS_BYTE, STATUS_WORD and STATUS_VOUT

VOUT_UV_FAULT_LIMIT [0x44]

Definition: Sets the V_{OUT} undervoltage fault threshold at the sense or output pins that causes an output voltage low fault. The value is in the format set by VOUT_MODE. This fault is masked until the unit reaches the programmed output voltage. There are 8 settings below VOUT that the fault limit can be set, ranging from 50mV to 400mV in 50mV increments. The fault threshold will be the value set in the register rounded up to the nearest lower setting. For example, if VOUT is set to 1V and VOUT_UV_FAULT_LIMIT is set to 0.93V, then the actual fault limit will be 0.95V. Any setting greater than 400mV below VOUT will result in a fault limit of VOUT - 400mV.

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0

Equation: $V_{OUT\_UV\_FAULT\_LIMIT}$ = VOUT_UV_FAULT_LIMIT x 2^{-8}

Range: 0 to 2.102 Default value 0.602V Units: V

VOUT_UV_FAULT_RESPONSE [0x45]

Definition: Configures the V_{OUT} undervoltage fault response. Module supports two responses, ignore and shutdown as per table below

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value - Shutdown	1	0	0	0	0	0	0	0
Ignore	0	0	0	0	0	0	0	0

The module also Sets the Fault bits in STATUS_BYTE, STATUS_WORD and STATUS_VOUT

IOUT_OC_FAULT_LIMIT [0x46]

Definition: Sets the I_{OUT} peak overcurrent fault threshold. Unit responds to instantaneous value and those values will not always show up in Iout Readback which has a slower sampling rate

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X

Equation: $I_{OUT\_OC\_FAULT\_LIMIT}$ = Y x 2^{1}

Range: 0A to 510A, Default value: depends on module

Technical Specifications (continued)

IOUT_OC_FAULT_RESPONSE [0x47]

Definition: Configures the I_{OUT} overcurrent fault response. Module supports three responses, hiccup 6 times, hiccup forever and shutdown and latches per table below

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value – Hiccup forever	1	1	1	1	1	0	0	0
Hiccup 6 times then shutdown	1	1	1	1	0	0	0	0
Shutdown and latch	1	1	0	0	0	0	0	0

The module also Sets the Fault bits in STATUS_BYTE, STATUS_WORD and STATUS_IOUT

IOUT_OC_WARN_LIMIT [0x4A]

Definition: Sets the I_{OUT} peak overcurrent warn threshold. Unit responds to instantaneous value and those values will not always show up in Iout Readback which has a slower sampling rate

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X

Equation: $I_{OUT\_OC\_WARN\_LIMIT} = Y \times 2^{1}$

Range: 0A to 510A, **Default value: Default value: depends on module** Units: A

OT_FAULT_LIMIT [0x4F]

Definition: Sets the temperature at which the module should indicate an over-temperature fault..

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed exponent									Signed mantissa						
Default Value	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1

Equation: OT_FAULT_LIMIT = $Y \times 2^{0}$

Range: 0°C to +255°C, **Default value: +125°C** Units: °C

The module also Sets the Fault bits in STATUS_BYTE and STATUS_TEMPERATURE

OT_FAULT_RESPONSE [0x50]

Definition: Instructs the module on what action to take in response to an over-temperature fault.

Module supports three responses, hiccup 6 times, hiccup forever and shutdown as per table below

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value – Shutdown, restart when temp is below internal limit	1	1	0	0	0	0	0	0
Shutdown	1	0	0	0	0	0	0	0
Ignore	0	0	0	0	0	0	0	0

The module also Sets the Fault bits in STATUS_BYTE and STATUS_TEMPERATURE

Technical Specifications (continued)

OT_WARN_LIMIT [0x51]

Definition: Sets the temperature at which the module should indicate an over-temperature warning alarm.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed exponent									Signed mantissa						
Default Value	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0

Equation: OT_WARN_LIMIT = Y x 2^0
Range: 0°C to +225°C, Default value: +110°C Units: °C
The module also Sets the Fault/Warning bits in STATUS_BYTE and STATUS_TEMPERATURE

VIN_OV_FAULT_LIMIT [0x55]

Definition: Sets the V_{IN} overvoltage fault threshold

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed exponent									Signed mantissa						
Default Value	1	1	1	0	0	0	0	0	1	1	1	0	1	0	0	1

Equation: $V_{IN\_OV\_FAULT\_LIMIT}$ = Y x 2^{-4}
Range: 0V to 63.93V, Default value: 14.5V Units: V

VIN_OV_FAULT_RESPONSE [0x56]

Definition: Configures the V_{IN} overvoltage fault response. Module supports two options only – Ignore or Shutdown.

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value - Shutdown	1	0	0	0	0	0	0	0
Ignore	0	0	0	0	0	0	0	0

The module also Sets the Fault bits in STATUS_BYTE, STATUS_WORD and STATUS_INPUT and pulls down SALERT. Any attempt to program a different response other than 2 options will cause Module to ignore the command and set the CML Bit in STATUS_BYTE, Invalid Bit in STATUS_CML and pull down SALERT

VIN_UV_WARN_LIMIT [0x58]

Definition: Sets the V_{IN} undervoltage warning threshold.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed exponent									Signed mantissa						
Default Value	1	1	1	0	0	0	0	0	0	1	1	0	1	0	0	0

Equation: $V_{IN\_UV\_WARN\_LIMIT}$ = Y x 2^{-4}
Range: 0V to 63.93V, **Default value: 6.5V** Units: V
The module also Sets the Fault/Warning bits in STATUS_BYTE, STATUS_WORD and STATUS_INPUT and pulls down SALERT

Technical Specifications (continued)

IIN_OC_WARN_LIMIT [0x5D]

Definition: Sets the I_{IN} overcurrent warning threshold.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X

Equation: $I_{IN\_OC\_WARN\_LIMIT} = Y \times 2^{-1}$

Range: 0 to 127.5, **Default value: depends on module** Units: A

The module also Sets the Fault/Warning bits in STATUS_BYTE, STATUS_WORD and STATUS_INPUT and pulls down SALERT

POWER_GOOD_ON [0x5E]

Definition: Sets the voltage threshold for power-good indication.

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1

Equation: $V_{OUT\_PG\_ON} = POWER\_GOOD\_ON \times 2^{-8}$ Default 0.395 Range: 0V to 2.1 V Units: V

POWER_GOOD_OFF [0x5F]

Definition: Sets the voltage threshold at which POWER_GOOD signal is deasserted

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1

Equation: $V_{OUT\_PG\_ON} = POWER\_GOOD\_OFF \times 2^{-8}$ Default 0.395 Range: 0V to 2.1 V Units: V

TON_DELAY [0x60]

Definition: Sets the delay time from when the module is enabled to the start of V_{OUT} rise.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed exponent					Signed mantissa										
Default Value	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Equation: $TON\_DELAY = Y \times 2^{-1}$

Range: 0ms to 63.5ms @0.5ms **Default value: depends on module** Units: ms

If a change of exponent, negative value or greater than 63.5ms is attempted, the module will ignore the value and fault will be recorded in STATUS_BYTE/CML. registers and SMBALERT will be pulled down

Technical Specifications (continued)

TON_RISE [0x61]

Definition: Sets the rise time of V_{OUT} after the TON_DELAY time has elapsed.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed exponent									Signed mantissa						
Default Value	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0

Equation: TON_RISE = Y x 2^{-2}

Range: 0ms to 31.75ms @0.25ms **Default value: 15ms** Units: ms

If a change of exponent, negative value or greater than 31.75ms is attempted, the module will ignore the value

TON_MAX_FAULT_LIMIT [0x62]

Definition: Sets the maximum time for the output to cross the undervoltage fault limit threshold upon startup.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed exponent									Signed mantissa						
Default Value	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Equation: TON_RISE = Y x 2^{-2}

Range: 0ms to 31.75ms @0.25ms **Default value: 0ms** Units: ms

If a change of exponent, negative value or greater than 31.75ms is attempted, the module will ignore the value and fault will be recorded in STATUS_BYTE/CML. registers and SMBALERT will be pulled down

TON_MAX_FAULT_RESPONSE [0x63]

Definition: Configures how the device responds to a TON_MAX. Module supports two options only – Ignore or Shutdown.

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value - Shutdown	1	0	0	0	0	0	0	0
Default Value - Ignore	0	0	0	0	0	0	0	0

The module also Sets the Fault bits in STATUS_BYTE, STATUS_WORD and STATUS_VOUT and pulls down SALERT and PGOOD/SRRDY LOW. Any attempt to program a different response other than 2 options will cause Module to ignore the command and set the CML Bit in STATUS_BYTE, Invalid Bit in STATUS_CML and pull down SALERT

Technical Specifications (continued)

TOFF_DELAY [0x64]

Definition: Sets the delay time for module to stop transferring energy to the output when commanded to stop with the ON_OFF_CONFIG

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed exponent					Signed mantissa										
Default Value	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Equation: TOFF_DELAY = Y x 2^{-1}

Range: 0ms to 63.5ms, @ 0.5ms **Default value: 0ms** Units: ms

If a change of exponent, negative value or greater than 63.5ms is attempted, the module will ignore the value and fault will be recorded in STATUS_BYTE/CML. registers and SMBALERT will be pulled down

TOFF_FALL [0x65]

Definition: Sets the fall time for V_{OUT} after the TOFF_DELAY has expired.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed exponent					Signed mantissa										
Default Value	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Equation: TOFF_FALL = Y x 2^{-2}

Range: 0ms to 31.75ms, @0.25ms **Default value: 0ms** Units: ms

If a change of exponent, negative value or greater than 31.75ms is attempted, the module will ignore the value

Technical Specifications (continued)

POUT_OP_WARN_LIMIT [0x6A]

Definition: Sets the value of the output power, in watts, that causes a warning that the output power is high. Exp = 0.

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Equation: TOFF_DELAY = Y x 2^0

Units: Watts

PIN_OP_WARN_LIMIT [0x6B]

Definition: Sets the value of the input power, in watts, that causes a warning that the input power is high. Exp = 0

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Equation: TOFF_FALL = Y x 2^0

Units: Watts

STATUS_BYTE [0x78]

Definition: Returns a summary of the module's fault condition. The host may get more information by reading the appropriate status registers.

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See below							
Default Value	0	0	0	0	0	0	0	0

Bit	Status bit name	Meaning
Bit 7		Not used
Bit 6	OFF.	Asserted when the module is not providing power regardless of the reason
Bit 5	VOUT_OV_FAULT	An output overvoltage fault has occurred
Bit 4	IOUT_OV_FAULT	An output overcurrent fault has occurred
Bit 3	VIN_UV_FAULT	An input undervoltage fault has occurred
Bit 2	TEMPERATURE	A temperature fault has occurred
Bit 1	CML	A communication, memory of logic fault has occurred
Bit 0	None of the abov	A fault other than those of bits [6:1] has occurred. The source of the fault will be in bits [15:8] of the STATUS_WORD

Technical Specifications (continued)

STATUS_WORD [0x79]

Definition: Returns two bytes of information with a summary of the module's fault condition. Based on the information in these bytes, the host may get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (0x78) command.

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See below															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Status bit name	Meaning
Bit 15	VOUT	An output voltage fault or warning has occurred
Bit 14	IOUT	An output current fault has occurred
Bit 13	INPUT	An input voltage fault or warning has occurred
Bit 12	MFR_SPECIFIC	A manufacturer specific fault or warning has occurred
Bit 11	POWER_GOOD #	A POWER_GOOD signal, if present, is negated. If the POWER_GOOD# bit is set, this indicates that the POWER_GOOD signal, if present, is signaling that the output power is not good.
Bit 10	n/a	Not used
Bit 9	n/a	Not used
Bit 8	n/a	Not used
Bit 7	n/a	Not used
Bit 6	OFF.	Asserted when the module is not providing power regardless of the reason
Bit 5	VOUT_OV_FAULT	An output overvoltage fault has occurred
Bit 4	IOUT_OV_FAULT	An output overcurrent fault has occurred
Bit 3	VIN_UV_FAULT	An input undervoltage fault has occurred
Bit 2	TEMPERATURE	A temperature fault has occurred
Bit 1	CML	A communication, memory of logic fault has occurred
Bit 0	None of the above	A fault other than those of bits [6:1] has occurred. The source of the fault will be in bits [15:8] of the STATUS_WORD

STATUS_VOUT [0x7A]

Definition: Returns one data byte with the status of the output voltage.

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See below							
Default Value	0	0	0	0	0	0	0	0

Bit	Status bit name	Meaning
Bit 7	VOUT_OV_FAULT	Indicates an output overvoltage fault
Bit 6	VOUT_OV_WARNING	Indicates an output overvoltage warning
Bit 5	VOUT_UV_WARNING	Indicates an output undervoltage warning
Bit 4	VOUT_UV_FAULT	Indicates an output undervoltage fault
Bit 3	VOUT_MIN_MAX_WARNING	Indicates an attempt to set VOUT_COMMAND greater than VOUT_MAX or below 0.45V
Bit 2	TON_MAX_FAULT	The Startup time has exceeded the time set by TON_MAX_FAULT_LIMIT
Bits 1:0	n/a	Not used

Technical Specifications (continued)

STATUS_IOUT [0x7B]

Definition: Returns one data byte with the status of the output current.

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See below							
Default Value	0	0	0	0	0	0	0	0

Bit	Status bit name	Meaning
Bit 7	IOUT_OC_FAULT	Indicates an output overcurrent fault
Bit 6	n/a	Not used
Bit 5	IOUT_OC_WARNING	Indicates an output overcurrent warning
Bits 4:1	n/a	Not used
Bit 0	POUT_OP_WARNING	Indicates an output over-power warning has occurred

STATUS_INPUT [0x7C]

Definition: Returns one data byte with the status of the input voltage.

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See below							
Default Value	0	0	0	0	0	0	0	0

Bit	Status bit name	Meaning
Bit 7	VIN_OV_FAULT	Indicates an input overvoltage fault
Bit 6	n/a	
Bit 5	VIN_UV_WARNING	Indicates an input undervoltage warning
Bit 4	n/a	
Bits 3	UNIT OFF for Insufficient VIN	Unit provide output because input is not above required threshold
Bit 2	n/a	
Bit 1	IIN_OC_WARNING	Indicates an input overcurrent warning
Bit 0	PIN_OP_WARNING	Indicates an input over-power warning
Bit 5	VIN_UV_WARNING	Indicates an input undervoltage warning

STATUS_TEMPERATURE [0x7D]

Definition: Returns one data byte with the status of the temperature related information. Note that warning bits may not be set when the corresponding fault bits are set. This can occur with rapidly changing fault conditions.

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See below							
Default Value	0	0	0	0	0	0	0	0

Bit	Status bit name	Meaning
Bit 7	OT_FAULT	Overtemperature Fault
Bit 6	OT_WARNING	Overtemperature Warning
Bit 5	Reserved	
Bit 4	Reserved	
Bits 3	Reserved	
Bit 2	Reserved	
Bit 1	Reserved	
Bit 0	Reserved	

Technical Specifications (continued)

STATUS_CML [0x7E]

Definition: Returns one byte of information with a summary of any Communications, Memory, and/or Logic errors. Status bits can only be cleared with the CLEAR_FAULTS command or by disabling, then re-enabling the module.

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See below							
Default Value	0	0	0	0	0	0	0	0

Bit	Assignment	Meaning
Bit 7	1	Invalid or unsupported PMBus command was received
Bit 6	1	The PMBus command was sent with invalid or unsupported data
Bit 5	1	A Packet Error Check (PEC) failed on a PMBus command
Bits 4:2	n/a	Not used
Bit 1	1	Other communication Fault
Bit 0	n/a	Not used

STATUS_MFR_SPECIFIC [0x80]

Definition: Returns one byte of information providing the status of the module's voltage monitoring and clock synchronization faults.

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See below							
Default Value	0	0	0	0	0	0	0	0

Bit	Status bit name	Meaning
Bit 7	Phase Fault	Phase has exceeded the phase current limit
Bit 6	Per Phase Current Warning	Phase has exceeded the per phase current limit threshold
Bit 5	Reserved	
Bit 4	Reserved	
Bits 3	Reserved	
Bit 2	VAUX_UV_FAULT	Auxiliary Undervoltage Fault has occurred
Bit 1	TSENSE FAULT	A TOUT Fault from a power stage has occurred
Bit 0	Phase Fault	A Phase has exceeded the phase current limit

READ_VIN [0x88]

Definition: Returns the input voltage reading.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed exponent									Signed mantissa						
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Equation: $V_{IN\_READ} = Y \times 2^{-5}$ Range: 0 to 31.968 @0.03125V Units: V

Technical Specifications (continued)

READ_IIN [0x89]

Definition: Returns the input current reading.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function		Signed exponent								Signed mantissa						
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Equation: $I_{IN\_READ} = Y \times 2^{-4}$ (loop 1), 2^{-5} (Loop2)

Range: 0 to 63.9375A @0.0625A (Loop1), 0 to 31.968A @ 0.03125A (Loop2) Units: A

READ_VOUT [0x8B]

Definition: Returns the output voltage reading.

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Mantissa															
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Equation: $V_{OUT\_READ} = READ\_VOUT \times 2^{-8}$

Range: 0 to 2.1V Units: V

READ_IOUT [0x8C]

Definition: Returns the output current reading.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function		Signed exponent								Signed mantissa						
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Equation: $I_{OUT\_READ} = Y \times 2^{-1}$ (Loop1), 2^{-2} (Loop1 or Loop2) - options

Range: 0 to 511.5A (Loop1) or 0 to 255.75A (Loop 2) Units: A

READ_TEMPERATURE_1 [0x8D]

Definition: Returns the temperature of the controller die.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function		Signed exponent								Signed mantissa						
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Equation: $T_{1\_READ} = Y \times 2^{0}$ Range: -256 to 255°C @1°C Units: °C

Technical Specifications (continued)

READ_DUTY_CYCLE [0x94]

Definition: Reports the actual duty cycle of the converter while the module is enabled.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function		Signed exponent								Signed mantissa						
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Equation: $D_{CYCLE\_READ} = Y \times 2^{-2}$ Range: 0 – 100% @0.25% Units: %

READ_POUT [0x96]

Definition: Returns the calculated output power in Watts.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function		Signed exponent								Signed mantissa						
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Equation: $P_{OUT\_READ} = Y \times 2^{-1}$
Range: 0 to 511W @0.5W Units: W

READ_PIN [0x97]

Definition: Returns the calculated input power in Watts.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function		Signed exponent								Signed mantissa						
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Equation: $P_{IN\_READ} = Y \times 2^{-1}$
Range: 0 to 511W @0.5W Units: W

PMBUS_REVISION [0x98]

Definition: Returns the revision of the PMBus Specification to which the module is compliant.

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See below							
Default Value	0	0	1	1	0	0	1	1

Bit	Value	Meaning
Bits 7:4	0011	PMBus Part 1 Revision is 1.3
Bits 3:0	0011	PMBus Part 2 Revision is 1.3

Technical Specifications (continued)

MFR_ID [0x99]

Definition: Sets a factory identification string not to exceed 2 Bytes. Default value is 4952(h)

MFR_MODEL [0x9A]

Definition: Sets a module's model string not to exceed 2 bytes. Default value depends on module

MFR_REVISION [0x9B]

Definition: Sets a module's revision string not to exceed 3 bytes. Default format is 12h XXh XXh

MFR_DATE [0x9D]

Definition: Sets a production date string not to exceed 2 bytes.

IC_DEVICE_ID [0xAD]

Definition: Reports controller identification information. 2 Bytes. First Byte is 01(h)

IC_DEVICE_REV [0xAE]

Definition: Reports controller revision information.2 Bytes. First Byte is 01(h)

MFR_READ_VAUX [C4]

Definition: Returns the Voltage of an aux voltage as sensed at the VAUXSEN pin in volts. The 2 data bytes are formatted in Linear Data format with the exponent as defined by VOUT_MODE (2^{-8}).

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Mantissa															
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Equation: $V_{MFR\_READ\_VAUX} = Y \times 2^{-8}$

MFR _VIN_PEAK [C5]

Definition: Returns the maximum measured input voltage in volts with a resolution of 1/32V. The previous value is cleared upon reading

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed exponent							Signed mantissa								
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Equation: $V_{MFR\_READ\_VAUX} = Y \times 2^{-5}$

Range: 0 to 31.968V @ 0.03125V Units: V

MFR_VOUT_PEAK [C6]

Definition: Returns the max output voltage in volts. The 2 data bytes are formatted in Linear Data format with the exponent as defined by VOUT_MODE (2^{-8}). The previous value is cleared upon reading

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Mantissa															
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Equation: $V_{MFR\_VOUT\_MAX} = Y \times 2^{-8}$

Technical Specifications (continued)

MFR _IOUT_PEAK [C7]

Definition: Returns the maximum measured output current in Amps. Loop 1 resolution can be 0.25A or 0.5A. Loop 2 resolution is always 0.25A. The previous value is cleared upon reading

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed exponent							Signed mantissa								
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Loop1 Range 0 to 511.5A @0.5A resolution or 0 to 255.75A @0.25A
Loop2 Range 0 to 255.75A @0.25A

MFR _TEMP_PEAK [C8]

Definition: Returns the maximum measured temperature in degrees C with a resolution of 1°C. The previous value is cleared upon reading.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed exponent							Signed mantissa								
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Range -256°C to 256°C @1°C resolution

MFR _VIN_VALLEY [C9]

Definition: Returns the minimum measured input voltage in volts with a resolution of 1/32V. The previous value is cleared upon reading

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed exponent							Signed mantissa								
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Equation: $V_{MFR\_READ\_VAUX} = Y \times 2^{-5}$

Range: 0 to 31.968V @ 0.03125V Units: V

MFR_VOUT_VALLEY [CA]

Definition: Returns the minimum output voltage in volts. The 2 data bytes are formatted in Linear Data format with the exponent as defined by VOUT_MODE (2^{-8}). The previous value is cleared upon reading

Format	16-bit unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Mantissa															
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Equation: $V_{MFR\_VOUT\_MAX} = Y \times 2^{-8}$

Technical Specifications (continued)

MFR _IOUT_VALLEY [CB]

Definition: Returns the maximum measured output current in Amps. Loop 1 resolution can be 0.25A or 0.5A. Loop 2 resolution is always 0.25A. The previous value is cleared upon reading

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function		Signed exponent								Signed mantissa						
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Loop1 Range 0 to 511.5A @0.5A resolution or 0 to 255.75A @0.25A

Loop2 Range 0 to 255.75A @0.25A

MFR _TEMP_VALLEY [CC]

Definition: Returns the minimum measured temperature in degrees C with a resolution of 1°C. The previous value is cleared upon reading.

Format	11-bit linear															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function		Signed exponent								Signed mantissa						
Default Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

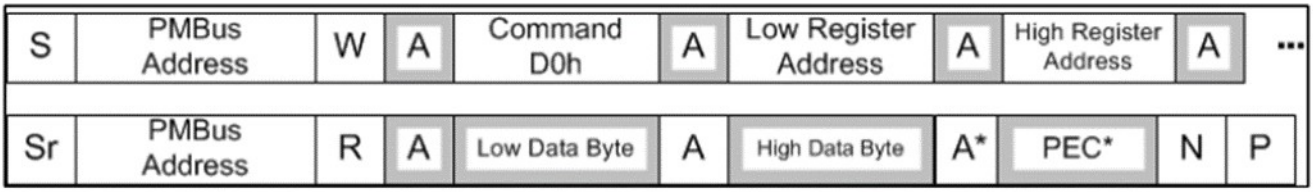
Range -256°C to 256°C @1°C resolution

Technical Specifications (continued)

MFR_REGISTER_ACCESS [D0]

Definition: Allows users to access I²C register map based advanced commands.

Read Process is through the following format



Write Process is through the following format

S	PMBUS Address	W	A	Command D0h	A	4	A	Low Register	A	High Register	.....

----------	A	Low Data Byte	A	High Data Byte	A	PEC	A	P	

Changing the values for some of the commands Table 4 require use of Simulation Tools available at https://abb.transim.com/login.aspx or else please contact your ABB FAE. Some commands are common to Loop 1 and 2 and some are specific to the individual loops.

Through the D0 command user can access some of the module advanced features which are covered in the command list at the end of the section. These features are:

ADAPTIVE TRANSIENT ALGORITHM (ATA)

This is a high speed non-linear control technique that uses a high speed digitizer to measure both the magnitude and slope of the error signal to the predict load current transient. The prediction is used to control pulse widths and phase relationships of the PWM pulses

POWER MODE STATES (PS)

The module uses Power States to set the power savings mode

Power State	Mode	Recommended Current
PS0	Full Power	Maximum
PS1	Light Load 1-2P	<20A
PS2	1Phase active discontinuous (Diode Emulation)	<5A

Entry and Exit Points

	Manual	Auto Mode
PS1 Entry	A) Through Command	n/a if Phase Shed enabled
PS1 Exit	A) Command to PS0 B) During DVID event C) Current Limit set to PS0 mode	n/a if Phase Shed enabled
PS2 Entry	A) Through Command	Current level in 1 Phase
PS2 Exit	A) Command to PS1 or PS0 B) During DVID event C) Current Limit set to PS0 mode	DVID to PS0 Current Limit to PS0

Technical Specifications (continued)

DYNAMIC PHASE CONTROL (DPC) in PS0

The module provides the option to adjust the number of phases with load current thus optimizing efficiency over a wide range of loads. The output current level at which a phase is added can be programmed for each phase. See Table below . These commands are covered in the complete list of commands at the end of this section

DO Register /Sub_command - implementation in 2A steps	Action
Phase1_thresh	2Phase when Iout > Phase 1_thresh
Phase2_delta	3Phase when Iout > Phase 1_thresh + Phase2_delta
Phase3_delta	4Phase when Iout > Phase 1_thresh + Phase2_delta + Phase3_delta
Phase4_delta	5Phase when Iout > Phase 1_thresh + Phase2_delta + Phase3_delta+ Phase4_delta
Phase5_delta*	6Phase when Iout > Phase 1_thresh + Phase2_delta + Phase3_delta+ Phase4_delta+ Phase5_delta
Phase6 delta*	7Phase when Iout > Phase 1_thresh + Phase2_delta + Phase3_delta+ Phase4_delta+ Phase5_delta + Phase6_delta
Phase7delta*	8Phase when Iout > Phase 1_thresh + Phase2_delta + Phase3_delta+ Phase4_delta+ Phase5_delta + Phase6_delta + Phase7_delta

.* Only possible with use of Satellites

EFFICIENCY SHAPING

The DPC techniques described above helps the module user achieve the best efficiency for the application

DISCONTINUOUS MODE OPERATION—PS2 (active diode emulation mode)

Under very light loads the module is dominated by switching losses. In PS2 Mode the module operates in constant on-time mode where the user sets the desired peak-to-peak ripple by programming an error threshold and on-time duration. The module estimates when the inductor current declines to zero on a cycle-by-cycle basis, and shuts off the low-side MOSFET at an appropriate time in each cycle. This effectively lowers switching frequency, resulting in lower switching losses and thus improved efficiency

MTP Register	Action
Ni_thresh	Sets the current level below which PS2/PS3 is entered
de_thresh	Sets the error threshold to start a pulse during diode emulation, in 3 mV resolution
DE_On_Pulse_Width	Sets the duration of the ON time pulse in 40 ns steps during diode emulation
Reduce_DE_Off_Time	Reduces the calculated low-side FET ON time during diode emulation in 60 ns steps. Useful for compensating for FET drivers' tri-state delay for better zero-crossing pre-

Technical Specifications (continued)

Table 1 – D0 Specific Commands for Advanced Functions

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value (M – Master, S – Satellite) HEX(DEC)
Disable Output	D0 0040 [9:8]	COMMON	0 (Loop1 and 2 enabled) 1 (Loop 2 enabled only) 2 (Loop 1 enabled only) 3(Loop1 and 2 both disabled)	02(2)
Loop1__phase_active_ps1 (The number of active phases in PS1 mode)	D0 0024 [3:3]	COMMON	0 (The number of active phases in PS1 mode that is 1) 1 (The number of active phases in PS1 mode that is 2)	0—M only 01(1)—M + S
Loop1_phase_active_max (The maximum number of phases that can be active on loop 1)	D0 0024 [2:0]	COMMON	0 (The maximum number of phase that active on loop 1 is 1) 1 (The maximum number of phase that active on loop 1 is 2) 2 (The maximum number of phase that active on loop 1 is 3) 3 (The maximum number of phase that active on loop 1 is 4) 4 (The maximum number of phase that active on loop 1 is 5) 5 (The maximum number of phase that active on loop 1 is 6) 6 (The maximum number of phase that active on loop 1 is 7) 7 (The maximum number of phase that active on loop 1 is 8)	0 –M40, 01(1) - M80 02(2) - M120 03(3) - M160
Loop_2_phase_active_ps1 (the number of active phases in PS1 mode)	D0 0024 [6:6]	COMMON	0 (The number of active phases in PS1 mode that is 1) 1 (The number of active phases in PS1 mode that is 2)	0—M only 01(0)—M+S
Loop2_phase_active_max (The max no. of phases that can be active on Loop1)	D0 0024 [5:4]	COMMON	0 (The maximum number of phase that active on loop 2 is 1) 1 (The maximum number of phase that active on loop 2 is 2) 2 (The maximum number of phase that active on loop 2 is 3) 3(The maximum number of phase that active on loop 2 is 4)	0—M or M+S40 01(1)– M + 2xS40 02(2)—M+3xS40 03(3)—M+4xS40(or S160)

Technical Specifications (continued)

ACCURACY OPTIMIZATION REGISTERS

The module offers registers to fine tune the accuracy of the reported measurements

NVM Register	Action
IIN Fixed Offset	Offsets the input current in 1/32A steps
IIN Per Phase Offset	Offsets the input current dependent upon the number of active phases in 1/128A steps e.g. the drive current for the MOSFET's. This current increases every time a new phase is added.
Duty Cycle Adjust	Adjusts the input current calculation to compensate for a non-ideal driver
Phase Current Offset	Offsets individual phase current from -8A to +7.75A 0.25A steps
Phase Current Gain	Calibrate the individual phase current's gain from -32/128 to +32/128mV/A at 1/128mV/A steps
IOUT Current Offset	Offsets the total output current from -16A to +15.75A at 0.25A steps
IOUT Current Gain	Calibrate the total output current's gain from -32/128 to +32/128mV/A at 1/128mV/A steps
Vout Offset	Offsets the output voltage +40 mV to -35 mV in 5 mV steps (Intel® VR12 mode), or +80 mV to -70 mV in 10 mV steps
Temperature Offset	Offsets the temperature -32 °C to +31 °C in 1 °C steps to compensate for offset between the hottest component and the NTC sensing location.

DIGITAL FEEDBACK LOOP & PWM

The MLX/SLX modules use a digital feedback loop to minimize the requirement for output decoupling, and to maintain a tightly regulated output voltage. The error between the target and the output voltage is digitized and passed through a low pass filter. This filtered signal is then passed through an initial single-pole filter stage, followed by the PID (Proportional Integral Derivative) compensator, and an additional single-pole filter stage. The loop compensation parameters Kp (proportional coefficient), Ki (integral coefficient), and Kd (derivative coefficient), as well as the low-pass filter pole locations are user-configurable to optimize the module for the chosen external components. The adaptive PID control used intelligently scales the coefficients and the low-pass filters in realtime, to maintain optimum stability, as phases are added and dropped dynamically in the application. This auto-scaling feature significantly reduces design time by virtue of having to design the PID coefficients design only for one loop combination.

Each of the proportional, integral and derivative terms is a 6-bit value stored in user memory register (24 writes) that is decoded by the modules digital core. This allows the designer to set the converter bandwidth and phase margin to the desired values.

In addition there are the two configurable poles (kpole1 and kpole2), typically positioned to filter noise, and to roll off the high-frequency gain that the Kd term creates. The outputs of the compensator and the phase current balance block are fed into a digital PWM pulse generator to generate the PWM pulses for the active phases. The digital PWM generator has a native time resolution of 1.3 ns which is combined with digital dithering to provide an effective PWM resolution of 163 ps.

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
loop1_phase1_thresh (The current threshold for loop 1, above which it is 2 phase operation)	D0 0026 [15:12]	COMMON	(The current threshold for loop 1, above which it is 2 phase operation 0A to 30A and step is 2A.) 0-->0A 9-->18A 1-->2A 10-->20A 2-->4A 11-->22A 3-->6A 12-->24A 4-->8A 13-->26A 5-->10A 14-->28A 6-->12A 15-->30A 7-->14A 8-->16A	0—M40,M80,M120,m160
loop1_phase2_delta (Value when added to loop_1_phase1_thresh gives loop_1_phase2_thresh, the current threshold above which it is3 phase operation)	D0 0026 [11:8]	COMMON	(loop_1_phase1_thresh gives loop_1_phase2_thresh, the current threshold above which it is 3 phase operation. 0A to 30A and step is 2A.) 0-->0A 9-->18A 1-->2A 10-->20A 2-->4A 11-->22A 3-->6A 12-->24A 4-->8A 13-->26A 5-->10A 14-->28A 6-->12A 15-->30A 7-->14A 8-->16A	0—M40,M80,M120,M160
loop1_phase3_delta (Value, when added to loop_1_phase2_thresh gives loop_1_phase3_thresh, the current threshold above which it is4 phase operation)	D0 0026 [7:4]	COMMON	(loop_1_phase2_thresh gives loop_1_phase3_thresh, the current threshold above which it is 4 phase operation. 0A to 30A and step is 2A.) 0-->0A 9-->18A 1-->2A 10-->20A 2-->4A 11-->22A 3-->6A 12-->24A 4-->8A 13-->26A 5-->10A 14-->28A 6-->12A 15-->30A 7-->14A 8-->16A	0—M40,M80,M120,M160

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
loop1_phase4_delta (Value, when added to loop_1_phase3_thresh gives loop_1_phase4_thresh, the current threshold above which it is5 phase operation)	D0 0026 [3:0]	COMMON	(loop_1_phase3_thresh gives loop_1_phase4_thresh, the current threshold above which it is5 phase operation.. 0A to 30A and step is 2A.) 0-->0A 9-->18A 1-->2A 10-->20A 2-->4A 11-->22A 3-->6A 12-->24A 4-->8A 13-->26A 5-->10A 14-->28A 6-->12A 15-->30A 7-->14A 8-->16A	0— M40,M80,M120,M160
loop1_phase5_delta (Value, when added to loop_1_phase4_thresh gives loop_1_phase5_thresh, the current threshold above which it is6 phase operation)	D0 0028 [15:12]	COMMON	(loop_1_phase4_thresh gives loop_1_phase5_thresh, the current threshold above which it is 6 phase operation. 0A to 30A and step is 2A.) 0-->0A 9-->18A 1-->2A 10-->20A 2-->4A 11-->22A 3-->6A 12-->24A 4-->8A 13-->26A 5-->10A 14-->28A 6-->12A 15-->30A 7-->14A 8-->16A	0— M40,M80,M120,M160
loop1_phase6_delta (Value, when added to loop_1_phase5/6_thresh gives loop_1_phase6/7_thresh, the current threshold above which it is7 or 8 phase operation)	D0 0028 [11:8]	COMMON	(loop_1_phase5/6_thresh gives loop_1_phase6 / 7_thresh, the current threshold above which it is 7 or 8 phase operation. 0A to 30A and step is 2A.) 0-->0A 9-->18A 1-->2A 10-->20A 2-->4A 11-->22A 3-->6A 12-->24A 4-->8A 13-->26A 5-->10A 14-->28A 6-->12A 15-->30A 7-->14A 8-->16A	0— M40,M80,M120,M160

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
loop2_phase1_thresh (The current threshold for loop 2, above which it is 2 phase operation)	D0 0028 [7:4]	COMMON	(The current threshold for loop 2, above which it is 2 phase operation. . 0A to 30A and step is 2A.) 0-->0A 9-->18A 1-->2A 10-->20A 2-->4A 11-->22A 3-->6A 12-->24A 4-->8A 13-->26A 5-->10A 14-->28A 6-->12A 15-->30A 7-->14A 8-->16A	0—M only >0—M+S
loop2_phase2_delta (Value when added to loop_2_phase1,2_thresh gives loop_2_phase2/3_thresh, the current threshold above which it is3 or 4 phase operation)	D0 0028 [3:0]	COMMON	(loop_2_phase1,2_thresh gives loop_2_phase2 /3_thresh, the current threshold above which it is3 or 4 phase operation. 0A to 30A and step is 2A.) 0-->0A 9-->18A 1-->2A 10-->20A 2-->4A 11-->22A 3-->6A 12-->24A 4-->8A 13-->26A 5-->10A 14-->28A 6-->12A 15-->30A 7-->14A 8-->16A	0—M 0—M+S40 0–M+2xS40 >0—M+3xS40 >0—M+4XS40
psi_oc_en (Over current fault enable during power states other than 0. 1 = shutdown loop, 0 = add phases)	D0 043E [15:15]	LOOP1	0-->(Add phases) 1-->(Shutdown loop.)	0
pi_fault_en (Enable phase current fault. If the current in any phase is too high/low, the loop is shutdown)	D0 0440 [6:6]	LOOP1	0-->(Disable phase current fault) 1-->(Shutdown the faulted loop.)	0

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
diode_emu_x2 (1=doubles ON/OFF times for diode emulation. Used when using large L & C.)	D0 0428 [11:11]	LOOP1	0-->(Disabled) 1-->(Doubles ON/OFF times.)	0
diode_emu_pw (Fixed pulse width 'on' time during diode emulation)	D0 0428 [10:8]	LOOP1	0-->(Fixed pulse width 'on' time during diode emulation time is 107 ns) 1-->(Fixed pulse width 'on' time during diode emulation time is 133 ns) 2-->(Fixed pulse width 'on' time during diode emulation time is 53 ns) 3-->(Fixed pulse width 'on' time during diode emulation time is 107 ns) 4-->(Fixed pulse width 'on' time during diode emulation time is 160 ns) 5-->(Fixed pulse width 'on' time during diode emulation time is 213 ns) 6-->(Fixed pulse width 'on' time during diode emulation time is 53 ns) 7-->(Fixed pulse width 'on' time during diode emulation time is 160 ns)	07 (7)
diode_emu_thresh (Error threshold to start a pulse during diode emulation)	D0 0428 [6:4]	LOOP1	0-->(Error threshold to start a pulse during diode emulation ,data is 0mV) 1-->(Error threshold to start a pulse during diode emulation ,data is 4mV) 2-->(Error threshold to start a pulse during diode emulation ,data is 8mV) 3-->(Error threshold to start a pulse during diode emulation ,data is 12mV) 4-->(Error threshold to start a pulse during diode emulation ,data is 16mV) 5-->(Error threshold to start a pulse during diode emulation ,data is 20mV) 6-->(Error threshold to start a pulse during diode emulation ,data is 24mV) 7-->(Error threshold to start a pulse during diode emulation ,data is 28mV)	01 (1)
de_off_time_adj (Reduction in the diode emulation off time)	D0 0428 [3:0]	LOOP1	0-->(Reduction in the diode emulation off time data is 0 ns.) 1-->(Reduction in the diode emulation off time data is 41.7 ns.) 2-->(Reduction in the diode emulation off time data is 83.4 ns.) 3-->(Reduction in the diode emulation off time data is 125.1 ns.) 4-->(Reduction in the diode emulation off time data is 166.8 ns.) 5-->(Reduction in the diode emulation off time data is 208.5 ns.) 6-->(Reduction in the diode emulation off time data is 250.2 ns.) 7-->(Reduction in the diode emulation off time data is 291.9 ns.) 8-->(Reduction in the diode emulation off time data is 333.6 ns.) 9-->(Reduction in the diode emulation off time data is 375.3 ns.) 10-->(Reduction in the diode emulation off time data is 417 ns.) 11-->(Reduction in the diode emulation off time data is 458.7 ns.) 12-->(Reduction in the diode emulation off time data is 500.4 ns.) 13-->(Reduction in the diode emulation off time data is 542.1 ns.) 14-->(Reduction in the diode emulation off time data is 583.8 ns.) 15-->(Reduction in the diode emulation off time data is 625.5 ns.)	04 (4)

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	De-fault Value
le_th (error threshold to go from discontinu-ous to continuous mode. Creates large error signal when in PS1/2/3,)	D0 042A [3:0]	LOOP1	0-->(error threshold to go from discontinuous to continuous mode. Data is 8 mV) 1-->(error threshold to go from discontinuous to continuous mode. Data is 16 mV) 2-->(error threshold to go from discontinuous to continuous mode. Data is 20 mV) 3-->(error threshold to go from discontinuous to continuous mode. Data is 24 mV) 4-->(error threshold to go from discontinuous to continuous mode. Data is 28 mV) 5-->(error threshold to go from discontinuous to continuous mode. Data is 64 mV) 6-->(error threshold to go from discontinuous to continuous mode. Data is 32 mV) 7-->(error threshold to go from discontinuous to continuous mode. Data is 36 mV) 8-->(error threshold to go from discontinuous to continuous mode. Data is 40 mV) 9-->(error threshold to go from discontinuous to continuous mode. Data is 44 mV) 10-->(error threshold to go from discontinuous to continuous mode. Data is 48 mV) 11-->(error threshold to go from discontinuous to continuous mode. Data is 52 mV) 12-->(error threshold to go from discontinuous to continuous mode. Data is 56 mV) 13-->(error threshold to go from discontinuous to continuous mode. Data is 60 mV) 14-->(error threshold to go from discontinuous to continuous mode. Data is 64 mV) 15--> (Disabled)	09 (9)
auto_ps_mode (Enables automatic power state mode.)	D0 0432 [4:4]	LOOP1	0-->(Disable automatic power state mode.) 1-->(Enables automatic power state mode.)	0

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
inductor_ni_thresh (Total current threshold below which it is assumed that the inductor current has a negative component. Resolution=1/4 A)	D0 0440 [5:0]	LOOP1	inductor_ni_thresh: 0 --> 0A, 1 --> 0.25A, 2 --> 0.5A, 3 --> 0.75A, 4 --> 1A, 5 --> 1.25A, 6 --> 1.5A, 7 --> 1.75A, 8 --> 2A, 9 --> 2.25A, 10 --> 2.5A, 11 --> 2.75A, 12 --> 3A, 13 --> 3.25A, 14 --> 3.5A, 15 --> 3.75A 16 --> 4A, 17 --> 4.25A, 18 --> 4.5A, 19 --> 4.75A, 20 --> 5A, 21 --> 5.25A, 22 --> 5.5A, 23 --> 5.75A, 24 --> 6A, 25 --> 6.25A, 26 --> 6.5A, 27 --> 6.75A, 28 --> 7A, 29 --> 7.25A, 30 --> 7.5A, 31 --> 7.75A 32 --> 8A, 33 --> 8.25A, 34 --> 8.5A, 35 --> 8.75A, 36 --> 9A, 37 --> 9.25A, 38 --> 9.5A, 39 --> 9.75A, 40 --> 10A, 41 --> 10.25A, 42 --> 10.5A, 43 --> 10.75A, 44 --> 11A, 45 --> 11.25A, 46 --> 11.5A, 47 --> 11.75A 48 --> 12A, 49 --> 12.25A, 50 --> 12.5A, 51 --> 12.75A, 52 --> 13A, 53 --> 13.25A, 54 --> 13.5A, 55 --> 13.75A, 56 --> 14A, 57 --> 14.25A, 58 --> 14.5A, 59 --> 14.75A, 60 --> 15A, 61 --> 15.25A, 62 --> 15.5A, 63 --> 15.75A	0
psi_oc_en (Over current fault enable during power states other than 0)	D0 083E [15:15]	LOOP2	0-->(Add phases) 1-->(Shutdown loop.)	0
pi_fault_en (Enable phase current fault. If the current in any phase is too high/low, the loop is shutdown.)	D0 0840 [6:6]	LOOP2	0-->(Disable phase current fault) 1-->(Shutdown the faulted loop.)	0
diode_emu_x2 (1=doubles ON/OFF times for diode emulation. Used when using large L & C.)	D0 0828 [11:11]	LOOP2	0-->(Disabled) 1-->(Doubles ON/OFF times.)	0
diode_emu_pw (Fixed pulse width 'on' time during diode emulation.)	D0 0828 [10:8]	LOOP2	0-->(Fixed pulse width 'on' time during diode emulation time is 107 ns) 1-->(Fixed pulse width 'on' time during diode emulation time is 133 ns) 2-->(Fixed pulse width 'on' time during diode emulation time is 53 ns) 3-->(Fixed pulse width 'on' time during diode emulation time is 107 ns) 4-->(Fixed pulse width 'on' time during diode emulation time is 160 ns) 5-->(Fixed pulse width 'on' time during diode emulation time is 213 ns) 6-->(Fixed pulse width 'on' time during diode emulation time is 53 ns) 7-->(Fixed pulse width 'on' time during diode emulation time is 160 ns)	07 (7)

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
diode_emu_thresh (Error threshold to start a pulse during diode emulation. The resolution is 4mv)	D0 0828 [6:4]	LOOP2	0-->(Error threshold to start a pulse during diode emulation ,data is 0mV) 1-->(Error threshold to start a pulse during diode emulation ,data is 4mV) 2-->(Error threshold to start a pulse during diode emulation ,data is 8mV) 3-->(Error threshold to start a pulse during diode emulation ,data is 12mV) 4-->(Error threshold to start a pulse during diode emulation ,data is 16mV) 5-->(Error threshold to start a pulse during diode emulation ,data is 20mV) 6-->(Error threshold to start a pulse during diode emulation ,data is 24mV) 7-->(Error threshold to start a pulse during diode emulation ,data is 28mV)	01(1)
de_off_time_adj (Reduction in the diode emulation off time, to adjust for some drivers. Q=41.7 ns)	D0 0828 [3:0]	LOOP2	0-->(Reduction in the diode emulation off time data is 0 ns.) 1-->(Reduction in the diode emulation off time data is 41.7 ns.) 2-->(Reduction in the diode emulation off time data is 83.4 ns.) 3-->(Reduction in the diode emulation off time data is 125.1 ns.) 4-->(Reduction in the diode emulation off time data is 166.8 ns.) 5-->(Reduction in the diode emulation off time data is 208.5 ns.) 6-->(Reduction in the diode emulation off time data is 250.2 ns.) 7-->(Reduction in the diode emulation off time data is 291.9 ns.) 8-->(Reduction in the diode emulation off time data is 333.6 ns.) 9-->(Reduction in the diode emulation off time data is 375.3 ns.) 10-->(Reduction in the diode emulation off time data is 417 ns.) 11-->(Reduction in the diode emulation off time data is 458.7 ns.) 12-->(Reduction in the diode emulation off time data is 500.4 ns.) 13-->(Reduction in the diode emulation off time data is 542.1 ns.) 14-->(Reduction in the diode emulation off time data is 583.8 ns.) 15-->(Reduction in the diode emulation off time data is 625.5 ns.)	04 (4)
le_th (error threshold to go from discontinuous to continuous mode. Creates large error signal when in PS1/2/3)	D0 082A [3:0]	LOOP2	0-->(error threshold to go from discontinuous to continuous mode. Data is 8 mV) 1-->(error threshold to go from discontinuous to continuous mode. Data is 16 mV) 2-->(error threshold to go from discontinuous to continuous mode. Data is 20 mV) 3-->(error threshold to go from discontinuous to continuous mode. Data is 24 mV) 4-->(error threshold to go from discontinuous to continuous mode. Data is 28 mV) 5-->(error threshold to go from discontinuous to continuous mode. Data is 64 mV) 6-->(error threshold to go from discontinuous to continuous mode. Data is 32 mV) 7-->(error threshold to go from discontinuous to continuous mode. Data is 36 mV) 8-->(error threshold to go from discontinuous to continuous mode. Data is 40 mV) 9-->(error threshold to go from discontinuous to continuous mode. Data is 44 mV) 10-->(error threshold to go from discontinuous to continuous mode. Data is 48 mV) 11-->(error threshold to go from discontinuous to continuous mode. Data is 52 mV) 12-->(error threshold to go from discontinuous to continuous mode. Data is 56 mV) 13-->(error threshold to go from discontinuous to continuous mode. Data is 60 mV) 14-->(error threshold to go from discontinuous to continuous mode. Data is 64 mV) 15--> (Disabled)	09 (9)

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
auto_ps_mode (Enables automatic power state mode.)	D0 0832 [4:4]	LOOP2	0-->(Disable automatic power state mode.) 1-->(Enables automatic power state mode.)	0
inductor_ni_thresh (Total current threshold below which it is assumed that the inductor current has a negative component. Resolution=1/4 A.)	D0 0840[5:0]	LOOP2	inductor_ni_thresh: 0 --> 0A 16 --> 4A 32 --> 8A 48 -->12A 1 --> 0.25A 17 --> 4.25A 33 --> 8.25A 49 -->12.25A 2 --> 0.5A 18 --> 4.5A 34 --> 8.5A 50 -->12.5A 3 --> 0.75A 19 --> 4.75A 35 --> 8.75A 51 -->12.75A 4 --> 1A 20 --> 5A 36 --> 9A 52 -->13A 5 --> 1.25A 21 --> 5.25A 37 --> 9.25A 53 -->13.25A 6 --> 1.5A 22 --> 5.5A 38 --> 9.5A 54 -->13.5A 7 --> 1.75A 23 --> 5.75A 39 --> 9.75A 55 -->13.75A 8 --> 2A 24 --> 6A 40 --> 10A 56 -->14A 9 --> 2.25A 25 --> 6.25A 41 --> 10.25A 57 -->14.25A 10 --> 2.5A 26 --> 6.5A 42 --> 10.5A 58 -->14.5A 11 --> 2.75A 27 --> 6.75A 43 --> 10.75A 59 -->14.75A 12 --> 3A 28 --> 7A 44 --> 11A 60 -->15A 13 --> 3.25A 29 --> 7.25A 45 --> 11.25A 61 -->15.25A 14 --> 3.5A 30 --> 7.5A 46 --> 11.5A 62 -->15.5A 15 --> 3.75A 31 --> 7.75A 47 --> 11.75A 63 --> 15.75A	0

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
fixed_measured_Iin_offset (2's complement offset to the measured IIN)	D0 003E [14:10]	COMMON	0 (offset IIN Current 0A) 1 (offset IIN Current 0.03125A) 31 (offset IIN Current -0.03125A) 2 (offset IIN Current 0.0625A) 30 (offset IIN Current -0.0625A) 3 (offset IIN Current 0.09375A) 29 (offset IIN Current -0.09375A) 4 (offset IIN Current 0.125A) 28 (offset IIN Current -0.125A) 5 (offset IIN Current 0.15625A) 27 (offset IIN Current-0.15625A) 6 (offset IIN Current 0.1875A) 26 (offset IIN Current -0.1875A) 7 (offset IIN Current 0.21875A) 25 (offset IIN Current -0.21875A) 8 (offset IIN Current 0.25A) 24 (offset IIN Current -0.25A) 9 (offset IIN Current 0.28125A) 23 (offset IIN Current -0.28125A) 10 (offset IIN Current 0.3125A) 22 (offset IIN Current -0.3125A) 11 (offset IIN Current 0.34375A) 21 (offset IIN Current -0.34375A) 12 (offset IIN Current 0.375A) 20 (offset IIN Current -0.375A) 13 (offset IIN Current 0.40625A) 19 (offset IIN Current -0.40625A) 14 (offset IIN Current 0.4375A) 18 (offset IIN Current -0.4375A) 15 (offset IIN Current 0.46875A) 17 (offset IIN Current -0.46875A) 16 (offset IIN Current -0.5A)	0

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
temperature_offset (Temperature offset trim. 2's complement,)	D0 043E [8:4]	LOOP1	0-->(Temperature offset trim 0 C) 16-->(Temperature offset trim -16 C) 1-->(Temperature offset trim 1 C) 17-->(Temperature offset trim -15 C) 2-->(Temperature offset trim 2 C) 18-->(Temperature offset trim -14 C) 3-->(Temperature offset trim 3 C) 19-->(Temperature offset trim -13 C) 4-->(Temperature offset trim 4 C) 20-->(Temperature offset trim -12 C) 5-->(Temperature offset trim 5 C) 21-->(Temperature offset trim -11 C) 6-->(Temperature offset trim 6 C) 22-->(Temperature offset trim -10 C) 7-->(Temperature offset trim 7 C) 23-->(Temperature offset trim -9 C) 8-->(Temperature offset trim 8 C) 24-->(Temperature offset trim -8 C) 9-->(Temperature offset trim 9 C) 25-->(Temperature offset trim -7 C) 10-->(Temperature offset trim 10 C) 26-->(Temperature offset trim -6 C) 11-->(Temperature offset trim 11 C) 27-->(Temperature offset trim -5 C) 12-->(Temperature offset trim 12 C) 28-->(Temperature offset trim -4 C) 13-->(Temperature offset trim 13 C) 29-->(Temperature offset trim -3 C) 14-->(Temperature offset trim 14 C) 30-->(Temperature offset trim -2 C)	0

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or	Description, Range	Default Value
lin_per_phase_offset (A signed per-phase offset to adjust the estimated input current. Q = 1/128 A. 2's complement)	D0 0444 [12:8]	LOOP1	0-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0A) 1-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.008 A) 2-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.016 A) 3-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.023A) 4-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.031 A) 5-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.039 A) 6-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.047A) 7-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.055 A) 8-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.063 A) 9-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.070A) 10-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.078 A) 11-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.086 A) 12-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.094A) 13-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.102 A) 14-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.109 A) 15-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.117A) 16-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.125 A) 17-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.117 A) 18-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.109A) 19-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.102 A) 20-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.094 A) 21-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.086A) 22-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.078 A) 23-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.070 A) 24-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.063A) 25-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.055A) 26-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.047 A) 27-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.039 A) 28-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.031 A) 29-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.023A) 30-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.016 A) 31-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.008 A)	0

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
fixed_lin_offset (A fixed offset (2's complement) to adjust the estimated input current. Q = 1/32 A. 2's complement)	D0 0444 [4:0]	LOOP1	A fixed offset (2's complement) to adjust the estimated input current: 0-->(A fixed offset is 0A) 16-->(A fixed offset is -0.5A) 1-->(A fixed offset is 0.031A) 17-->(A fixed offset is -0.469A) 2-->(A fixed offset is 0.063A) 18-->(A fixed offset is -0.438A) 3-->(A fixed offset is 0.094A) 19-->(A fixed offset is -0.406A) 4-->(A fixed offset is 0.125A) 20-->(A fixed offset is -0.375A) 5-->(A fixed offset is 0.156A) 21-->(A fixed offset is -0.344A) 6-->(A fixed offset is 0.188A) 22-->(A fixed offset is -0.313A) 7-->(A fixed offset is 0.219A) 23-->(A fixed offset is -0.281A) 8-->(A fixed offset is 0.250A) 24-->(A fixed offset is -0.250A) 9-->(A fixed offset is 0.281A) 25-->(A fixed offset is -0.219A) 10-->(A fixed offset is 0.313A) 26-->(A fixed offset is -0.188A) 11-->(A fixed offset is 0.344A) 27-->(A fixed offset is -0.156A) 12-->(A fixed offset is 0.375A) 28-->(A fixed offset is -0.125A) 13-->(A fixed offset is 0.406A) 29-->(A fixed offset is -0.094A) 14-->(A fixed offset is 0.438A) 30-->(A fixed offset is -0.063A) 15-->(A fixed offset is 0.469A) 31-->(A fixed offset is -0.031A)	0

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
temperature_offset (Temperature offset trim. 2's comple-ment,)	D0 083E [8:4]	LOOP2	0-->(Temperature offset trim 0 °C) 16-->(Temperature offset trim -16 °C) 1-->(Temperature offset trim 1 °C) 17-->(Temperature offset trim -15 °C) 2-->(Temperature offset trim 2 °C) 18-->(Temperature offset trim -14 °C) 3-->(Temperature offset trim 3 °C) 19-->(Temperature offset trim -13 °C) 4-->(Temperature offset trim 4 °C) 20-->(Temperature offset trim -12 °C) 5-->(Temperature offset trim 5 °C) 21-->(Temperature offset trim -11 °C) 6-->(Temperature offset trim 6 °C) 22-->(Temperature offset trim -10 °C) 7-->(Temperature offset trim 7 °C) 23-->(Temperature offset trim -9 °C) 8-->(Temperature offset trim 8 °C) 24-->(Temperature offset trim -8 °C) 9-->(Temperature offset trim 9 °C) 25-->(Temperature offset trim -7 °C) 10-->(Temperature offset trim 10 °C) 26-->(Temperature offset trim -6 °C) 11-->(Temperature offset trim 11 °C) 27-->(Temperature offset trim -5 °C) 12-->(Temperature offset trim 12 °C) 28-->(Temperature offset trim -4 °C) 13-->(Temperature offset trim 13 °C) 29-->(Temperature offset trim -3 °C) 14-->(Temperature offset trim 14 °C) 30-->(Temperature offset trim -2 °C) 15-->(Temperature offset trim 15 °C) 31-->(Temperature offset trim -1 °C)	0

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
lin_per_phase_offset (A signed per-phase offset to adjust the estimated input current)	D0 0844 [12:8]	LOOP2	0-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0A) 1-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.008 A) 2-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.016 A) 3-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.023A) 4-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.031 A) 5-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.039 A) 6-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.047A) 7-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.055 A) 8-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.063 A) 9-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.070A) 10-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.078 A) 11-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.086 A) 12-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.094A) 13-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.102 A) 14-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.109 A) 15-->(A signed per-phase offset to adjust the estimated input current 1/128 data is 0.117A) 16-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.125 A) 17-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.117 A) 18-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.109A) 19-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.102 A) 20-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.094 A) 21-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.086A) 22-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.078 A) 23-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.070 A) 24-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.063A) 25-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.055A) 26-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.047 A) 27-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.039 A) 28-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.031 A) 29-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.023A) 30-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.016 A) 31-->(A signed per-phase offset to adjust the estimated input current 1/128 data is -0.008 A)	0

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
fixed_lin_offset (A fixed offset (2's complement) to adjust the estimated input current. Q = 1/32 A. 2's complement)	D0 0844 [4:0]	LOOP2	A fixed offset (2's complement) to adjust the estimated input current: 0-->(A fixed offset is 0A) 16-->(A fixed offset is -0.5A) 1-->(A fixed offset is 0.031A) 17-->(A fixed offset is -0.469A) 2-->(A fixed offset is 0.063A) 18-->(A fixed offset is -0.438A) 3-->(A fixed offset is 0.094A) 19-->(A fixed offset is -0.406A) 4-->(A fixed offset is 0.125A) 20-->(A fixed offset is -0.375A) 5-->(A fixed offset is 0.156A) 21-->(A fixed offset is -0.344A) 6-->(A fixed offset is 0.188A) 22-->(A fixed offset is -0.313A) 7-->(A fixed offset is 0.219A) 23-->(A fixed offset is -0.281A) 8-->(A fixed offset is 0.250A) 24-->(A fixed offset is -0.250A) 9-->(A fixed offset is 0.281A) 25-->(A fixed offset is -0.219A) 10-->(A fixed offset is 0.313A) 26-->(A fixed offset is -0.188A) 11-->(A fixed offset is 0.344A) 27-->(A fixed offset is -0.156A) 12-->(A fixed offset is 0.375A) 28-->(A fixed offset is -0.125A) 13-->(A fixed offset is 0.406A) 29-->(A fixed offset is -0.094A) 14-->(A fixed offset is 0.438A) 30-->(A fixed offset is -0.063A) 15-->(A fixed offset is 0.469A) 31-->(A fixed offset is -0.031A)	0
I²C_device_addr (Sets the I2C device address. If set to 0, the I2C interface is effectively disabled. In test mode, the chip also accepts a default value of 0x14. Locked by register i2c_pmb_addr_lock)	D0 0020 [14:8]	COMMON	Sets the I²C device address. If set to 0, the I²C interface is effectively disabled. In test mode, the chip also accepts a default value of 0x14. Locked by register I²C_pmb_addr_lock. Reserved I²C addresses:(0x00 to 0x07), 0x08, 0x0c, 0x28, 0x37, 0x61, (0x78 to 0x7F).	10 (16)
pmb_device_addr (Sets the PMBus device address. If set to 0, the PMBus interface is effectivelydisabled)	D0 0020 [6:0]	COMMON	Set this bit to lock I²C and PMBus address registers 0-->Unlock I²C and PMBus address 1-->Lock I²Cand PMBus address	40 (64)
I²C/PMBUS Adress lock (Set this bit to lock I2C and PMBus address registers)	D0 0094 [2:2]	COMMON	Set this bit to lock I²C and PMBus address registers 0-->Unlock I²C and PMBus address 1-->Lock I²C and PMBus address	01 (1)

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
isns_user_gain_phase_1 (High-speed ADC user settable gain for phase 1. This is added to isns_gain_trim. Resolution:[s-1.7]. 2's complement)	D0 0044 [13:8]	COMMON	High speed ADC user settable gain for phase 1: 0-->(gain for phase1: 0) 63-->(gain for phase -0.78 %) 1-->(gain for phase1: 0.78%) 62-->(gain for phase -1.56 %) 2-->(gain for phase 1.56 %) 61-->(gain for phase -2.34 %) 3-->(gain for phase 2.34 %) 60-->(gain for phase -3.13 %) 4-->(gain for phase 3.13 %) 59-->(gain for phase -3.91 %) 5-->(gain for phase 3.91 %) 58-->(gain for phase -4.69 %) 6-->(gain for phase 4.69 %) 57-->(gain for phase -5.47 %) 7-->(gain for phase 5.47 %) 56-->(gain for phase -6.25 %) 8-->(gain for phase 6.25 %) 55-->(gain for phase -7.03 %) 9-->(gain for phase 7.03 %) 54-->(gain for phase -7.81 %) 10-->(gain for phase 7.81 %) 53-->(gain for phase -8.59 %) 11-->(gain for phase 8.59 %) 52-->(gain for phase -9.38 %) 12-->(gain for phase 9.38 %) 51-->(gain for phase -10.16 %) 13-->(gain for phase 10.16 %) 50-->(gain for phase -10.94 %) 14-->(gain for phase 10.94 %) 49-->(gain for phase -11.72 %) 15-->(gain for phase 11.72 %) 48-->(gain for phase -12.50 %) 16-->(gain for phase 12.50 %) 47-->(gain for phase -13.28 %) 17-->(gain for phase 13.28 %) 46-->(gain for phase -14.06 %) 18-->(gain for phase 14.06 %) 45-->(gain for phase -14.84 %) 19-->(gain for phase 14.84 %) 44-->(gain for phase -15.63 %) 20-->(gain for phase 15.63 %) 43-->(gain for phase -16.41 %) 21-->(gain for phase 16.41 %) 42-->(gain for phase -17.19 %) 22-->(gain for phase 17.19 %) 41-->(gain for phase -17.97 %) 23-->(gain for phase 17.97 %) 40-->(gain for phase -18.75 %) 24-->(gain for phase 18.75 %) 39-->(gain for phase -19.53 %) 25-->(gain for phase 19.53 %) 38-->(gain for phase -20.31 %) 26-->(gain for phase 20.31 %) 37-->(gain for phase -21.09 %) 27-->(gain for phase 21.09 %) 36-->(gain for phase -21.88 %) 28-->(gain for phase 21.88 %) 35-->(gain for phase -22.66 %) 29-->(gain for phase 22.66 %) 34-->(gain for phase -23.44 %) 30-->(gain for phase 23.44 %) 33-->(gain for phase -24.22 %) 31-->(gain for phase 24.22 %) 32-->(gain for phase -25.00 %)	Varies

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
isns_user_gain_phase_2 (High-speed ADC user settable gain for phase 2. This is added to isns_gain_trim. Resolution:[s-1.7]. 2's complement)	D0 0044 [5:0]	COMMON	High speed ADC user settable gain for phase 2: 0-->(gain for phase1: 0) 63-->(gain for phase -0.78 %) 1-->(gain for phase1: 0.78 %) 62-->(gain for phase -1.56 %) 2-->(gain for phase 1.56 %) 61-->(gain for phase -2.34 %) 3-->(gain for phase 2.34 %) 60-->(gain for phase -3.13 %) 4-->(gain for phase 3.13 %) 59-->(gain for phase -3.91 %) 5-->(gain for phase 3.91 %) 58-->(gain for phase -4.69 %) 6-->(gain for phase 4.69 %) 57-->(gain for phase -5.47 %) 7-->(gain for phase 5.47 %) 56-->(gain for phase -6.25 %) 8-->(gain for phase 6.25 %) 55-->(gain for phase -7.03 %) 9-->(gain for phase 7.03 %) 54-->(gain for phase -7.81 %) 10-->(gain for phase 7.81 %) 53-->(gain for phase -8.59 %) 11-->(gain for phase 8.59 %) 52-->(gain for phase -9.38 %) 12-->(gain for phase 9.38 %) 51-->(gain for phase -10.16 %) 13-->(gain for phase 10.16 %) 50-->(gain for phase -10.94 %) 14-->(gain for phase 10.94 %) 49-->(gain for phase -11.72 %) 15-->(gain for phase 11.72 %) 48-->(gain for phase -12.50 %) 16-->(gain for phase 12.50 %) 47-->(gain for phase -13.28 %) 17-->(gain for phase 13.28 %) 46-->(gain for phase -14.06 %) 18-->(gain for phase 14.06 %) 45-->(gain for phase -14.84 %) 19-->(gain for phase 14.84 %) 44-->(gain for phase -15.63 %) 20-->(gain for phase 15.63 %) 43-->(gain for phase -16.41 %) 21-->(gain for phase 16.41 %) 42-->(gain for phase -17.19 %) 22-->(gain for phase 17.19 %) 41-->(gain for phase -17.97 %) 23-->(gain for phase 17.97 %) 40-->(gain for phase -18.75 %) 24-->(gain for phase 18.75 %) 39-->(gain for phase -19.53 %) 25-->(gain for phase 19.53 %) 38-->(gain for phase -20.31 %) 26-->(gain for phase 20.31 %) 37-->(gain for phase -21.09 %) 27-->(gain for phase 21.09 % 36-->(gain for phase -21.88 %) 28-->(gain for phase 21.88 %) 35-->(gain for phase -22.66 %) 29-->(gain for phase 22.66 %) 34-->(gain for phase -23.44 %) 30-->(gain for phase 23.44 %) 33-->(gain for phase -24.22 %) 31-->(gain for phase 24.22 %) 32-->(gain for phase -25.00 %)	0—M40 Varies

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
isns_user_gain_phase_3 (High-speed ADC user settable gain for phase 3. This is added to isns_gain_trim. Resolution:[s-1.7]. 2's complement)	D0 0046 [13:8]	COMMON	High speed ADC user settable gain for phase 3: 0-->(gain for phase1: 0) 63-->(gain for phase -0.78 %) 1-->(gain for phase1: 0.78 %) 62-->(gain for phase -1.56 %) 2-->(gain for phase 1.56 %) 61-->(gain for phase -2.34 %) 3-->(gain for phase 2.34 %) 60-->(gain for phase -3.13 %) 4-->(gain for phase 3.13 %) 59-->(gain for phase -3.91 %) 5-->(gain for phase 3.91 %) 58-->(gain for phase -4.69 %) 6-->(gain for phase 4.69 %) 57-->(gain for phase -5.47 %) 7-->(gain for phase 5.47 %) 56-->(gain for phase -6.25 %) 8-->(gain for phase 6.25 %) 55-->(gain for phase -7.03 %) 9-->(gain for phase 7.03 %) 54-->(gain for phase -7.81 %) 10-->(gain for phase 7.81 %) 53-->(gain for phase -8.59 %) 11-->(gain for phase 8.59 %) 52-->(gain for phase -9.38 %) 12-->(gain for phase 9.38 %) 51-->(gain for phase -10.16 %) 13-->(gain for phase 10.16 %) 50-->(gain for phase -10.94 %) 14-->(gain for phase 10.94 %) 49-->(gain for phase -11.72 %) 15-->(gain for phase 11.72 %) 48-->(gain for phase -12.50 %) 16-->(gain for phase 12.50 %) 47-->(gain for phase -13.28 %) 17-->(gain for phase 13.28 %) 46-->(gain for phase -14.06 %) 18-->(gain for phase 14.06 %) 45-->(gain for phase -14.84 %) 19-->(gain for phase 14.84 %) 44-->(gain for phase -15.63 %) 20-->(gain for phase 15.63 %) 43-->(gain for phase -16.41 %) 21-->(gain for phase 16.41 %) 42-->(gain for phase -17.19 %) 22-->(gain for phase 17.19 %) 41-->(gain for phase -17.97 %) 23-->(gain for phase 17.97 %) 40-->(gain for phase -18.75 %) 24-->(gain for phase 18.75 %) 39-->(gain for phase -19.53 %) 25-->(gain for phase 19.53 %) 38-->(gain for phase -20.31 %) 26-->(gain for phase 20.31 %) 37-->(gain for phase -21.09 %) 27-->(gain for phase 21.09 %) 36-->(gain for phase -21.88 %) 28-->(gain for phase 21.88 %) 35-->(gain for phase -22.66 %) 29-->(gain for phase 22.66 %) 34-->(gain for phase -23.44 %) 30-->(gain for phase 23.44 %) 33-->(gain for phase -24.22 %) 31-->(gain for phase 24.22 %) 32-->(gain for phase -25.00 %)	0–M40,M80 Rest—Varies

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
isns_user_gain_phase_4 (High-speed ADC user settable gain for phase 4. This is added to isns_gain_trim. Resolution:[s -1.7]. 2's complement)	D0 0046 [5:0]	COMMON	High speed ADC user settable gain for phase 4: 0-->(gain for phase1: 0) 63-->(gain for phase -0.78 %) 1-->(gain for phase1: 0.78 %) 62-->(gain for phase -1.56 %) 2-->(gain for phase 1.56 %) 61-->(gain for phase -2.34 %) 3-->(gain for phase 2.34 %) 60-->(gain for phase -3.13 %) 4-->(gain for phase 3.13 %) 59-->(gain for phase -3.91 %) 5-->(gain for phase 3.91 %) 58-->(gain for phase -4.69 %) 6-->(gain for phase 4.69 %) 57-->(gain for phase -5.47 %) 7-->(gain for phase 5.47 %) 56-->(gain for phase -6.25 %) 8-->(gain for phase 6.25 %) 55-->(gain for phase -7.03 %) 9-->(gain for phase 7.03 %) 54-->(gain for phase -7.81 %) 10-->(gain for phase 7.81 %) 53-->(gain for phase -8.59 %) 11-->(gain for phase 8.59 %) 52-->(gain for phase -9.38 %) 12-->(gain for phase 9.38 %) 51-->(gain for phase -10.16 %) 13-->(gain for phase 10.16 %) 50-->(gain for phase -10.94 %) 14-->(gain for phase 10.94 %) 49-->(gain for phase -11.72 %) 15-->(gain for phase 11.72 %) 48-->(gain for phase -12.50 %) 16-->(gain for phase 12.50 %) 47-->(gain for phase -13.28 %) 17-->(gain for phase 13.28 %) 46-->(gain for phase -14.06 %) 18-->(gain for phase 14.06 %) 45-->(gain for phase -14.84 %) 19-->(gain for phase 14.84 %) 44-->(gain for phase -15.63 %) 20-->(gain for phase 15.63 %) 43-->(gain for phase -16.41 %) 21-->(gain for phase 16.41 %) 42-->(gain for phase -17.19 %) 22-->(gain for phase 17.19 %) 41-->(gain for phase -17.97 %) 23-->(gain for phase 17.97 %) 40-->(gain for phase -18.75 %) 24-->(gain for phase 18.75 %) 39-->(gain for phase -19.53 %) 25-->(gain for phase 19.53 %) 38-->(gain for phase -20.31 %) 26-->(gain for phase 20.31 %) 37-->(gain for phase -21.09 %) 27-->(gain for phase 21.09 %) 36-->(gain for phase -21.88 %) 28-->(gain for phase 21.88 %) 35-->(gain for phase -22.66 %) 29-->(gain for phase 22.66 %) 34-->(gain for phase -23.44 %) 30-->(gain for phase 23.44 %) 33-->(gain for phase -24.22 %) 31-->(gain for phase 24.22 %) 32-->(gain for phase -25.00 %))	0 – M40,M80,M120 Rest – varies

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
isns_user_gain_phase_5 (High-speed ADC user settable gain for phase 5. This is added to isns_gain_trim. Resolution:[s-1.7]. 2's complement)	D0 0048 [13:8]	COMMON	High speed ADC user settable gain for phase 5: 0-->(gain for phase1: 0) 63-->(gain for phase -0.78 %) 1-->(gain for phase1: 0.78 %) 62-->(gain for phase -1.56 %) 2-->(gain for phase 1.56 %) 61-->(gain for phase -2.34 %) 3-->(gain for phase 2.34 %) 60-->(gain for phase -3.13 %) 4-->(gain for phase 3.13 %) 59-->(gain for phase -3.91 %) 5-->(gain for phase 3.91 %) 58-->(gain for phase -4.69 %) 6-->(gain for phase 4.69 %) 57-->(gain for phase -5.47 %) 7-->(gain for phase 5.47 %) 56-->(gain for phase -6.25 %) 8-->(gain for phase 6.25 %) 55-->(gain for phase -7.03 %) 9-->(gain for phase 7.03 %) 54-->(gain for phase -7.81 %) 10-->(gain for phase 7.81 %) 53-->(gain for phase -8.59 %) 11-->(gain for phase 8.59 %) 52-->(gain for phase -9.38 %) 12-->(gain for phase 9.38 %) 51-->(gain for phase -10.16 %) 13-->(gain for phase 10.16 %) 50-->(gain for phase -10.94 %) 14-->(gain for phase 10.94 %) 49-->(gain for phase -11.72 %) 15-->(gain for phase 11.72 %) 48-->(gain for phase -12.50 %) 16-->(gain for phase 12.50 %) 47-->(gain for phase -13.28 %) 17-->(gain for phase 13.28 %) 46-->(gain for phase -14.06 %) 18-->(gain for phase 14.06 %) 45-->(gain for phase -14.84 %) 19-->(gain for phase 14.84 %) 44-->(gain for phase -15.63 %) 20-->(gain for phase 15.63 %) 43-->(gain for phase -16.41 %) 21-->(gain for phase 16.41 %) 42-->(gain for phase -17.19 %) 22-->(gain for phase 17.19 %) 41-->(gain for phase -17.97 %) 23-->(gain for phase 17.97 %) 40-->(gain for phase -18.75 %) 24-->(gain for phase 18.75 %) 39-->(gain for phase -19.53 %) 25-->(gain for phase 19.53 %) 38-->(gain for phase -20.31 %) 26-->(gain for phase 20.31 %) 37-->(gain for phase -21.09 %) 27-->(gain for phase 21.09 %) 36-->(gain for phase -21.88 %) 28-->(gain for phase 21.88 %) 35-->(gain for phase -22.66 %) 29-->(gain for phase 22.66 %) 34-->(gain for phase -23.44 %) 30-->(gain for phase 23.44 %) 33-->(gain for phase -24.22 %) 31-->(gain for phase 24.22 %) 32-->(gain for phase -25.00 %)	0—M40,M80,M120,M160 Rest Varies

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
isns_user_gain_phase_6 (High-speed ADC user settable gain for phase 6. This is added to isns_gain_trim. Resolution:[s-1.7]. 2's complement.)	D0 0048 [5:0]	COMMON	High speed ADC user settable gain for phase 6: 0-->(gain for phase1: 0) 63-->(gain for phase -0.78 %) 1-->(gain for phase1: 0.78 %) 62-->(gain for phase -1.56 %) 2-->(gain for phase 1.56 %) 61-->(gain for phase -2.34 %) 3-->(gain for phase 2.34 %) 60-->(gain for phase -3.13 %) 4-->(gain for phase 3.13 %) 59-->(gain for phase -3.91 %) 5-->(gain for phase 3.91 %) 58-->(gain for phase -4.69 %) 6-->(gain for phase 4.69 %) 57-->(gain for phase -5.47 %) 7-->(gain for phase 5.47 %) 56-->(gain for phase -6.25 %) 8-->(gain for phase 6.25 %) 55-->(gain for phase -7.03 %) 9-->(gain for phase 7.03 %) 54-->(gain for phase -7.81 %) 10-->(gain for phase 7.81 %) 53-->(gain for phase -8.59 %) 11-->(gain for phase 8.59 %) 52-->(gain for phase -9.38 %) 12-->(gain for phase 9.38 %) 51-->(gain for phase -10.16 %) 13-->(gain for phase 10.16 %) 50-->(gain for phase -10.94 %) 14-->(gain for phase 10.94 %) 49-->(gain for phase -11.72 %) 15-->(gain for phase 11.72 %) 48-->(gain for phase -12.50 %) 16-->(gain for phase 12.50 %) 47-->(gain for phase -13.28 %) 17-->(gain for phase 13.28 %) 46-->(gain for phase -14.06 %) 18-->(gain for phase 14.06 %) 45-->(gain for phase -14.84 %) 19-->(gain for phase 14.84 %) 44-->(gain for phase -15.63 %) 20-->(gain for phase 15.63 %) 43-->(gain for phase -16.41 %) 21-->(gain for phase 16.41 %) 42-->(gain for phase -17.19 %) 22-->(gain for phase 17.19 %) 41-->(gain for phase -17.97 %) 23-->(gain for phase 17.97 %) 40-->(gain for phase -18.75 %) 24-->(gain for phase 18.75 %) 39-->(gain for phase -19.53 %) 25-->(gain for phase 19.53 %) 38-->(gain for phase -20.31 %) 26-->(gain for phase 20.31 %) 37-->(gain for phase -21.09 %) 27-->(gain for phase 21.09 %) 36-->(gain for phase -21.88 %) 28-->(gain for phase 21.88 %) 35-->(gain for phase -22.66 %) 29-->(gain for phase 22.66 %) 34-->(gain for phase -23.44 %) 30-->(gain for phase 23.44 %) 33-->(gain for phase -24.22 %) 31-->(gain for phase 24.22 %) 32-->(gain for phase -25.00 %)	0—M40,M80,M120,M160 Rest—Varies

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
isns_user_gain_phase_7 (High-speed ADC user settable gain for phase 7. This is added to isns_gain_trim. Resolution:[s -1.7]. 2's complement)	D0 004A [13:8]	COMMON	High speed ADC user settable gain for phase 7: 0-->(gain for phase1: 0) 63-->(gain for phase -0.78 %) 1-->(gain for phase1: 0.78 %) 62-->(gain for phase -1.56 %) 2-->(gain for phase 1.56 %) 61-->(gain for phase -2.34 %) 3-->(gain for phase 2.34 %) 60-->(gain for phase -3.13 %) 4-->(gain for phase 3.13 %) 59-->(gain for phase -3.91 %) 5-->(gain for phase 3.91 %) 58-->(gain for phase -4.69 %) 6-->(gain for phase 4.69 %) 57-->(gain for phase -5.47 %) 7-->(gain for phase 5.47 %) 56-->(gain for phase -6.25 %) 8-->(gain for phase 6.25 %) 55-->(gain for phase -7.03 %) 9-->(gain for phase 7.03 %) 54-->(gain for phase -7.81 %) 10-->(gain for phase 7.81 %) 53-->(gain for phase -8.59 %) 11-->(gain for phase 8.59 %) 52-->(gain for phase -9.38 %) 12-->(gain for phase 9.38 %) 51-->(gain for phase -10.16 %) 13-->(gain for phase 10.16 %) 50-->(gain for phase -10.94 %) 14-->(gain for phase 10.94 %) 49-->(gain for phase -11.72 %) 15-->(gain for phase 11.72 %) 48-->(gain for phase -12.50 %) 16-->(gain for phase 12.50 %) 47-->(gain for phase -13.28 %) 17-->(gain for phase 13.28 %) 46-->(gain for phase -14.06 %) 18-->(gain for phase 14.06 %) 45-->(gain for phase -14.84 %) 19-->(gain for phase 14.84 %) 44-->(gain for phase -15.63 %) 20-->(gain for phase 15.63 %) 43-->(gain for phase -16.41 %) 21-->(gain for phase 16.41 %) 42-->(gain for phase -17.19 %) 22-->(gain for phase 17.19 %) 41-->(gain for phase -17.97 %) 23-->(gain for phase 17.97 %) 40-->(gain for phase -18.75 %) 24-->(gain for phase 18.75 %) 39-->(gain for phase -19.53 %) 25-->(gain for phase 19.53 %) 38-->(gain for phase -20.31 %) 26-->(gain for phase 20.31 %) 37-->(gain for phase -21.09 %) 27-->(gain for phase 21.09 %) 36-->(gain for phase -21.88 %) 28-->(gain for phase 21.88 %) 35-->(gain for phase -22.66 %) 29-->(gain for phase 22.66 %) 34-->(gain for phase -23.44 %) 30-->(gain for phase 23.44 %) 33-->(gain for phase -24.22 %) 31-->(gain for phase 24.22 %) 32-->(gain for phase -25.00 %)	0—M40,M80,M120,M160 Rest—Varies

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
isns_user_gain_phase_8 (High-speed ADC user settable gain for phase 8. This is added to isns_gain_trim. Resolution:[s-1.7]. 2's complement.)	D0 004A [5:0]	COMMON	High speed ADC user settable gain for phase 8: 0-->(gain for phase1: 0) 63-->(gain for phase -0.78 %) 1-->(gain for phase1: 0.78 %) 62-->(gain for phase -1.56 %) 2-->(gain for phase 1.56 %) 61-->(gain for phase -2.34 %) 3-->(gain for phase 2.34 %) 60-->(gain for phase -3.13 %) 4-->(gain for phase 3.13 %) 59-->(gain for phase -3.91 %) 5-->(gain for phase 3.91 %) 58-->(gain for phase -4.69 %) 6-->(gain for phase 4.69 %) 57-->(gain for phase -5.47 %) 7-->(gain for phase 5.47 %) 56-->(gain for phase -6.25 %) 8-->(gain for phase 6.25 %) 55-->(gain for phase -7.03 %) 9-->(gain for phase 7.03 %) 54-->(gain for phase -7.81 %) 10-->(gain for phase 7.81 %) 53-->(gain for phase -8.59 %) 11-->(gain for phase 8.59 %) 52-->(gain for phase -9.38 %) 12-->(gain for phase 9.38 %) 51-->(gain for phase -10.16 %) 13-->(gain for phase 10.16 %) 50-->(gain for phase -10.94 %) 14-->(gain for phase 10.94 %) 49-->(gain for phase -11.72 %) 15-->(gain for phase 11.72 %) 48-->(gain for phase -12.50 %) 16-->(gain for phase 12.50 %) 47-->(gain for phase -13.28 % 17-->(gain for phase 13.28 %) 46-->(gain for phase -14.06 %) 18-->(gain for phase 14.06 %) 45-->(gain for phase -14.84 %) 19-->(gain for phase 14.84 %) 44-->(gain for phase -15.63 %) 20-->(gain for phase 15.63 %) 43-->(gain for phase -16.41 %) 21-->(gain for phase 16.41 %) 42-->(gain for phase -17.19 %) 22-->(gain for phase 17.19 %) 41-->(gain for phase -17.97 %) 23-->(gain for phase 17.97 %) 40-->(gain for phase -18.75 %) 24-->(gain for phase 18.75 %) 39-->(gain for phase -19.53 %) 25-->(gain for phase 19.53 %) 38-->(gain for phase -20.31 %) 26-->(gain for phase 20.31 %) 37-->(gain for phase -21.09 %) 27-->(gain for phase 21.09 %) 36-->(gain for phase -21.88 %) 28-->(gain for phase 21.88 %) 35-->(gain for phase -22.66 %) 29-->(gain for phase 22.66 %) 34-->(gain for phase -23.44 %) 30-->(gain for phase 23.44 %) 33-->(gain for phase -24.22 %) 31-->(gain for phase 24.22 %) 32-->(gain for phase -25.00 %)	0—M40,M80, M120,M160 Rest—Varies

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
ph1_current_offset (Offset to the measured phase current. Q= 1/4 A. 2's complement)	D0 004C [13:8]	COMMON	Offset to the measured phase 1 current: 0-->(offset for phase 0A) 63-->(offset for phase -0.25A) 1-->(offset for phase 0.25A) 62-->(offset for phase -0.5A) 2-->(offset for phase 0.5A) 61-->(offset for phase -0.75A) 3-->(offset for phase 0.75A) 60-->(offset for phase -1.0A) 4-->(offset for phase 1.0A) 59-->(offset for phase -1.25A) 5-->(offset for phase 1.25A) 58-->(offset for phase -1.5A) 6-->(offset for phase 1.5A) 57-->(offset for phase -1.75A) 7-->(offset for phase 1.75A%) 56-->(offset for phase -2.0A) 8-->(offset for phase 2.0A) 55-->(offset for phase -2.25A) 9-->(offset for phase 2.25A) 54-->(offset for phase -2.5A) 10-->(offset for phase 2.5A) 53-->(offset for phase -2.75A) 11-->(offset for phase 2.75A) 52-->(offset for phase -3.0A) 12-->(offset for phase 3.0A) 51-->(offset for phase -3.25A) 13-->(offset for phase 3.25A) 50-->(offset for phase -3.5A) 14-->(offset for phase 3.5A) 49-->(offset for phase -3.75A) 15-->(offset for phase 3.75A) 48-->(offset for phase -4.0A) 16-->(offset for phase 4.0A) 47-->(offset for phase -4.25A) 17-->(offset for phase 4.25A) 46-->(offset for phase -4.5A) 18-->(offset for phase 4.5A) 45-->(offset for phase -4.75A) 19-->(offset for phase 4.75A) 44-->(offset for phase -5.0A) 20-->(offset for phase 5.0A) 43-->(offset for phase -5.25A) 21-->(offset for phase 5.25A) 42-->(offset for phase -5.5A) 22-->(offset for phase 5.5A) 41-->(offset for phase -5.75A) 23-->(offset for phase 5.75A) 40-->(offset for phase -6.0A) 24-->(offset for phase 6.0A) 39-->(offset for phase -6.25A) 25-->(offset for phase 6.25A) 38-->(offset for phase -6.5A) 26-->(offset for phase 6.5A) 37-->(offset for phase -6.75A) 27-->(offset for phase 6.75A) 36-->(offset for phase -7.0A) 28-->(offset for phase 7.0A) 35-->(offset for phase -7.25A) 29-->(offset for phase 7.25A) 34-->(offset for phase 7.5A) 30-->(offset for phase 7.5A) 33-->(offset for phase 7.75A) 31-->(offset for phase 7.75A) 32-->(offset for phase -8.0A)	Varies

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
ph2_current_offset (Offset to the measured phase current. Q= 1/4 A. 2's complement)	D0 004C [5:0]	COMMON	Offset to the measured phase 2 current: 0-->(offset for phase 0A) 63-->(offset for phase -0.25A) 1-->(offset for phase 0.25A) 62-->(offset for phase -0.5A) 2-->(offset for phase 0.5A) 61-->(offset for phase -0.75A) 3-->(offset for phase 0.75A) 60-->(offset for phase -1.0A) 4-->(offset for phase 1.0A) 59-->(offset for phase -1.25A) 5-->(offset for phase 1.25A) 58-->(offset for phase -1.5A) 6-->(offset for phase 1.5A) 57-->(offset for phase -1.75A) 7-->(offset for phase 1.75A%) 56-->(offset for phase -2.0A) 8-->(offset for phase 2.0A) 55-->(offset for phase -2.25A) 9-->(offset for phase 2.25A) 54-->(offset for phase -2.5A) 10-->(offset for phase 2.5A) 53-->(offset for phase -2.75A) 11-->(offset for phase 2.75A) 52-->(offset for phase -3.0A) 12-->(offset for phase 3.0A) 51-->(offset for phase -3.25A) 13-->(offset for phase 3.25A) 50-->(offset for phase -3.5A) 14-->(offset for phase 3.5A) 49-->(offset for phase -3.75A) 15-->(offset for phase 3.75A) 48-->(offset for phase -4.0A) 16-->(offset for phase 4.0A) 47-->(offset for phase -4.25A) 17-->(offset for phase 4.25A) 46-->(offset for phase -4.5A) 18-->(offset for phase 4.5A) 45-->(offset for phase -4.75A) 19-->(offset for phase 4.75A) 44-->(offset for phase -5.0A) 20-->(offset for phase 5.0A) 43-->(offset for phase -5.25A) 21-->(offset for phase 5.25A) 42-->(offset for phase -5.5A) 22-->(offset for phase 5.5A) 41-->(offset for phase -5.75A) 23-->(offset for phase 5.75A) 40-->(offset for phase -6.0A) 24-->(offset for phase 6.0A) 39-->(offset for phase -6.25A) 25-->(offset for phase 6.25A) 38-->(offset for phase -6.5A) 26-->(offset for phase 6.5A) 37-->(offset for phase -6.75A) 27-->(offset for phase 6.75A) 36-->(offset for phase -7.0A) 28-->(offset for phase 7.0A) 35-->(offset for phase -7.25A) 29-->(offset for phase 7.25A) 34-->(offset for phase 7.5A) 30-->(offset for phase 7.5A) 33-->(offset for phase 7.75A) 31-->(offset for phase 7.75A) 32-->(offset for phase -8.0A)	0—M40 Varies

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
ph3_current_offset (Offset to the measured phase current. Q= 1/4 A. 2's complement)	D0 004E [13:8]	COMMON	Offset to the measured phase 3 current: 0-->(offset for phase 0A) 63-->(offset for phase -0.25A) 1-->(offset for phase 0.25A) 62-->(offset for phase -0.5A) 2-->(offset for phase 0.5A) 61-->(offset for phase -0.75A) 3-->(offset for phase 0.75A) 60-->(offset for phase -1.0A) 4-->(offset for phase 1.0A) 59-->(offset for phase -1.25A) 5-->(offset for phase 1.25A) 58-->(offset for phase -1.5A) 6-->(offset for phase 1.5A) 57-->(offset for phase -1.75A) 7-->(offset for phase 1.75A%) 56-->(offset for phase -2.0A) 8-->(offset for phase 2.0A) 55-->(offset for phase -2.25A) 9-->(offset for phase 2.25A) 54-->(offset for phase -2.5A) 10-->(offset for phase 2.5A) 53-->(offset for phase -2.75A) 11-->(offset for phase 2.75A) 52-->(offset for phase -3.0A) 12-->(offset for phase 3.0A) 51-->(offset for phase -3.25A) 13-->(offset for phase 3.25A) 50-->(offset for phase -3.5A) 14-->(offset for phase 3.5A) 49-->(offset for phase -3.75A) 15-->(offset for phase 3.75A) 48-->(offset for phase -4.0A) 16-->(offset for phase 4.0A) 47-->(offset for phase -4.25A) 17-->(offset for phase 4.25A) 46-->(offset for phase -4.5A) 18-->(offset for phase 4.5A) 45-->(offset for phase -4.75A) 19-->(offset for phase 4.75A) 44-->(offset for phase -5.0A) 20-->(offset for phase 5.0A) 43-->(offset for phase -5.25A) 21-->(offset for phase 5.25A) 42-->(offset for phase -5.5A) 22-->(offset for phase 5.5A) 41-->(offset for phase -5.75A) 23-->(offset for phase 5.75A) 40-->(offset for phase -6.0A) 24-->(offset for phase 6.0A) 39-->(offset for phase -6.25A) 25-->(offset for phase 6.25A) 38-->(offset for phase -6.5A) 26-->(offset for phase 6.5A) 37-->(offset for phase -6.75A) 27-->(offset for phase 6.75A) 36-->(offset for phase -7.0A) 28-->(offset for phase 7.0A) 35-->(offset for phase -7.25A) 29-->(offset for phase 7.25A) 34-->(offset for phase 7.5A) 30-->(offset for phase 7.5A) 33-->(offset for phase 7.75A) 31-->(offset for phase 7.75A) 32-->(offset for phase -8.0A)	0 – M40,M80 Rest—varies

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
ph4_current_offset (Offset to the measured phase current. Q= 1/4 A. 2's complement.)	D0 004E [5:0]	COMMON	Offset to the measured phase 4 current: 0-->(offset for phase 0A) 63-->(offset for phase -0.25A) 1-->(offset for phase 0.25A) 62-->(offset for phase -0.5A) 2-->(offset for phase 0.5A) 61-->(offset for phase -0.75A) 3-->(offset for phase 0.75A) 60-->(offset for phase -1.0A) 4-->(offset for phase 1.0A) 59-->(offset for phase -1.25A) 5-->(offset for phase 1.25A) 58-->(offset for phase -1.5A) 6-->(offset for phase 1.5A) 57-->(offset for phase -1.75A) 7-->(offset for phase 1.75A%) 56-->(offset for phase -2.0A) 8-->(offset for phase 2.0A) 55-->(offset for phase -2.25A) 9-->(offset for phase 2.25A) 54-->(offset for phase -2.5A) 10-->(offset for phase 2.5A) 53-->(offset for phase -2.75A) 11-->(offset for phase 2.75A) 52-->(offset for phase -3.0A) 12-->(offset for phase 3.0A) 51-->(offset for phase -3.25A) 13-->(offset for phase 3.25A) 50-->(offset for phase -3.5A) 14-->(offset for phase 3.5A) 49-->(offset for phase -3.75A) 15-->(offset for phase 3.75A) 48-->(offset for phase -4.0A) 16-->(offset for phase 4.0A) 47-->(offset for phase -4.25A) 17-->(offset for phase 4.25A) 46-->(offset for phase -4.5A) 18-->(offset for phase 4.5A) 45-->(offset for phase -4.75A) 19-->(offset for phase 4.75A) 44-->(offset for phase -5.0A) 20-->(offset for phase 5.0A) 43-->(offset for phase -5.25A) 21-->(offset for phase 5.25A) 42-->(offset for phase -5.5A) 22-->(offset for phase 5.5A) 41-->(offset for phase -5.75A) 23-->(offset for phase 5.75A) 40-->(offset for phase -6.0A) 24-->(offset for phase 6.0A) 39-->(offset for phase -6.25A) 25-->(offset for phase 6.25A) 38-->(offset for phase -6.5A) 26-->(offset for phase 6.5A) 37-->(offset for phase -6.75A) 27-->(offset for phase 6.75A) 36-->(offset for phase -7.0A) 28-->(offset for phase 7.0A) 35-->(offset for phase -7.25A) 29-->(offset for phase 7.25A) 34-->(offset for phase 7.5A) 30-->(offset for phase 7.5A) 33-->(offset for phase 7.75A) 31-->(offset for phase 7.75A) 32-->(offset for phase -8.0A)	0— M40,M80 ,M120 Rest _ varies

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
ph5_current_offset (Offset to the measured phase current. Q= 1/4 A. 2's complement)	D0 0050 [13:8]	COMMON	Offset to the measured phase 5 current: 0-->(offset for phase 0A) 63-->(offset for phase -0.25A) 1-->(offset for phase 0.25A) 62-->(offset for phase -0.5A) 2-->(offset for phase 0.5A) 61-->(offset for phase -0.75A) 3-->(offset for phase 0.75A) 60-->(offset for phase -1.0A) 4-->(offset for phase 1.0A) 59-->(offset for phase -1.25A) 5-->(offset for phase 1.25A) 58-->(offset for phase -1.5A) 6-->(offset for phase 1.5A) 57-->(offset for phase -1.75A) 7-->(offset for phase 1.75A%) 56-->(offset for phase -2.0A) 8-->(offset for phase 2.0A) 55-->(offset for phase -2.25A) 9-->(offset for phase 2.25A) 54-->(offset for phase -2.5A) 10-->(offset for phase 2.5A) 53-->(offset for phase -2.75A) 11-->(offset for phase 2.75A) 52-->(offset for phase -3.0A) 12-->(offset for phase 3.0A) 51-->(offset for phase -3.25A) 13-->(offset for phase 3.25A) 50-->(offset for phase -3.5A) 14-->(offset for phase 3.5A) 49-->(offset for phase -3.75A) 15-->(offset for phase 3.75A) 48-->(offset for phase -4.0A) 16-->(offset for phase 4.0A) 47-->(offset for phase -4.25A) 17-->(offset for phase 4.25A) 46-->(offset for phase -4.5A) 18-->(offset for phase 4.5A) 45-->(offset for phase -4.75A) 19-->(offset for phase 4.75A) 44-->(offset for phase -5.0A) 20-->(offset for phase 5.0A) 43-->(offset for phase -5.25A) 21-->(offset for phase 5.25A) 42-->(offset for phase -5.5A) 22-->(offset for phase 5.5A) 41-->(offset for phase -5.75A) 23-->(offset for phase 5.75A) 40-->(offset for phase -6.0A) 24-->(offset for phase 6.0A) 39-->(offset for phase -6.25A) 25-->(offset for phase 6.25A) 38-->(offset for phase -6.5A) 26-->(offset for phase 6.5A) 37-->(offset for phase -6.75A) 27-->(offset for phase 6.75A) 36-->(offset for phase -7.0A) 28-->(offset for phase 7.0A) 35-->(offset for phase -7.25A) 29-->(offset for phase 7.25A) 34-->(offset for phase 7.5A) 30-->(offset for phase 7.5A) 33-->(offset for phase 7.75A) 31-->(offset for phase 7.75A) 32-->(offset for phase -8.0A)	0— M40,M80, M120,M160 Rest— Varies

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
ph6_current_offset (Offset to the measured phase current. Q= 1/4 A. 2's complement)	D0 0050 [5:0]	COMMON	Offset to the measured phase 6 current: 0-->(offset for phase 0A) 63-->(offset for phase -0.25A) 1-->(offset for phase 0.25A) 62-->(offset for phase -0.5A) 2-->(offset for phase 0.5A) 61-->(offset for phase -0.75A) 3-->(offset for phase 0.75A) 60-->(offset for phase -1.0A) 4-->(offset for phase 1.0A) 59-->(offset for phase -1.25A) 5-->(offset for phase 1.25A) 58-->(offset for phase -1.5A) 6-->(offset for phase 1.5A) 57-->(offset for phase -1.75A) 7-->(offset for phase 1.75A%) 56-->(offset for phase -2.0A) 8-->(offset for phase 2.0A) 55-->(offset for phase -2.25A) 9-->(offset for phase 2.25A) 54-->(offset for phase -2.5A) 10-->(offset for phase 2.5A) 53-->(offset for phase -2.75A) 11-->(offset for phase 2.75A) 52-->(offset for phase -3.0A) 12-->(offset for phase 3.0A) 51-->(offset for phase -3.25A) 13-->(offset for phase 3.25A) 50-->(offset for phase -3.5A) 14-->(offset for phase 3.5A) 49-->(offset for phase -3.75A) 15-->(offset for phase 3.75A) 48-->(offset for phase -4.0A) 16-->(offset for phase 4.0A) 47-->(offset for phase -4.25A) 17-->(offset for phase 4.25A) 46-->(offset for phase -4.5A) 18-->(offset for phase 4.5A) 45-->(offset for phase -4.75A) 19-->(offset for phase 4.75A) 44-->(offset for phase -5.0A) 20-->(offset for phase 5.0A) 43-->(offset for phase -5.25A) 21-->(offset for phase 5.25A) 42-->(offset for phase -5.5A) 22-->(offset for phase 5.5A) 41-->(offset for phase -5.75A) 23-->(offset for phase 5.75A) 40-->(offset for phase -6.0A) 24-->(offset for phase 6.0A) 39-->(offset for phase -6.25A) 25-->(offset for phase 6.25A) 38-->(offset for phase -6.5A) 26-->(offset for phase 6.5A) 37-->(offset for phase -6.75A) 27-->(offset for phase 6.75A) 36-->(offset for phase -7.0A) 28-->(offset for phase 7.0A) 35-->(offset for phase -7.25A) 29-->(offset for phase 7.25A) 34-->(offset for phase 7.5A) 30-->(offset for phase 7.5A) 33-->(offset for phase 7.75A) 31-->(offset for phase 7.75A) 32-->(offset for phase -8.0A)	0—M40,M80,M120,M160 Rest—Varies

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
ph7_current_offset (Offset to the measured phase current. Q= 1/4 A. 2's complement)	D0 0052 [13:8]	COMMON	Offset to the measured phase 7 current: 0-->(offset for phase 0A) 63-->(offset for phase -0.25A) 1-->(offset for phase 0.25A) 62-->(offset for phase -0.5A) 2-->(offset for phase 0.5A) 61-->(offset for phase -0.75A) 3-->(offset for phase 0.75A) 60-->(offset for phase -1.0A) 4-->(offset for phase 1.0A) 59-->(offset for phase -1.25A) 5-->(offset for phase 1.25A) 58-->(offset for phase -1.5A) 6-->(offset for phase 1.5A) 57-->(offset for phase -1.75A) 7-->(offset for phase 1.75A%) 56-->(offset for phase -2.0A) 8-->(offset for phase 2.0A) 55-->(offset for phase -2.25A) 9-->(offset for phase 2.25A) 54-->(offset for phase -2.5A) 10-->(offset for phase 2.5A) 53-->(offset for phase -2.75A) 11-->(offset for phase 2.75A) 52-->(offset for phase -3.0A) 12-->(offset for phase 3.0A) 51-->(offset for phase -3.25A) 13-->(offset for phase 3.25A) 50-->(offset for phase -3.5A) 14-->(offset for phase 3.5A) 49-->(offset for phase -3.75A) 15-->(offset for phase 3.75A) 48-->(offset for phase -4.0A) 16-->(offset for phase 4.0A) 47-->(offset for phase -4.25A) 17-->(offset for phase 4.25A) 46-->(offset for phase -4.5A) 18-->(offset for phase 4.5A) 45-->(offset for phase -4.75A) 19-->(offset for phase 4.75A) 44-->(offset for phase -5.0A) 20-->(offset for phase 5.0A) 43-->(offset for phase -5.25A) 21-->(offset for phase 5.25A) 42-->(offset for phase -5.5A) 22-->(offset for phase 5.5A) 41-->(offset for phase -5.75A) 23-->(offset for phase 5.75A) 40-->(offset for phase -6.0A) 24-->(offset for phase 6.0A) 39-->(offset for phase -6.25A) 25-->(offset for phase 6.25A) 38-->(offset for phase -6.5A) 26-->(offset for phase 6.5A) 37-->(offset for phase -6.75A) 27-->(offset for phase 6.75A) 36-->(offset for phase -7.0A) 28-->(offset for phase 7.0A) 35-->(offset for phase -7.25A) 29-->(offset for phase 7.25A) 34-->(offset for phase 7.5A) 30-->(offset for phase 7.5A) 33-->(offset for phase 7.75A) 31-->(offset for phase 7.75A) 32-->(offset for phase -8.0A)	0— M40,M80, M120,M160 Rest _ Varies

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
ph8_current_offset (Offset to the measured phase current. Q= 1/4 A. 2's complement.)	D0 0052 [5:0]	COMMON	Offset to the measured phase 8 current: 0-->(offset for phase 0A) 63-->(offset for phase -0.25A) 1-->(offset for phase 0.25A) 62-->(offset for phase -0.5A) 2-->(offset for phase 0.5A) 61-->(offset for phase -0.75A) 3-->(offset for phase 0.75A) 60-->(offset for phase -1.0A) 4-->(offset for phase 1.0A) 59-->(offset for phase -1.25A) 5-->(offset for phase 1.25A) 58-->(offset for phase -1.5A) 6-->(offset for phase 1.5A) 57-->(offset for phase -1.75A) 7-->(offset for phase 1.75A%) 56-->(offset for phase -2.0A) 8-->(offset for phase 2.0A) 55-->(offset for phase -2.25A) 9-->(offset for phase 2.25A) 54-->(offset for phase -2.5A) 10-->(offset for phase 2.5A) 53-->(offset for phase -2.75A) 11-->(offset for phase 2.75A) 52-->(offset for phase -3.0A) 12-->(offset for phase 3.0A) 51-->(offset for phase -3.25A) 13-->(offset for phase 3.25A) 50-->(offset for phase -3.5A) 14-->(offset for phase 3.5A) 49-->(offset for phase -3.75A) 15-->(offset for phase 3.75A) 48-->(offset for phase -4.0A) 16-->(offset for phase 4.0A) 47-->(offset for phase -4.25A) 17-->(offset for phase 4.25A) 46-->(offset for phase -4.5A) 18-->(offset for phase 4.5A) 45-->(offset for phase -4.75A) 19-->(offset for phase 4.75A) 44-->(offset for phase -5.0A) 20-->(offset for phase 5.0A) 43-->(offset for phase -5.25A) 21-->(offset for phase 5.25A) 42-->(offset for phase -5.5A) 22-->(offset for phase 5.5A) 41-->(offset for phase -5.75A) 23-->(offset for phase 5.75A) 40-->(offset for phase -6.0A) 24-->(offset for phase 6.0A) 39-->(offset for phase -6.25A) 25-->(offset for phase 6.25A) 38-->(offset for phase -6.5A) 26-->(offset for phase 6.5A) 37-->(offset for phase -6.75A) 27-->(offset for phase 6.75A) 36-->(offset for phase -7.0A) 28-->(offset for phase 7.0A) 35-->(offset for phase -7.25A) 29-->(offset for phase 7.25A) 34-->(offset for phase 7.5A) 30-->(offset for phase 7.5A) 33-->(offset for phase 7.75A) 31-->(offset for phase 7.75A) 32-->(offset for phase -8.0A)	0— M40,M80,M120, M160 Rest _ Varies

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Off-set	Application: Common, Loop1 or Loop2	Description, Range	Default Value
Iout_Calibration_EN (Used to enter Iout Calibration process)	D0 009A [15:0]	COMMON	0--> Exit Iout Calibration 42330-->Enter Iout Calibration	0
Debug_Lock (Used to access Iout Calibration Registers)	D0 0094 [1:1]	COMMON	0--> Unlock Iout Calibration Registers 1-->Lock Iout Calibration Registers	01(1)
phase_gate (This register allows only 1 phase to operate per loop. Can be used for current sense gain trimming of each phase. This should be set when the VR is disabled)	D0 0082 [8:8]	COMMON	0-->(phase_gate Disable) 1-->(phase_gate Enable)	0
loop1_select_phase (Used to choose the 1 phase to operate in L0.)	D0 0094 [12:10]	COMMON	0-->(The 1 phase to operate in L0 , phase :1) 1->(The 1 phase to operate in L0 , phase :2) 2-->(The 1 phase to operate in L0 , phase :3) 3-->(The 1 phase to operate in L0 , phase :4) 4-->(The1 phase to operate in L0 , phase :5) 5-->(The 1 phase to operate in L0 , phase :6) 6-->(The 1 phase to operate in L0 , phase :7) 7-->(The 1 phase to operate in L0 , phase :8)	0
loop2_select_phase (Used to choose the 1 phase to operate in L1.)	D0 0094 [9:8]	COMMON	0007 (The 1 phase to operate in L1 , phase :1) 0107 (The 1 phase to operate in L1 , phase :2) 0207 (The 1 phase to operate in L1 , phase :3) 0307 (The 1 phase to operate in L1 , phase :4)	0
write_protect_mode (Select the write protection mode for the USER section of the REGMAP. write_protect_mode applies only to the USER sections. CNFG (configuration) and TRIM sections are write-protected by their respective passwords)	D0 002A [13:13]	COMMON	0-->(password) 1-->(pin/lock_forever.)	0
read_protect_mode (Select the read protection mode for the CNFG, TRIM and USER sections of the REGMAP. 0= protection is enabled by the USER password. 1= protection is always enabled (the USER password is ignored))	D0 002A [12:12]	COMMON	0-->(password) 1-->(pin/lock_forever.)	0
write_protect_selection (Select the REGMAP section to be write-protected. Writes to protected registers will be silently ignored. write_protect_section applies only to the USER sections. CNFG and TRIM sections are write-protected by their respective passwords)	D0 002A [11:10]	COMMON	0-->(No Protection) 1-->(Protect configuration) 2-->(Reserved) 3-->(Protect all)	0
read_protect_selection (Select the REGMAP section to be read-protected. Reads from protected registers return 0xFFFF. read_protect_section applies to all sections (CNFG, TRIM and USER). Note that only the USER password is used for read protection, and it applies to CNFG, TRIM and USER sections. CNFG and TRIM passwords are used for write protection only)	D0 002A [9:8]	COMMON	0-->(No Protection) 1-->(Protect configuration) 2-->(Protect all but telemetry) 3-->(Protect all)	0

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Off-set	Application: Common, Loop1 or Loop2	Description, Range	Default Value
user_password (A 16 bit password that provides read/ write protection for the USER section in all REGMAPs. Use of this password is enabled by the Protect Section and Protect Mode registers. This register resets to zero, which is the default password. Once the password is set, access protection is enabled until user_try_password is set to the same value)	D0 005C [15:0]	COMMON	Password:0 to 65535	FFFF (65535)
user_try_password (Input a 16 bit password to access proteced register/ pmbus untill user_try_password is set and matches with user_password)	D0 009C [15:0]	COMMON	Password:0 to 65535	0
d2p_enable_LVT_Thresh (Sets the input threshold level)	D0 0048 [15:15]	COMMON	0 (Sets the input threshold level TTL for the EN input pads.) 1 (Sets the input threshold level LVT for the EN input pads.)	0
en_delay_mode (Specify the sequencing of the outputs based on the VR_EN pin(s). This is only useful when the Enable pin(s) are used to control the outputs (see the PMBus ON_OFF_CONFIG command))	D0 0040 [6:4]	COMMON	0-->(Independent ENs) 1-->(Shared EN) 2-->(L1 EN -> L2) 3-->(L2 EN -> L1) 4-->(L1 PG -> L2) 5-->(L2 PG -> L1) 6-->(Off) 7-->(Off)	0
en_delay_time (Specify a startup delay for the loops.)	D0 0040 [2:0]	COMMON	0-->(Specify a startup delay for the loops 0ms.) 1-->(Specify a startup delay for the loops 0.25ms.) 2-->(Specify a startup delay for the loops 0.5ms) 3-->(Specify a startup delay for the loops 1ms) 4-->(Specify a startup delay for the loops 2.5ms) 5-->(Specify a startup delay for the loops 5ms) 6-->(Specify a startup delay for the loops 10ms) 7-->(Reserved)	0
imon_max_code (Code for IMON reference current. This register is set at 4. Imon ref current = 2^ (imon_max_code+5) A.The IMON DAC gets 512*(actual current/IMON ref current))	D0 0022 [10:8]	COMMON	0-->(Code for IMON reference current 32A.) 1-->(Code for IMON reference current 64A.) 2-->(Code for IMON reference current 128A.) 3-->(Code for IMON reference current 256A.) 4-->(Code for IMON reference current 512A.) 5-->(Code for IMON reference current 1024A.) 6-->(Code for IMON reference current 2048A.) 7-->(Code for IMON reference current 4096A.)	04 (4)

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
telemetry_bw (Telemetry bandwidth for input and output currents, input and output voltages, and temperatures)	D0 0022 [2:0]	COMMON	0-->(Telemetry bandwidth 0.81 Hz.) 1-->(Telemetry bandwidth 1.62 Hz.) 2-->(Telemetry bandwidth 3.24 Hz.) 3-->(Telemetry bandwidth 6.48 Hz.) 4-->(Telemetry bandwidth 12.96 Hz.) 5-->(Telemetry bandwidth 25.96 Hz.) 6-->(Telemetry bandwidth 52.01 Hz) 7-->(Telemetry bandwidth 104.44 HZ.)	04 (4)
loop1_read_iout_scale (Select the range/ resolution for the PMBus command READ_IOUT)	D0 0024 [7:7]	COMMON	0-->(Range: 0 to 511.5A Resolution: 0.5A.) 1-->(Range: 0 to 256A Resolution: 0.25A .)	0
fc_d (ATA differential term. Resolution is 2^3)	D0 0434 [15:12]	LOOP1	ATA differential Term: 0-->0 8-->64 1-->8 9-->72 2-->16 10-->80 3-->24 11-->88 4-->32 12-->96 5-->40 13-->104 6-->48 14-->112 7-->56 15-->120	0
fc_hth (Undershoot threshold when ATA will start. Creates large error signal when in PS0, signifying undershoot. 4 mV Q.A value of 15 disables this)	D0 0434 [11:8]	LOOP1	0-->(Undershoot threshold when ATA will start fc_hth is 0 mV) 1-->(Undershoot threshold when ATA will start fc_hth is 4 mV) 2-->(Undershoot threshold when ATA will start fc_hth is 8 mV) 3-->(Undershoot threshold when ATA will start fc_hth is 12 mV) 4-->(Undershoot threshold when ATA will start fc_hth is 16 mV) 5-->(Undershoot threshold when ATA will start fc_hth is 0 mV) 6-->(Undershoot threshold when ATA will start fc_hth is 4 mV) 7-->(Undershoot threshold when ATA will start fc_hth is 8 mV) 8-->(Undershoot threshold when ATA will start fc_hth is 12 mV) 9-->(Undershoot threshold when ATA will start fc_hth is 16 mV) 10-->(Undershoot threshold when ATA will start fc_hth is 0 mV) 11-->(Undershoot threshold when ATA will start fc_hth is 4 mV) 12-->(Undershoot threshold when ATA will start fc_hth is 8 mV) 13-->(Undershoot threshold when ATA will start fc_hth is 12 mV) 14-->(Undershoot threshold when ATA will start fc_hth is 16 mV) 15-->(Disable)	0F (15)
fc_shape (ATA response non-linear shaping term. (approx resolution is 3%))	D0 0434 [7:5]	LOOP1	0-->(ATA response non-linear shaping term 0%) 1-->(ATA response non-linear shaping term 3%) 2-->(ATA response non-linear shaping term 6%) 3-->(ATA response non-linear shaping term 9%) 4-->(ATA response non-linear shaping term 12%) 5-->(ATA response non-linear shaping term 15%) 6-->(ATA response non-linear shaping term 18%) 7-->(ATA response non-linear shaping term 21%)	0

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
fc_p (ATA proportional term (0 disable ATA). Resolution is 2^-2)	D0 0434 [4:0]	LOOP1	0-->(ATA disabled) 16-->(ATA proportional term is 4.0) 1-->(ATA proportional term is 0.25) 17-->(ATA proportional term is 4.25) 2-->(ATA proportional term is 0.5) 18-->(ATA proportional term is 4.5) 3-->(ATA proportional term is 0.75) 19-->(ATA proportional term is 4.75) 4-->(ATA proportional term is 1) 20-->(ATA proportional term is 5.0) 5-->(ATA proportional term is 1.25) 21-->(ATA proportional term is 5.25) 6-->(ATA proportional term is 1.5) 22-->(ATA proportional term is 5.5) 7-->(ATA proportional term is 1.75) 23-->(ATA proportional term is 5.75) 8-->(ATA proportional term is 2.0) 24-->(ATA proportional term is 6.0) 9-->(ATA proportional term is 2.25) 25-->(ATA proportional term is 6.25) 10-->(ATA proportional term is 2.5) 26-->(ATA proportional term is 6.5) 11-->(ATA proportional term is 2.75) 27-->(ATA proportional term is 6.75) 12-->(ATA proportional term is 3.0) 28-->(ATA proportional term is 7.0) 13-->(ATA proportional term is 3.25) 29-->(ATA proportional term is 7.25) 14-->(ATA proportional term is 3.5) 30-->(ATA proportional term is 7.5) 15-->(ATA proportional term is 3.75) 31-->(ATA proportional term is 7.75)	0
v_lift (added voltage offset during load oscillation. 2 mV Q)	D0 0438 [3:0]	LOOP1	0-->(added voltage offset during load oscillation. 2 mV Q data is 0 mV) 1-->(added voltage offset during load oscillation. 2 mV Q data is 2 mV) 2-->(added voltage offset during load oscillation. 2 mV Q data is 4 mV) 3-->(added voltage offset during load oscillation. 2 mV Q data is 6 mV) 4-->(added voltage offset during load oscillation. 2 mV Q data is 8 mV) 5-->(added voltage offset during load oscillation. 2 mV Q data is 10 mV) 6-->(added voltage offset during load oscillation. 2 mV Q data is 12 mV) 7-->(added voltage offset during load oscillation. 2 mV Q data is 14 mV) 0-->(added voltage offset during load oscillation. 2 mV Q data is 16 mV) 9-->(added voltage offset during load oscillation. 2 mV Q data is 18 mV) 10-->(added voltage offset during load oscillation. 2 mV Q data is 20 mV) 11-->(added voltage offset during load oscillation. 2 mV Q data is 22 mV) 12-->(added voltage offset during load oscillation. 2 mV Q data is 24 mV) 13-->(added voltage offset during load oscillation. 2 mV Q data is 26 mV) 14-->(added voltage offset during load oscillation. 2 mV Q data is 28 mV) 15-->(added voltage offset during load oscillation. 2 mV Q data is 30 mV)	0
db_duration (Maximum duration of diode braking = (db_duration + 1) *666ns)	D0 043A [15:13]	LOOP1	0-->(Maximum duration of diode braking ,data is 666ns) 1-->(Maximum duration of diode braking ,data is 1332 ns) 2-->(Maximum duration of diode braking ,data is 1998 ns) 3-->(Maximum duration of diode braking ,data is 2664 ns) 4-->(Maximum duration of diode braking ,data is 3330 ns) 5-->(Maximum duration of diode braking ,data is 3996 ns) 6-->(Maximum duration of diode braking ,data is 4662 ns) 7-->(Maximum duration of diode braking ,data is 5328 ns)	01 (1)

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
err_lth (Overshoot threshold beyond which PWM pulses are not issued. A value of 0 disables the feature. 4 mV Q.)	D0 043A [7:4]	LOOP1	Overshoot threshold beyond which PWM pulses are not issued: 0-->Disable 1-->4mV 2-->8mV 3-->12mV 4-->16mV 5-->20mV 6-->24mV 7-->28mV 8-->32mV 9-->36mV 10-->40mV 11-->44mV 12-->48mV 13-->52mV 14-->56mV 15-->60mV	0
fc_slope_th (slope threshold when ATA will start. 12 mV/us Q)	D0 043A [2:0]	LOOP1	0-->(slope threshold when ATA will start,data is 0mV) 1-->(slope threshold when ATA will start,data is 12mV) 2-->(slope threshold when ATA will start,data is 24mV) 3-->(slope threshold when ATA will start,data is 36mV) 4-->(slope threshold when ATA will start,data is 48mV) 5-->(slope threshold when ATA will start,data is 60mV) 6-->(slope threshold when ATA will start,data is 72mV) 7-->(slope threshold when ATA will start,data is 84mV)	07 (7)
diode_brake (During load release, enable diode braking)	D0 0440 [7:7]	LOOP1	0-->(During load release, disable diode braking.) 1-->(During load release, enable diode braking.)	0
bbrk_freq_th (load oscillation frequency below which body braking is allowed)	D0 0444 [6:5]	LOOP1	0-->(load oscillation frequency below which body braking is allowed ,data is 187.6 KHz.) 1-->(load oscillation frequency below which body braking is allowed ,data is 281.4 KHz.) 2-->(load oscillation frequency below which body braking is allowed ,data is 375.2 KHz.) 3-->(load oscillation frequency below which body braking is allowed ,data is 469 KHz.)	0
fc_d (ATA differential term. Resolution is 2^3.)	D0 0834 [15:12]	LOOP2	ATA differential Term: 0-->0 8-->64 1-->8 9-->72 2-->16 10-->80 3-->24 11-->88 4-->32 12-->96 5-->40 13-->104 6-->48 14-->112 7-->56 15-->120	0

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
fc_hth (Undershoot threshold when ATA will start. Creates large error signal when in PS0, signifying undershoot. 4 mV Q.A value of 15 disables this)	D0 0834 [11:8]	LOOP2	0-->(Undershoot threshold when ATA will start fc_hth is 0 mV) 1-->(Undershoot threshold when ATA will start fc_hth is 4 mV) 2-->(Undershoot threshold when ATA will start fc_hth is 8 mV) 3-->(Undershoot threshold when ATA will start fc_hth is 12 mV) 4-->(Undershoot threshold when ATA will start fc_hth is 16 mV) 5-->(Undershoot threshold when ATA will start fc_hth is 0 mV) 6-->(Undershoot threshold when ATA will start fc_hth is 4 mV) 7-->(Undershoot threshold when ATA will start fc_hth is 8 mV) 8-->(Undershoot threshold when ATA will start fc_hth is 12 mV) 9-->(Undershoot threshold when ATA will start fc_hth is 16 mV) 10-->(Undershoot threshold when ATA will start fc_hth is 0 mV) 11-->(Undershoot threshold when ATA will start fc_hth is 4 mV) 12-->(Undershoot threshold when ATA will start fc_hth is 8 mV) 13-->(Undershoot threshold when ATA will start fc_hth is 12 mV) 14-->(Undershoot threshold when ATA will start fc_hth is 16 mV) 15-->(Disable)	0F(15)
fc_shape (ATA response non-linear shaping term. (approx resolution is 3%).)	D0 0834 [7:5]	LOOP2	0-->(ATA response non-linear shaping term 0%) 1-->(ATA response non-linear shaping term 3%) 2-->(ATA response non-linear shaping term 6%) 3-->(ATA response non-linear shaping term 9%) 4-->(ATA response non-linear shaping term 12%) 5-->(ATA response non-linear shaping term 15%) 6-->(ATA response non-linear shaping term 18%) 7-->(ATA response non-linear shaping term 21%)	0
fc_p (ATA proportional term (0 disable ATA). Resolution is 2^-2.)	D0 0834 [4:0]	LOOP2	0-->(ATA disabled) 1-->(ATA proportional term is 0.25) 2-->(ATA proportional term is 0.5) 3-->(ATA proportional term is 0.75) 4-->(ATA proportional term is 1) 5-->(ATA proportional term is 1.25) 6-->(ATA proportional term is 1.5) 7-->(ATA proportional term is 1.75) 8-->(ATA proportional term is 2.0) 9-->(ATA proportional term is 2.25) 10-->(ATA proportional term is 2.5) 11-->(ATA proportional term is 2.75) 12-->(ATA proportional term is 3.0) 13-->(ATA proportional term is 3.25) 14-->(ATA proportional term is 3.5) 15-->(ATA proportional term is 3.75) 16-->(ATA proportional term is 4.0) 17-->(ATA proportional term is 4.25) 18-->(ATA proportional term is 4.5) 19-->(ATA proportional term is 4.75) 20-->(ATA proportional term is 5.0) 21-->(ATA proportional term is 5.25) 22-->(ATA proportional term is 5.5) 23-->(ATA proportional term is 5.75) 24-->(ATA proportional term is 6.0) 25-->(ATA proportional term is 6.25) 26-->(ATA proportional term is 6.5) 27-->(ATA proportional term is 6.75) 28-->(ATA proportional term is 7.0) 29-->(ATA proportional term is 7.25) 30-->(ATA proportional term is 7.5) 31-->(ATA proportional term is 7.75)	0

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
v_lift (added voltage offset during load oscillation. 2 mV Q)	D0 0838 [3:0]	LOOP2	0-->(added voltage offset during load oscillation. 2 mV Q data is 0 mV) 1-->(added voltage offset during load oscillation. 2 mV Q data is 2 mV) 2-->(added voltage offset during load oscillation. 2 mV Q data is 4 mV) 3-->(added voltage offset during load oscillation. 2 mV Q data is 6 mV) 4-->(added voltage offset during load oscillation. 2 mV Q data is 8 mV) 5-->(added voltage offset during load oscillation. 2 mV Q data is 10 mV) 6-->(added voltage offset during load oscillation. 2 mV Q data is 12 mV) 7-->(added voltage offset during load oscillation. 2 mV Q data is 14 mV) 0-->(added voltage offset during load oscillation. 2 mV Q data is 16 mV) 9-->(added voltage offset during load oscillation. 2 mV Q data is 18 mV) 10-->(added voltage offset during load oscillation. 2 mV Q data is 20 mV) 11-->(added voltage offset during load oscillation. 2 mV Q data is 22 mV) 12-->(added voltage offset during load oscillation. 2 mV Q data is 24 mV) 13-->(added voltage offset during load oscillation. 2 mV Q data is 26 mV) 14-->(added voltage offset during load oscillation. 2 mV Q data is 28 mV) 15-->(added voltage offset during load oscillation. 2 mV Q data is 30 mV)	0
db_duration (Maximum duration of diode braking = (db_duration + 1) *666ns.)	D0 083A [15:13]	LOOP2	0-->(Maximum duration of diode braking ,data is 666ns) 1-->(Maximum duration of diode braking ,data is 1332 ns) 2-->(Maximum duration of diode braking ,data is 1998 ns) 3-->(Maximum duration of diode braking ,data is 2664 ns) 4-->(Maximum duration of diode braking ,data is 3330 ns) 5-->(Maximum duration of diode braking ,data is 3996 ns) 6-->(Maximum duration of diode braking ,data is 4662 ns) 7-->(Maximum duration of diode braking ,data is 5328 ns)	01(1)
err_lth (Overshoot threshold beyond which PWM pulses are not issued. A value of 0 disables the feature. 4 mV Q.)	D0 083A [7:4]	LOOP2	Overshoot threshold beyond which PWM pulses are not issued: 0-->Disable 1-->4mV 2-->8mV 3-->12mV 4-->16mV 5-->20mV 6-->24mV 7-->28mV 8-->32mV 9-->36mV 10-->40mV 11-->44mV 12-->48mV 13-->52mV 14-->56mV 15-->60mV	0

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
fc_slope_th (slope threshold when ATA will start. 12 mV/us Q.)	D0 083A [2:0]	LOOP2	0-->(slope threshold when ATA will start,data is 0mV) 1-->(slope threshold when ATA will start,data is 12mV) 2-->(slope threshold when ATA will start,data is 24mV) 3-->(slope threshold when ATA will start,data is 36mV) 4-->(slope threshold when ATA will start,data is 48mV) 5-->(slope threshold when ATA will start,data is 60mV) 6-->(slope threshold when ATA will start,data is 72mV) 7-->(slope threshold when ATA will start,data is 84mV)	07(7)
diode_brake (During load release, enable diode braking.)	D0 0840 [7:7]	LOOP2	0-->(During load release, disable diode braking.) 1-->(During load release, enable diode braking.)	0
bbrk_freq_th (load oscillation frequency below which body braking is allowed)	D0 0844 [6:5]	LOOP2	0-->(load oscillation frequency below which body braking is allowed ,data is 187.6 KHz.) 1-->(load oscillation frequency below which body braking is allowed ,data is 281.4 KHz.) 2-->(load oscillation frequency below which body braking is allowed ,data is 375.2 KHz.) 3-->(load oscillation frequency below which body braking is allowed ,data is 469 KHz.)	0
tsen_fault_en (Enable TSEN fault reporting.)	D0 0420 [5:5]	LOOP1	0-->(Disable TSEN fault reporting.) 1-->(Enable TSEN fault reporting.)	0
tsen__fault_shutdown (Shutdown the output in response to a TSEN fault.)	D0 0422 [14:14]	LOOP1	0-->(Not shutdown the output in response to a TSEN fault.) 1-->(Shutdown the output in response to a TSEN fault.)	0

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
tsen_fault_en (Enable TSEN fault reporting.)	D0 0820 [5:5]	LOOP2	0-->(Disable TSEN fault reporting.) 1-->(Enable TSEN fault reporting.)	0
tsen__fault_shutdown (Shutdown the output in response to a TSEN fault.)	D0 0822 [14:14]	LOOP2	0-->(Not shutdown the output in response to a TSEN fault.) 1-->(Shutdown the output in response to a TSEN fault.)	0
loadline_bw (Load line bandwidth. Value = (loadline_bw+1)*30KHz)	D0 043A [12:8]	LOOP1	0-->30KHz 1-->60KHz 2-->90KHz 3-->120KHz 4-->150KHz 5-->180KHz 6-->210KHz 7-->340KHz 8-->270KHz 9-->300KHz 10-->330KHz 11-->360KHz 12-->390KHz 13-->420KHz 14-->450KHz 15-->480KHz 16-->510KHz 17-->540KHz 18-->570KHz 19-->600KHz 20-->630KHz 21-->660KHz 22-->690KHz 23-->720KHz 24-->750KHz 25-->780KHz 26-->810KHz 27-->840KHz 28-->870KHz 29-->900KHz 30-->930KHz 31-->960KHz	0A(10)
loadline_bw (Load line bandwidth. Value = (loadline_bw+1)*30KHz)	D0 083A [12:8]	LOOP2	0-->30KHz 1-->60KHz 2-->90KHz 3-->120KHz 4-->150KHz 5-->180KHz 6-->210KHz 7-->340KHz 8-->270KHz 9-->300KHz 10-->330KHz 11-->360KHz 12-->390KHz 13-->420KHz 14-->450KHz 15-->480KHz 16-->510KHz 17-->540KHz 18-->570KHz 19-->600KHz 20-->630KHz 21-->660KHz 22-->690KHz 23-->720KHz 24-->750KHz 25-->780KHz 26-->810KHz 27-->840KHz 28-->870KHz 29-->900KHz 30-->930KHz 31-->960KHz	0A(10)
Kp (Single-phase proportional coefficient.)	D0 0422 [13:8]	LOOP1	0-->-42.1dB 1-->-40.2dB 2-->-38.6dB 3-->-37.3dB 4-->-36.1dB 5-->-34.2dB 6-->-32.6dB 7-->-31.3dB 8-->-30.1dB 9-->-28.2dB 10-->-26.6dB 11-->-25.2dB 12-->-24.1dB 13-->-22.1dB 14-->-20.6dB 15-->-19.2dB 16-->-18.1dB 17-->-16.1dB 18-->-14.5dB 19-->-13.2dB 20-->-12dB 21-->-10.1dB 22-->-8.5dB 23-->-7.2dB 24-->-6dB 25-->-4.1dB 26-->-2.5dB 27-->-1.2dB 28-->0dB 29-->1.9dB 30-->3.5dB 31-->4.9dB 32-->6dB 33-->8dB 34-->9.5dB 35-->10.9dB 36-->12dB 37-->14dB 38-->15.6dB 39-->16.9dB 40-->18.1dB 41-->20dB 42-->21.6dB 43-->22.9dB 44-->24.1dB 45-->26dB 46-->27.6dB 47-->28.9dB 48-->30.1dB 49-->32dB 50-->33.6dB 51-->35dB 52-->36.1dB 53-->38.1dB 54-->39.6dB 55-->41dB 56-->42.1dB 57-->44.1dB 58-->45.7dB 59-->47dB 60-->48.2dB 61-->50.1dB 62-->51.7dB 63-->53dB	1C (28)

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or	Description, Range	Default Value
Ki (Single-phase integration coefficient)	D0 0422 [5:0]	LOOP1	0-->-114.4dB 1-->-112.5dB 2-->-110.9dB 3-->-109.5dB 4-->-108.4dB 5-->-106.4dB 6-->-104.8dB 7-->-103.5dB 8-->-102.4dB 9-->-100.4dB 10-->-98.8dB 11-->-97.5dB 12-->-96.3dB 13-->-94.4dB 14-->-92.8dB 15-->-91.5dB 16-->-90.3dB 17-->-88.4dB 18-->-86.8dB 19-->-85.4dB 20-->-84.3dB 21-->-82.4dB 22-->-80.8dB 23-->-79.4dB 24-->-78.3dB 25-->-76.3dB 26-->-74.7dB 27-->-73.4dB 28-->-72.2dB 29-->-70.3dB 30-->-68.7dB 31-->-67.4dB 32-->-66.2dB 33-->-64.3dB 34-->-62.7dB 35-->-61.4dB 36-->-60.2dB 37-->-58.3dB 38-->-56.7dB 39-->-55.3dB 40-->-54.2dB 41-->-52.2dB 42-->-50.7dB 43-->-49.3dB 44-->-48.2dB 45-->-46.2dB 46-->-44.6dB 47-->-43.3dB 48-->-42.1dB 49-->-40.2dB 50-->-38.6dB 51-->-37.3dB 52-->-36.1dB 53-->-34.2dB 54-->-32.6dB 55-->-31.3dB 56-->-30.1dB 57-->-28.2dB 58-->-26.6dB 59-->-25.2dB 60-->-24.1dB 61-->-22.1dB 62-->-20.6dB 63-->-19.2dB	0E (14)
Kd (Single-phase differentiation coefficient)	D0 0424 [13:8]	LOOP1	0-->-48.2dB 1-->-48.2dB 2-->-48.2dB 3-->-48.2dB 4-->-48.2dB 5-->-48.2dB 6-->-48.2dB 7-->-48.2dB 8-->-48.2dB 9-->-46.2dB 10-->-44.6dB 11-->-43.3dB 12-->-42.1dB 13-->-40.2dB 14-->-38.6dB 15-->-37.3dB 16-->-36.1dB 17-->-34.2dB 18-->-32.6dB 19-->-31.3dB 20-->-30.1dB 21-->-28.2dB 22-->-26.6dB 23-->-25.2dB 24-->-24.1dB 25-->-22.1dB 26-->-20.6dB 27-->-19.2dB 28-->-18.1dB 29-->-16.1dB 30-->-14.5dB 31-->-13.2dB 32-->-12dB 33-->-10.1dB 34-->-8.5dB 35-->-7.2dB 36-->-6dB 37-->-4.1dB 38-->-2.5dB 39-->-1.2dB 40-->0dB 41-->1.9dB 42-->3.5dB 43-->4.9dB 44-->6dB 45-->8dB 46-->9.5dB 47-->10.9dB 48-->12dB 49-->14dB 50-->15.6dB 51-->16.9dB 52-->18.1dB 53-->20dB 54-->21.6dB 55-->22.9dB 56-->24.1dB 57-->26dB 58-->27.6dB 59-->28.9dB 60-->30.1dB 61-->32dB 62-->33.6dB 63-->35dB	2F (47)

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
Kpole1 (Single-phase pole1 coefficient)	D0 0424 [7:4]	LOOP1	Single-phase pole1 coefficient ,Bandwidth: 0-->120.314kHz 1-->150.694 2-->181.198kHz 3-->211.827kHz 4-->242.583kHz 5-->304.481kHz 6-->366.904kHz 7-->429.866kHz 8-->493.381kHz 9-->622.121kHz 10-->753.244kHz 11-->886.875kHz 12-->1023.149kHz 13-->1304.22kHz 14-->1597.764kHz 15-->1905.308kHz	05 (5)
Kpole2 (Single-phase pole2 coefficient)	D0 0424 [3:0]	LOOP1	Single-phase pole2 coefficient ,Bandwidth: 0-->121.291kHz 1-->152.24kHz 2-->183.452kHz 3-->214.933kHz 4-->246.69kHz 5-->311.061kHz 6-->376.622kHz 7-->443.437kHz 8-->511.575kHz 9-->652.11kHz 10-->798.882kHz 11-->952.654kHz 12-->1114.326kHz 13-->1465.873kHz 14-->1865.066kHz 15-->2329.454kHz	07 (7)
NVM Programming	0x0064 [15:0]		If module is programmed 3 times, 0x0064[15:0]=0000h and 0x0066[15:0]=0007h If module is programmed 10 times, 0x0064[15:0]=0000h and 0x0066[15:0]=03FFh If module is programmed 22 times, 0x0064[15:0]=003Fh and 0x0066[15:0]=FFFFh	
NVM Programming2	0x0066 [15:0]			

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range		Default Value
Kp (Single-phase proportional coefficient)	D0 0822 [13:8]	LOOP2	0-->-42.1dB 1-->-40.2dB 2-->-38.6dB 3-->-37.3dB 4-->-36.1dB 5-->-34.2dB 6-->-32.6dB 7-->-31.3dB 8-->-30.1dB 9-->-28.2dB 10-->-26.6dB 11-->-25.2dB 12-->-24.1dB 13-->-22.1dB 14-->-20.6dB 15-->-19.2dB 16-->-18.1dB 17-->-16.1dB 18-->-14.5dB 19-->-13.2dB 20-->-12dB 21-->-10.1dB 22-->-8.5dB 23-->-7.2dB 24-->-6dB 25-->-4.1dB 26-->-2.5dB 27-->-1.2dB 28-->0dB 29-->1.9dB 30-->3.5dB 31-->4.9dB	32-->6dB 33-->8dB 34-->9.5dB 35-->10.9dB 36-->12dB 37-->14dB 38-->15.6dB 39-->16.9dB 40-->18.1dB 41-->20dB 42-->21.6dB 43-->22.9dB 44-->24.1dB 45-->26dB 46-->27.6dB 47-->28.9dB 48-->30.1dB 49-->32dB 50-->33.6dB 51-->35dB 52-->36.1dB 53-->38.1dB 54-->39.6dB 55-->41dB 56-->42.1dB 57-->44.1dB 58-->45.7dB 59-->47dB 60-->48.2dB 61-->50.1dB 62-->51.7dB 63-->53dB	1C (28)

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
Ki (Single-phase integration coefficient.)	D0 0822 [5:0]	LOOP2	0-->-114.4dB 1-->-112.5dB 2-->-110.9dB 3-->-109.5dB 4-->-108.4dB 5-->-106.4dB 6-->-104.8dB 7-->-103.5dB 8-->-102.4dB 9-->-100.4dB 10-->-98.8dB 11-->-97.5dB 12-->-96.3dB 13-->-94.4dB 14-->-92.8dB 15-->-91.5dB 16-->-90.3dB 17-->-88.4dB 18-->-86.8dB 19-->-85.4dB 20-->-84.3dB 21-->-82.4dB 22-->-80.8dB 23-->-79.4dB 24-->-78.3dB 25-->-76.3dB 26-->-74.7dB 27-->-73.4dB 28-->-72.2dB 29-->-70.3dB 30-->-68.7dB 31-->-67.4dB 32-->-66.2dB 33-->-64.3dB 34-->-62.7dB 35-->-61.4dB 36-->-60.2dB 37-->-58.3dB 38-->-56.7dB 39-->-55.3dB 40-->-54.2dB 41-->-52.2dB 42-->-50.7dB 43-->-49.3dB 44-->-48.2dB 45-->-46.2dB 46-->-44.6dB 47-->-43.3dB 48-->-42.1dB 49-->-40.2dB 50-->-38.6dB 51-->-37.3dB 52-->-36.1dB 53-->-34.2dB 54-->-32.6dB 55-->-31.3dB 56-->-30.1dB 57-->-28.2dB 58-->-26.6dB 59-->-25.2dB 60-->-24.1dB 61-->-22.1dB 62-->-20.6dB 63-->-19.2dB	0E (14)
Kd (Single-phase differentiation coefficient)	D0 0824 [13:8]	LOOP2	0-->-48.2dB 1-->-48.2dB 2-->-48.2dB 3-->-48.2dB 4-->-48.2dB 5-->-48.2dB 6-->-48.2dB 7-->-48.2dB 8-->-48.2dB 9-->-46.2dB 10-->-44.6dB 11-->-43.3dB 12-->-42.1dB 13-->-40.2dB 14-->-38.6dB 15-->-37.3dB 16-->-36.1dB 17-->-34.2dB 18-->-32.6dB 19-->-31.3dB 20-->-30.1dB 21-->-28.2dB 22-->-26.6dB 23-->-25.2dB 24-->-24.1dB 25-->-22.1dB 26-->-20.6dB 27-->-19.2dB 28-->-18.1dB 29-->-16.1dB 30-->-14.5dB 31-->-13.2dB 32-->-12dB 33-->-10.1dB 34-->-8.5dB 35-->-7.2dB 36-->-6dB 37-->-4.1dB 38-->-2.5dB 39-->-1.2dB 40-->0dB 41-->1.9dB 42-->3.5dB 43-->4.9dB 44-->6dB 45-->8dB 46-->9.5dB 47-->10.9dB 48-->12dB 49-->14dB 50-->15.6dB 51-->16.9dB 52-->18.1dB 53-->20dB 54-->21.6dB 55-->22.9dB 56-->24.1dB 57-->26dB 58-->27.6dB 59-->28.9dB 60-->30.1dB 61-->32dB 62-->33.6dB 63-->35dB	2F (47)

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
Kpole1 (Single-phase pole1 coefficient)	D0 0824 [7:4]	LOOP2	Single-phase pole1 coefficient ,Bandwidth: 0-->120.314kHz 1-->150.694kHz 2-->181.198kHz 3-->211.827kHz 4-->242.583kHz 5-->304.481kHz 6-->366.904kHz 7-->429.866kHz 8-->493.381kHz 9-->622.121kHz 10-->753.244kHz 11-->886.875kHz 12-->1023.149kHz 13-->1304.22kHz 14-->1597.764kHz 15-->1905.308kHz	05 (5)
Kpole2 (Single-phase pole2 coefficient.)	D0 0824 [3:0]	LOOP2	Single-phase pole2 coefficient ,Bandwidth: 0-->121.291kHz 1-->152.24kHz 2-->183.452kHz 3-->214.933kHz 4-->246.69kHz 5-->311.061kHz 6-->376.622kHz 7-->443.437kHz 8-->511.575kHz 9-->652.11kHz 10-->798.882kHz 11-->952.654kHz 12-->1114.326kHz 13-->1465.873kHz 14-->1865.066kHz 15-->2329.454kHz	07 (7)
Relative_OVP_thresh_en (Use register relative_ovp_thresh to specify the OVP threshold. This register overrides the PMBus commands.)	D0 0420 [15:15]	LOOP1	0-->Disable 1-->Enable	01 (1)
Relative_OVP_thresh (Specify the relative OVP threshold.)	D0 0420 [14:12]	LOOP1	Th=(Val+1)*50mV 0-->50mV 1-->100mV 2-->150mV 3-->200mV 4-->250mV 5-->300mV 6-->350mV 7-->400mV	03 (3)
Relative_UVP_thresh_en (Use register relative_uvp_thresh to specify the UVP threshold. This register overrides the PMBus commands.)	D0 0420 [11:11]	LOOP1	0-->Disable 1-->Enable	01 (1)

Technical Specifications (continued)

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
Relative_UVP_thresh (Specify the relative UVP threshold.)	D0 0420 [10:8]	LOOP1	Th=(Val+1)*50mV 0-->50mV 1-->100mV 2-->150mV 3-->200mV 4-->250mV 5-->300mV 6-->350mV 7-->400mV	03 (3)
Relative_OVP_thresh_en (Use register relative_ovp_thresh to specify the OVP threshold. This register overrides the PMBus commands.)	D0 0820 [15:15]	LOOP2	0-->Disable 1-->Enable	01 (1)
Relative_OVP_thresh (Specify the relative OVP threshold.)	D0 0820 [14:12]	LOOP2	Th=(Val+1)*50mV 0-->50mV 1-->100mV 2-->150mV 3-->200mV 4-->250mV 5-->300mV 6-->350mV 7-->400mV	03 (3)
Relative_UVP_thresh_en (Use register relative_uvp_thresh to specify the UVP threshold. This register overrides the PMBus commands.)	D0 0820 [11:11]	LOOP2	0-->Disable 1-->Enable	01 (1)
Relative_UVP_thresh (Specify the relative UVP threshold.)	D0 0820 [10:8]	LOOP2	Th=(Val+1)*50mV 0-->50mV 1-->100mV 2-->150mV 3-->200mV 4-->250mV 5-->300mV 6-->350mV 7-->400mV	03 (3)

Technical Specifications (continued)

MFR_I²C_ADDRESS [D6]

Definition: Allows the user to set the 7-bit I²C base address for the module. If the offset setting resistor on the address pin is also used then that offset has to be added to the value of the address on this register to arrive at the actual address. For example if MFR_I²C_ADDRESS is set to 10h and the resistor on the address pin has on offset of +05h, the device will respond to commands sent to address 15h

If I²C address is set to 00h, then I²C bus will be disabled

Format	8-bit unsigned (bit field)							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	1	0	0	0	0

Change History (excludes grammar & clarifications)

Version	Date	Description of the change
1.3	12/xx/2022	Removed CE and CF commands

ABB
601 Shiloh Rd.
Plano, TX USA

abbpowerconversion.com