PIC32CX-BZ3 Family Silicon Errata

PIC32CX-BZ3 Family

Overview

The PIC32CX-BZ3 family of devices conform functionally to the device data sheet, except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the device and revision IDs listed in the following table. The silicon issues are summarized in Table 1-1.

The errata described in this document will be addressed in future revisions of the PIC32CX-BZ3 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon: previous, as well as current.

Table 1. PIC32CX-BZ3 Family Silicon Device Identification

Part Number	Device Identification (DID[31:0])	Revision ID (DID.REVISION[3:0])
		A0
PIC32CX5109BZ31048, WBZ351	0x00009E03	0x0
PIC32CX5109BZ31032, WBZ350	0x00009E02	

Note: Refer to the Device Service Unit chapter in the device's data sheet for detailed information on device identification and revision IDs for your specific device.

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1. Silicon Errata Summary

Table 1-1. Errata Summary

Module	Feature	Issue Summary	Affected Revisions	
			PIC32CX5109BZ3 1048, WBZ351	PIC32CX5109BZ3 1032, WBZ350
			A0	
Supply Voltage and Power Mode	2.1.1. Device parts are not powering at 1.9V	Device parts are not powering at 1.9V	X	
Supply Voltage and Power Mode	2.1.2. Power Management Support	The PIC32CX-BZ3 Power Management Unit (PMU) supports only the MLDO mode in the revision "A0" of silicon and supports the Buck mode in the revision "B0" of silicon.	X	
Supply Voltage and Power Mode	2.1.3. System Does Not Enter Sleep Mode with Flash Power Down (NVMCON2.SLEEP = 0) Bit Disabled and System Clock Equal to or Less than the FRC Frequency	The system is not entering the Sleep mode when the Flash power down (NVMCON2.SLEEP = 0) bit is disabled and the system is working at FRC frequency.	X	
Supply Voltage and Power Mode	2.1.4. GPIO Output Configuration in Deep Sleep and Extreme Deep Sleep	In the Deep Sleep and Extreme Deep Sleep mode, GPIO must not be set to the output state of pin HIGH. Configuring the GPIO state to pin High during the Deep Sleep mode or Extreme Deep Sleep mode will causes leakage current and potential reliability issues on the silicon. This issue is only applicable when the CPU is in the Deep Sleep mode or Extreme Deep Sleep mode and when GPIO is configured as the output state pin HIGH.	X	
Supply Voltage and Power Mode	2.1.5. POR Rearm Event	The POR event is not getting triggered even when the voltage is going below 1.45V.	X	
Analog Comparator (AC)	2.2.1. AC_CMPx Output is Not Gated Either by COMPCTRLx.ENABLE or PMD1.ACMD	The Analog Comparator output (AC_CMPx) will not be disabled by setting either COMPCTRLx.ENABLE = 0 or PMD1.ACMD = 1.	X	
Analog Comparator (AC)	2.2.2. Wrong VDD Scaler Reference for AC_CMP0	AC_CMP0 uses a fixed VDD/2 reference, but the observed reference voltage is not equal to VDD/2.	X	
Analog Comparator (AC)	2.2.3. Wrong VDD Scaler Reference with CMP0 and CMP1 Enabled Concurrently	An incorrect VDD scaler reference voltage is observed when AC_CMP0 and AC_CMP1 are enabled concurrently with VDD scaler as reference for both the comparators. Both comparators will see the same VDD scaler reference.	X	
Analog-to-Digital Converter (ADC)	2.3.1. Scan	The scan list conversions defined in the ADCCSS1 register will restart without finishing the current scan list and does not generate an EOSRDY bit (ADCCON2[29]) end of scan interrupt status if a new trigger event from the STRGSRC[4:0] bits (ADCCON1[20:16]) trigger source occurs before the scan list completion on the shared ADC core.	X	
Analog-to-Digital Converter (ADC)	2.3.2. Glitches in ADC Conversion Result	When the ADC Control clock is asynchronous with the System clock, the conversion result may have glitches if the CPU reads ADCBUFx while the new conversion result is being updated.	X	

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Module	Feature	Issue Summary	Affected Revisions	
			PIC32CX5109BZ3 1048, WBZ351	PIC32CX5109BZ3 1032, WBZ350
			A0	
Analog-to-Digital Converter (ADC)	2.3.3. Wrong VDD33/2 for ADC Internal Input Channel AN11	The ADC internal input channel, AN11, is connected with VDD33/2, but the observed input voltage is not equal to VDD/2.	X	
Capacitive Voltage Divider (CVD) Controller	2.4.1. False CVD event	An invalid CVD event can be created while the FIFO counter is incrementing.	X	
Direct Memory Access Controller (DMAC)	2.5.1. Linked Descriptors	When at least one channel using linked descriptors is already active, a channel Fetch Error (FERR) may occur, enabling a channel with no linked descriptor. Or when one of the already active channels using linked descriptors fetches the enabled second descriptor (index 1) of the channel. These errors can occur when a channel is enabled during the link request of another channel, and if the channel number of the enabled channel is lower than the already active channel.	X	
External Interrupt Controller (EIC)	2.6.1. Edge Detection	When enabling EIC, the SYNCBUSY.ENABLE bit resets before EIC is fully enabled. Edge detection can be done only after three cycles of the selected GCLK (GCLK_EIC or 32KHz_LPCLK).	X	
External Interrupt Controller (EIC)	2.6.2. Asynchronous Edge detection	When the asynchronous edge detection is enabled and the system is in the Standby Sleep mode, only the first edge will be detected. The edges following the first edge of the waveform are ignored until the system wakes up.	X	
External Interrupt Controller (EIC)	2.6.3. Asynchronous Edge Detection	When the asynchronous edge detection is enabled (without debouncer) and the system is in the Standby Sleep mode, only the first edge will generate an event. The edges following the first edge of the waveform do not generate events until the system wakes up.	X	
Event System (EVSYS)	2.7.1. Software Event	The BUSYCH flag never resets upon software events in synchronous/resynchronized path modes with event detection on falling edges.	X	
Event System (EVSYS)	2.7.2. Spurious Overrun	The overrun interrupt flag may be incorrectly set upon software events in synchronous/resynchronized path modes with event detection on both rising and falling edges.	X	
Event System (EVSYS)	2.7.3. Spurious Overrun	In the Synchronous mode, spurious overrun interrupts can happen when the generic clock for a channel is always CHANNEL.ONDEMAND = 0.	X	
Flash Controller Module	2.8.1. SYS Reset Not Getting Released when Asserted Post-Erase Retry	After the Erase Retry operation (using NVMCON2.VREAD1 = 1), all the operations work as expected until a SYS reset is asserted. After the SYS reset is asserted post-Erase Retry, the reset is stuck and is not being released.	X	
Flash Controller Module	2.8.2. DMA in Sleep Mode	The Flash read/write by DMA is not working in Standby Sleep mode if the Flash power down is enabled.	X	
Peripheral Access Controller (PAC)	2.9.1. PAC Protection Error in FREQM	FREQM reads on the Control B register (FREQM.CTRLB) generate a PAC protection error.	X	
Quad I/O Serial Peripheral Interface (QSPI)	2.10.1. QSPI Status Register Bits Not Updated when PB-Bridge-B (PB2_CLK) is Not Equal to System Clock (SYS_CLK)	QSPI Status register bits not updated when PB-Bridge-B (PB2_CLK) are not equal to System Clock (SYS_CLK).	X	

.....continued

Module	Feature	Issue Summary	Affected Revisions	
			PIC32CX5109BZ31048, WBZ351	PIC32CX5109BZ31032, WBZ350
			A0	
RAM Error Correction Code (RAMECC)	2.11.1. ERRADDR Register May Read as '0' When PB-Bridge-B (PB2_CLK) is Not Equal to System Clock (SYS_CLK)	If PB2_CLK is not equal to the System clock (sys_clk), the ERRADDR register read will not return the failing address (caused by Single Bit Error/Dual Bit Error); instead, it may return '0'.	X	
Real-Time Counter (RTC)	2.12.1. Write Corruption	An 8-bit or 16-bit write access for a 32-bit register or an 8-bit write access for a 16-bit register can fail for the following registers: • COUNT register in the COUNT32 mode • COUNT register in the COUNT16 mode • CLOCK register in the CLOCK mode	X	
Real-Time Counter (RTC)	2.12.2. COUNTSYNC	When COUNTSYNC is enabled, the first COUNT value is not correctly synchronized and, thus, the value is incorrect.	X	
Real-Time Counter (RTC)	2.12.3. Tamper Input Filter	Majority debouncing, as part of RTC tamper detection, does not work when enabled by setting the Debouncer Majority Enable bit, CTRLB.DEBMAJ.	X	
Real-Time Counter (RTC)	2.12.4. Tamper Detection	Upon enabling the RTC tamper detection feature, a false tamper detection can be reported by the RTC.	X	
Real-Time Counter (RTC)	2.12.5. Tamper Detection Timestamp	If an external Reset occurs during a tamper detection, the TIMESTAMP register will not be updated when the next tamper detection is triggered.	X	
Real-Time Counter (RTC)	2.12.6. Periodic Event Generation	When CTRLA.PRESCALER is set to OFF and either CTRLB.RTCOUT is set or one of the TAMCTRL.DEBNCn bits is set, the RTC prescaler behaves like CTRLA.PRESCALER = DIV1. The Periodic events and Periodic interrupts will be generated.	X	
Real-Time Counter (RTC)	2.12.7. General Purpose Register	General Purpose Registers n (GPn) are Reset on tamper detection even if GPTRST = 0.	X	
Real-Time Counter (RTC)	2.12.8. Tamper Detection	False tamper detections may occur when configuring the RTC INn and OUTn pins.	X	
Real-Time Counter (RTC)	2.12.9. SYNCBUSY Register	Entering the Deep Sleep mode without waiting for SYNCBUSY.ENABLE and SYNCBUSY.COUNTSYNC synchronization completion may freeze these bits statuses.	X	
Real-Time Counter (RTC)	2.12.10. TIMESTAMP Lock by INFLAG.TAMPER	Clear the INTFLAG.TAMPER bit by writing a '1' to this bit when the Timestamp value was read from the TIMESTAMP register.	X	
Serial Communication Interface (SERCOM)	2.13.1. SERCOM-USART: Collision Detection	In the USART operating mode, if DBGCTRL.DBGSTOP = 1, data transmission is not halted after entering the Debug mode.	X	
Serial Communication Interface (SERCOM)	2.13.2. SERCOM-USART: Debug Mode	The 32-bit Extension mode is enabled and data to be sent is not in multiples of 4 bytes, which means the length counter must be enabled, and additional bytes will be sent over the line.	X	
Serial Communication Interface (SERCOM)	2.13.3. SERCOM-USART: 32-Bit Extension Mode	The TXINV and RXINV bits in CTRLA are interchanged. TXINV controls the RX signal inversion and RXINV controls the TX signal inversion.	X	

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Module	Feature	Issue Summary	Affected Revisions	
			PIC32CX5109BZ31048, WBZ351	PIC32CX5109BZ31032, WBZ350
			A0	
Serial Communication Interface (SERCOM)	2.13.4. SERCOM-USART: TXINV and RXINV Bits	When the USART is used in the 32-bit mode with hardware handshaking (CTS/RTS), the TXC flag may be set before the transmission is complete. TXC may incorrectly be set regardless of whether Data Length Enable (LENGTH.LENEN) is set to '0' or '1'.	X	
Serial Communication Interface (SERCOM)	2.13.5. SERCOM-USART: Flow Control in 32-Bit Extension Mode	The SERCOM USART does not wake from the Standby Sleep mode for ERROR interrupts FERR and PERR.	X	
Serial Communication Interface (SERCOM)	2.13.6. SERCOM-USART: Error Interrupts	When the SERCOM USART is configured as CTRLA.RUNSTDBY = 0 and the Receiver is disabled (CTRLB.RXEN = 0), the clock request to the SERCOM generic clock generator feeding the SERCOM will stay asserted during the Standby Sleep mode, leading to unexpected overconsumption.	X	
Serial Communication Interface (SERCOM)	2.13.7. SERCOM-USART: SERCOM USART in TX Mode Only	The STATUS.CLKHOLD bit in the Host and Client modes can be written even though it is specified as a read-only status bit.	X	
Serial Communication Interface (SERCOM)	2.13.8. SERCOM-I2C: STATUS.CLKHOLD Bit in the Host and Client Modes	In the I^2C mode, LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR bits are not cleared when INTFLAG.AMATCH is cleared.	X	
Serial Communication Interface (SERCOM)	2.13.9. SERCOM-I2C: I2C in Client Mode	In the I^2C Client Transmitter mode, at the reception of a NACK, if there are still data to be sent in the DMA buffer, the DMA will push data to the DATA register. Because a NACK was received, the transfer on the I^2C bus will not occur, causing the loss of this data.	X	
Serial Communication Interface (SERCOM)	2.13.10. SERCOM-I2C: Client Mode with DMA	When SERCOM is configured as an I^2C client in the 32-bit Data mode (DATA32B = 1) and the I^2C host reads from the I^2C client (client transmitter) and outputs its NACK (indicating no more data is needed), the I^2C client still receives a DRDY interrupt. If the CPU does not write a new data to the I^2C client DATA register, the I^2C client will pull the SDA line, which will result in stalling the bus permanently.	X	
Serial Communication Interface (SERCOM)	2.13.11. SERCOM-I2C: I2C Client in DATA32B Mode	When SERCOM is configured as an I^2C client in the 32-bit Data mode (DATA32B = 1) and the I^2C host reads from the I^2C client (client transmitter) and outputs its NACK (indicating no more data is needed), the I^2C client still receives a DRDY interrupt. If the CPU does not write a new data to the I^2C client DATA register, the I^2C client will pull the SDA line, which will result in stalling the bus permanently.	X	
Serial Communication Interface (SERCOM)	2.13.12. SERCOM-I2C: Repeated Start	When the Quick command is enabled (CTRLB.QCEN = 1), software can issue a repeated Start by writing either CTRLB.CMD or ADDR.ADDR bit fields. If in these conditions the SCL Stretch mode is CTRLA.SCLSM = 1, a bus error will be generated.		
Serial Communication Interface (SERCOM)	2.13.13. SERCOM-I2C: 10-Bit Addressing Mode	The 10-bit addressing in the I^2C Client mode is not functional.	X	
Serial Communication Interface (SERCOM)	2.13.14. SERCOM-I2C: Repeated Start	For the Host Write operations (excluding the High-Speed mode), in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not issue a Repeated Start command correctly.	X	

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Module	Feature	Issue Summary	Affected Revisions	
			PIC32CX5109BZ3 1048, WBZ351	PIC32CX5109BZ3 1032, WBZ350
			A0	
Serial Communication Interface (SERCOM)	2.13.15. SERCOM-I2C Client: Error Interrupt INTFLAG.ERROR Repeated Start	When an unexpected STOP occurs on the I^2C bus, the STATUS.BUSERR and INTFLAG.ERROR bits are set but may not wake the system from the Standby Sleep mode. An unexpected START will not produce this issue.	X	
Serial Communication Interface (SERCOM)	2.13.16. SERCOM-SPI: Data Preload	In the SPI Client mode with Client Data Preload Enabled (CTRLB.PLOADEN = 1), the client transmitter may discard some data if the host cannot keep the Client Select pin low until the end of transmission.	X	
Serial Communication Interface (SERCOM)	2.13.17. SERCOM-SPI: Client Data Preload	Preloading a new SPI data (CTRLB.PLOADEN = 1) before going into the Standby Sleep mode may lead to extra power consumption.	X	
Serial Communication Interface (SERCOM)	2.13.18. SERCOM-SPI: Hardware Client Select Control	When Hardware Client Select Control is enabled (CTRLB.MSSEN = 1), the Client Select (SS) pin goes high after each byte transfer even if new data is ready to be sent.	X	
Serial Communication Interface (SERCOM)	2.13.19. I2C Client Auto Ack is Not Usable	The I^2C client AACKEN feature is not usable when doing a repeated start.	X	
Timer/Counter for Control Applications (TCC)	2.14.1. Re-trigger in RAMP2 Operations	A re-trigger in RAMP2 operations (RAMP2, RAMP2A, RAMP2C) is not supported if a prescaler is used (CTRLA.PRESCALER ! = 0), and the re-trigger of the counter is done on the next GCLK (CTRLA.PRESCSYNC = GCLK or CTRLA.PRESCSYNC = RESYNC).	X	
Timer/Counter for Control Applications (TCC)	2.14.2. Re-trigger	If a Re-trigger event (EVCTRL.EVACTn = 0x1, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.	X	
Timer/Counter for Control Applications (TCC)	2.14.3. TCC with EVSYS in SYNC/RESYNC Mode	The TCC peripheral is not compatible with an EVSYS channel in the SYNC or RESYNC mode.	X	
Timer/Counter for Control Applications (TCC)	2.14.4. Dithering Mode with External Re-trigger Events	Using the TCC in the Dithering mode with external retrigger events can lead to an unexpected stretch of right-aligned pulses or shrink of left-aligned pulses.	X	
Timer/Counter for Control Applications (TCC)	2.14.5. LUPD Feature in Down-Counting Mode	When the TCC is used in the Down-counting mode, transfer of PERBUF register value to PER register is delayed by one counter cycle and, therefore, the LUPD feature must not be used with the PER register.	X	
Timer/Counter for Control Applications (TCC)	2.14.6. RAMP2 Feature in Down-Counting Mode	The Timer/Counter counting-down mode (CTRLBCLR.DIR = CTRLBSET.DIR = 1) is not supported in RAMP2 operations (RAMP2, RAMP2A, RAMP2C, RAMP2CS).	X	
Timer/Counter for Control Applications (TCC)	2.14.7. ALOCK Feature	The ALOCK feature is not functional.	X	
Timer/Counter for Control Applications (TCC)	2.14.8. In 2RAMP Mode with Hi-resolution Reference	In 2RAMP mode with Hi-resolution, multiple restarts can be observed when a fault occurred.	X	
Timer/Counter for Control Applications (TCC)	2.14.9. MCx Interrupt Status Flag is Not Cleared Automatically	In a capture operation, MC0/MC1 interrupt status flags (INTFLAG.MC0/INTFLAG.MC1) are not automatically cleared when the CC0/CC1 registers are read.	X	
Timer/Counter (TC)	2.15.1. PERBUF/ CCBUFx Register	When clearing the STATUS.PERBUFV/STATUS.CCBUFx flag, the SYNCBUSY flag is released before the PERBUF/CCBUFx register is restored to its appropriate value.	X	

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Module	Feature	Issue Summary	Affected Revisions	
			PIC32CX5109BZ31048, WBZ351	PIC32CX5109BZ31032, WBZ350
			A0	
Timer/Counter (TC)	2.15.2. Re-trigger	If a Re-trigger event (EVCTRL.EVACTn = 0x1, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.	X	
Timer/Counter (TC)	2.15.3. PER Register Reference	In the 8-bit mode, the PER register updates using the DMA are not possible in the Standby mode.	X	
Timer/Counter (TC)	2.15.4. MCx Interrupt Status Flag is Not Cleared Automatically	In capture operation, MC0/MC1 interrupt status flags (INTFLAG.MC0/INTFLAG.MC1) are not automatically cleared when the CC0/CC1 registers are read.	X	
Watchdog Timer (WDT)	2.16.1. RUN Mode WDT Counter is Not Cleared Before Standby Sleep Instruction	When the interval between clearing the watch dog timer and the sleep instruction is less than 1 WDT clock cycle, the Run mode watchdog counter is not cleared. While in the Standby Sleep mode, the Sleep mode watchdog counter is incrementing, and, at the end of the WDTPS, it generates an NMI which causes the CPU to wake up. After wake-up, the user will expect that because WDT is cleared just before going to sleep, they have an entire WDT period available to them before they have to clear WDT again. But because the Run mode counter was not cleared before going into sleep, the WDT Reset will occur earlier than expected.	X	

Notes:

- Cells with 'X' indicate the issue is present in this revision of the silicon.
- Cells with '—' indicate the issue does not exist in this revision of the silicon.
- The blank cell indicates the issue is corrected or does not exist in this revision of the silicon.

2. Silicon Errata Issues

The following errata issues apply to the PIC32CX-BZ3 family of devices.

Notes:

1. Cells with an 'X' indicate the issue is present in this revision of the silicon.
2. Cells with a dash ('—') indicate the issue does not exist for this revision of the silicon.
3. Blank cells indicate the issue is corrected or does not exist in this revision of the silicon.

Note: Traditional Inter-Integrated Circuit (I^2C) and Serial Peripheral Interface (SPI) documentation uses the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively.

2.1 Supply Voltage and Power Mode

2.1.1 Device parts are not powering at 1.9V

Work Around

Ensure the minimum supply voltage is 2.1V.

Affected Silicon Revisions

A0						
X						

2.1.2 Power Management Support

The PIC32CX-BZ3 Power Management Unit (PMU) supports only the MLDO mode in the revision "A0" of silicon and supports the Buck mode in the revision "B0" of silicon.

Work Around

None

Affected Silicon Revisions

A0						
X						

2.1.3 System Does Not Enter Sleep Mode with Flash Power Down (NVMCON2.SLEEP = 0) Bit Disabled and System Clock Equal to or Less than the FRC Frequency

The system is not entering the Sleep mode when the Flash power down (NVMCON2.SLEEP = 0) bit is disabled and system is working at equal to or less than the FRC frequency.

Work Around

Flash power down (NVMCON2.SLEEP = 1) bit to be enabled to enter into the Flash Deep Sleep mode if system is running at equal to or less than the FRC frequency.

Affected Silicon Revisions

A0						
X						

2.1.4 GPIO Output Configuration in Deep Sleep and Extreme Deep Sleep

In the Deep Sleep and Extreme Deep Sleep modes, GPIO must not be set to the output state of pin HIGH.

Configuring the GPIO state to pin High during the Deep Sleep and Extreme Deep Sleep modes will cause leakage current and potential reliability issues on the silicon.

This issue is only applicable when the CPU is in the Deep Sleep/Extreme Deep Sleep mode and when GPIO is configured as the output state pin HIGH.

Work Around

None

Affected Silicon Revisions

A0						
X						

2.1.5 POR Rearm Event

The POR event is not getting triggered even when the voltage is going below 1.45V.

Work Around

Discharge VDD to Zero.

Affected Silicon Revisions

A0						
X						

2.2 Analog Comparator (AC)

2.2.1 AC_CMPx Output is Not Gated Either by COMPCTRLx.ENABLE or PMD1.ACMD

Analog Comparator output (AC_CMPx) will not be disabled by setting either COMPCTRLx.ENABLE = 0 or PMD1.ACMD = 1.

Work Around

Write the CFGCON1.CMPx_OE register bit to '0' to disable AC.

Affected Silicon Revisions

A0						
X						

2.2.2 Wrong VDD Scaler Reference for AC_CMP0

AC_CMP0 uses a fixed VDD/2 reference, but the observed reference voltage is not equal to VDD/2.

Work Around

Get the expected VDD scaler for AC_CMP0 from SCALER1.VALUE[3:0] = 0x02 value. For example, VDD = 3.3V voltage, the VDD scaler reference for AC_CMP0 is:

VScale = VDD x (R_Bottom)/R_Total

VScale = 3.3 x 598.5/900 = 2.1945V

Affected Silicon Revisions

A0						
X						

2.2.3 Wrong VDD Scaler Reference with CMP0 and CMP1 Enabled Concurrently

Incorrect VDD scaler reference voltage is observed when AC_CMP0 and AC_CMP1 are enabled concurrently with VDD scaler as reference for both the comparators. Both the comparators will see the same VDD scaler reference.

Work Around

Get the expected VDD scaler for both AC_CMP0, AC_CMP1 comparators using the following formula:

R_Bottom = R_Bottom of configured SCALER1.VALUE[3:0]

R_Total = 900 – [598.5 – R_Bottom]

VScale = VDD(R_Bottom)/R_Total

For details on R_Bottom and R_Total values, refer to the *Analog Comparator (AC)* chapter of the device's data sheet.

Affected Silicon Revisions

A0						
X						

2.3 Analog-to-Digital Converter (ADC)

2.3.1 Scan

The scan list conversions defined in the ADCCSS1 register will restart without finishing the current scan list and does not generate an EOSRDY bit (ADCCON2[29]) end of scan interrupt status if a new trigger event from the STRGSRC[4:0] bits (ADCCON1[20:16]) trigger source occurs before the scan list completion on the shared ADC core.

Work Around

Ensure that the STRGSRC[4:0] bits trigger source repetition rate.

Affected Silicon Revisions

A0						
X						

2.3.2 Glitches in ADC Conversion Result

When the ADC Control clock is asynchronous with the System clock, the conversion result may have glitches if the CPU reads ADCBUFx while a new conversion result is being updated.

Work Around

The user has to accurately read ADCBUFx before the next conversion begins. If the ADC is operated in the free running mode, ensure that each converted value is read immediately after the ready bit is set. This can be achieved either by implementing a tight polling loop or using low latency interrupts.

Affected Silicon Revisions

A0						
X						

2.3.3 Wrong VDD33/2 for ADC Internal Input Channel AN11

The ADC internal input channel, AN11, is connected with VDD33/2, but the observed input voltage is not equal to VDD/2.

Work Around

Get the expected input using the below formula:

VDD33/2 = VDD x (598.5/900)

For example, VDD = 3.3V

VDD33/2 = 3.3 x (598.5/900) = 2.1945V

Affected Silicon Revisions

A0						
X						

2.4 Capacitive Voltage Divider (CVD) Controller

2.4.1 False CVD event

Invalid CVD event can get created while FIFO counter is incrementing.

Work Around

Check the status of CVDSTAT[FIFOCNT] >= CVDCON[FIFOTH] after getting CVD interrupt to confirm true interrupt.

Affected Silicon Revisions

A0						
X						

2.5 Direct Memory Access Controller (DMAC)

2.5.1 Linked Descriptors

When at least one channel using linked descriptors is already active, a channel Fetch Error (FERR) may occur on enabling a channel with no linked descriptor or when one of the already active channels using linked descriptors may fetch the enabled second descriptor (index 1) of the channel. These errors can occur when a channel is enabled during the link request of another channel and if the channel number of the enabled channel is lower than the already active channel.

Work Around

When enabling a channel while other channels using linked descriptors are already active, the channel number of the new channel to enable must be greater than the other channel numbers.

Affected Silicon Revisions

A0						
X						

2.6 External Interrupt Controller (EIC)

2.6.1 Edge Detection

When enabling EIC, the SYNCBUSY.ENABLE bit resets before EIC is fully enabled. Edge detection can be done only after three cycles of the selected GCLK (GCLK_EIC or 32KHz_LPCLK).

Work Around

None

Affected Silicon Revisions

A0						
X						

2.6.2 Asynchronous Edge detection

When the asynchronous edge detection is enabled and the system is in the Standby Sleep mode, only the first edge will be detected. The edges following the first edge of the waveform are ignored until the system wakes up.

Work Around

Use the asynchronous edge detection with debouncer enabled. It is recommended to set the DPRESCALER.PRESCALER and DPRESCALER.TICKON to have the lowest frequency possible. To reduce the power consumption, set the EIC GCLK frequency as low as possible or select the 32KHz_LPCLK clock (EIC CTRLA.CKSEL set).

Affected Silicon Revisions

A0						
X						

2.6.3 Asynchronous Edge Detection

When the asynchronous edge detection is enabled (without debouncer), and the system is in the Standby Sleep mode, only the first edge will generate an event. The edges following the first edge of the waveform do not generate events until the system wakes up.

Work Around

Asynchronous edge detection does not work; instead use the synchronous edge detection (ASYNCH.ASYNCH[x] = 0). To reduce power consumption when using synchronous edge detection, either set the GCLK_EIC frequency as low as possible or select the 32KHz_LPCLK clock (EIC CTRLA.CKSEL = 1).

Affected Silicon Revisions

A0						
X						

2.7 Event System (EVSYS)

2.7.1 Software Event

BUSYCH flag never resets upon software events in synchronous/resynchronized path modes with event detection on falling edges.

If a software event occurs when the EVSYS is set in synchronous/resynchronized path modes (CHANNELn.PATH = 0x0/0x1) with event detection set on falling edges (CHANNELn.EDGSEL = 0x2), the CHSTATUS.BUSYCHn flag will be set but will never come back to 0. It is, then, impossible to know if the event user for this channel is ready or not to accept new events.

Work Around

Generate software events for this user through a dedicated channel configured with event detection set on rising edges (CHANNELn.EDGSEL = 0x1).

Affected Silicon Revisions

A0						
X						

2.7.2 Spurious Overrun

The overrun interrupt flag may be incorrectly set upon software events in synchronous/ resynchronized path modes with event detection on both rising and falling edges.

If a software event occurs when the EVSYS is set in synchronous/resynchronized path modes (CHANNELn.PATH = 0x0/0x1) with event detection set on both rising and falling edges (CHANNELn.EDGSEL = 0x3), spurious overrun interrupts may occur (INTFLAG.OVRn).

Work Around

Generate software events for the event user through a dedicated channel configured with event detection set on rising edges (CHANNELn.EDGSEL = 0x1).

Affected Silicon Revisions

A0						
X						

2.7.3 Spurious Overrun

In the Synchronous mode, spurious overrun interrupts can happen when the generic clock for a channel is always CHANNEL.ONDEMAND = 0.

Work Around

Set Generic Clock on Demand feature by setting CHANNEL.ONDEMAND = 1.

Affected Silicon Revisions

A0						
X						

2.8 Flash Controller Module

2.8.1 SYS Reset Not Getting Released when Asserted Post-Erase Retry

After the Erase Retry operation (using NVMCON2.VREAD1 = 1), all the operations work as expected until a SYS Reset is asserted. When the SYS Reset is asserted post-Erase Retry, the Reset is stuck and not getting released.

Work Around

To eliminate the risk of getting stuck in reset, execute one of the below mentioned options after the VREAD operation:

1. Power-on-Reset
2. Configure the CFGCON1.SMCLR bit to 0 to make MLCR create Faux-POR. Assert MCLR.
3. Enter and Exit Deep Sleep mode

Affected Silicon Revisions

A0						
X						

2.8.2 DMA in Sleep Mode

Flash read/write by DMA not working in Standby Sleep mode if Flash power down is enabled.

Work Around

If DMA is used in Standby Sleep mode, do not enable the Flash power down (NVMCON2.SLEEP = 0).

Affected Silicon Revisions

A0						
X						

2.9 Peripheral Access Controller (PAC)

2.9.1 PAC Protection Error in FREQM

FREQM reads on the Control B register (FREQM.CTRLB) to generate a PAC protection error.

Work Around

None

Affected Silicon Revisions

A0						
X						

2.10 Quad I/O Serial Peripheral Interface (QSPI)

2.10.1 QSPI Status Register Bits Not Updated when PB-Bridge-B (PB2_CLK) is Not Equal to System Clock (SYS_CLK)

If PB2_CLK is not equal to System Clock (sys_clk), the QSPI Status register bits are not updated.

Work Around

When using the QSPI Status register bits in the application, configure PB2_CLK to be equal to SYS_CLK without any divisions.

Affected Silicon Revisions

A0						
X						

2.11 RAM Error Correction Code (RAMECC)

2.11.1 ERRADDR Register May Read as '0' When PB-Bridge-B (PB2_CLK) is Not Equal to System Clock (SYS_CLK)

If PB2_CLK is not equal to System Clock (sys_clk), the ERRADDR register read will not return the failing address (caused by Single Bit Error/Dual Bit Error). Instead, it may return '0'.

Work Around

When using RAM ECC in the application, configure PB2_CLK to be equal to SYS_CLK without any divisions.

Affected Silicon Revisions

A0						
X						

2.12 Real-Time Counter (RTC)

2.12.1 Write Corruption

An 8-bit or 16-bit write access for a 32-bit register or an 8-bit write access for a 16-bit register can fail for the following registers:

- COUNT register in the COUNT32 mode
- COUNT register in the COUNT16 mode
- CLOCK register in the CLOCK mode

Work Around

Write the registers with:

- A 32-bit write access for the COUNT register in the COUNT32 mode; CLOCK register in the CLOCK mode
- A 16-bit write access for the COUNT register in the COUNT16 mode

Affected Silicon Revisions

A0						
X						

2.12.2 COUNTSYNC

When COUNTSYNC is enabled, the first COUNT value is not correctly synchronized, and, thus, its value is incorrect.

Work Around

After enabling COUNTSYNC, read the COUNT register until its value is changed when compared to its first value read. After this, all consequent value reads from the COUNT register are valid.

Affected Silicon Revisions

A0						
X						

2.12.3 Tamper Input Filter

Majority debouncing, as part of RTC tamper detection, does not work when enabled by setting the Debouncer Majority Enable bit, CTRLB.DEBMAJ.

Work Around

None

Affected Silicon Revisions

A0						
X						

2.12.4 Tamper Detection

Upon enabling the RTC tamper detection feature, a false tamper detection can be reported by the RTC.

Work Around

Use any one of the following workarounds:

1. Configure TAMPER detection to ONLY falling edge.
2. If the user software has to use TAMPER detection as the rising edge, it must ignore the first tamper interrupt generated after enabling the RTC tamper detection.

Affected Silicon Revisions

A0						
X						

2.12.5 Tamper Detection Timestamp

If an external Reset occurs during a tamper detection, the TIMESTAMP register will not be updated when the next tamper detection is triggered.

Work Around

Enable the RTC tamper interrupt and copy the timestamp from the RTC CLOCK register to one of the following destinations:

- SRAM
- GPx register in RTC
- BKUPx register in RTC

Affected Silicon Revisions

A0						
X						

2.12.6 Periodic Event Generation

When CTRLA.PRESCALER is set to OFF and either CTRLB.RTCOUT is set or one of the TAMCTRL.DEBNCn bits is set, the RTC prescaler behaves like CTRLA.PRESCALER = DIV1. The Periodic events and Periodic interrupts will be generated.

Work Around

When the above conditions are met, clear the EVTCTRL.PEREOn bits to avoid unwanted event generation, and clear the INTENCLR.PERn bits to avoid unwanted interrupt generation.

Affected Silicon Revisions

A0						
X						

2.12.7 General Purpose Register

General Purpose Registers n (GPn) are reset on tamper detection even if GPTRST = 0.

Work Around

None

Affected Silicon Revisions

A0						
X						

2.12.8 Tamper Detection

False tamper detections may occur when configuring the RTC INn and OUTn pins.

Work Around

1. Configure the different RTC registers before configuring the GPIO PORT (as below).
2. Select the RTC INn and OUTn peripheral function(s) on the GPIO PORT module.

Affected Silicon Revisions

A0						
X						

2.12.9 SYNCBUSY Register

Entering the Deep Sleep mode without waiting for SYNCBUSY.ENABLE and SYNCBUSY.COUNTSYNC synchronization completion may freeze these bits status.

Work Around

The RTC must always be configured and enabled before enabling the Deep Sleep mode.

Affected Silicon Revisions

A0						
X						

2.12.10 TIMESTAMP Lock by INFLAG.TAMPER

The INTFLAG.TAMPER bit does not reset by reading the TIMESTAMP register.

Work Around

Clear the INTFLAG.TAMPER bit by writing a '1' to this bit after the Timestamp value is read from the TIMESTAMP register.

Affected Silicon Revisions

A0						
X						

2.13 Serial Communication Interface (SERCOM)

2.13.1 SERCOM-USART: Collision Detection

In the USART operating mode with Collision Detection enabled (CTRLB.COLDEN = 1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB (PBx_CLK) Clock is lower than the SERCOM Generic Clock.

Work Around

The SERCOM APB (PBx_CLK) clock must always be higher than the SERCOM Generic Clock to support collision detection.

Affected Silicon Revisions

A0						
X						

2.13.2 SERCOM-USART: Debug Mode

In the USART operating mode, if DBGCTRL.DBGSTOP = 1, data transmission is not halted after entering the Debug mode.

Work Around

None

Affected Silicon Revisions

A0						
X						

2.13.3 SERCOM-USART: 32-Bit Extension Mode

When the 32-bit Extension mode is enabled and data to be sent are not in multiples of 4 bytes, which means the length counter must be enabled, and additional bytes will be sent over the line.

Work Around

Use any one of the following workarounds:

1. Write the Inter-Character Spacing bits (CTRLC.ICSPACE) to a non-zero-value.
2. Do not use the length counter in firmware by keeping the data to be sent in multiples of 4 bytes.

Affected Silicon Revisions

A0						
X						

2.13.4 SERCOM-USART: TXINV and RXINV Bits

The TXINV and RXINV bits in CTRLA are interchanged. TXINV controls the RX signal inversion and RXINV controls the TX signal inversion.

Work Around

In software, interpret the TXINV bit as a functionality of RXINV, and, conversely, interpret the RXINV bit as a functionality of TXINV.

Affected Silicon Revisions

A0						
X						

2.13.5 SERCOM-USART: Flow Control in 32-Bit Extension Mode

When the USART is used in the 32-bit mode with hardware handshaking (CTS/RTS), the TXC flag may be set before transmission has completed. TXC may incorrectly be set regardless of whether Data Length Enable (LENGTH.LENEN) is set to '0' or '1'.

Work Around

Use the 8-bit mode if using Hardware Flow control.

Affected Silicon Revisions

A0						
X						

2.13.6 SERCOM-USART: Error Interrupts

The SERCOM USART does not wake from the Standby Sleep mode for ERROR interrupts FERR and PERR.

Work Around

Configure the SERCOM-USART to wake up on RX complete and check any PERR/FERR interrupt flag on wake-up.

Affected Silicon Revisions

A0						
X						

2.13.7 SERCOM-USART: SERCOM USART in TX Mode Only

When the SERCOM USART is configured as CTRLA.RUNSTDBY = 0 and the Receiver is disabled (CTRLB.RXEN = 0), the clock request to the SERCOM generic clock generator feeding the SERCOM will stay asserted during the Standby Sleep mode, leading to unexpected overconsumption.

Work Around

Configure CTRLA.RXPO and CTRLA.TXPO to use the same SERCOM PAD for RX and TX or add an external pull-up on the RX pin.

Affected Silicon Revisions

A0						
X						

2.13.8 SERCOM-I^{2}C: STATUS.CLKHOLD Bit in the Host and Client Modes

The STATUS.CLKHOLD bit in the Host and Client modes can be written even though it is specified as a read-only status bit.

Work Around

Do not clear the STATUS.CLKHOLD bit to preserve the current clock hold state.

Affected Silicon Revisions

A0						
X						

2.13.9 SERCOM-I^{2}C: I^{2}C in Client Mode

In the I^{2}C mode, the LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR bits are not cleared when INTFLAG.AMATCH is cleared.

Work Around

Manually clear the status bits: LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR by writing these bits to '1' when set.

Affected Silicon Revisions

A0						
X						

2.13.10 SERCOM-I²C: Client Mode with DMA

In the I²C Client Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push data to the DATA register. Because a NACK was received, the transfer on the I ²C bus will not occur, causing the loss of this data.

Work Around

Configure the DMA transfer size to the number of data to be received by the I²C host. The DMA cannot be used if the number of data to be received by the host is not known.

Affected Silicon Revisions

A0						
X						

2.13.11 SERCOM-I²C: I²C Client in DATA32B Mode

When SERCOM is configured as an I²C client in the 32-bit Data mode (DATA32B = 1) and the I²C host reads from the I²C client (client transmitter) and outputs its NACK (indicating no more data is needed), the I²C client still receives a DRDY interrupt.

If the CPU does not write a new data to the I²C client DATA register, the I²C client will pull the SDA line, which will result in stalling the bus permanently.

Work Around

1. Write dummy data to the data register when a NACK is received from the host.
2. Use command #2 (SERCOMx->I2CS.CTRLB.bit.CMD = 2) when a NACK is received from the host.

Important: Because STATUS.RXNACK always indicates the last received ACK to determine when a NACK is received from the I²C host, the I²C client software needs to consider I2CS.STATUS.RXNACK only on the second DRDY interrupt after receiving the AMATCH interrupt.

Affected Silicon Revisions

A0						
X						

2.13.12 SERCOM-I²C: Repeated Start

When the Quick command is enabled (CTRLB.QCEN = 1), software can issue a repeated Start by writing either CTRLB.CMD or ADDR.ADDR bit fields. If, in these conditions, the SCL Stretch mode is CTRLA.SCLSM = 1, a bus error will be generated.

Work Around

Use the Quick Command mode (CTRLB.QCEN = 1) only if the SCL Stretch mode is CTRLA.SCLSM = 0.

Affected Silicon Revisions

A0						
X						

2.13.13 SERCOM-I²C: 10-Bit Addressing Mode

The 10-bit addressing in the I²C Client mode is not functional.

Work Around

None

Affected Silicon Revisions

A0						
X						

2.13.14 SERCOM-I²C: Repeated Start

For the Host Write operations (excluding the High-Speed mode), in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not issue a Repeated Start command correctly.

Work Around

Write the same 10-bit address with the same direction bit to the ADDR.ADDR register to generate a Repeated Start.

Affected Silicon Revisions

A0						
X						

2.13.15 SERCOM-I²C Client: Error Interrupt INTFLAG.ERROR Repeated Start

When an unexpected STOP occurs on the I²C bus, the STATUS.BUSERR and INTFLAG.ERROR bits are set but may not wake the system from the Standby Sleep mode. An unexpected START will not produce this issue.

Work Around

None

Affected Silicon Revisions

A0						
X						

2.13.16 SERCOM-SPI: Data Preload

In the SPI Client mode with Client Data Preload Enabled (CTRLB.PLOADEN = 1), the client transmitter may discard some data if the host cannot keep the Client Select pin low until the end of transmission.

Work Around

In the SPI Client mode, the Client Select pin (SS) must be kept low by the host until the end of the transmission if the Client Data Preload feature is used (CTRLB.PLOADEN = 1).

Affected Silicon Revisions

A0						
X						

2.13.17 SERCOM-SPI: Client Data Preload

Preloading a new SPI data (CTRLB.PLOADEN = 1) before going into the Standby Sleep mode may lead to extra power consumption.

Work Around

None

Affected Silicon Revisions

A0						
X						

2.13.18 SERCOM-SPI: Hardware Client Select Control

When Hardware Client Select Control is enabled (CTRLB.MSSEN = 1), the Client Select (SS) pin goes high after each byte transfer even if new data is ready to be sent.

Work Around

Set CTRLB.MSSEN = 0 and handle the Client Select (SS) pin by software.

Affected Silicon Revisions

A0						
X						

2.13.19 I²C Client Auto Ack is Not Usable

The I²C client AACKEN feature is not usable when doing a repeated start.

Work Around

Do not use the AACKEN feature; implement an AMATCH handler instead.

Affected Silicon Revisions

A0						
X						

2.14 Timer/Counter for Control Applications (TCC)

2.14.1 Re-trigger in RAMP2 Operations

A re-trigger in RAMP2 operations (RAMP2, RAMP2A, RAMP2C) is not supported if a prescaler is used (CTRLA.PRESCALER ! = 0), and the re-trigger of the counter is done on the next GCLK (CTRLA.PRESCSYNC = GCLK or CTRLA.PRESCSYNC = RESYNC).

Work Around

Configure the re-trigger of the counter on the next prescaler clock (CTRLA.PRESCSYNC = PRESC).

Affected Silicon Revisions

A0						
X						

2.14.2 Re-trigger

If a Re-trigger event (EVCTRL.EVACTn = 0x1, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.

Work Around

Use two channels to store their two successive (n and n+1) CC register values and combine their related waveform outputs to make signal redundancy.

Affected Silicon Revisions

A0						
X						

2.14.3 TCC with EVSYS in SYNC/RESYNC Mode

The TCC peripheral is not compatible with an EVSYS channel in the SYNC or RESYNC mode.

Work Around

Use the TCC with an EVSYS channel in the ASYNC mode.

Affected Silicon Revisions

A0						
X						

2.14.4 Dithering Mode with External Re-trigger Events

Using the TCC in the Dithering mode with external re-trigger events can lead to an unexpected stretch of right-aligned pulses or shrink of left-aligned pulses.

Work Around

Do not use re-trigger events or actions when the TCC module is configured in the Dithering mode.

Affected Silicon Revisions

A0						
X						

2.14.5 LUPD Feature in Down-Counting Mode

When the TCC is used in the Down-counting mode, the transfer of PERBUF register value to PER register is delayed by one counter cycle; therefore, the LUPD feature must not be used with the PER register.

Work Around

In the Down-counting mode, write period value directly to the PER register instead of writing to PERBUF. Alternatively, the Up-counting mode in the TCC can be used if the LUPD feature is required.

Affected Silicon Revisions

A0							
X							

2.14.6 RAMP2 Feature in Down-Counting Mode

The Timer/Counter Counting-down mode (CTRLBCLR.DIR = CTRLBSET.DIR = 1) is not supported in RAMP2 operations (RAMP2, RAMP2A, RAMP2C, RAMP2CS).

Work Around

Use the Timer/Counter Up-counting mode (CTRLBCLR.DIR = CTRLBSET.DIR = 0).

Affected Silicon Revisions

A0							
X							

2.14.7 ALOCK Feature

The ALOCK feature is not functional.

Work Around

None

Affected Silicon Revisions

A0						
X						

2.14.8 In 2RAMP Mode with Hi-resolution Reference

In 2RAMP mode with Hi-resolution, multiple restarts can be observed when a fault occurs.

Work Around

In two Ramp modes (RAMP2, RAMP2A, RAMP2C, RAMP2CS), a re-trigger is not supported in Dithering mode.

Affected Silicon Revisions

A0						
X						

2.14.9 MCx Interrupt Status Flag is Not Cleared Automatically

In the capture operation, MC0/MC1 interrupt status flags (INTFLAG.MC0/INTFLAG.MC1) are not automatically cleared when the CC0/CC1 registers are read.

Work Around

The MC0/MC1 interrupt status flags must be cleared by software (INTFLAG.MC0 = 1/INTFLAG.MC1 = 1).

Affected Silicon Revisions

A0						
X						

2.15 Timer/Counter (TC)

2.15.1 PERBUF/CCBUFx Register

When clearing the STATUS.PERBUFV/STATUS.CCBUFx flag, the SYNCBUSY flag is released before the PERBUF/CCBUFx register is restored to its appropriate value.

Work Around

Clear the STATUS.PERBUFV/STATUS.CCBUFx flag successively twice to ensure that the PERBUF/CCBUFx register value is restored before updating it.

Affected Silicon Revisions

A							
X							

2.15.2 Re-trigger

If a Re-trigger event (EVCTRL.EVACTn = 0x1, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.

Work Around

Use two channels to store their two successive (n and n+1) CC register values and combine their related waveform outputs to make signal redundancy.

Affected Silicon Revisions

A							
X							

2.15.3 PER Register Reference

In the 8-bit mode, the PER register updates using the DMA are not possible in the Standby mode.

Work Around

None

Affected Silicon Revisions

A0						
X						

2.15.4 MCx Interrupt Status Flag is Not Cleared Automatically

In a capture operation, MC0/MC1 interrupt status flags (INTFLAG.MC0/INTFLAG.MC1) are not automatically cleared when CC0/CC1 registers are read.

Work Around

The MC0/MC1 interrupt status flags must be cleared by software (INTFLAG.MC0 = 1/INTFLAG.MC1 = 1).

Affected Silicon Revisions

A0						
X						

2.16 Watchdog Timer (WDT)

2.16.1 RUN Mode WDT Counter is Not Cleared Before Standby Sleep Instruction

When the interval between clearing the watchdog timer (in other words, clearing the Run mode watchdog counter) and the sleep instruction is less than 1 WDT clock cycle, the Run mode watchdog counter is not cleared. When using LPRC as a clock source, the interval is 1 LPRC clock. Because the watchdog timer is in the LPRC domain, which is much slower than the CPU clock, the sleep instruction is executed even before the Run mode watchdog counter is cleared. Hence, the Run mode watchdog counter remains frozen to its last count instead of clearing to '0'.

While in the Standby Sleep mode, the Sleep mode watchdog counter increments. At the end of the WDTPS, it generates an NMI, which causes the CPU to wake up.

After wake-up, the user will expect that because WDT is cleared just before going to sleep, they have an entire WDT period available to them before they have to clear WDT again, but, because the Run mode counter was not cleared before going into sleep, the WDT Reset occurs earlier than expected.

Work Around (Either or Both Can be Used)

1. Add a delay of more than 1 WDT Clock (LPRC clock) between clearing of the WDT and execution of sleep instruction.
2. Execute the WDT clear instruction as soon as the CPU wakes up.

Affected Silicon Revisions

A0						
X						

3. Document Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Section	Description
A	03/2024	Document	Initial revision

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