PIC16F180XX Family Product Brief

Introduction

The PIC16F180 microcontroller family has a suite of digital and analog peripherals that enable cost-sensitive sensor and real-time control applications. This product family is available from 8 to 44-pin packages in a memory range of 3.5 KB to 28 KB, with speeds up to 32 MHz. The family includes a 10-bit Analog-to-Digital Converter with Computation (ADCC), automated Capacitive Voltage Divider (CVD) techniques for advanced capacitive touch sensing, an 8-bit Digital-to-Analog Converter (DAC) module, and many more waveform control and communication peripherals. This small form factor, feature-rich device is well suited for low-cost sensor and control applications.

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PIC16F180 Family Summary

Table 1. Devices Included in This Data Sheet

Device	Program Flash Memory (bytes)	Data Flash Memory (EEPROM)(bytes)	Data SRAM (bytes)	Memory Access Partition/ Device Information Area	I/O Pins(1)/ Peripheral Pin Select	8-Bit Timers with HLT/ 16-Bit Timers(2)	10-Bit PWM/ CCP	10-Bit ADC Channels (External/Internal)	Charge Pump	I2C/SPI	EUSART	NCO	CWG	CLC	FVR	CMP	8-bit DAC	ZCD	SMBus Compatible I/O Pads	External Interrupt Pins	Interrupt-on-Change Pins	Watchdog Timer
PIC16F18013	3.5k	128	256	Y/Y	6/Y	3/3	3/2	5/4	1	1/1	1	1	0	4	2	1	1	1	Y	1	6	Y
PIC16F18014	7k	128	512	Y/Y	6/Y	3/3	3/2	5/4	1	1/1	1	1	0	4	2	1	1	1	Y	1	6	Y
PIC16F18015	14k	128	1024	Y/Y	6/Y	3/3	3/2	5/4	1	2/2	2	1	1	4	2	1	1	1	Y	1	6	Y
PIC16F18023	3.5k	128	256	Y/Y	12/Y	3/3	3/2	11/4	1	1/1	1	1	0	4	2	1	1	1	Y	1	12	Y
PIC16F18024	7k	128	512	Y/Y	12/Y	3/3	3/2	11/4	1	1/1	1	1	0	4	2	1	1	1	Y	1	12	Y
PIC16F18025	14k	128	1024	Y/Y	12/Y	3/3	3/2	11/4	1	2/2	2	1	1	4	2	1	1	1	Y	1	12	Y
PIC16F18026	28k	256	2048	Y/Y	12/Y	3/3	3/2	11/4	1	2/2	2	1	1	4	2	1	1	1	Y	1	12	Y
PIC16F18044	7k	128	512	Y/Y	18/Y	3/3	3/2	17/4	1	2/2	2	1	1	4	2	1	1	1	Y	1	18	Y
PIC16F18045	14k	128	1024	Y/Y	18/Y	3/3	3/2	17/4	1	2/2	2	1	1	4	2	1	1	1	Y	1	18	Y
PIC16F18046	28k	256	2048	Y/Y	18/Y	3/3	3/2	17/4	1	2/2	2	1	1	4	2	1	1	1	Y	1	18	Y
PIC16F18054	7k	128	512	Y/Y	25/Y	3/3	3/2	24/4	1	2/2	2	1	1	4	2	1	1	1	Y	1	25	Y
PIC16F18055	14k	128	1024	Y/Y	25/Y	3/3	3/2	24/4	1	2/2	2	1	1	4	2	1	1	1	Y	1	25	Y
PIC16F18056	28k	256	2048	Y/Y	25/Y	3/3	3/2	24/4	1	2/2	2	1	1	4	2	1	1	1	Y	1	25	Y
PIC16F18074	7k	128	512	Y/Y	36/Y	3/3	3/2	35/4	1	2/2	2	1	1	4	2	1	1	1	Y	1	25	Y
PIC16F18075	14k	128	1024	Y/Y	36/Y	3/3	3/2	35/4	1	2/2	2	1	1	4	2	1	1	1	Y	1	25	Y
PIC16F18076	28k	256	2048	Y/Y	36/Y	3/3	3/2	35/4	1	2/2	2	1	1	4	2	1	1	1	Y	1	25	Y

Notes:

1. Total I/O count includes one input-only pin ($\overline{MCLR}$).
2. Timer0 can be configured as either an 8 or 16-bit timer.

Core Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - DC-32 MHz clock input
  - 125 ns minimum instruction time
- 16-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR)

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- Watchdog Timer (WDT)

Memory

- Up to 28 KB of Program Flash Memory
- Up to 2 KB of Data SRAM Memory
- Up to 256 Bytes of Data EEPROM Memory
- Memory Access Partition (MAP) with Program Flash Memory Partitioned Into:
  - Application block
  - Boot block
  - Storage Area Flash (SAF) block
- Programmable Code Protection and Write Protection
- Device Information Area (DIA) Stores:
  - Fixed Voltage Reference (FVR) measurement data
  - Microchip Unique Identifier (MUI)
- Device Characteristics Area (DCI) Stores:
  - Program/erase row sizes
  - Pin count details
- Direct, Indirect and Relative Addressing Modes

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 5.5V
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Functionality

- Sleep:
  - Reduce device power consumption
  - Reduce system electrical noise while performing ADC conversions
- Low Power Mode Features:
  - Sleep:
    - < 900 nA typical @ 3V/25°C (WDT enabled)
    - < 600 nA typical @ 3V/25°C (WDT disabled)
  - Operating Current:
    - 48 µA typical @ 32 kHz, 3V/25°C
    - < 1 mA typical @ 4 MHz, 5V/25°C

Digital Peripherals

- Two Capture/Compare/PWM (CCP) Modules:
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for Pulse-Width Modulator (PWM) mode
- Three Pulse-Width Modulators (PWM):
  - 10-bit resolution
- Four Configurable Logic Cells (CLC):

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  - Integrated combinational and sequential logic
- One Complimentary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, and 1-channel drive
  - Multiple signal sources
  - Programmable dead band
  - Fault-shutdown input
- One Configurable 8/16-Bit Timer (TMR0)
- Two 16-Bit Timers (TMR1/3) with Gate Control
- Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT)
- One Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input clock up to 64 MHz
- Up to Two Enhanced Universal Synchronous Asynchronous Receiver Transmitters (EUSART):
  - RS-232, RS-485, and LIN compatible
  - Auto wake-up on Start
- Up to Two Host Synchronous Serial Ports (MSSP):
  - Serial Peripheral Interface (SPI) mode:
    - Client Select Synchronization
  - Inter-Integrated Circuit (I^2C) mode:
    - 7/10-bit Addressing modes
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O
- Device I/O Port Features:
  - Up to 35 I/O pins
  - 1 input-only pin
  - Individual I/O direction, open-drain, input threshold, slew rate, and weak pull-up control
  - Interrupt-on-Change (IOC) on up to 25 pins
  - One external interrupt pin

Analog Peripherals

- Analog-to-Digital Converter with Computation (ADCC):
  - 10-bit resolution
  - Up to 35 external input channels
  - Four internal input channels
  - Internal ADC oscillator (ADCRC)
  - Operates in Sleep
  - Selectable auto-conversion trigger sources
- Charge Pump Module:
  - Improves accuracy of analog modules at low voltages
- 8-Bit Digital-to-Analog Converter (DAC):
  - Output available on one I/O pin
  - Internal connections to ADC and Comparators
- One Comparator (CMP):
  - Up to four external inputs
  - Configurable output polarity
  - External output via Peripheral Pin Select
- Zero-Cross Detect (ZCD):

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  - Detect when AC signal on pin crosses ground
- Two Fixed Voltage References (FVR):
  - Selectable 1.024V, 2.048V, and 4.096V output levels
  - FVR1 internally connected to ADC
  - FVR2 internally connected to Comparator

Clocking Structure

- High-Precision Internal Oscillator Block (HFINTOSC):
  - Selectable frequencies up to 32 MHz
  - ±2% at calibration
- Internal 31 kHz Oscillator (LFINTOSC)
- External High-Frequency Clock Input:
  - Two External Clock (EC) Power modes
- Secondary Oscillator (SOSC)

Programming/Debug Features

- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Debug Integrated On-Chip

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Packages

Table 2. Packages (8 - 20-pin packages)

Device	8-Pin PDIP	8-Pin SOIC	8-Pin DFN	14-Pin PDIP	14-Pin SOIC	14-Pin TSSOP	16-Pin VQFN	20-Pin PDIP	20-Pin SOIC	20-Pin SSOP	20-Pin QFN
PIC16F18013	•	•	•								
PIC16F18014	•	•	•								
PIC16F18015	•	•	•								
PIC16F18023				•	•	•	•				
PIC16F18024				•	•	•	•				
PIC16F18025				•	•	•	•				
PIC16F18026				•	•	•	•				
PIC16F18044								•	•	•	•
PIC16F18045								•	•	•	•
PIC16F18046								•	•	•	•

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Table 3. Packages (28 - 44-pin packages)

Device	28-Pin SPDIP	28-Pin SOIC	28-Pin SSOP	28-Pin VQFN	40-Pin PDIP	40-Pin QFN	44-Pin TQFP
PIC16F18054	•	•	•	•			
PIC16F18055	•	•	•	•			
PIC16F18056	•	•	•	•			
PIC16F18074					•	•	•
PIC16F18075					•	•	•
PIC16F18076					•	•	•

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Pin Diagrams

Figure 1. 8-Pin PDIP, SOIC, DFN

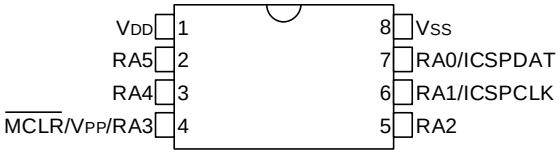


Figure 2. 14-Pin PDIP, SOIC, TSSOP

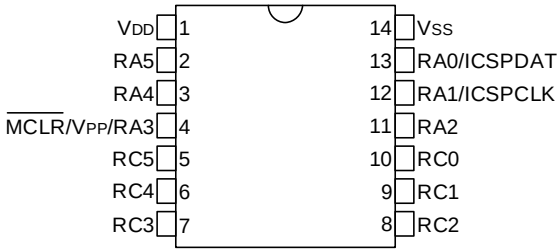
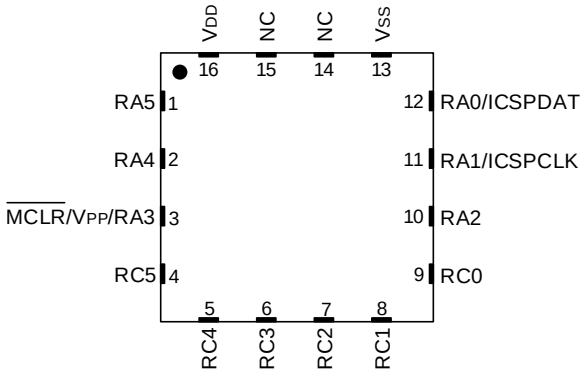


Figure 3. 16-Pin VQFN



Note: It is recommended that the exposed bottom pad be connected to V_{SS}; however, it must not be the only V_{SS} connection to the device.

Figure 4. 20-Pin PDIP, SOIC, SSOP

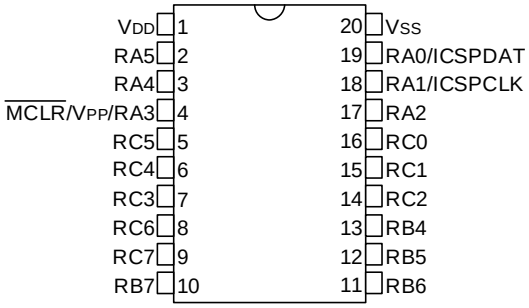
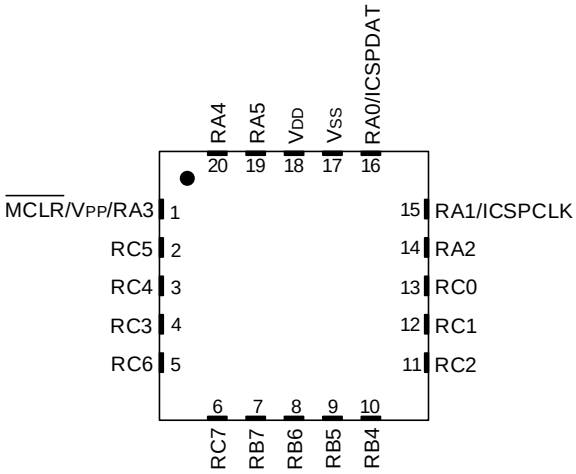


Figure 5. 20-Pin QFN



Note: It is recommended that the exposed bottom pad be connected to V_{SS}; however, it must not be the only V_{SS} connection to the device.

Figure 6. 28-Pin SPDIP, SOIC, SSOP

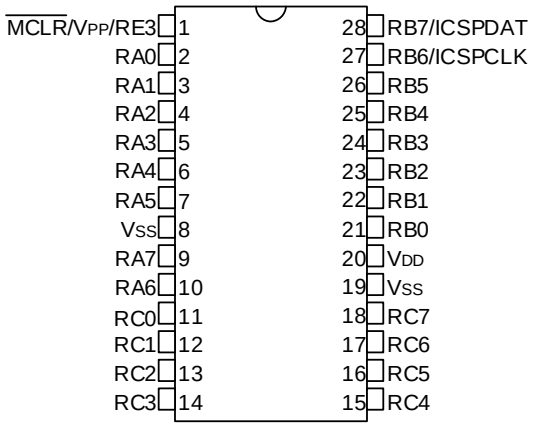


Figure 7. 28-Pin VQFN

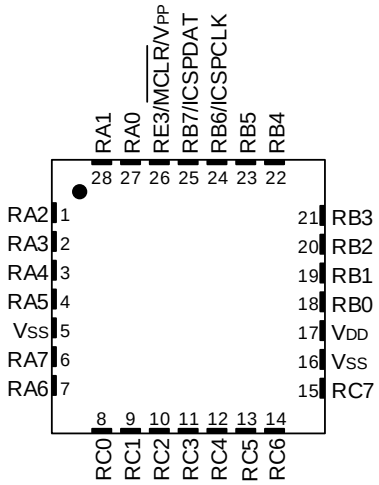


Figure 8. 40-Pin PDIP

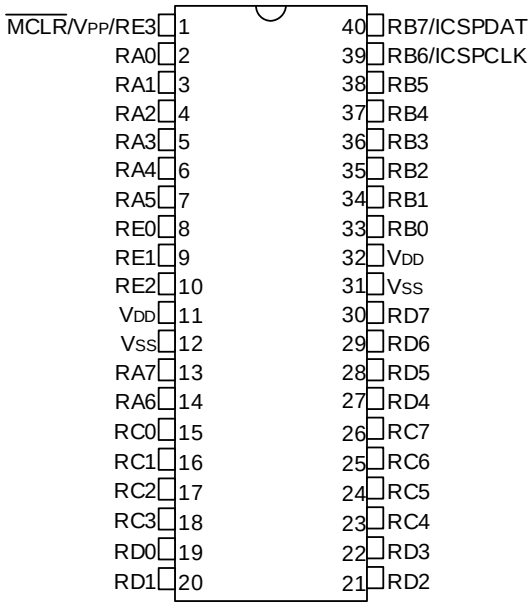


Figure 9. 40-Pin QFN

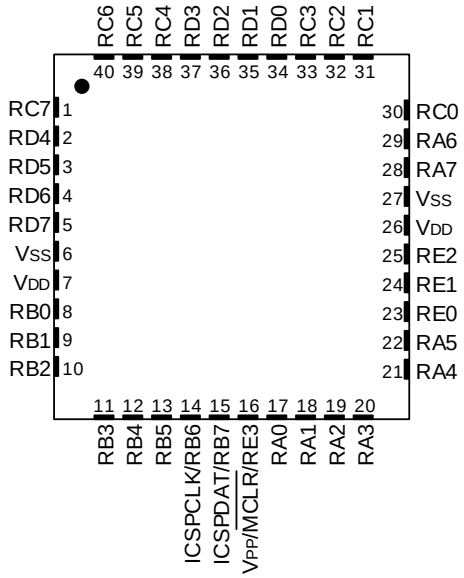
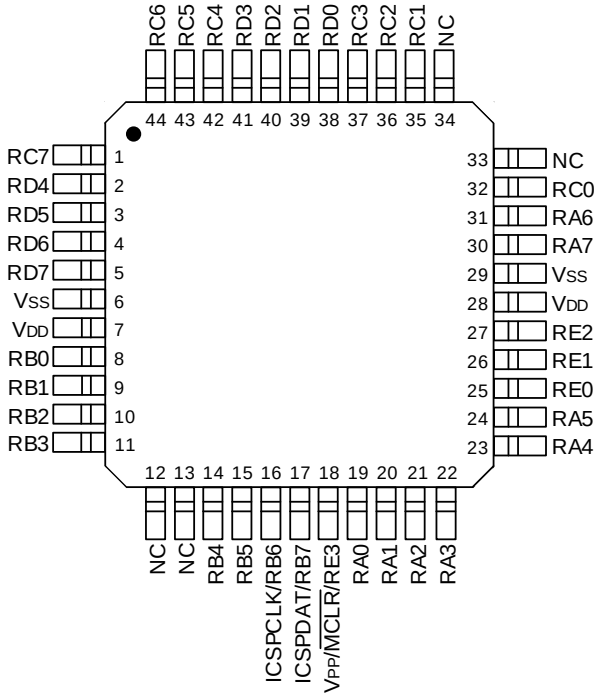


Figure 10. 44-Pin TQFP



Pin Allocation Tables

Table 4. 8-Pin Allocation Table

I/O	8-Pin PDIP SOIC DFN	ADC	Reference	Comparator	ZCD	Timers	CCP/PWM	CWG	CLC	MSSP	EUSART	IOC	Interrupt	Basic
RA0	7	ANA0	DAC1OUT1	C1IN0+	—	T3CKI(1) T3G(1) T4IN(1)	—	—	CLCIN3(1)	SCL2(1,3,4) SCK2(1,3,4) SDA2(1,3,4) SDI2(1,3,4) $\overline{SS2}$(1,4)	CK1(1,3) CK2(1,3,4)	IOCA0	—	ICSPDAT ICDDAT
RA1	6	ANA1	V_{REF}+ (ADC) DAC1REF0+	C1IN0-	—	T6IN(1)	—	—	CLCIN2(1)	SCL1(1,3) SCK1(1,3)	RX1(1) DT1(1,3) RX2(1,4) DT2(1,3,4)	IOCA1	—	ICSPCLK ICDCLK
RA2	5	ANA2	DAC1REF0-	—	ZCD1	T0CKI(1)	—	CWG1(1,4)	—	SDA1(1,3) SDI1(1,3)	—	IOCA2	INT(1)	—
RA3	4	—	—	—	—	—	—	—	CLCIN0 (1)	$\overline{SS1}$(1)	—	IOCA3	—	$\overline{MCLR}$ V_{PP}
RA4	3	ANA4	—	C1IN1-	—	T1G(1)	—	—	—	—	—	IOCA4	—	CLKOUT SOSCO
RA5	2	ANA5 ADACT(1)	—	—	—	T1CKI(1) T2IN(1)	CCP1(1) CCP2(1)	—	CLCIN1(1)	—	—	IOCA5	—	CLKIN SOSCI
V_{DD}	1	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	8	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	ADGRDA ADGRDB	—	CMP1	—	TMR0	CCP1 CCP2 PWM3 PWM4 PWM5	CWG1A(4) CWG1B(4) CWG1C(4) CWG1D(4)	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	SCL1 SCK1 SDA1 SDO1 SCL2(4) SCK2(4) SDA2(4) SDO2(4)	TX1 DT1 CK1 TX2(4) DT2(4) CK2(4)	—	—	—

Notes:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to any PORTx pin.
2. All output signals shown in this row are PPS remappable.
3. This is a bidirectional signal. For normal operation, user software must map this signal to the same pin via the PPS input and PPS output registers.
4. Only available on the 8-pin PIC16F18015.

Table 5. 14/16-Pin Allocation Table

I/O	14-Pin PDIP SOIC TSSOP	16-Pin VQFN	ADC	Reference	Comparator	ZCD	Timers	CCP	CWG	CLC	MSSP	EUSART	IOC	Interrupt	Basic
RA0	13	12	ANA0	DAC1OUT1	C1IN0+	—	—	—	—	—	SS2(1)	—	IOCA0	—	ICSPDAT ICDDAT
RA1	12	11	ANA1	V_{REF}+(ADC) DAC1REF0+	C1IN0-	—	—	—	—	—	—	—	IOCA1	—	ICSPCLK ICDCLK
RA2	11	10	ANA2	DAC1REF0-	—	ZCD1	T0CKI(1)	—	CWG1(1)	—	—	—	IOCA2	INT(1)	—
RA3	4	3	—	—	—	—	—	—	—	—	—	—	IOCA3	—	$\overline{MCLR}$ V_{PP}
RA4	3	2	ANA4	—	—	—	T1G(1)	—	—	—	—	—	IOCA4	—	CLKOUT SOSCO
RA5	2	1	ANA5	—	—	—	T1CKI(1) T2IN(1)	—	—	CLCIN3(1)	—	—	IOCA5	—	CLKIN SOSCI
RC0	10	9	ANC0	—	—	—	—	—	—	—	SCL1(1,3,4) SCK1(1,3,4)	CK2(1,3)	IOCC0	—	—
RC1	9	8	ANC1	—	C1IN1-	—	T4IN (1)	—	—	CLCIN2(1)	SDA1(1,3,4) SDI1(1,3,4)	RX2(1) DT2(1,3)	IOCC1	—	—
RC2	8	7	ANC2 ADACT(1)	—	C1IN2-	—	T6IN (1)	—	—	—	—	—	IOCC2	—	—
RC3	7	6	ANC3	—	C1IN3-	—	—	CCP2(1)	—	CLCIN0(1)	$\overline{SS1}$(1)	—	IOCC3	—	—
RC4	6	5	ANC4	—	—	—	T3G(1)	—	—	CLCIN1(1)	SCL2(1,3,4) SCK2(1,3,4)	CK1(1,3)	IOCC4	—	—
RC5	5	4	ANC5	—	—	—	T3CKI(1)	CCP1(1)	—	—	SDA2(1,3,4) SDI2(1,3,4)	RX1(1) DT1(1,3)	IOCC5	—	—
V_{DD}	1	16	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	14	13	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}

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I/O	14-Pin PDIP SOIC TSSOP	16-Pin VQFN	ADC	Reference	Comparator	ZCD	Timers	CCP	CWG	CLC	MSSP	EUSART	IOC	Interrupt	Basic
OUT(2)	—	—	ADGRDA ADGRDB	—	CMP1	—	TMR0	CCP1 CCP2 PWM3 PWM4 PWM5	CWG1A CWG1B CWG1C CWG1D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	SCL1 SCK1 SDA1 SDO1 SCL2 SCK2 SDA2 SDO2	TX1 DT1 CK1 TX2 DT2 CK2	—	—	—

Notes:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to any PORTx pin.
2. All output signals shown in this row are PPS remappable.
3. This is a bidirectional signal. For normal operation, user software must map this signal to the same pin via the PPS input and PPS output registers.
4. These pins can be configured for I^2C or SMBus logic levels via the RxyI2C registers. The SCL1/SDA1 signals may be assigned to these pins for expected operation. PPS assignments of these signals to other pins will operate; however, the logic levels will be standard TTL/ST as selected by the INLVL register.

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Table 6. 20-Pin Allocation Table

I/O	20-Pin PDIP SOIC SSOP	20-Pin QFN	ADC	Reference	Comparator	ZCD	Timers	CCP	CWG	CLC	MSSP	EUSART	IOC	Interrupt	Basic
RA0	19	16	ANA0	DAC1OUT1	C1IN0+	—	—	—	—	—	—	—	IOCA0	—	ICSPDAT ICDDAT
RA1	18	15	ANA1	V_{REF}+(ADC) DAC1REF0+	C1IN0-	—	—	—	—	—	SS2(1)	—	IOCA1	—	ICSPCLK ICDCLK
RA2	17	14	ANA2	DAC1REF0-	—	ZCD1	T0CKI(1)	—	CWG1(1)	CLCIN0(1)	—	—	IOCA2	INT(1)	—
RA3	4	1	—	—	—	—	—	—	—	—	—	—	IOCA3	—	$\overline{MCLR}$ V_{PP}
RA4	3	20	ANA4	—	—	—	T1G(1)	—	—	—	—	—	IOCA4	—	CLKOUT SOSCO
RA5	2	19	ANA5	—	—	—	T1CKI(1) T2IN(1)	—	—	—	—	—	IOCA5	—	CLKIN SOSCI
RB4	13	10	ANB4	—	—	—	—	—	—	CLCIN2(1)	SDA1(1,3,4) SDI1(1,3,4)	—	IOCB4	—	—
RB5	12	9	ANB5	—	—	—	—	—	—	CLCIN3(1)	SDA2(1,3,4) SDI2(1,3,4)	RX1(1) DT1(1,3)	IOCB5	—	—
RB6	11	8	ANB6	—	—	—	—	—	—	—	SCL1(1,3,4) SCK1(1,3,4)	—	IOCB6	—	—
RB7	10	7	ANB7	—	—	—	—	—	—	—	SCL2(1,3,4) SCK2(1,3,4)	CK1(1,3)	IOCB7	—	—
RC0	16	13	ANC0	—	—	—	—	—	—	—	—	CK2(1,3)	IOCC0	—	—
RC1	15	12	ANC1	—	C1IN1-	—	T4IN(1)	—	—	—	—	RX2(1) DT2(1,3)	IOCC1	—	—
RC2	14	11	ANC2 ADACT(1)	—	C1IN2-	—	T6IN(1)	—	—	—	—	—	IOCC2	—	—
RC3	7	4	ANC3	—	C1IN3-	—	—	CCP2(1)	—	CLCIN1(1)	—	—	IOCC3	—	—
RC4	6	3	ANC4	—	—	—	T3G(1)	—	—	—	—	—	IOCC4	—	—
RC5	5	2	ANC5	—	—	—	T3CKI(1)	CCP1(1)	—	—	—	—	IOCC5	—	—
RC6	8	5	ANC6	—	—	—	—	—	—	—	$\overline{SS1}$(1)	—	IOCC6	—	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	IOCC7	—	—
V_{DD}	1	18	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	20	17	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}

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I/O	20-Pin PDIP SOIC SSOP	20-Pin QFN	ADC	Reference	Comparator	ZCD	Timers	CCP	CWG	CLC	MSSP	EUSART	IOC	Interrupt	Basic
OUT(2)	—	—	ADGRDA ADGRDB	—	CMP1	—	TMR0	CCP1 CCP2 PWM3 PWM4 PWM5	CWG1A CWG1B CWG1C CWG1D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	SCL1 SCK1 SDA1 SDO1 SCL2 SCK2 SDA2 SDO2	TX1 DT1 CK1 TX2 DT2 CK2	—	—	—

Notes:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to any PORTx pin.
2. All output signals shown in this row are PPS remappable.
3. This is a bidirectional signal. For normal operation, user software must map this signal to the same pin via the PPS input and PPS output registers.
4. These pins can be configured for I^2C or SMBus logic levels via the RxyI2C registers. The SCL1/SDA1 signals may be assigned to these pins for expected operation. PPS assignments of these signals to other pins will operate; however, the logic levels will be standard TTL/ST as selected by the INLVL register.

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Table 7. 28-Pin Allocation Table

I/O	28-Pin SPDIP SOIC SSOP	28-Pin VQFN	ADC	Reference	Comparator	ZCD	Timers	CCP	CWG	CLC	MSSP	EUSART	IOC	Interrupt	Basic
RA0	2	27	ANA0	—	C1IN0-	—	—	—	—	CLCIN0(1)	—	—	IOCA0	—	—
RA1	3	28	ANA1	—	C1IN1-	—	—	—	—	CLCIN1(1)	—	—	IOCA1	—	—
RA2	4	1	ANA2	DAC1REF0-	C1IN0+	—	—	—	—	—	—	—	IOCA2	—	—
RA3	5	2	ANA3	DAC1REF0+ V_{REF+} (ADC)	C1IN1+	—	—	—	—	—	—	—	IOCA3	—	—
RA4	6	3	ANA4	—	—	—	T0CKI(1)	—	—	—	—	—	IOCA4	—	—
RA5	7	4	ANA5	—	—	—	—	—	—	—	$\overline{SS}$1(1)	—	IOCA5	—	—
RA6	10	7	ANA6	—	—	—	—	—	—	—	—	—	IOCA6	—	CLKOUT
RA7	9	6	ANA7	—	—	—	—	—	—	—	—	—	IOCA7	—	CLKIN
RB0	21	18	ANB0	—	—	ZCD1	—	—	CWG1(1)	—	SS2	—	IOCB0	INT(1)	—
RB1	22	19	ANB1	—	C1IN3-	—	—	—	—	—	SCL2(1,3,4) SCK2(1,3,4)	—	IOCB1	—	—
RB2	23	20	ANB2	—	—	—	—	—	—	—	SDA2(1,3,4) SDI2(1,3,4)	—	IOCB2	—	—
RB3	24	21	ANB3	—	C1IN2-	—	—	—	—	—	—	—	IOCB3	—	—
RB4	25	22	ANB4 ADACT(1)	—	—	—	—	—	—	—	—	—	IOCB4	—	—
RB5	26	23	ANB5	—	—	—	T1G(1)	—	—	—	—	—	IOCB5	—	—
RB6	27	24	ANB6	—	—	—	—	—	—	CLCIN2(1)	—	CK2(1,3)	IOCB6	—	ICSPCLK ICDCLK
RB7	28	25	ANB7	DAC1OUT2	—	—	T6IN(1)	—	—	CLCIN3(1)	—	RX2(1) DT2(1,3)	IOCB7	—	ICSPDAT ICDDAT
RC0	11	8	ANC0	—	—	—	T1CKI(1) T3CKI(1) T3G(1)	—	—	—	—	—	IOCC0	—	SOSCO
RC1	12	9	ANC1	—	—	—	—	CCP2(1)	—	—	—	—	IOCC1	—	SOSCI
RC2	13	10	ANC2	—	—	—	—	CCP1(1)	—	—	—	—	IOCC2	—	—
RC3	14	11	ANC3	—	—	—	T2IN(1)	—	—	—	SCL1(1,3,4) SCK1(1,3,4)	—	IOCC3	—	—
RC4	15	12	ANC4	—	—	—	—	—	—	—	SDA1(1,3,4) SDI1(1,3,4)	—	IOCC4	—	—
RC5	16	13	ANC5	—	—	—	T4IN(1)	—	—	—	—	—	IOCC5	—	—
RC6	17	14	ANC6	—	—	—	—	—	—	—	—	CK1(1,3)	IOCC6	—	—

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I/O	28-Pin SPDIP SOIC SSOP	28-Pin VQFN	ADC	Reference	Comparator	ZCD	Timers	CCP	CWG	CLC	MSSP	EUSART	IOC	Interrupt	Basic
RC7	18	15	ANC7	—	—	—	—	—	—	—	—	RX1(1) DT1(1,3)	IOCC7	—	—
RE3	1	26	—	—	—	—	—	—	—	—	—	—	IOCE3	—	$\overline{MCLR}$ V_{PP}
V_{DD}	20	17	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	8 19	5 16	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	—	ADGRDA ADGRDB	—	CMP1	—	TMR0	CCP1 CCP2 PWM3 PWM4 PWM5	CWG1A CWG1B CWG1C CWG1D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	SCL1 SCK1 SDA1 SDO1 SCL2 SCK2 SDA2 SDO2	TX1 DT1 CK1 TX2 DT2 CK2	—	—	—

Notes:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to the PPS input table in the device data sheet for details on which PORT pins may be used for this signal.
2. All output signals shown in this row are PPS remappable.
3. This is a bidirectional signal. For normal operation, user software must map this signal to the same pin via the PPS input and PPS output registers.
4. These pins can be configured for I^2C or SMBus logic levels via the RxyI2C registers. The SCL1/SDA1 signals may be assigned to these pins for expected operation. PPS assignments of these signals to other pins will operate; however, the logic levels will be standard TTL/ST as selected by the INLVL register.

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Table 8. 40/44-Pin Allocation Table

I/O	40-Pin PDIP	40-Pin QFN	44-Pin TQFP	ADC	Reference	Comparator	ZCD	Timers	CCP	CWG	CLC	MSSP	EUSART	IOC	Interrupt	Basic
RA0	2	17	19	ANA0	—	C1IN0-	—	—	—	—	CLCIN0(1)	—	—	IOCA0	—	—
RA1	3	18	20	ANA1	—	C1IN1-	—	—	—	—	CLCIN1(1)	—	—	IOCA1	—	—
RA2	4	19	21	ANA2	DAC1REF0-	C1IN0+	—	—	—	—	—	—	—	IOCA2	—	—
RA3	5	20	22	ANA3	DAC1REF0+ V_{REF+} (ADC)	C1IN1+	—	—	—	—	—	—	—	IOCA3	—	—
RA4	6	21	23	ANA4	—	—	—	T0CKI(1)	—	—	—	—	—	IOCA4	—	—
RA5	7	22	24	ANA5	—	—	—	—	—	—	—	$\overline{SS1}$(1)	—	IOCA5	—	—
RA6	14	29	31	ANA6	—	—	—	—	—	—	—	—	—	IOCA6	—	CLKOUT
RA7	13	28	30	ANA7	—	—	—	—	—	—	—	—	—	IOCA7	—	CLKIN
RB0	33	8	8	ANB0	—	—	ZCD1	—	—	CWG1(1)	—	SS2(1)	—	IOCB0	INT(1)	—
RB1	34	9	9	ANB1	—	C1IN3-	—	—	—	—	—	SCL2(1,3,4) SCK2(1,3,4)	—	IOCB1	—	—
RB2	35	10	10	ANB2	—	—	—	—	—	—	—	SDA2(1,3,4) SDI2(1,3,4)	—	IOCB2	—	—
RB3	36	11	11	ANB3	—	C1IN2-	—	—	—	—	—	—	—	IOCB3	—	—
RB4	37	12	14	ANB4 ADACT(1)	—	—	—	—	—	—	—	—	—	IOCB4	—	—
RB5	38	13	15	ANB5	—	—	—	T1G(1)	—	—	—	—	—	IOCB5	—	—
RB6	39	14	16	ANB6	—	—	—	—	—	—	CLCIN2(1)	—	CK2(1,3)	IOCB6	—	ICSPCLK ICDCLK
RB7	40	15	17	ANB7	DAC1OUT2	—	—	T6IN(1)	—	—	CLCIN3(1)	—	RX2(1) DT2(1,3)	IOCB7	—	ICSPDAT ICDDAT
RC0	15	30	32	ANC0	—	—	—	T1CKI(1) T3CKI(1) T3G(1)	—	—	—	—	—	IOCC0	—	SOSCO
RC1	16	31	35	ANC1	—	—	—	—	CCP2(1)	—	—	—	—	IOCC1	—	SOSCI
RC2	17	32	36	ANP2	—	—	—	—	CCP1(1)	—	—	—	—	IOCC2	—	—
RC3	18	33	37	ANC3	—	—	—	T2IN(1)	—	—	—	SCL1(1,3,4) SCK1(1,3,4)	—	IOCC3	—	—
RC4	23	38	42	ANC4	—	—	—	—	—	—	—	SDA1(1,3,4) SDI1(1,3,4)	—	IOCC4	—	—
RC5	24	39	43	ANC5	—	—	—	T4IN(1)	—	—	—	—	—	IOCC5	—	—
RC6	25	40	44	ANC6	—	—	—	—	—	—	—	—	CK1(1,3)	IOCC6	—	—
RC7	26	1	1	ANC7	—	—	—	—	—	—	—	—	RX1(1) DT1(1,3)	IOCC7	—	—

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I/O	40-Pin PDIP	40-Pin QFN	44-Pin TQFP	ADC	Reference	Comparator	ZCD	Timers	CCP	CWG	CLC	MSSP	EUSART	IOC	Interrupt	Basic
RD0	19	34	38	AND0	—	—	—	—	—	—	—	—	—	—	—	—
RD1	20	35	39	AND1	—	—	—	—	—	—	—	—	—	—	—	—
RD2	21	36	40	AND2	—	—	—	—	—	—	—	—	—	—	—	—
RD3	22	37	41	AND3	—	—	—	—	—	—	—	—	—	—	—	—
RD4	27	2	2	AND4	—	—	—	—	—	—	—	—	—	—	—	—
RD5	28	3	3	AND5	—	—	—	—	—	—	—	—	—	—	—	—
RD6	29	4	4	AND6	—	—	—	—	—	—	—	—	—	—	—	—
RD7	30	5	5	AND7	—	—	—	—	—	—	—	—	—	—	—	—
RE0	8	23	25	ANE0	—	—	—	—	—	—	—	—	—	IOCE0	—	—
RE1	9	24	26	ANE1	—	—	—	—	—	—	—	—	—	IOCE1	—	—
RE2	10	25	27	ANE2	—	—	—	—	—	—	—	—	—	IOCE2	—	—
RE3	1	16	18	—	—	—	—	—	—	—	—	—	—	IOCE3	—	$\overline{MCLR}$ V_{PP}
V_{DD}	11 32	7 26	7 28	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	12 31	6 27	6 29	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	—	—	ADGRDA ADGRDB	—	CMP1	—	TMR0	CCP1 CCP2 PWM3 PWM4 PWM5	CWG1A CWG1B CWG1C CWG1D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	SCL1 SCK1 SDA1 SDO1 SCL2 SCK2 SDA2 SDO2	TX1 DT1 CK1 TX2 DT2 CK2	—	—	—

Notes:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to the PPS input table in the device data sheet for details on which PORT pins may be used for this signal.
2. All output signals shown in this row are PPS remappable.
3. This is a bidirectional signal. For normal operation, user software must map this signal to the same pin via the PPS input and PPS output registers.
4. These pins can be configured for I^2C or SMBus logic levels via the RxyI2C registers. The SCL1/SDA1 signals may be assigned to these pins for expected operation. PPS assignments of these signals to other pins will operate; however, the logic levels will be standard TTL/ST as selected by the INLVL register.

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Revision	Date	Description
B	01/2022	Updates and corrections.
A	06/2021	Initial document release.

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