A Product Line of Diodes Incorporated

PI3HDX12311

12Gbps 4-Channel HDMI 2.1 Hybrid ReDriver with DDC Listener

Description

The PI3HDX12311 is a 3.3V quad–channel Hybrid ReDriver™ supporting HDMI 2.1 Fixed Rate Link (FRL) up to 12Gbps, TMDS up to 6Gbps. For HDMI1.4 application, the ReDriver is configured as a limited ReDriver, where the ReDriver differential output swing is defined by the ReDriver swing setting, to ensure the HDMI compliant levels at the receptacle . For HDMI2.0 and HDMI 2.1, the ReDriver is configured as a linear ReDriver, where the ReDriver differential output swing is directly proportional to the received signal, to ensure the ReDriver is function as a trace canceller. The linear ReDriver mode is also inherently transparent to link training signals.

The PI3HDX12311 ReDriver input and outputs signals could be either AC or DC coupled or mixed, which can eliminate the need for additional level shifter components from the data channels.

The PI3HDX12311 is equipped with pin mode control for operation mode, Equalization, Flat Gain, Output Swing (SW), and Output -1dB linearity Swing (N1SW).

The device can support dual-mode DisplayPort (DP++) level shift application for HDMI TMDS output signals.

Application(s)

- Laptops and Desktop PCs
- Gaming Consoles
- DTV and Commercial Display Panel
- Docking Station and Peripherals
- KVM Switch Box and HDMI Active Cable

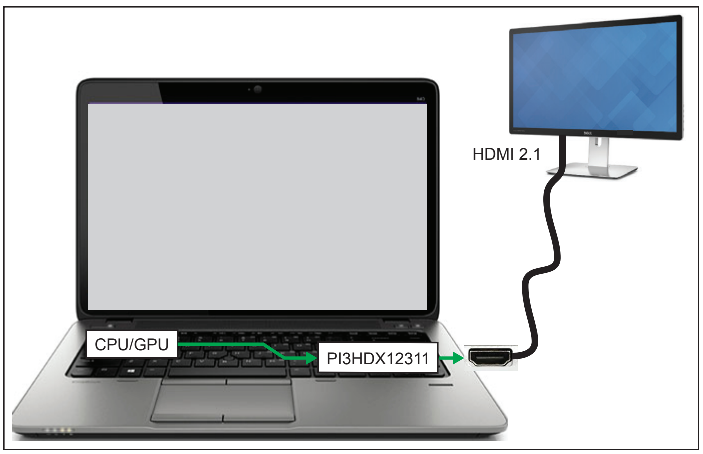


Figure 1. HDMI 2.1 ReDriver or Level Shifter

Features

- Supports Up to 12Gbps Signals with Non-Blocking Linear ReDriver via Pin Control Settings
- Compliant to HDMI 1.4/2.0/2.1 and DisplayPort Dual-Mode V1.1 Standard
- Wide EQ Tuning Range from 5.6dB to 12.7dB at 6GHz
- Hybrid Redriving Mode to Ensure HDMI Compliant Levels at the Receptacle
- Integrated DDC Listener for HDMI FRL/TMDS and Speed Detection
- Auto Selects the Following Settings for Power and SI Optimization
  - TX Slew Rate
  - TX Impedance
  - Pre-Defined EQ/SW/N1SW/FG
- Supports Back Current Leakage Free (Ioff)
- Far-end Receiver Detection for TX DC Coupling Mode
- 726mW Typical Power Dissipation with a Maximus Output Swing
- Single 3.3V (±5%) Power Supply
- Operating Temperature Range: –40°C to +70°C
- Packaging (Pb-free & Green):
  - Tiny 32-pin X1QFN , 2.85 x 4.5 mm (0.4 mm pitch)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/

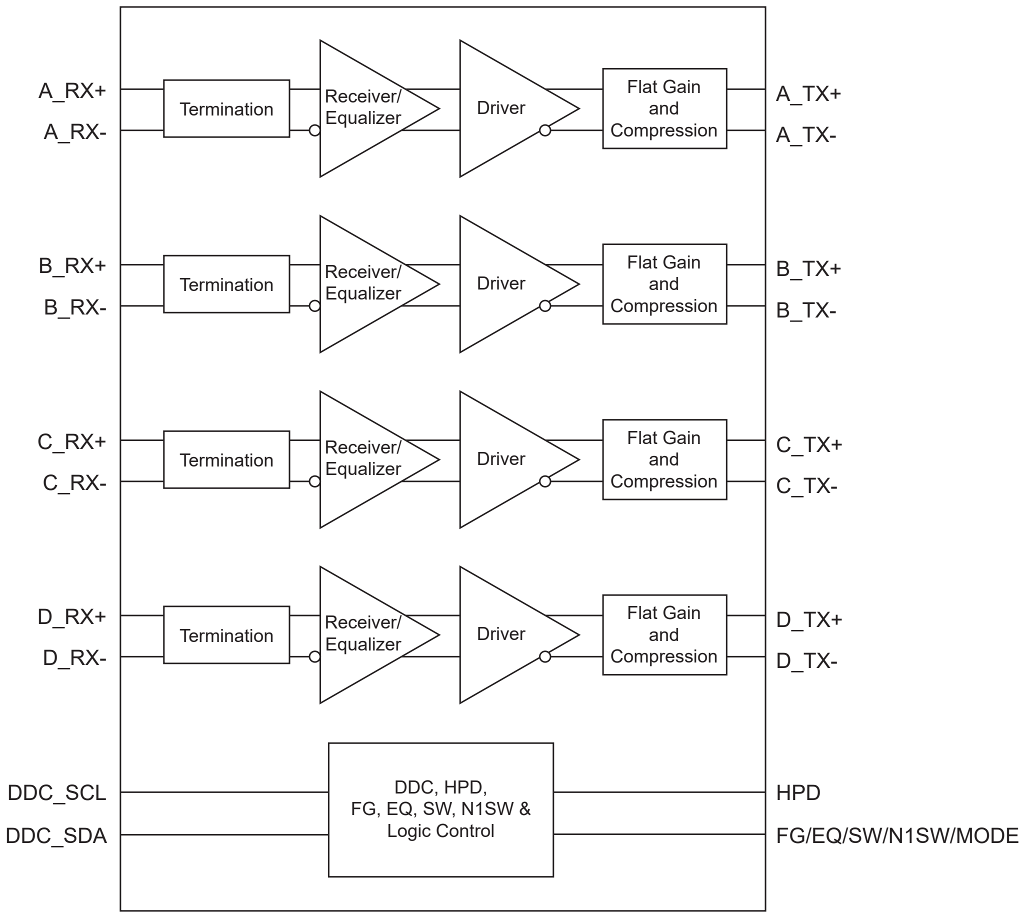
Ordering Information

Orderable Part Number	Package Code	Package Description
PI3HDX12311XEAEX	XEA	32-contact, X1-QFN2845-32

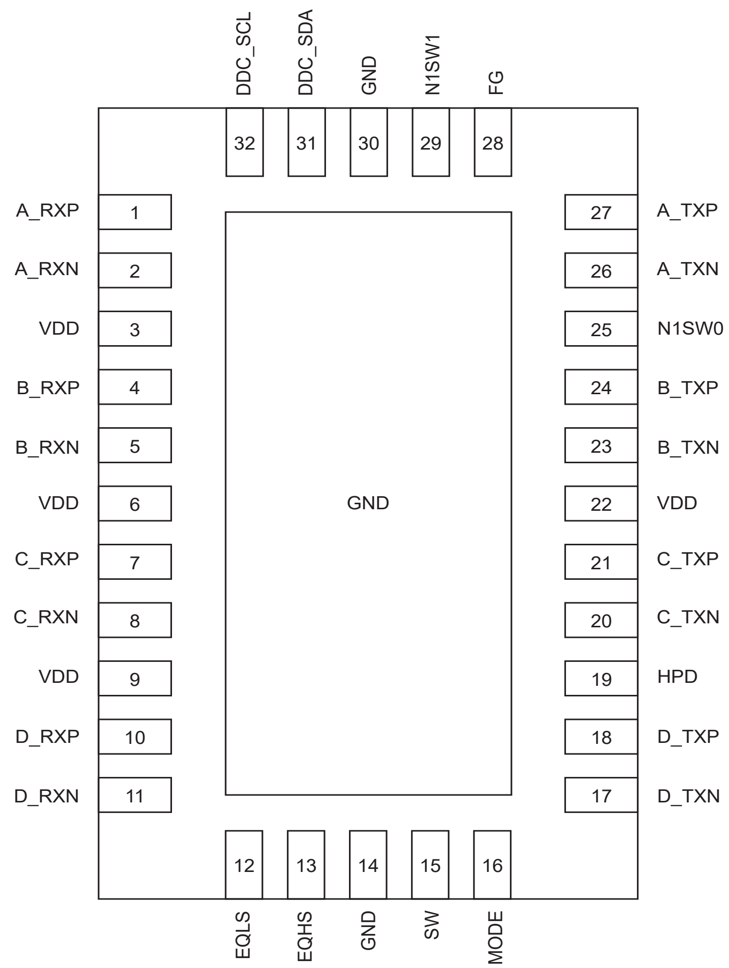
Notes:
- E = Pb-free and Green
- X suffix = Tape/Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Block Diagram



Pin Configuration (Top-Side View)



Pin Description

Pin Number	Pin Name	Type	Description
1	A_RXP	Differential Input	Input differential pair CML inputs, with internal 50Ω pull-up or ~78KΩ pull-up otherwise. Channel D is CLK input in default when TMDS mode.
2	A_RXN		
4	B_RXP	Differential Input	
5	B_RXN		
7	C_RXP	Differential Input	
8	C_RXN		
10	D_RXP	Differential Input	
11	D_RXN		

Pin Number	Pin Name	Type	Description
17	D_TXN	Differential Output	For HDMI 1.4, 50Ω/75Ω to VDD in AC/DC couple For HDMI 2.0/2.1, 100Ω line to line in DC couple, 50Ω to VDD in AC couple
18	D_TXP		
20	C_TXN	Differential Output	
21	C_TXP		
23	B_TXN	Differential Output	
24	B_TXP		
26	A_TXN	Differential Output	
27	A_TXP		
32	DDC_SCL	LVCMOS Input	Auxiliary channels for Display Data Channel snooping.
31	DDC_SDA		
28	FG	4-Level Input	For flat gain control of HDMI 2.0 & 2.1. Default value is “F”. 4-level input pins. With internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
12	EQLS	4-Level Input	LS EQ gain control for Data rate ≤6Gbps. Default “F” With internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
13	EQHS	4-Level Input	HS EQ gain control for Data rate >6Gbps. Default “F”. With internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
15	SW	4-Level Input	For HDMI1.4. Define the output max swing for the non-linear redriving mode, default value is “F”. 4-level input pins. With internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
19	HPD	LVCMOS Input	Hot plug detection from Sink. With internal 100kΩ pull-down resistor. 5V tolerant with external 100kΩ resistor at HPD pin.
25, 29	N1SW0, N1SW1	LVCMOS Input	HDMI2.0 output -1dB linearity swing. Default "L". With internal 300kΩ pull-down resistor.
16	MODE	4-Level Input	Mode selection. Default “F” With internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
3, 6, 9, 22	VDD	Power	3.3V power supply
14, 30, EP	GND	GND	Exposed pad (EP). EP on the package bottom is thermally connected to the die for improved heat transfer out of the package. The pad is electrically connected to the die and is required to be soldered to GND on the PCB board.

Note: All VDD and GND pins must be connected to the same power supply domain for proper device function

Functional Description & Circuit Block Description

Hot Plug Detection (HPD)

The ReDriver monitors the HPD pin of HDMI connector to control the power consumption. When the HPD pin is driven low for more than 2ms, the ReDriver will enter the low power state and all DDC registers will be reset to default value. It will stay in this state until the HPD signal pin is driven high for more than 2ms during a plug in event.
HPD pin with external serial 100kΩ could be connected to HPD 5V signal leveling directly.

Short Circuit Detection

While the short circuit detection feature operates when the TX is in DC coupled mode, the short circuit detection block is active and it will monitor the common mode voltage of the transmitter continuously. If the TX common mode voltage drops below 2 volts, the ReDriver will go into the low power state. The ReDriver will exit low power state once the common mode voltage is driven high. The short circuit detection is on by default in TX DC coupled modes only.

Power Mode

- Short Circuit Mode

This feature is enabled when the TX terminal is in DC coupling. If there is no far-end RX termination present in the TX terminal. Or, if the common mode voltage drops below SCB_VTH. The ReDriver will entry the short circuit mode.

- Unplug Mode

When HPD is low > THPD_UNPLUG, then the channel will go to unplug mode.

- Active Mode

When HPD is high > THPD_ACTIVE. The PI3HDX12311 will enter active mode immediately.

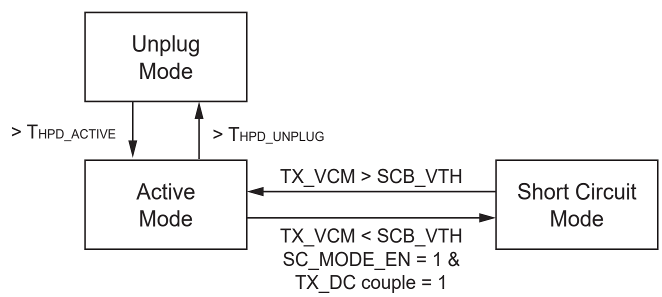


Figure 2. Power Mode

Table 1. Power Mode

HPD Pin	IN_X Pins	OUT_Xx	DDC	Mode
L	RX ~78kΩ to VDD	High-Z	Disabled	UNPLUG Mode
H	RX 50Ω to VDD	TX Active	Active	Normal Operation when HPD = 1

Equalization Setting

The EQLS is the EQ control pin for the datarate ≤6Gbps and the EQHS is the EQ control pin for the datarate > 6Gbps. The EQLS/EQHS pins support real time change. When set to 'L', it will increase about 100% slew rate of CLK and Data channel for HDMI1.4 (FG = H), and increase about 114% slew rate of CLK channel and 73% slew rate of Data channel for HDMI2.0 (FG = F).

Table 2. HDMI1.4 Mode, TX = 50Ω/75Ω to VDD (Typical)

Pin Setting EQLS	EQ @0.825GHz (dB)	EQ @1.7GHz (dB)
L	0.4	1.5
R	1.3	2.7
F (Default)	1.7	3.7
H	2.7	5.6

Table 3. HDMI2.0 mode, TX = 50Ω to VDD or 100Ω line2line, FG = R (Typical)

Pin Setting EQLS	EQ @0.825GHz (dB)	EQ @1.7GHz (dB)	EQ @3GHz (dB)
L	0.4	1.1	2.2
R	1.3	2.3	3.8
F (Default)	1.7	3.3	5.5
H	2.7	5.2	8.3

Table 4. HDMI2.1 Mode, DR = 3Gbps & 6Gbps, TX = 50Ω to VDD or 100Ω line2line, FG = R (Typical)

Pin Setting EQLS	EQ @1.5GHz (dB)	EQ @3GHz (dB)
L	1.1	2.8
R	2.1	4.4
F (Default)	3.0	6.1
H	4.0	7.9

Table 5. HDMI2.1 Mode, DR = 8/10/12Gbps, TX = 50Ω to VDD or 100Ω line2line, FG = R (Typical)

Pin Setting EQHS	EQ @4GHz (dB)	EQ @5GHz (dB)	EQ @6GHz (dB)
L	3.9	4.8	5.6
R	5.7	6.8	7.7
F (Default)	7.8	9.2	10.4
H	9.9	11.5	12.7

Flat Gain Setting

The FG pin is used to set the flat gain of all channels. FG pin supports real time change.

Table 6. Flat Gain Setting (Typical)

FG Pin Setting	FG @100MHz (dB)
L	-0.2
R	0.6
F (Default)	1.4
H	2.3

Output Swing for the Non-Linear ReDriving Mode

The SW pin is used to set the TX output swing for HDMI1.4. The TX output swing is selected based on the Single-Ended Low level voltage range. SW pin supports real time change.

Table 7. TX Swing for HDMI 1.4, TX = 50Ω to VDD (Typical)

SW Pin	VSW_SE_14 (V)		VL_SE_14 (V)
	50Ω to VDD, FG = L TX AC Couple	50Ω to VDD, FG = H TX DC Couple	50Ω to VDD, FG = H TX DC Couple
L	0.53	0.53	−0.54
R	0.55	0.55	−0.56
F (Default)	0.58	0.58	−0.59
H	0.60	0.60	−0.62

Notes: VL_SE_14 relative to VDD.

Output -1dB Linearity Swing for Linear ReDriving Mode

The N1SW[1:0] pins are used to set the -1dB Linearity Swing for HDMI2.0, the -1dB Linearity Swing of HDMI2.1 is fixed internally.

Table 8. TX N1SW[1:0] for HDMI2.0 TX DC/AC Coupling Mode, FG = R

N1SW[1:0] Pins	freq = 100MHz (V)	freq = 3GHz (V)
00	0.87	0.97
01	0.93	1.03
10	0.98	1.09
11	1.03	1.14

Table 9. TX Swing for HDMI 2.0, TX = 100Ω line2line (Typical)

N1SW[1:0] Pins	Vsw_SE_20 (V)	VL_SE_20 (V)
00	0.56	-0.84
01	0.59	-0.89
10	0.61	-0.93
11	0.63	-0.98

Mode Selection Setting

The MODE selection pin is used to set the TX termination type which could be AC/DC coupled and whether the DDC Listener is enabled/disabled.

Table 10. Mode of Operation by Pin Strap Only

MODE	Description
L	• RX = AC/DC Coupled, TX = AC Coupled • DDC_LISTENER_EN=0, TX_SHORT_CIR_DETECT_EN=0 • Default = HDMI 2.1, 12Gbps, All 4 channels enabled, ZTX = 50Ω to VDD
R	• RX = AC/DC Coupled, TX = DC Coupled • DDC_LISTENER_EN=1, TX_SHORT_CIR_DETECT_EN=0 when in HDMI 1.4, TX_SHORT_CIR_DETECT_EN=1 when in HDMI 2.0 & 2.1 • Default = HDMI 1.4 • For HDMI 1.4, ZTX = 150Ω to VDD, DAT_EQ follows EQLS pin, Output Swing follows SW14 pin, CLK_tr/tf > 75ps min, DAT tr/tf > 75ps min • For HDMI 2.0, ZTX = 100Ω line2line, DAT_EQ follows EQLS pin, -1db Linearity Swing follows N1SW1, N1SW0 pins, Flat Gain follows FG pin, CLK_tr/tf > 75ps min, DAT tr/tf > 42.5ps min • For HDMI 2.1, ZTX = 100Ω line2line (Lane3 = 300Ω line2line when in 3-lane mode), EQ Gain follows EQLS or EQHS pins respectively for data rate <= or > 6Gbps, Flat Gain follows FG pin, tr/tf > 22.5ps min • TMDS CLK / FRL D3 = Channel D
F	• RX = AC/DC Coupled, TX = DC Coupled • DDC_LISTENER_EN=1, TX_SHORT_CIR_DETECT_EN=0 when in HDMI 1.4, TX_SHORT_CIR_DETECT_EN=1 when in HDMI 2.0 & 2.1 • Default = HDMI 1.4 • For HDMI 1.4, ZTX = 75Ω to VDD, DAT_EQ follows EQLS pin, Output Swing follows SW14 pin, CLK_tr/tf > 75ps min, DAT tr/tf > 75ps min • For HDMI 2.0, ZTX = 100Ω line2line, DAT_EQ follows EQLS pin, -1db Linearity Swing follows N1SW1, N1SW0 pins, Flat Gain follows FG pin, CLK_tr/tf > 75ps min, DAT tr/tf > 42.5ps min • For HDMI 2.1, ZTX = 100Ω line2line (Lane3 = 300Ω line2line when in 3-lane mode), EQ Gain follows EQLS or EQHS pins respectively for data rate <= or > 6Gbps, Flat Gain follows FG pin, tr/tf > 22.5ps min • TMDS CLK / FRL D3 = Channel D
H	• RX = AC/DC Coupled, TX = DC Coupled • DDC_LISTENER_EN=1, TX_SHORT_CIR_DETECT_EN=0 when in HDMI 1.4, TX_SHORT_CIR_DETECT_EN=1 when in HDMI 2.0 & 2.1 • Default = HDMI 1.4 • For HDMI 1.4, ZTX = 50Ω to VDD, DAT_EQ follows EQLS pin, Output Swing follows SW14 pin, CLK_tr/tf > 75ps min, DAT tr/tf > 75ps min • For HDMI 2.0, ZTX = 100Ω line2line, DAT_EQ follows EQLS pin, -1db Linearity Swing follows N1SW1, N1SW0 pins, Flat Gain follows FG pin, CLK_tr/tf > 75ps min, DAT tr/tf > 42.5ps min • For HDMI 2.1, ZTX = 100Ω line2line (Lane3 = 300Ω line2line when in 3-lane mode), EQ Gain follows EQLS or EQHS pins respectively for data rate <= or > 6Gbps, Flat Gain follows FG pin, tr/tf > 22.5ps min • TMDS CLK / FRL D3 = Channel D

DDC Listener Specification

The DDC_SDA and DDC_SCL shall meet the requirements specified in the I2C bus specification, version 2.1, section 15 for "Standard-Mode" devices. The HDMI devices must have DDC electrical characteristics complying with the values shown in Table 11.

Table 11. DDC Snoop I2C Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IL}	Low-level input voltage	–0.3		0.3*VDD	V
V_{IH}	High-level input voltage	0.7*VDD		VDD+0.3	V
f_{SCL}	I^2C DDC clock frequency			1	MHz
t_{BUF}	Bus free time between START and STOP conditions	4.7			µs
t_{HD_STA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	4			µs
t_{LOW}	Low period of the I^2C clock	4.7			µs
t_{HIGH}	High period of the I^2C clock	4			µs
t_{SU_STA}	Setup time for a repeated START condition	4.7			µs
t_{HD_DAT}	Data hold time	0			µs
t_{SUDAT}	Data setup time	250			ns

By the DDC_SDA and DDC_SCL pins, the HDMI Forum Vendor Specific Data Block (HF-VSDB) located at target address 0xA8 will be snooped. The DDC snoop function will monitor both reads and writes to specific offsets of the Status and Control Data Channel Structure (SCDCS) located within the HF-VSDB.

The following SCDCS offsets registers are monitored:

1. 20h: TMDS Configuration.
2. 31h: Sink Configuration.
3. 35h: Source Test Configuration.
4. 40h, 41h and 42h: Status Flags.

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	−65°C to +150°C
Supply Voltage[1]	−0.3V to +3.8V
Voltage Range at Any Input or Output Terminal	
Differential I/O, Voltage Between Differential Pairs	−0.3V to +1.89V
LVCMOS Inputs	−0.3V to VDD+0.3V
Voltage Range for HPD Input Pin	−0.3V to +3.8V
Electrostatic Discharge	
Human Body Model (All Pins) [2]	7KV
Charged Device Model (All pins) [2]	1KV
Max Junction Temperature	125°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
1. All voltage values are with respect to the GND terminals.
2. Tested in accordance with JEDEC Standard.
3. IEC 61000−4−2 system level ESD cannot be guaranteed or defined, since it is a system level specification. It is up to the system designer to determine the correct method to meet their IEC requirements and to protect the ReDriver device from electrical overstress events. The PI3HDX12311 is not designed or intended to protect systems from IEC 61000−4−2 events.

Recommended Operating Conditions

Over operating free−air temperature range (unless otherwise noted)

Symbol	Description	Min.	Typ.	Max.	Units
V_{DD_DC}	Main power supply when the RX terminals are in DC couple.	3.135	3.3	3.465	V
V_{DD_AC}	Main power supply when the RX terminals are in AC couple.	3.0	3.3	3.6	V
T_A	Operating free−air temperature	−40		+70	°C
C_{AC}	AC coupling capacitor	75	100	265	nF

Thermal Information

Symbol	Parameter	X1-QFN32 (XEA32)	Units
Theta JA	Junction-to-ambient resistance	34.29	°C/W

Power Supply Characteristics

Parameter		Test Conditions	Min.	Typ.[1]	Max.	Units
ICC	Active	HDMI 2.1/2.0 Active link with 4 channels enabled. AC coupled RX and DC coupled TX. N1SW<1:0> = 11.		130	170	mA
		HDMI 1.4 Active link with 4 channels enabled. AC coupled RX and DC coupled TX. SW = R. 50Ω to VDD.		180	220	mA
		HDMI 2.1/2.0/1.4 Active link with 4 channels enabled. AC coupled RX and AC coupled TX. 50Ω to VDD.		220	310	mA
	TX Short Circuit	TX common mode voltage drops below the short circuit detection threshold (SCB_VTH).		1.7	5	mA
	Unplug	HPD is Low for > THPD_UNPLUG		280	1500	uA
T_{VDD_Ramp}		Supply ramp up time required, 10 to 90%.	0.1		50	ms

Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
T_{POR}	Internal POR de-assertion delay	0.01		5	ms

Note:
1. Typ values use VDD = 3.3V, T_A = 25°C.
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

LVCMOS Control Pin Characteristics

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
2–STATE LVCMOS INPUTS (N1SW[1:0])						
V_{IH}	High–level input voltage		0.7*VDD		VDD+0.3	V
V_{IL}	Low–level input voltage				0.30*VDD	V
I_{IH}	High–level input current	V_{IN} = 3.465V, VDD = 3.465V		16	25	µA
I_{IL}	Low–level input current	V_{IN} = GND, VDD = 3.465V	–25	–10		µA
4–STATE LVCMOS INPUTS (EQLS, EQHS, SW, MODE, FG)						
V_{IH}	DC input logic High, setting “H”		0.92*VDD	VDD	VDD+0.3	V
V_{IF}	DC input logic 2/3 VDD, setting “F”		0.59*VDD	0.67*VDD	0.75*VDD	V
V_{IR}	DC input logic 1/3 VDD, setting “R”		0.25*VDD	0.33*VDD	0.41*VDD	V
V_{IL}	DC input logic Low, setting “L”			GND	0.08*VDD	V
R_{ext}	External resistor for setting “R”	Rext connects to GND	64	68	71	kΩ
I_{IH}	High–level input current	V_{IN} = 3.465V, VDD = 3.465V		16	21	µA
I_{IL}	Low–level input current	V_{IN} = GND, VDD = 3.465V	–41	–32		µA
R_{PU}	Internal pull–up resistance			100		kΩ
R_{PD}	Internal pull–down resistance			200		kΩ

HPD Characteristics

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{HPD_UNPLUG}	HPD de-bounce time before declaring Unplug. Enter Unplug if HPD is low after de-bounce time.		2		4	ms
T_{HPD_ACTIVE}	HPD de-bounce time required for exiting Unplug to Active. Exit Unplug if HPD is high after de-bounce time.		2		4	ms
V_{IH_SNK}	High level input voltage to HPD with external 100KΩ resister is connected to HPD	Test with external 100KΩ resistor is connected to HPD pin	2		5.5	V

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{IL_SNK}	Low level input voltage to HPD with external 100KΩ resister is connected to HPD	Test with external 100KΩ resistor is connected to HPD pin	−0.3		0.8	V
I_{IH_SNK}	High-level input current for HPD	Device powered; V_{IH_SNK} = 3.6V; Includes internal pull-down resistor	25		50	µA
I_{IL_SNK}	Low-level input current for HPD	Device powered; V_{IL_SNK} = 0V; Includes internal pull-down resistor	–5		5	µA
R_{pdHPD}	HPD termination to GND	VDD = 3.3V		100		KΩ

Receiver AC/DC Characteristics

Over operating free–air temperature range (unless otherwise noted)

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
$VID_{(EYE)}$	Input differential, High frequency eye height	PRBS7 pattern	50		1200	mVppd
$VID\_DAT_{(SW)}$	Input differential voltage pk–pk Swing for Data Channel		800		1200	mVppd
$VID\_CLK_{(SW)}$	Input differential voltage pk–pk Swing for TMDS Clock		400		1200	mVppd
V_{RX-CM}	Common–mode bias voltage for the receiver terminal.	Any ReDriver settings	2.5		VDD	V
$Z_{RX-DIFF}$	Differential input impedance (DC)	Active state	85	100	115	Ω
$Z_{RX-HIGH-IMP}$	Common–mode input impedance with termination disabled (DC)	Enable = 0V, measured from RX pins to VDD.	50			kΩ
$D_{R\_RX\_DATA}$	Data lanes data rate		0.25		12	Gbps
$D_{R\_RX\_CLK}$	Clock lanes data rate		0.25		12	Gbps
G_{TMDS14}	Peaking gain (Compensation at 1.7GHz, relative to 100MHz, 100mVppd sine wave input)	EQLS = L EQLS = R EQLS = F EQLS = H TX in AC/DC coupling mode, 50Ω/75Ω to VDD		1.5 2.7 3.7 5.6		dB
		Variation around typical	–3		+3	dB

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
G_{TMDS20}	Peaking gain (Compensation at 3GHz, relative to 100MHz, 100mVppd sine wave input)	EQLS = L EQLS = R EQLS = F EQLS = H TX in AC/DC coupling mode, 50Ω to VDD/100Ω line2line. Pin mode default FG		2.2 3.8 5.5 8.3		dB
		Variation around typical	–3		+3	
G_{FRL}	Peaking gain (Compensation at 6GHz, relative to 100MHz, 100mVppd sine wave input)	EQHS = L EQHS = R EQHS = F EQHS = H TX in AC/DC coupling mode, 50Ω to VDD/100Ω line2line. Pin mode default FG		5.6 7.7 10.4 12.7		dB
		Variation around typical	–3		+3	

Transmitter AC/DC Characteristics

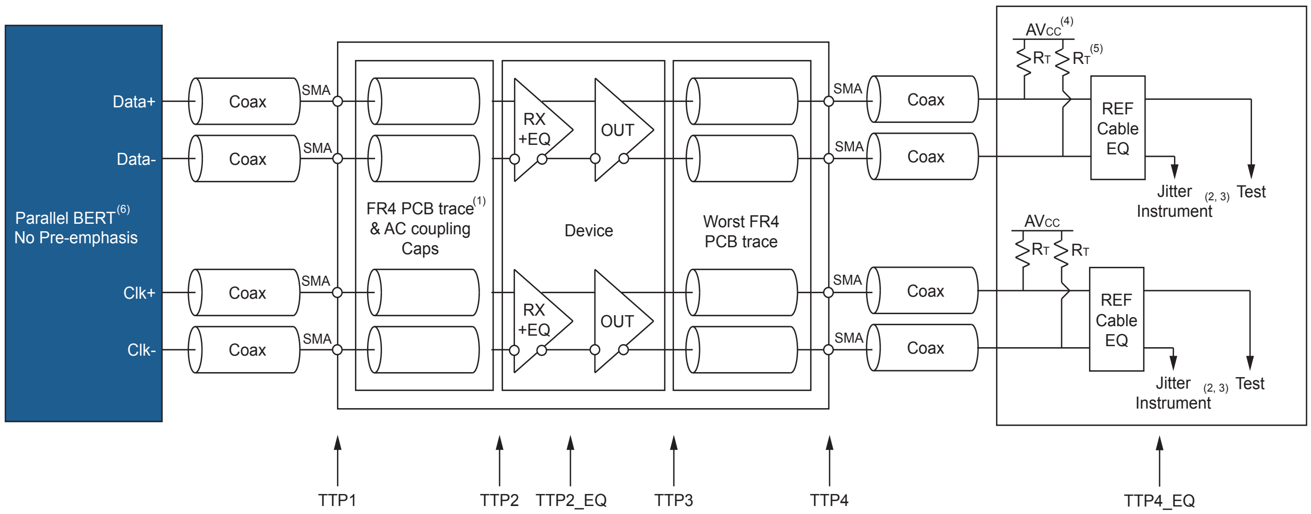
Over operating free–air temperature range (unless otherwise noted)

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
Z_{TX-L2L}	Differential line to line output impedance	Refer to mode tables	255 85	300 100	345 115	Ω
Z_{TX-SE}	Single-Ended output impedance to VDD	Refer to mode tables	127.5 63.75 42.5	150 75 50	172.5 86.25 57.5	Ω
I_{TX-SC}	TX short circuit current	TX ± shorted to GND, maximum current supplied by device. Any DC coupled mode.		1	10	uA
FG	Flat gain at 100MHz. For both TX with AC/DC coupling.	FG = L FG = R FG = F FG = H		-0.2 0.6 1.4 2.3		dB
		Variation around typical	–3		+3	
$V_{TMDS\_OL\_14}$	Single-Ended Low Level voltage range for HDMI 1.4	At TTP3; RX Data SW = 800-1200mVppd, SW pin = L; TX 50Ω to VDD.	VDD –600		VDD –400	mV
$V_{TMDS\_DAT\_OL\_20}$	Single-Ended Low Level voltage range for TMDS Data channels 0, 1, 2	At TTP3; RX Data SW = 800-1200mVppd	VDD –1000		VDD –400	mV
$V_{TMDS\_CLK\_OL\_20}$	Single-Ended Low Level voltage range for TMDS Clock channels	At TTP3; RX CLK SW = 400-1200mVppd	VDD –1000		VDD –200	mV

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{TMDS\_DAT\_SW}$	Single-Ended Swing Voltage: TMDS Data Channel 0, 1, 2	At TTP3; RX Data SW = 800-1200mVppd, SW pin = L; TX 50Ω to VDD.	0.4		0.6	Vpp
$V_{TMDS\_CLK\_SW}$	Single-Ended Swing Voltage: TMDS Clock Channel	At TTP3; RX CLK SW = 400-1200mVppd, SW pin = L; TX 50Ω to VDD.	0.2		0.6	Vpp
V_{FRL_CM}	DC Common Mode Voltage range for FRL channels	At TTP3; RX CLK SW= 400-1200mVppd	VDD −800		VDD +30	mV
V_{FRL_SW}	Differential Ended Swing Voltage: FRL Channel	At TTP3; RX Data SW = 400-1200mVppd	0.4		1.2	Vppd
$V_{FRL\_TX\_-1B\_100MHz}$	Differential transmitter output -1dB compression point @100MHz.			930		mVppd
$V_{FRL\_TX\_-1B\_6GHz}$	Differential transmitter output -1dB compression point @6GHz.			910		mVppd
$V_{CM\_L\_X\_pp}$	AC common mode noise (Peak to peak)	FRL modes, PRBS2^7 signal. VCM_L_X_pp = (Dp + Dn)/2			150	mVpp
$V_{TX\text{-}Idle\text{-}Diff\text{-}AC\text{-}pp}$	Idle mode AC common mode delta voltage|VTX-D+-VTX-D-|	Between Tx+ and Tx- in idle mode. Use the HPF to remove DC components. =1/LPF. No AC and DC signals are applied to Rx terminals			10	mV
$V_{TX\text{-}Idle\text{-}Diff\text{-}DC}$	Idle mode DC common mode delta voltage|VTX-D+-VTX-D-|	Between Tx+ and Tx- in idle mode. Use the LPF to remove DC components. =1/HPF. No AC and DC signals are applied to Rx terminals.			15	mV
V_{OFF}	Single−ended standby (off) output voltage	VDD = 0V, Power supply of far end receiver AVCC = 3.3V	AVCC −10		AVCC +10	mV
$t_{RF\text{-}CLK\text{-}14}$	Transition time (rise and fall time) for clock lane when operating at HDMI1.4	At TTP4; 20% to 80%; Clock Frequency = 300MHz	75			ps
$t_{RF\text{-}CLK\text{-}20}$	Transition time (rise and fall time) for clock lane when operating at HDMI 2.0	At TTP4; 20% to 80%; Clock Frequency = 150MHz	75			ps
$t_{RF\text{-}DAT\_14}$	Transition time (rise and fall time) for data lanes when operating at HDMI 1.4	At TTP4; 20% to 80%; DR = 3Gbps; PRBS7 pattern; Clock Frequency = 300MHz	75			ps
$t_{RF\text{-}DAT\_20}$	Transition time (rise and fall time) for data lanes when operating at HDMI 2.0	At TTP4; 20% to 80%; DR = 6Gbps; PRBS7 pattern; Clock Frequency = 150MHz	42.5			ps
t_{RF_FRL}	Transition time (rise and fall time) for FRL	At TTP4; 20% to 80%; DR = 12Gbps; PRBS7 pattern	22.5			ps

<table>
<tr><th>Symbol</th><th>Description</th><th colspan="2">Test Conditions</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Units</th></tr>
<tr><td>t_{RF-MM}</td><td>Output rise, fall time mismatch</td><td colspan="2">20% – 80% of differential voltage measured 1 inch from the output pin. Fastest rise and fall time setting, EQ = default, FG = R</td><td></td><td>5</td><td></td><td>ps</td></tr>
<tr><td>$t_{diff-LH}$, $t_{diff-HL}$</td><td>Differential propagation delay</td><td colspan="2">EQ = default, FG = R, SW = default, Fastest rise and fall time.</td><td></td><td>130</td><td></td><td>ps</td></tr>
<tr><td>T_{sk1}</td><td>Intra–pair output skew (within lane)</td><td colspan="2">EQ = default, FG =R, SW/N1SW = default, Fastest rise and fall time.</td><td></td><td></td><td>0.15</td><td>Tbit</td></tr>
<tr><td>T_{sk2}</td><td>Inter–pair output skew (lane to lane)</td><td colspan="2">EQ = default, FG =R, SW/N1SW = default, Fastest rise and fall time.</td><td></td><td></td><td>0.2</td><td>Tbit</td></tr>
<tr><td>$T_{TMDS14\_CLK\_TJ}$</td><td>HDMI 1.4 TMDS Clock pk-pk total jitter</td><td colspan="2">TTP4 TMDS Differential clock jitter. For HDMI 1.4</td><td></td><td></td><td>0.3</td><td>Tbit</td></tr>
<tr><td>$T_{TMDS20\_CLK\_TJ}$</td><td>HDMI 2.0 TMDS Clock pk-pk total jitter</td><td colspan="2">TTP4_EQ TMDS Differential clock jitter. For HDMI 2.0</td><td></td><td></td><td>0.3</td><td>Tbit</td></tr>
<tr><td>$T_{TMDS14\_DAT\_EW}$</td><td>HDMI 1.4 TMDS Data eye width</td><td colspan="2">TTP4 TMDS Differential eye Width. For HDMI 1.4</td><td>0.5</td><td></td><td></td><td>Tbit</td></tr>
<tr><td rowspan="3">$T_{TMDS14\_DAT\_EH}$</td><td rowspan="3">HDMI 1.4 TMDS Data eye height vs DataRate</td><td rowspan="3">TTP4 TMDS Differential eye opening For HDMI 1.4</td><td>0.25UI</td><td>0</td><td></td><td></td><td rowspan="3">mV</td></tr>
<tr><td>0.35 to 0.65UI</td><td>–75</td><td></td><td>75</td></tr>
<tr><td>0.75UI</td><td>0</td><td></td><td></td></tr>
<tr><td rowspan="3">$T_{TMDS20\_DAT\_EW}$</td><td rowspan="3">HDMI 2.0 TMDS Data eye width vs DataRate (Rbit)</td><td rowspan="3">TTP4_EQ TMDS Differential eye Width. For HDMI 1.4</td><td>3.4< Rbit ≤3.712</td><td>0.6</td><td></td><td></td><td rowspan="3">Tbit</td></tr>
<tr><td>3.712< Rbit <5.94</td><td>$-0.0332Rbit^2 + 0.2312Rbit + 0.1998$</td><td></td><td></td></tr>
<tr><td>5.94≤ Rbit ≤6.0</td><td>0.4</td><td></td><td></td></tr>
<tr><td rowspan="3">$T_{TMDS20\_DAT\_EH}$</td><td rowspan="3">HDMI 2.0 TMDS Data eye height at 0.5UI vs DataRate</td><td rowspan="3">TTP4_EQ TMDS Differential eye height for HDMI 2.0</td><td>3.4< Rbit ≤3.712</td><td>335</td><td></td><td></td><td rowspan="3">mVppd</td></tr>
<tr><td>3.712< Rbit <5.94</td><td>$-19.66Rbit^2 + 106.74Rbi + 209.58$</td><td></td><td></td></tr>
<tr><td>5.94≤ Rbit ≤6.0</td><td>150</td><td></td><td></td></tr>
<tr><td rowspan="5">T_{FRL_EW}</td><td rowspan="5">FRL Data eye width vs Datarate</td><td rowspan="5">TTP4_EQ FRL Differential eye height</td><td>3Gbps</td><td>0.5</td><td></td><td></td><td rowspan="5">Tbit</td></tr>
<tr><td>6Gbps</td><td>0.4</td><td></td><td></td></tr>
<tr><td>8Gbps</td><td>0.385</td><td></td><td></td></tr>
<tr><td>10Gbps</td><td>0.37</td><td></td><td></td></tr>
<tr><td>12Gbps</td><td>0.35</td><td></td><td></td></tr>
</table>

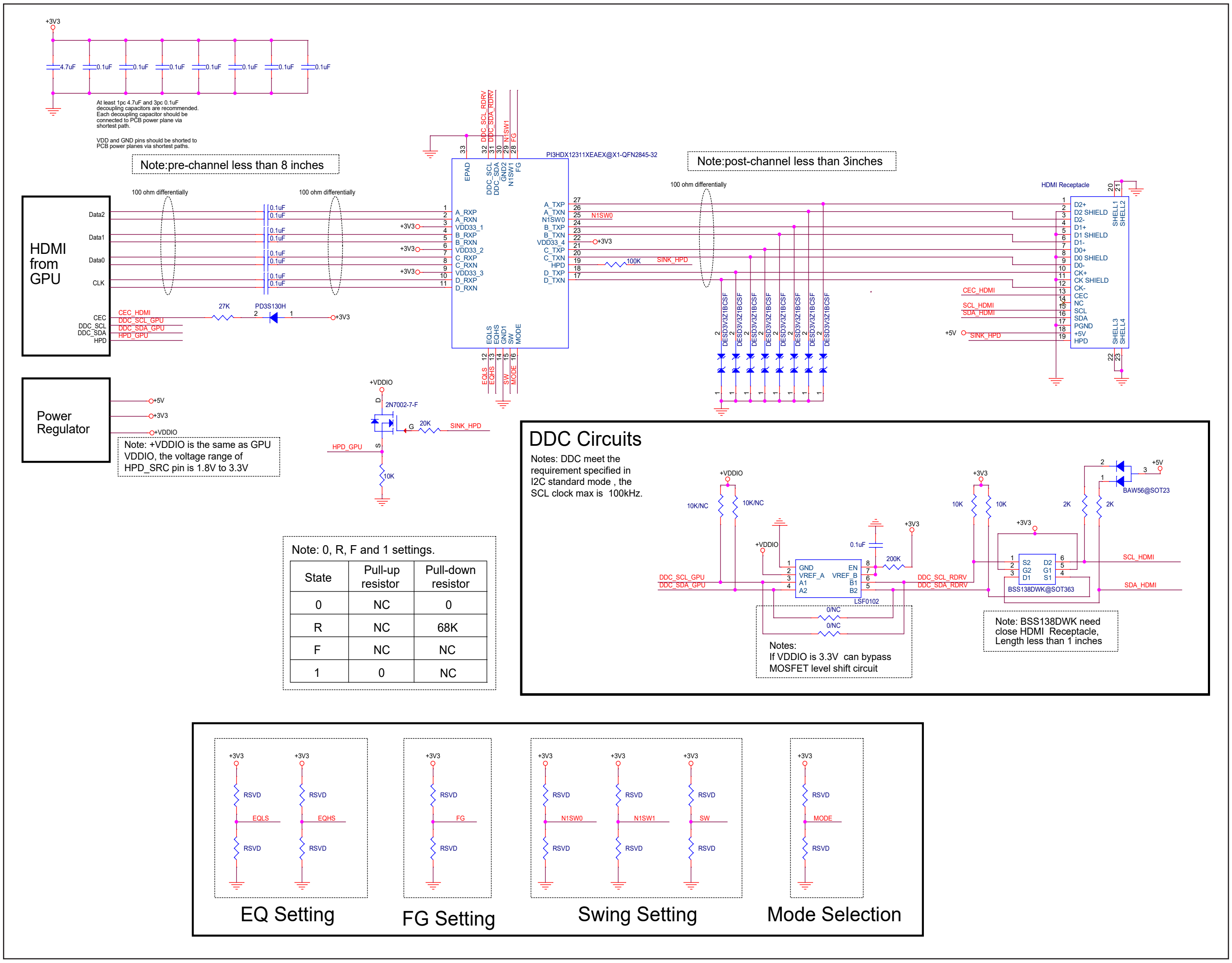
Symbol	Description	Test Conditions		Min.	Typ.	Max.	Units
T_{FRL_EH}	FRL Data eye height vs Datarate	TTP4_EQ FRL Differential eye height	3Gbps	150			mVppd
			6Gbps	150			
			8Gbps	135			
			10Gbps	120			
			12Gbps	100			
$X_{TALKDIFF}$	Differential near–end cross talk	Adjacent channels measured. Channel gain is subtracted.			–38		dB
$R_{LDIFF11}$	Differential return loss, SDD11	F ≤ 6GHz			–12		dB
$R_{LDIFF22}$	Differential return loss, SDD22	F ≤ 6GHz			–8		dB



1. The FR4 trace between TTP1 and TTP2 is designed to emulate 1-12” of FR4, AC-coupling cap, connector and another 2” of FR4. Trace width - 4mils. 100Ω differential impedance.
2. All Jitter is measured at a BER of 10^{9}. HDMI 2.1 jitter measured at BER 10^{-10}.
3. Residual jitter reflects the total jitter measured at TTP4 minus the jitter measured at TTP.
4. AVCC = 3.3V.
5. RT = 50Ω.
6. For HDMI 1.4 or 2.0, the input signal from parallel Bert does not have any pre-emphasis or de-emphasis. For HDMI 2.1 FRL, the input signal from BERT will have 2.18dB pre-shoot and -3.1dB de-emphasis. Refer to Recommended Operating Conditions.

Figure 3. HDMI Output Jitter Measurement Setup

Application Schematic



Note: 0, R, F and 1 settings.

State	Pull-up resistor	Pull-down resistor
0	NC	0
R	NC	68K
F	NC	NC
1	0	NC

Layout Design Guideline

As transmission data rate increases rapidly, any flaws and/or mis-matches on PCB layout are amplified in terms of signal integrity. Layout guideline for high-speed transmission is highlighted in this application note.

Power and GROUND

To provide a clean power supply for Diodes high-speed device, few recommendations are listed below:

- Power (VCC) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly without passing through any resistor.
- The thickness of the PCB dielectric layer should be minimized such that the VCC and GND planes create low inductance paths.
- One low-ESR 0.1uF decoupling capacitor should be mounted at each VCC pin. Capacitors of smaller body size, i.e. 0402 package, is more preferable as the insertion loss is lower. The capacitor should be placed next to the VCC pin.
- One capacitor with capacitance of 4.7uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- A ferrite bead (optional) for isolating the power supply for Diodes high-speed device from the power supplies for other parts on the printed circuit board should be implemented.
- Several thermal ground vias must be required on the thermal pad. 25-mil or less pad size and 14-mil or less finished hole are recommended.

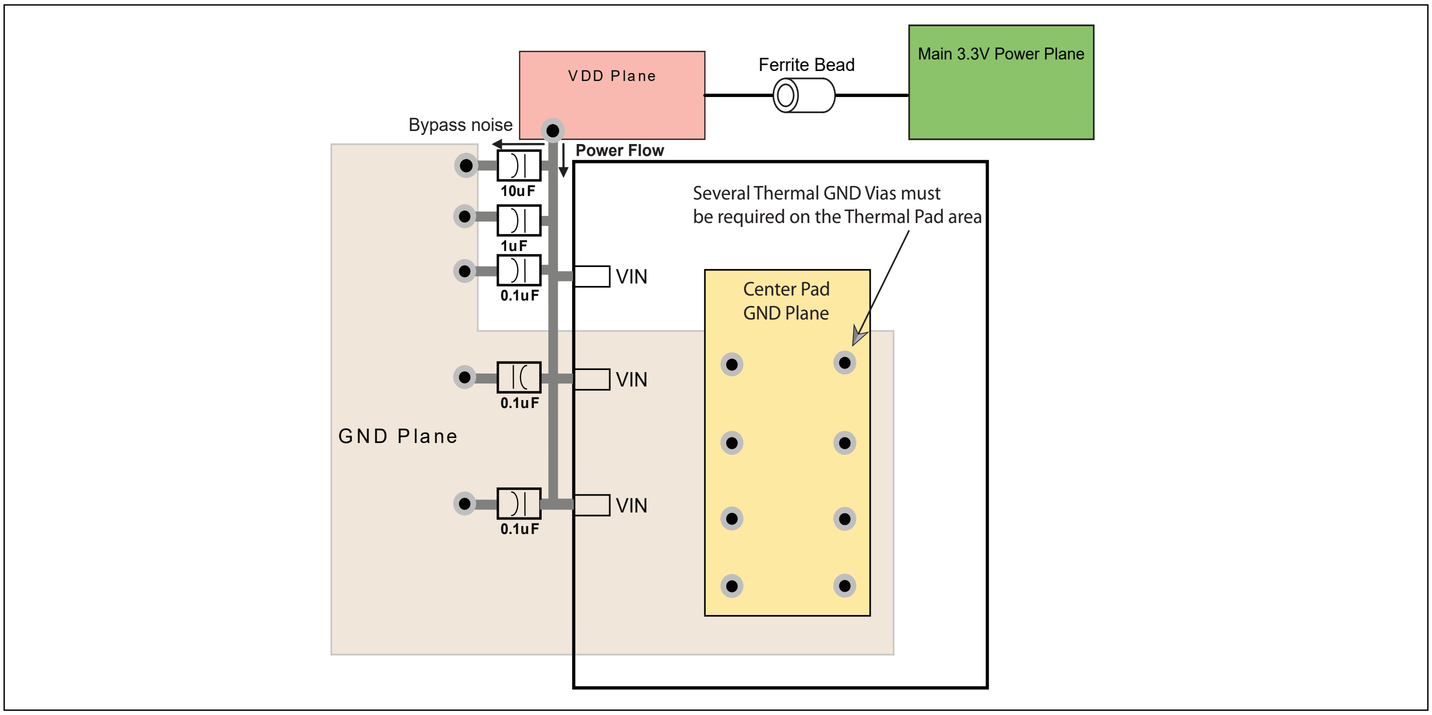


Figure 4. Decoupling Capacitor Placement Diagram

High-speed Signal Routing

Well-designed layout is essential to prevent signal reflection:

- For 100Ω differential impedance, width-spacing-width micro-strip of 5-7-5 mils is recommended.
- Differential impedance tolerance is targeted at ±15%.

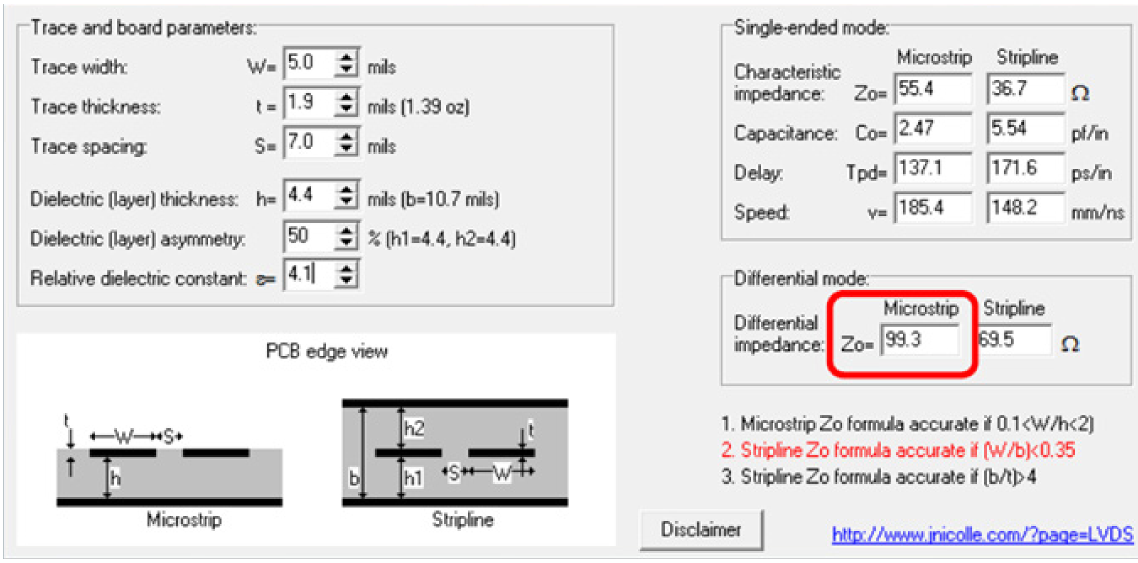


Figure 5. Trace Width and Clearance of Micro-strip and Strip-line

- For micro-strip, using 1/2oz Cu is fine. For strip-line in 6+ PCB layers, 1oz Cu is more preferable.

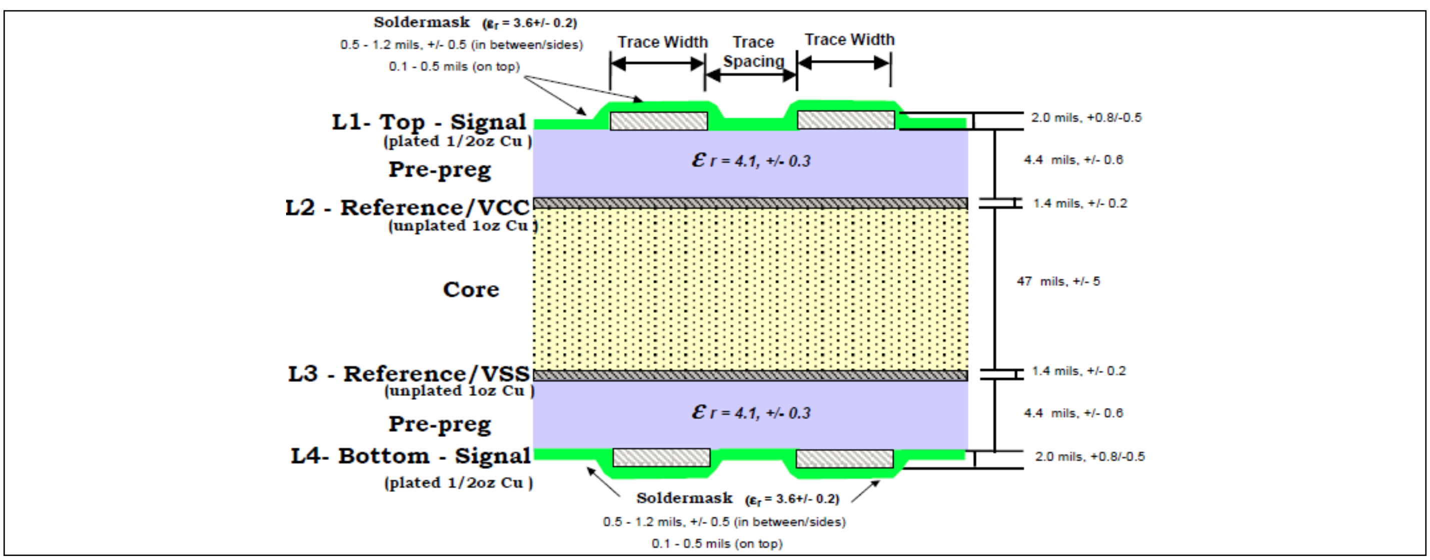


Figure 6. 4-Layer PCB Stack-up Example

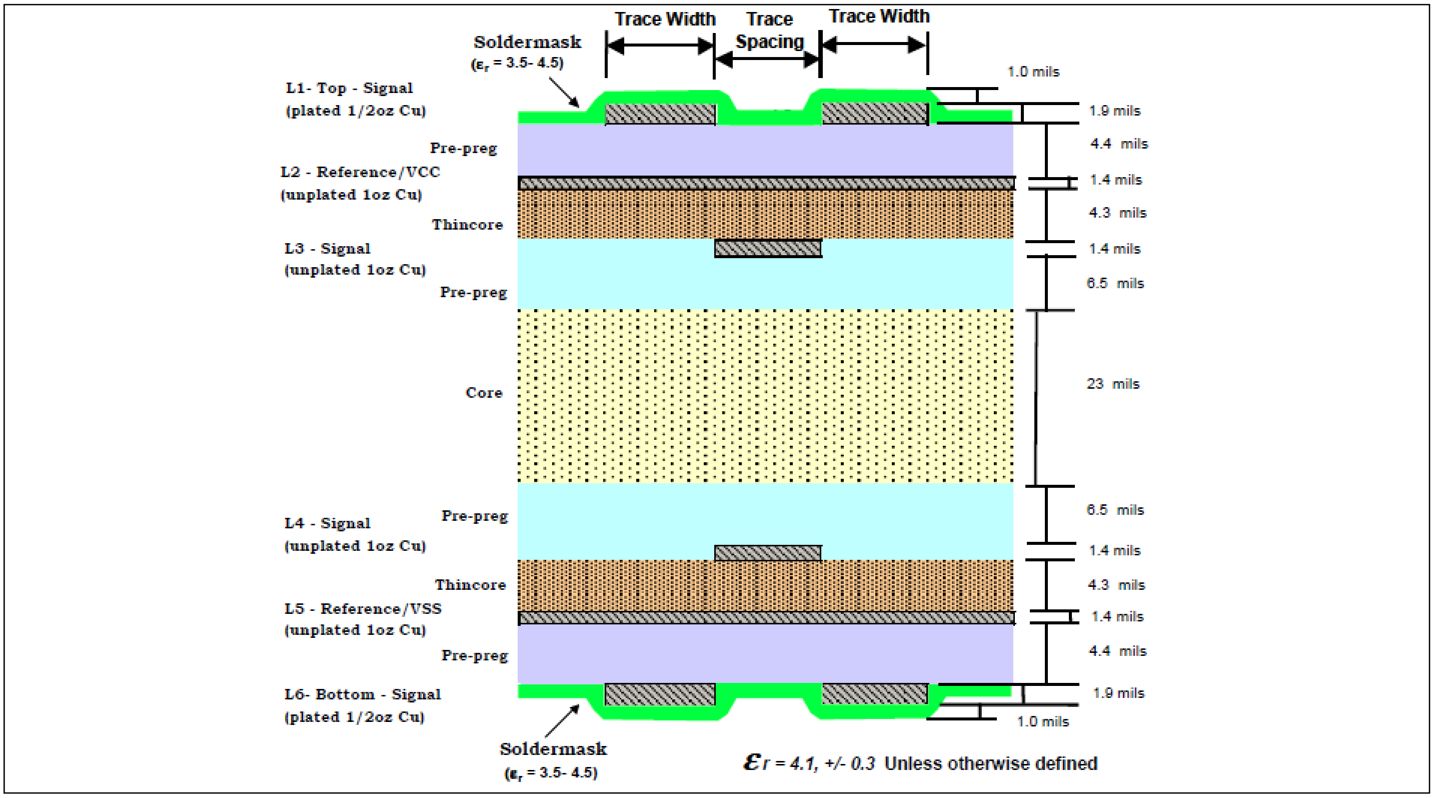


Figure 7. 6-Layer PCB Stack-up Example

- Ground referencing is highly recommended. If unavoidable, stitching capacitors of 0.1uF should be placed when reference plane is changed.

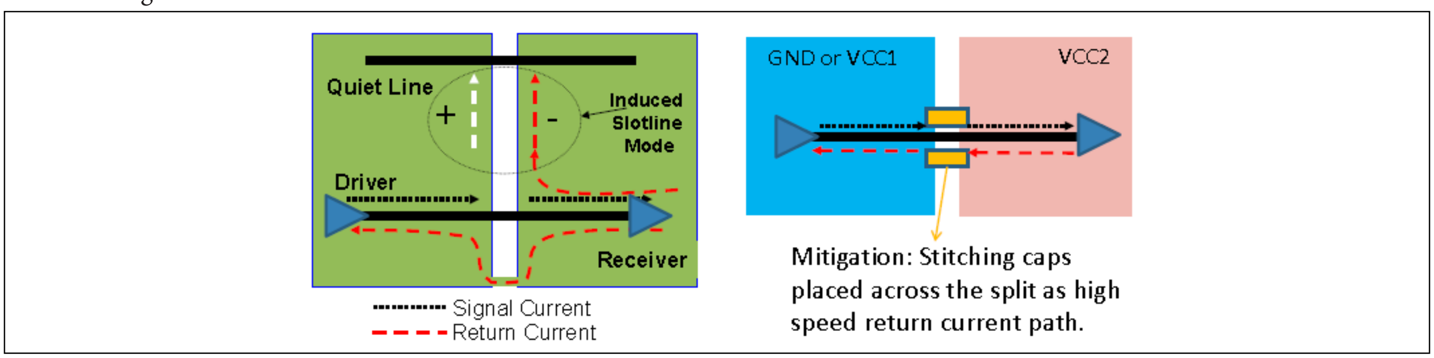


Figure 8. Stitching Capacitor Placement

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

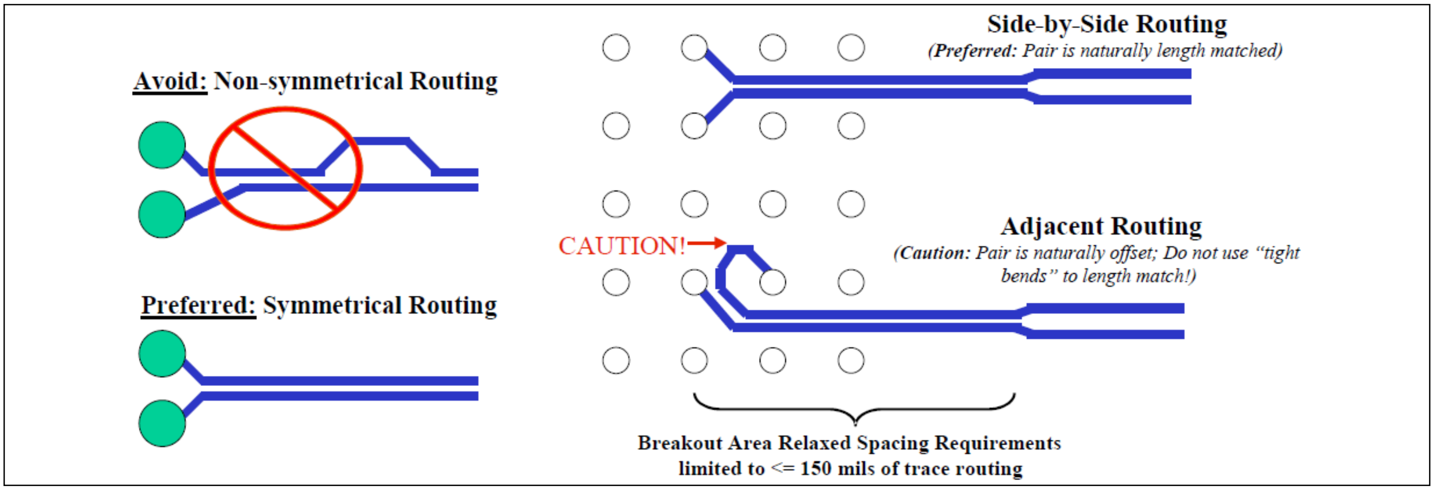


Figure 9. Layout Guidance of Matched Differential Pair

- For minimal cross-talk, inter-pair spacing between two differential micro-strip pairs should be at least 20 mils or 4 times the dielectric thickness of the PCB.
- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- To minimize signal loss and jitter, tight bend is not recommended. All angles α should be at least 135 degrees. The inner air gap A should be at least 4 times the dielectric thickness of the PCB.

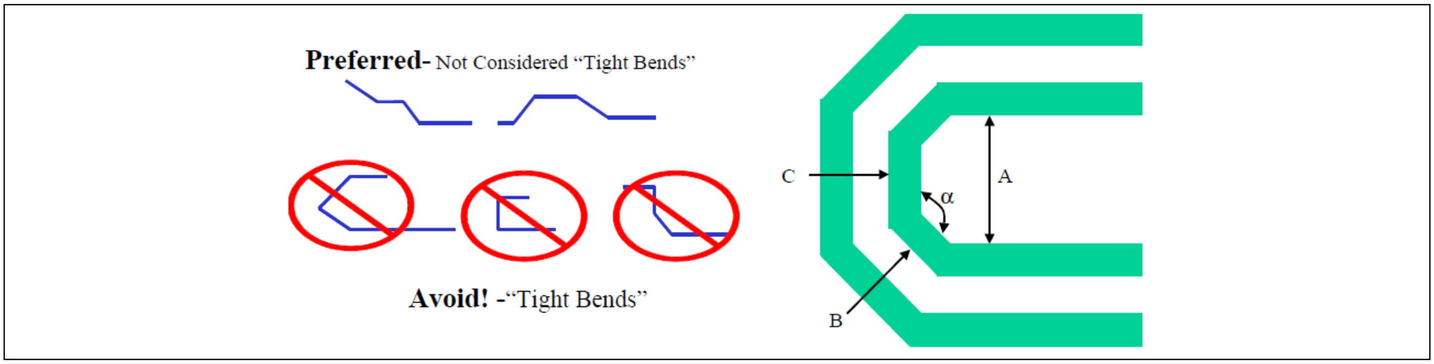


Figure 10. Layout Guidance of Bends

- Stub creation should be avoided when placing shunt components on a differential pair.

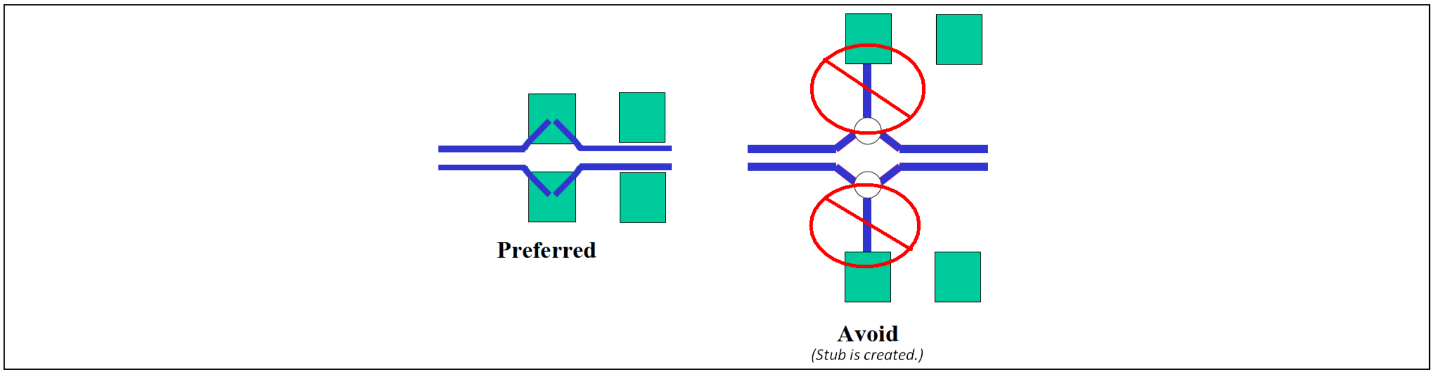


Figure 11. Layout Guidance of Shunt Component

- Placement of series components on a differential pair should be symmetrical.

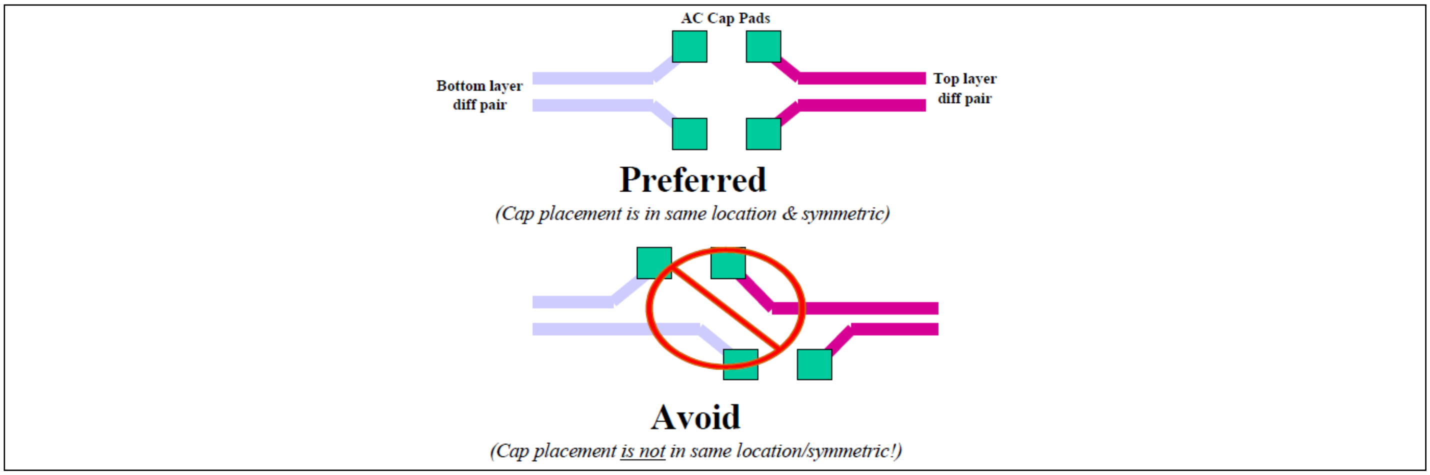


Figure 12. Layout Guidance of Series Component

- Stitching via or test points must be used sparingly and placed symmetrically on a differential pair.

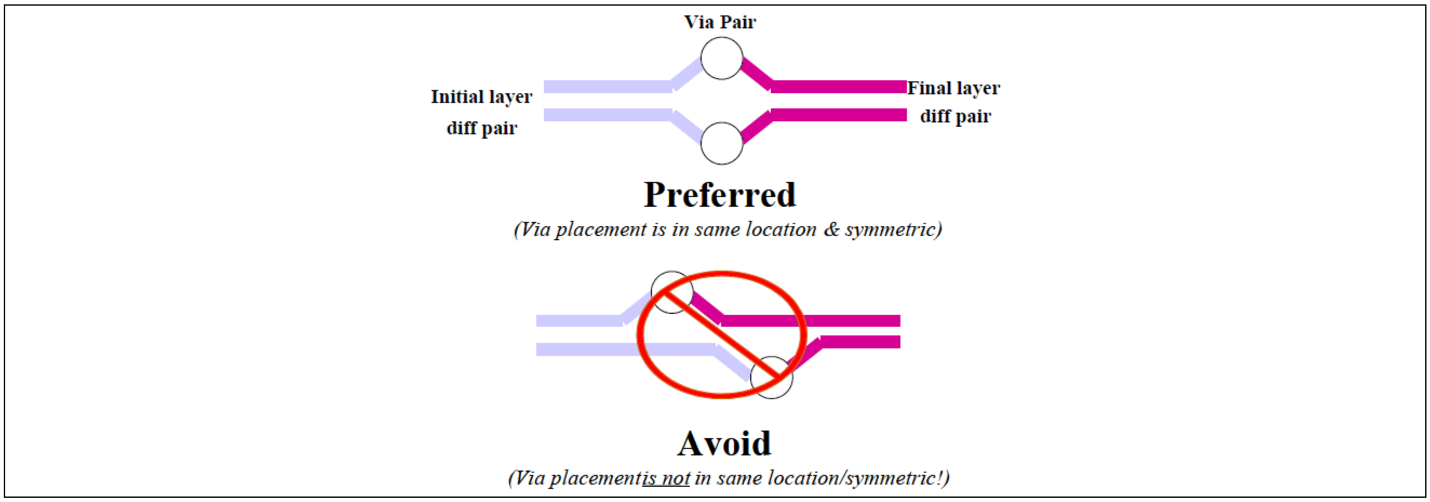
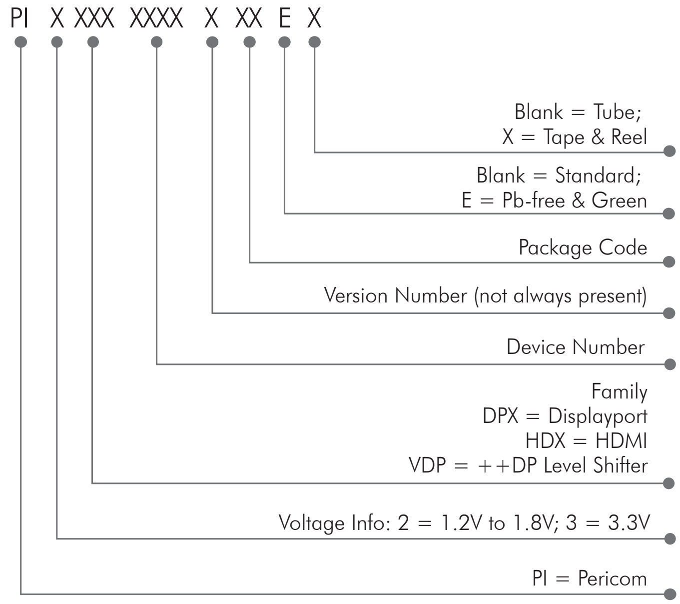
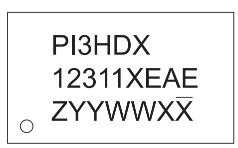


Figure 13. Layout Guidance of Stitching Via

Part Marking Information



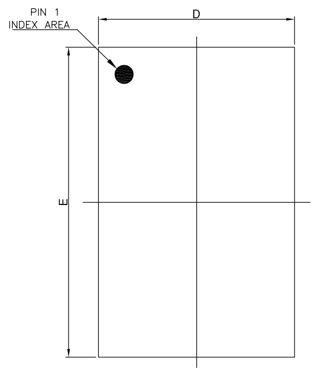
Part Marking



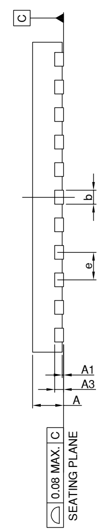
Z: Die Rev
YY: Date Code (Year)
WW: Date Code (Workweek)
1st X: Assembly Code
2nd X: Fab Code
Bar above 2nd "X" means Cu wire

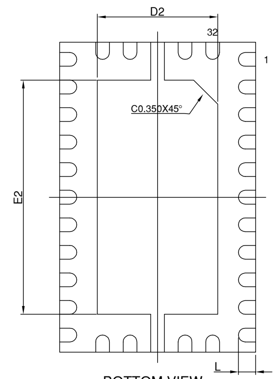
Packaging Mechanical

32-X1QFN (XEA)

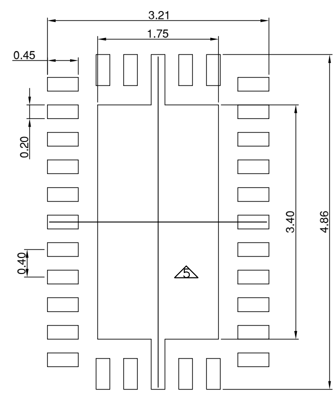


TOP VIEW





BOTTOM VIEW



RECOMMENDED LAND PATTERN

SYMBOLS	MIN.	NOM.	MAX.
A	0.40	0.45	0.50
A1	0.00	0.02	0.05
A3		0.127 REF.	
b	0.15	0.20	0.25
D	2.75	2.85	2.95
E	4.40	4.50	4.60
e		0.40 BSC	
L	0.20	0.25	0.30
D2	1.70	1.75	1.80
E2	3.35	3.40	3.45

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS
3. REFER JEDEC MO-288
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

PERICOM A PRODUCT LINE OF DIODES INCORPORATED
ENABLING SERIAL CONNECTIVITY

DATE: 01/14/22

DESCRIPTION: 32-contact, X1-QFN2845-32

PACKAGE CODE: XEA (XEA32)

DOCUMENT CONTROL #: PD-2259 **REVISION:** B

22-1546

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Plastic IC Package Information

Tape & Reel										
PKG. CODE	PKG. TYPE	REEL DIAMETER (inch)	TAPE WIDTH (mm)	TAPE PITCH (mm)	PIN 1 LOCATION	TAPE TRAILER LENGTH (Min# Pockets)	QTY PER REEL	TAPE LEADER LENGTH (Min# Pockets)	QTY PER TUBE	QTY PER TRAY
XEA32	X1QFN-32	13"	12	8	Top Left Corner	39 (12")	3500	64 (20")	N/A	N/A

Tape & Reel Materials and Design

Carrier Tape

The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is 106Ohm/sq. maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures C and D for carrier tape dimensions.

Cover Tape

Cover tape is made of Anti-static Transparent Polyester film. The surface resistivity is 107Ohm/Sq. Minimum to 1011Ohm sq. maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

Reel

The device loading orientation is in compliance with EIA-481, current version (Figure B). The loaded carrier tape is wound onto either a 13-inch reel, (Figure D) or 7-inch reel. The reel is made of Antistatic High-Impact Polystyrene. The surface resistivity 107Ohm/sq. minimum to 1011Ohm/sq. max.

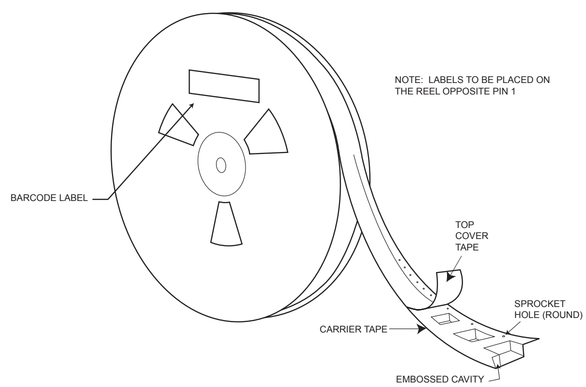


Figure A. Tape & Reel Label Information

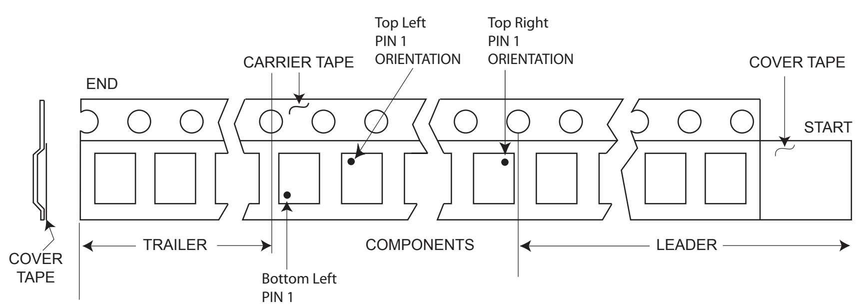


Figure B. Tape Leader and Trailer Pin 1 Orientations

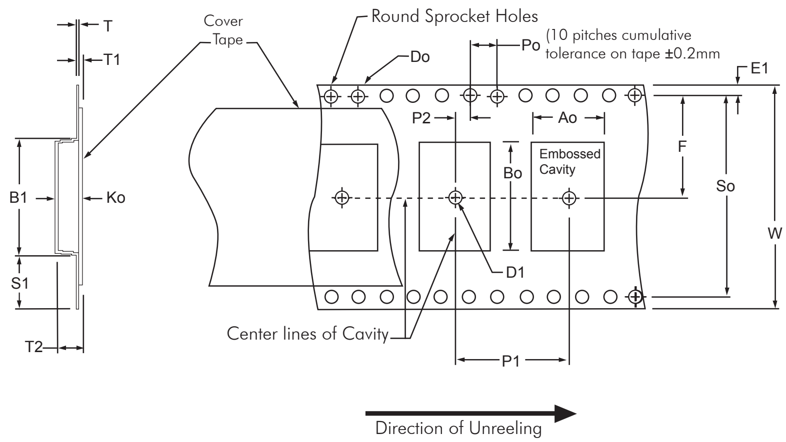


Figure C. Standard Embossed Carrier Tape Dimensions

Tape & Reel Dimensions

Constant Dimensions

<table>
<tr><th>TAPE SIZE</th><th>D_0</th><th>D_1 (Min)</th><th>E_1</th><th>P_0</th><th>P_2</th><th>R (2)</th><th>S_1 (Min)</th><th>T (Max)</th><th>T_1 (Max)</th></tr>
<tr><td>8mm</td><td rowspan="6">1.5 +0.1-0.0</td><td>1.0</td><td rowspan="6">1.75 ± 0.1</td><td rowspan="6">4.0 ± 0.1</td><td rowspan="2">2.0 ± 0.05</td><td>25</td><td rowspan="4">0.6</td><td rowspan="6">0.6</td><td rowspan="6">0.1</td></tr>
<tr><td>12mm</td><td rowspan="3">1.5</td><td rowspan="3">30</td></tr>
<tr><td>16mm</td><td rowspan="3">2.0 ± 0.1</td></tr>
<tr><td>24mm</td></tr>
<tr><td>32mm</td><td rowspan="2">2.0</td><td rowspan="2">50</td><td rowspan="2">N/A (3)</td></tr>
<tr><td>44mm</td><td>2.0 ± 0.15</td></tr>
</table>

Variable Dimensions

<table>
<tr><th>TAPE SIZE</th><th>P_1</th><th>B_1 (Max)</th><th>E_2 (Min)</th><th>F</th><th>So</th><th>T_2 (Max)</th><th>W (Max)</th><th>A_0, B_0 &K_0</th></tr>
<tr><td>8mm</td><td rowspan="6">Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information) or visit www.diodes.com/assets/MediaList-Attachments/Diodes-Tape-Reel-Tube.pdf</td><td>4.35</td><td>6.25</td><td>3.5 ± 0.05</td><td rowspan="4">N/A (4)</td><td>2.5</td><td>8.3</td><td rowspan="6">See Note 1</td></tr>
<tr><td>12mm</td><td>8.2</td><td>10.25</td><td>5.5 ± 0.05</td><td>6.5</td><td>12.3</td></tr>
<tr><td>16mm</td><td>12.1</td><td>14.25</td><td>7.5 ± 0.1</td><td>8.0</td><td>16.3</td></tr>
<tr><td>24mm</td><td>20.1</td><td>22.25</td><td>11.5 ± 0.1</td><td rowspan="2">12.0</td><td>24.3</td></tr>
<tr><td>32mm</td><td>23.0</td><td>N/A</td><td>14.2 ± 0.1</td><td>28.4 ± 0.1</td><td>32.3</td></tr>
<tr><td>44mm</td><td>35.0</td><td>N/A</td><td>20.2 ± 0.15</td><td>40.4 ± 0.1</td><td>16.0</td><td>44.3</td></tr>
</table>

NOTES:

1. A_0, B_0, and K_0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16 through 44mm.
2. Tape and components will pass around reel with radius "R" without damage.
3. S_1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where $D_o \geq S_1$.
4. S_o does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.

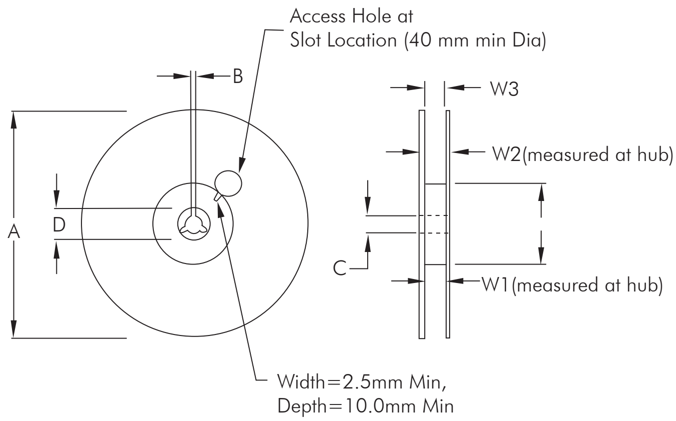


Figure D. Reel Dimensions

Reel Dimensions By Tape Size

TAPE SIZE	A	N (Min) [(1)]	W_1	W_2 (Max)	W_3	B (Min)	C	D (Min)
8mm	178 ± 2.0mm or 330 ± 2.0mm	60 ± 2.0mm or 100 ± 2.0mm	8.4 +1.5/-0.0 mm	14.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0 mm	18.4 mm				
16mm	330 ± 2.0mm	100 ± 2.0mm	16.4 +2.0/-0.0 mm	22.4 mm				
24mm			24.4 +2.0/-0.0 mm	30.4 mm				
32mm			32.4 +2.0/-0.0 mm	38.4 mm				
44mm			44.4 +2.0/-0.0 mm	50.4 mm				

NOTE:
1. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.

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