PI33xx-xx-EVAL1

ZVS Switching Regulators
Multi-Phase Guide

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Introduction

This multi-phase guide provides an overview to paralleling two or three PI33xx-xx devices together without any change required to the basic single-phase power stage or compensation design. Paralleling multiple PI33xx modules increases the output current capability and reduces the output voltage ripple. For information on paralleling more than three regulators, please contact Vicor.

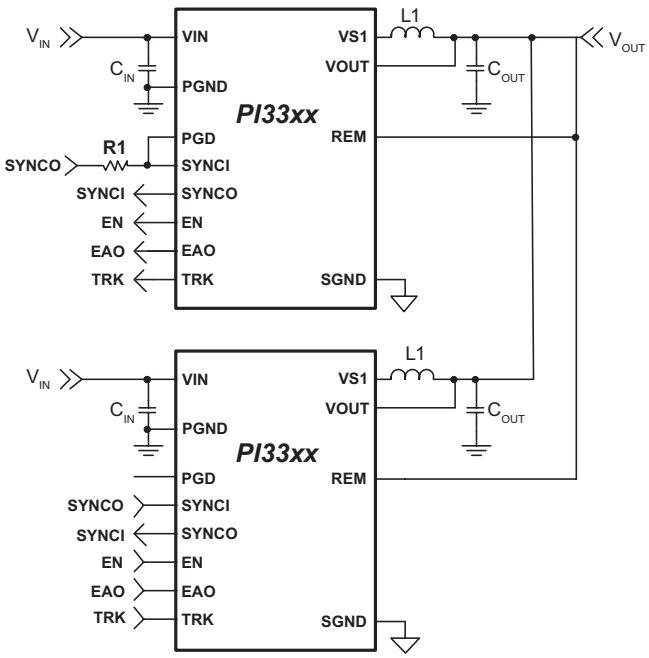
Basic Connections

The PI33xx family of products employs a Zero-Voltage Switching (ZVS) topology which operates exclusively in discontinuous and critical conduction mode. Therefore, to derive real-time output current information, each device's error amplifier output (EAO) is trimmed to a nominal level (2.2V) when supporting the maximum rated output load. This will allow the EAO to track the output load. By trimming the EAO this way, additional regulators can be connected in parallel to deliver equal amount of current to a single regulated point by linking each regulator's EAO pin together. The basic pin connections needed to parallel two or three regulators are shown in Figure 1. The SYNCO pins are for phase synchronization, TRK is for soft start and fault shut-down tracking. EAO is for current sharing between phases.

Two and Three Phases

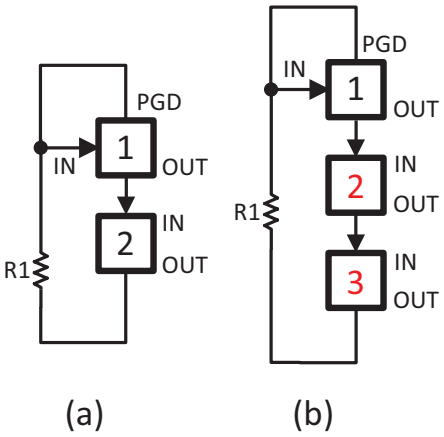
The PI33xx-2x can be synchronized in a closed-loop configuration to up to three phases by adding an additional 2.5kΩ (R1) feedback resistor to the design and incorporating the PGD pin.

Figure 1
Basic connections for parallel operation



This method will allow the regulators to remain in synchronization when the system's operational frequency stretches at high output loads. Figure 2 shows the basic synchronization connections and the phase requiring delays in red.

Figure 2
SYNCI (IN) and SYNCO (OUT) connection for two- and three-phase design



The required per-phase delay and programming code are presented in the following table:

Table 1
Phase programming codes

Sync Delay and Code			
Regulator	**1**	**2**	**3**
2-phase	–	–	
3-phase	–	**0Eh 1/3**	**0Eh 1/3**

Synchronization / Phase Delay

Two regulators connected in parallel operation do not require any delay programming. As a default setting, the PI33xx-xx will trigger on the falling edge and will operate 180° out of phase with the master. For a three-phase operation, a 1/3-phase delay is required for two of the regulators to ensure proper phase spacing. Synchronization and phase delay is only programmable with I²C option regulators (PI33xx-2x).

I²C™ Device Address

The PI33xx-2x supports floating addressing so that two address lines allows for up to eight programmable addresses.

The address is 7 bit with the read/write bit not included. Table 2 shows the address range that can be achieved using all possible combinations of ADR0 (pad G1) and ADR1 (pad H1). Bits A[6]-A[3] are fixed internally and may not be changed. The least significant 3 bits; A[2]-A[0], will assume the values in the table based on the decoding of ADR1 and ADR0. A zero or one indicates the logic strength of the bit and "NC" indicates that the pin is floating or not connected. The HEX column indicates the final address in hexadecimal, while the DEC column is the decimal address value.

Table 2
PI33xx-2x device addressing

A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	R/W	ADR1	ADR2	HEX	DEC
1	0	0	1	0	0	0	X	0	0	48	72
1	0	0	1	0	0	1	X	0	NC	49	73
1	0	0	1	0	1	0	X	0	1	4A	74
1	0	0	1	0	1	1	X	NC	0	4B	75
1	0	0	1	0	0	0	X	NC	NC	4C	76
1	0	0	1	1	0	1	X	NC	1	4D	77
1	0	0	1	1	1	0	X	1	0	4E	78
1	0	0	1	1	1	1	X	1	1+NC	4F	79

Programming Synchronization Delay

The PI33xx-2x provides an I²C™ standard-mode digital interface that enables the user to program phase delays. This is a one-time programmable option to the device. To set a delay, the user needs to assign a unique device address (see Table 2) to wake up the device during programming. Then send the synchronization delay address (21h) and the delay data (0Eh) while adhering to I²C protocols and Figure 4 sequencing.

The following figure demonstrates the proper steps to program a single-phase delay. The device address is determined by the user and the synchronization delay is provided in Table 1. The device address is represented as **XXh** (Bold) in Figure 3. Because this process in not reversible, it is important to follow all steps in Figure 3.

Figure 3
Showing the eight steps required to program a single 1/3-phase delay

1. Clear all registers to 00h with the device enabled.

Start	Addr. Device	Wr	Ack	Addr. Reg	Ack	Data	Ack	Stop
S	**XXh**	1	0	20h	0	00h	0	P
S	**XXh**	1	0	21h	0	00h	0	P
S	**XXh**	1	0	22h	0	00h	0	P

2. Enter test mode 5.

Start	Addr. Device	Wr	Ack	Addr. Reg	Ack	Data	Ack	Stop
S	**XXh**	1	0	18h	0	05h	0	P

3. Disable then re-enable the device (Enable Pin).

4. Set desired delay.

Start	Addr. Device	Wr	Ack	Addr. Reg	Ack	Data	Ack	Stop
S	**XXh**	1	0	21h	0	**0Eh**	0	P

5. Disable device (Enable Pin).

6. Return to test mode 0.

Start	Addr. Device	Wr	Ack	Addr. Reg	Ack	Data	Ack	Stop
S	**XXh**	1	0	18h	0	00h	0	P

7. Repeat #1; clearing all registers.

8. Enable device (Enable Pin); programming is complete.

Kill Bit 2 Option

Once synchronization has been programmed, a kill bit located at address 22h can be burned, to 01h to prevent any future erroneous blowing of remaining zero bits. The programming protocol is the same as shown above (Figure 3) except for step 4. Change the address register to 22h and the data sent to 01h.

For more detailed I²C interfacing information and available software please refer to the PI33xx-2x I²C Digital Interface Guide.

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