A Product Line of
Diodes Incorporated

PI2EQX16924

16Gbps 2-Lanes/4-Channel ReDriver with Linear Equalization

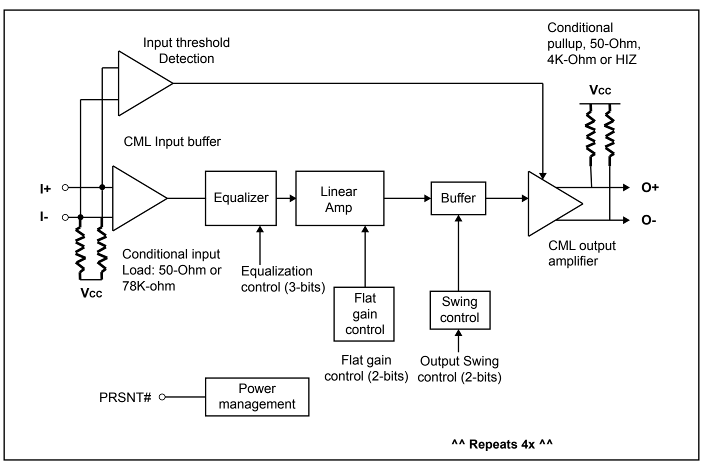
Features

- 2.5 to 16 Gbps Serial Link with Linear Equalizer
- Supports PCIe4
- Supports Four Differential Channels
- Independent Channel Configuration of Receiver Equalization, and Flat Gain
- I²C Slave Support with up to 1MHz
- 3-bit Selectable Address bit for I2C
- Supply Voltage: 1.8V±5%
- Industrial Temperature Range: -40°C to 85°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 32-contact, 2.85 x 4.5mm X2QFN (XUA)

Applications

- Networking
- Enterprise
- Server
- Storage

Block Diagram



Description

Diodes' PI2EQX16924 is a multi-data rate, four differential channel ReDriver™. The device provides programmable linear equalization, and flat gain, by I²C Control, to optimize performance over a variety of physical mediums by reducing intersymbol interference.

P2EQX16924 supports four 100Ω differential CML data I/Os and extends the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver, whereas the integrated linear amplifier/buffer circuitry provides flexibility with signal integrity of the signal after the ReDriver.

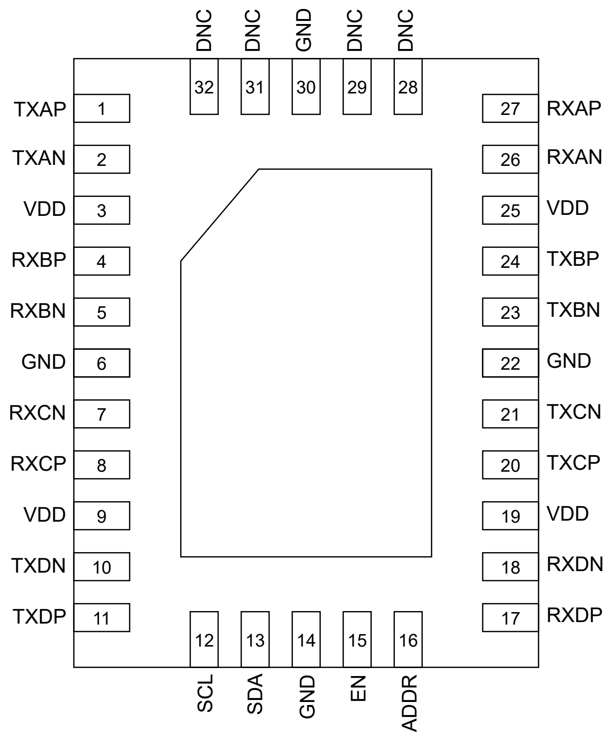
Ordering Information

Ordering Number	Package Code	Package Description
PI2EQX16924XUAEX	XUA	32-pin, 2.85x4.5mm (X2QFN)

Notes:
1. No purposely added lead. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
3. E = Pb-free and Green
4. X suffix = Tape/Reel

ReDriver is a trademark of Diodes Incorporated.

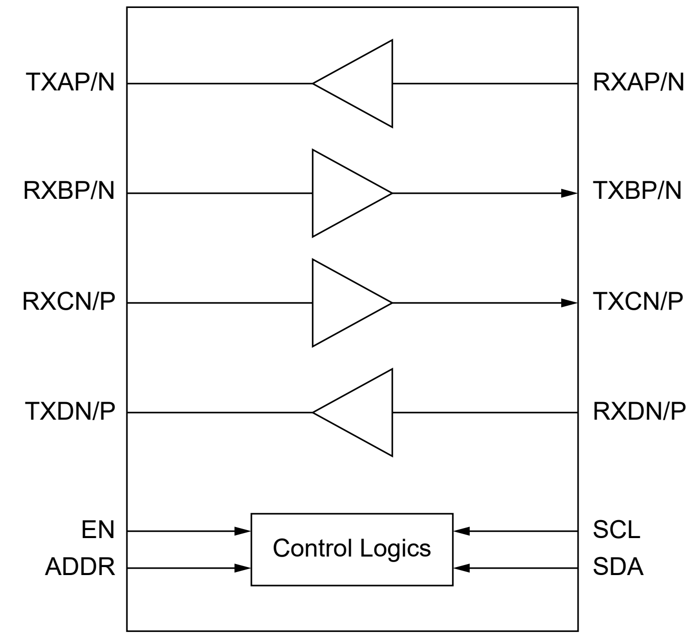
Pin Configuration



Pin Description

Pin Name	Pin #	Type	Description
Power and GND			
3, 9, 19, 25	VDD18	Power	1.8V power supply, +/- 5%
6, 14, 22, 30, Center Pad	GND	Ground	Supply Ground
28, 29, 31, 32	DNC		Do Not Connect
Control Pins			
12	SCL	I	SCL is I2C control bus clock. Open drain structure.
13	SDA	I/O	SDA is I2C control bus data. Open drain structure.
15	EN	I	With internal 300kΩ pull-up resistor. Low: Chip Power Down High: Normal Operation (Default)
16	ADDR	I	The I2C address select. 3-level input pins. With internal 150kΩ pull-up and pull-down resistors.
High Speed I/O Pins			
21, 20 24, 23	TXCN, TXCP TXBP, TXBN	O	CML output terminals. With selectable output termination between 50Ω, 6kΩ to internal VbiasTx or Hi-Z.
1, 2 10, 11	TXAP, TXAN TXDN, TXDP	O	CML output terminals. With selectable output termination between 50Ω, 6kΩ to internal VbiasTx or Hi-Z.
18, 17 27, 26	RXDN, RXDP RXAP, RXAN	I	CML input terminals. With selectable input termination between 50Ω to internal VbiasRx, 78kΩ to internal VbiasRx or 78kΩ to GND.
4, 5 7, 8	RXBP, RXBN RXCN, RXCP	I	CML input terminals. With selectable input termination between 50Ω to internal VbiasRx, 78kΩ to internal VbiasRx or 78kΩ to GND.

Functional Block Diagram



Description of Operation

Power Enable Function:

When EN is set to HIGH, the IC goes into power down mode—both input and output termination set to 78K and high impedance respectively. Individual Channel Enabling is done through the I2C register programming.

Equalization Setting:

EQ[2:0] are the selection pins for the equalization selection.

Table 1. Equalization Setting

I2C Register Setting EQ<2:0>			Equalizer Setting (dB)			
EQ<2>	EQ<1>	EQ<0>	@1.25GHz	@2.5GHz	@4GHz	@8GHz
0	0	0	0	0.1	0.6	5.0
0	0	1	0	0.4	1.4	7.2
0	1	0	0.1	0.9	2.4	9.3
0	1	1	0.4	1.8	4.0	11.2
1	0	0	1.1	3.2	5.9	13.0
1	0	1	1.7	4.4	7.3	14.2
1	1	0	2.7	5.9	8.9	15.1
1	1	1	3.6	7.1	10.0	15.7

Table 2. Flat Gain Setting (FG)

I2C Register FG[1:0]		Flat Gain Setting
0	0	-4 dB
0	1	-2 dB
1	0	+0 dB (Default)
1	1	+2 dB

Table 3. Chip Enable Control

I2C Register Setting or EN (pin#15)	Flat Gain Setting
0	Disabled
1	Enabled (Default)

Detail Programming Registers

I2C Slave Address Selection

Tri-level Input Pin ADDR	I^2C 7 Bit Slave Address						
L	1	0	1	0	0	0	1
M/F	1	0	1	0	0	1	0
H	1	0	1	0	1	0	0

Indexed Read/Write Protocol

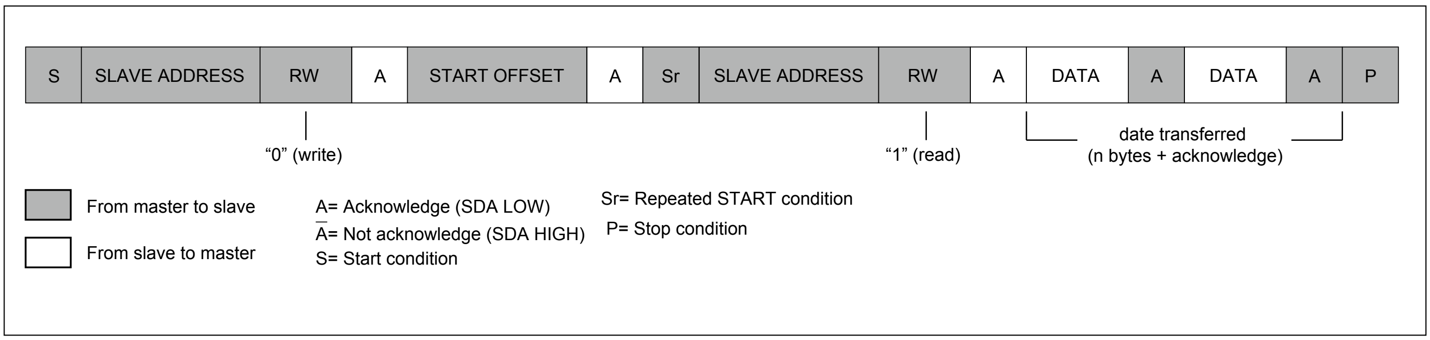


Figure 1. Indexed Read

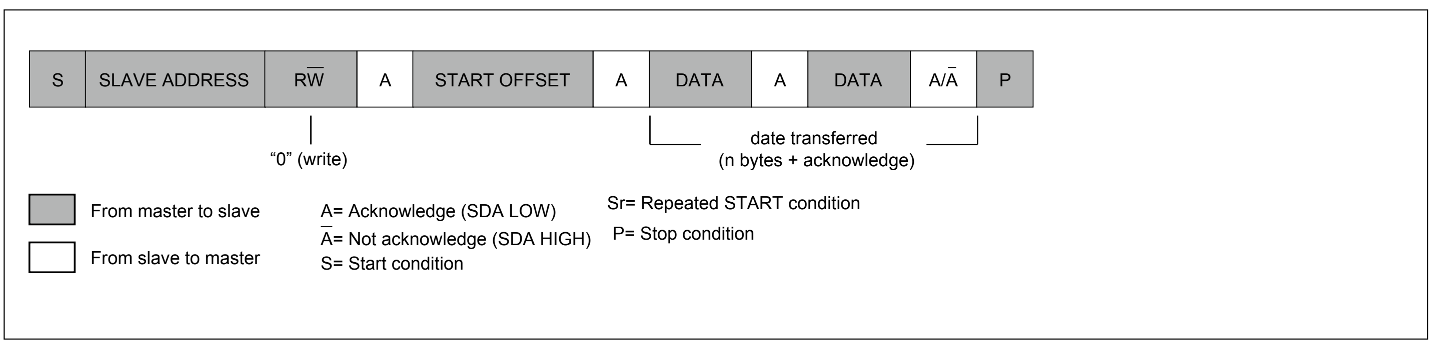


Figure 2. Indexed Write

I2C Register Definitions

BYTE 0 (Revision and Vendor ID Register)

Bit	Type	Power up condition	Comment
7	RO	0	Revision ID = 0000
6	RO	0	
5	RO	0	
4	RO	0	
3	RO	0	Revision ID = 0011
2	RO	0	
1	RO	1	
0	RO	1	

BYTE 1 (Device Type/Device ID Register)

Bit	Type	Power up condition	Comment
7	RO	0	Reserved
6	RO	0	
5	RO	0	
4	RO	1	
3	RO	0	Device ID = 0010
2	RO	0	
1	RO	1	
0	RO	0	

BYTE 2 (Byte count Register 32 bytes)

Bit	Type	Power up condition	Comment
7	RO	0	I2C register byte count = 32 bytes
6	RO	0	
5	RO	1	
4	RO	0	
3	RO	0	
2	RO	0	
1	RO	0	
0	RO	0	

BYTE 3 (Channel assignment of RXDET_EN and configuration mode)

Bit	Type	Power up condition	Comment
7	R/W	1	Operation mode setting. Default OP_MODE[3:0]=1100, OP_MODE[3:0]=1101 for 2 lanes PCIe
6	R/W	1	
5	R/W	0	
4	R/W	0	
3	R/W	0	Reserved
2	R/W	0	Enable/Disable RXDET_EN 0 – RXDET is Enabled. 1 – RXDET is Disabled.
1	R/W	0	Reserved
0	R/W	0	Reserved

BYTE 4

Bit	Type	Power up condition	Comment
7	R/W	0	RXD power down override 0 – Do not force the RXD to power down state 1 – Force the RXD to power down state
6	R/W	0	TXC power down override 0 – Do not force the TXC to power down state 1 – Force the TXC to power down state
5	R/W	0	TXB power down override 0 – Do not force the TXB to power down state 1 – Force the TXB to power down state
4	R/W	0	RXA power down override 0 – Do not force the RXA to power down state 1 – Force the RXA to power down state
3	R/W	0	Reserved
2	R/W	1	
1	R/W	0	Reserved
0	R/W	0	Reserved

BYTE 5 (Equalization and Flat gain setting of RXA)

Bit	Type	Power up condition	Comment
7	R/W	0	Reserved
6	R/W	0	EQ<2> Equalizer setting
5	R/W	0	EQ<1> Equalizer setting
4	R/W	0	EQ<0> Equalizer setting
3	R/W	1	FG<1> Flat gain setting
2	R/W	0	FG<0> Flat gain setting
1	R/W	0	Reserved
0	R/W	0	Reserved

BYTE 6 (Equalization and Flat gain setting of TXB)

Bit	Type	Power up condition	Comment
7	R/W	0	Reserved
6	R/W	0	EQ<2> Equalizer setting
5	R/W	0	EQ<1> Equalizer setting
4	R/W	0	EQ<0> Equalizer setting
3	R/W	1	FG<1> Flat gain setting
2	R/W	0	FG<0> Flat gain setting
1	R/W	0	Reserved
0	R/W	0	Reserved

BYTE 7 (Equalization and Flat gain setting of TXC)

Bit	Type	Power up condition	Comment
7	R/W	0	Reserved
6	R/W	0	EQ<2> Equalizer setting
5	R/W	0	EQ<1> Equalizer setting
4	R/W	0	EQ<0> Equalizer setting
3	R/W	1	FG<1> Flat gain setting
2	R/W	0	FG<0> Flat gain setting
1	R/W	0	Reserved
0	R/W	0	Reserved

BYTE 8 (Equalization and Flat gain setting of RXD)

Bit	Type	Power up condition	Comment
7	R/W	0	Reserved
6	R/W	0	EQ<2> Equalizer setting
5	R/W	0	EQ<1> Equalizer setting
4	R/W	0	EQ<0> Equalizer setting
3	R/W	1	FG<1> Flat gain setting
2	R/W	0	FG<0> Flat gain setting
1	R/W	0	Reserved
0	R/W	0	Reserved

BYTE 9 - BYTE 31 (Reserved)

Electrical Specification

Absolute Maximum Ratings

Supply Voltage to Ground Potential	–0.5V to V_{DD} +0.3V
Voltage Input to High Speed Differential Pins	–0.5V to V_{DD}
Voltage Input to Low Speed Pins (SCL, SDA)	–0.5V to +2.5V
Voltage Input to Low Speed Pins (EN)	–0.5V to V_{DD} +0.3V
Storage Temperature	–65 °C to +150 °C
Junction Temperature	125°C
ESD HBM	±2000V
ESD CDM	±500V

Note:
(1) Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to beyond the absolute maximum rating conditions for extended periods may affect interoperability and degradation of device reliability and performance.

Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max	Units
V_{DD}	VDD Supply Voltage	1.71	1.8	1.89	V
V_{DD_Noise}	Supply Noise up to 50 MHz(1)			50	mVpp
$C_{ac\_coupling}$	System AC coupling capacitance	75		265	nF
T_A	Ambient Temperature, Commercial C-temp range	-40(1)		+85	°C

Notes:
(1) The minimum temperature -40°C can be guaranteed by design

Thermal Information

Symbol	Parameter	32-pin X2QFN	Unit
Theta JA	Junction-to-ambient resistance	33.88	°C/W

Power Consumption

Over operating temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
I_{active}	Supply Current at Active Mode	EN = 1		160	220	mA
I_{lowp}	Supply Current at Low Power Mode	EN = 1, Without Input Signal		15	21	mA
I_{unplug}	Supply Current at Unplug Mode, Without Device Plugged	EN = 1, Without Device		0.7	1	mA
$I_{standby}$	Supply Current at Standby Mode	EN = 0		25	50	uA

AC/DC Characteristics

(VDD=1.8V ± 5% TA = -40 to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		1.71	1.8	1.89	V
Receiver (RX) Electrical Specification						
$C_{RX\text{-}PARASITIC}$	Rx input capacitance	At 8GHz			0.5	pF
$R_{RX\text{-}DIFF\text{-}DC}$	DC Differential Input Impedance		72		120	Ω
$R_{RX\text{-}SINGLE\text{-}DC}$	DC single ended input impedance to guarantee RxDet	Measured with respect to GND over a voltage of 500mV max	18		30	
$Z_{RX\text{-}HIZ\text{-}DC\text{-}PD}$	DC input CM input impedance for V>0 during reset or power down	(Vcm=0 to 500mV)	25			kΩ
$V_{RX\text{-}CM\text{-}AC\text{-}P}$	Rx common mode peak voltage	AC up to 8GHz			150	mVpeak
Transmitter (TX) Electrical Specification						
$C_{TX\text{-}PARASITIC}$	Tx input capacitance				1.1	pF
$V_{TX\text{-}DIFF\text{-}PP\_8G}$	Output differential p-p voltage Swing	Differential Swing $\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-}\rvert$ at -1dB compression point of 8GHz		0.87		Vppd
$V_{TX\text{-}DIFF\text{-}PP\_100M}$	Output differential p-p voltage Swing	Differential Swing $\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-}\rvert$ at -1dB compression point of 100MHz		0.91		Vppd
$R_{TX\text{-}DIFF\text{-}DC}$	DC Differential TX Impedance		72		120	Ω
$V_{TX\text{-}RCV\text{-}DET}$	The amount of Voltage change allowed during RxDet				600	mV
$I_{TX\text{-}SHORT}$	Transmitter short circuit current to ground		-60		60	mA
$R_{TX\text{-}DC\text{-}CM}$	Common mode DC output Impedance		18		30	Ω
$V_{TX\text{-}C}$	Common-Mode Voltage	$\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-} \rvert /2$	V_{DD}-1V		V_{DD}	V
$V_{TX\text{-}CM\text{-}AC\text{-}PP\text{-}ACTIVE}$	Active mode TX AC common mode voltage	$V_{TX\text{-}D+} + V_{TX\text{-}D-}$ for both time and amplitude			100	mVpp
High-Speed Channel Electrical Specification						
t_{pd}	Channel latency	From input pin to output pin		150	300	Ps

AC/DC Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
G_P	Peaking gain (Compensation at 8GHz, relative to 100MHz, 100mVp-p sine wave input)	EQ<2:0> = 000 EQ<2:0> = 001 EQ<2:0> = 010 EQ<2:0> = 011 EQ<2:0> = 100 EQ<2:0> = 101 EQ<2:0> = 110 EQ<2:0> = 111		5 7.2 9.3 11.2 13 14.2 15.1 15.7		dB
		Variation around typical	-2		+2	dB
G_F	Flat gain (100MHz, EQ<2:0>=000)	FG<1:0> = 00 FG<1:0> = 01 FG<1:0> = 10 FG<1:0> = 11		-4 -2 0 +2		dB
V_{sw_100M}	Output linear swing (at 100MHz)	EQ<2:0>=111, FG<1:0>=10		910		mVppd
V_{sw_8G}	Output linear swing (at 8GHz)	EQ<2:0>=111, FG<1:0>=10		900		mVppd
D_{DNEXT} (2)	Differential near-end crosstalk	100MHz to 8GHz, EQ<2:0>=111, FG<1:0>=10		-38		dB
D_{DFEXT} (2)	Differential far-end crosstalk	100MHz to 8GHz, EQ<2:0>=111, FG<1:0>=10		-29		dB
V_{NOISE_IN}	Input-referred noise	100MHz to 8GHz, EQ<2:0>=000, FG<1:0>=10, Figure x		0.8		mV_{RMS}
		100MHz to 8GHz, EQ<2:0>=111, FG<1:0>=10,		0.5		
V_{NOISE_OUT}	Output-referred noise	100MHz to 8GHz, EQ<2:0>=000, FG<1:0>=10,		0.5		mV_{RMS}
		100MHz to 8GHz, EQ<2:0>=111, FG<1:0>=10,		0.7		
S11DM	Input differential mode return loss	10MHz to 8GHz differential mode		-9.1	-7	dB
S11CM	Input common mode return loss	1GHz to 8GHz common mode		-9	-7	dB
S22DM	Output differential mode return loss	10MHz to 8GHz differential mode		-9.3	-7	dB
S22CM	Output common mode return loss	1GHz to 8GHz common mode		-8.5	-7	dB

Note:
(1) Measured using a vector-network analyzer (VNA) with -15dbm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.
(2) Subtract the Channel Gain from the Total Gain to get the Actual Crosstalk

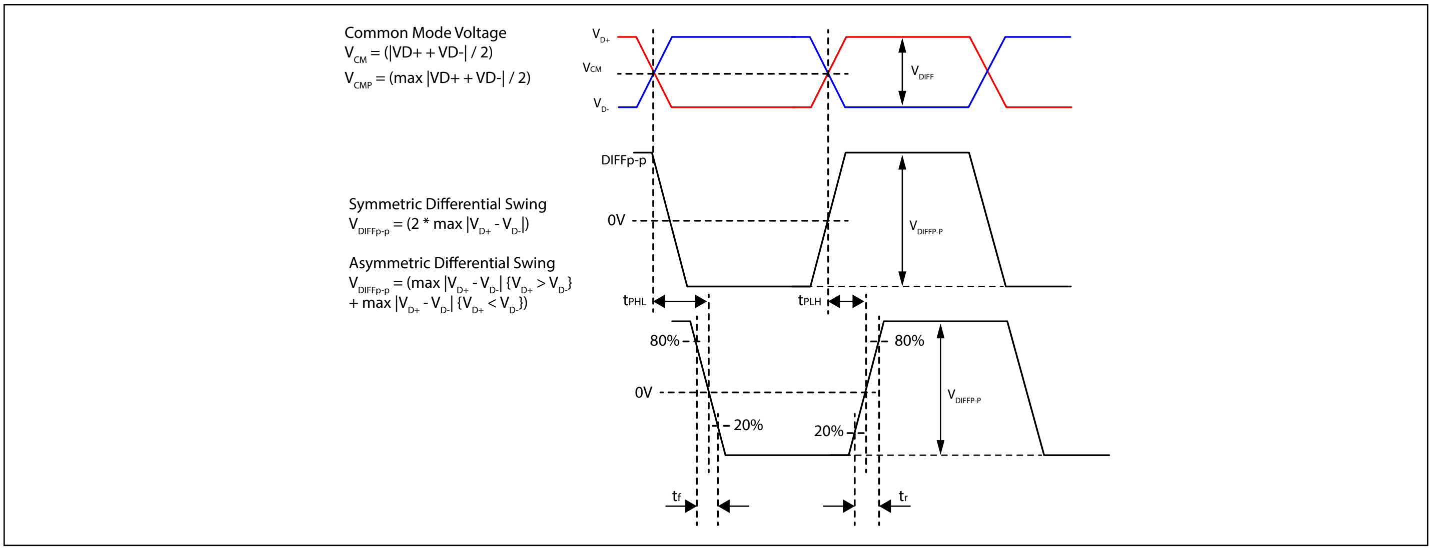


Figure 3. Definition of Peak-to-peak Differential Voltage

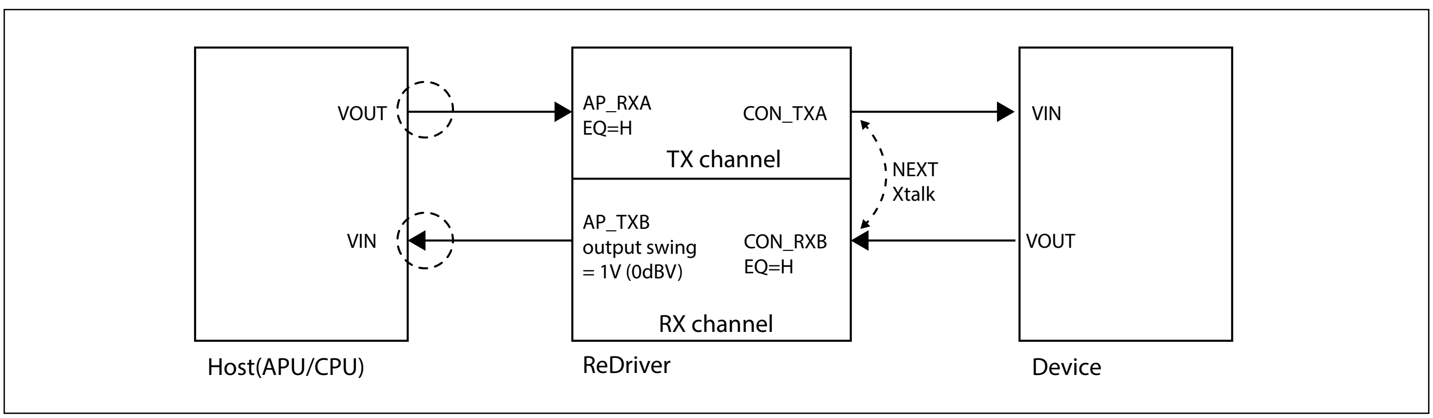


Figure 4. NEXT Crosstalk Definition

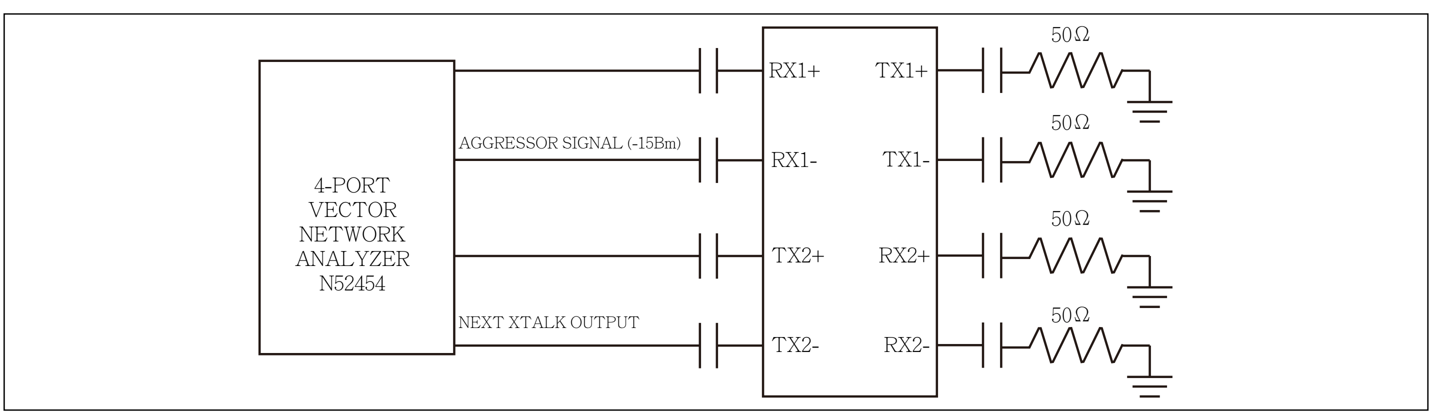


Figure 5. NEXT Channel-isolation Test Configuration

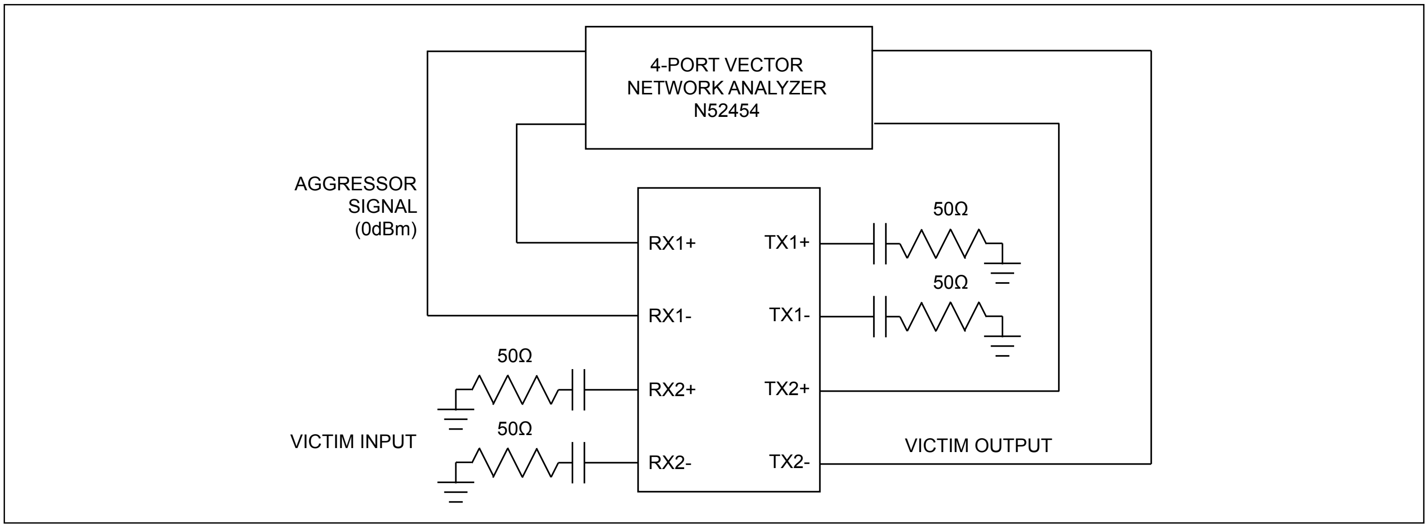


Figure 6. FEXT Channel-isolation Test Configuration

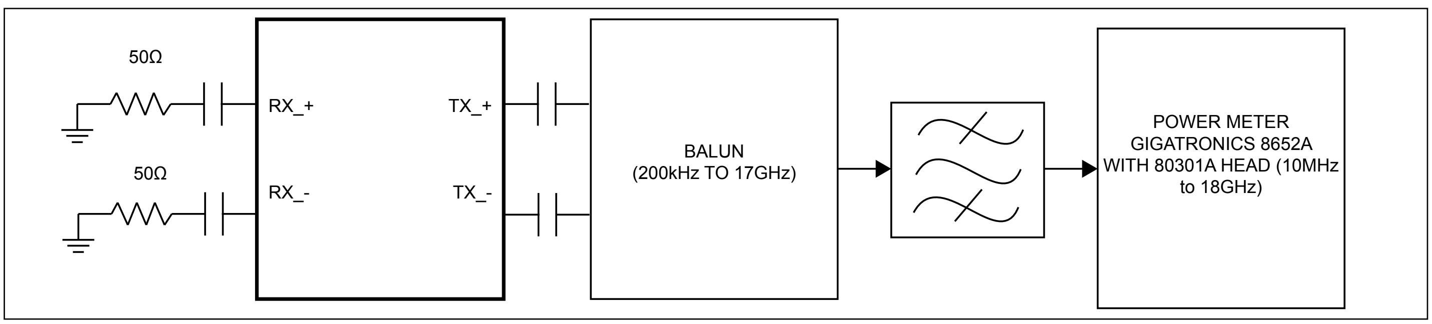
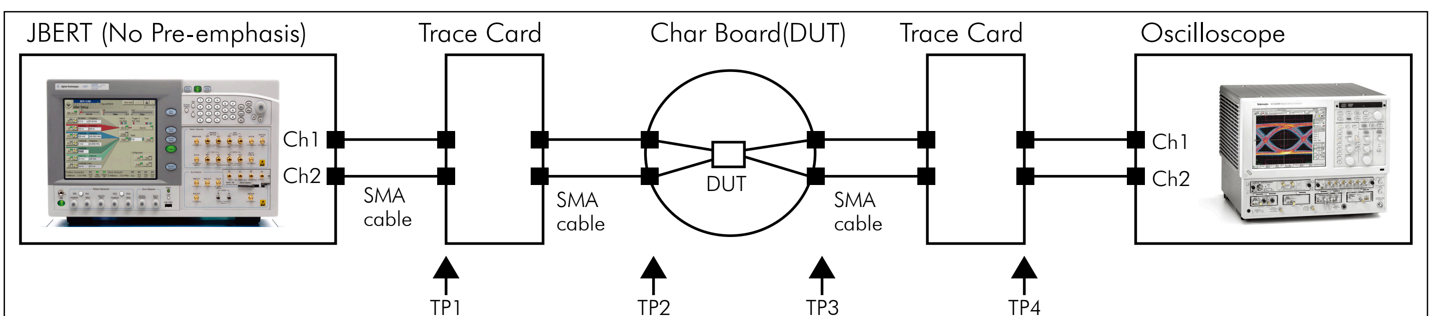


Figure 7. Noise Test Configuration



1) Trace card between TP1 and TP2 is designed to emulate 6-48" of FR4. Trace width -4 mils,100Ω differnetial impedance
2) All jitter is measured at a BER of 10-9
3) Residual jitter reflects the total jitter measured at TP4 jitter minus TP1 jitter
4) VDD = 1.8V, RT = 50Ω
5) The input signal from JBERT does not have any pre-emphasis.

Figure 8. AC Electrical Parameter Test Setup

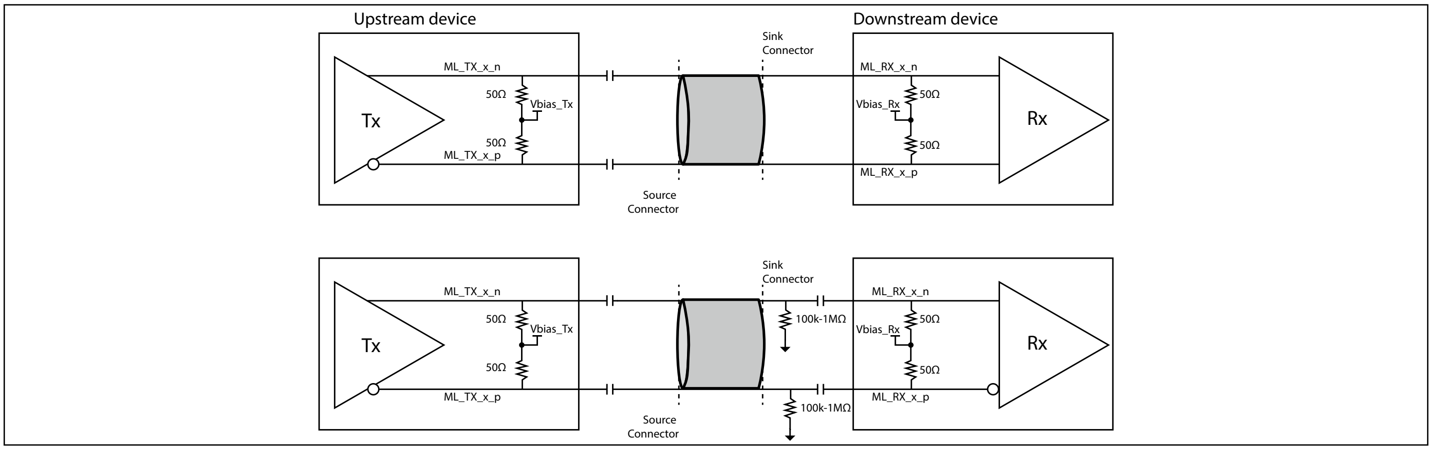


Figure 9. High-speed Chanel Test Circuit

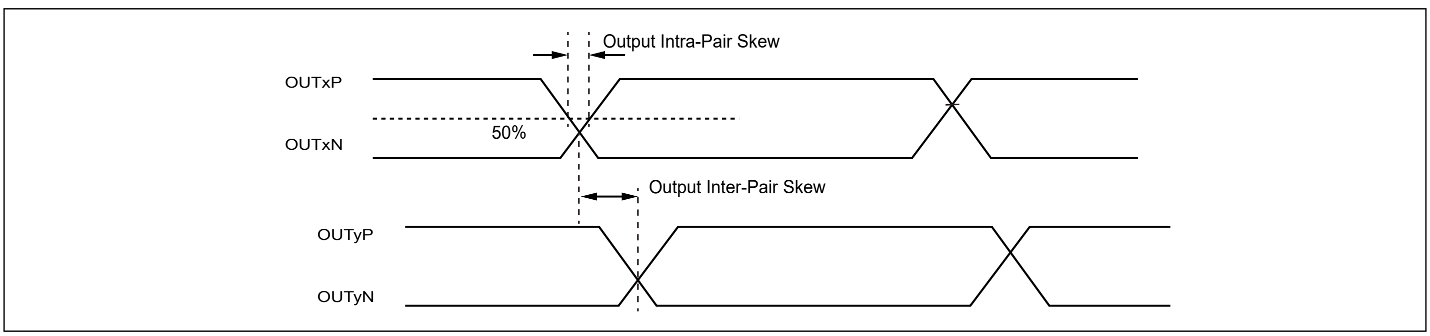


Figure 10. Intra and Inter-pair Differential Skew Definition

I2C Electrical Specification and Timing

Characteristics of the SDA and SCL I/O Stages

Symbol	Parameter	Conditions	Min	Max	Units
V_{IL}	LOW-level input voltage		−0.5	0.4	V
V_{IH}	HIGH-level input voltage		1.2		V
V_{hys}	Hysteresis of Schmitt trigger inputs		0.05VDD		V
V_{OL}	LOW-level output voltage	Open-drain or open-collector at 3mA sink current; VDD >2V	0	0.4	V
I_{OL}	LOW-level output current	V_{OL} =0.4V	20		mA
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}		12	120	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0	50	ns
I_I	Input current each I/O pin	0.1VDD < V_I < 0.9VDDmax	−10	+10	uA
C_I	Capacitance for each I/O pin			10	pF
f_{SCL}	SCL clock frequency		10	1000	kHz
$t_{HD;STA}$	Hold time (repeated) START condition	After this period, the first clock pulse is generated.	0.26		us
t_{LOW}	LOW period of the SCL clock		0.5		us
t_{HIGH}	HIGH period of the SCL clock		0.26		us
$t_{SU;STA}$	Set-up time for a repeated START condition		0.26		us
$t_{SU;DAT}$	Data set-up time		50		ns
Tr	Rise time of both SDA and SCL signals			120	ns
Tf	Fall time of both SDA and SCL signals		12	120	ns
$t_{SU;STO}$	Set-up time for STOP condition		0.26		us
t_{BUF}	Bus free time between a STOP and START condition		0.5		us
Cb	Capacitive load for each bus line			550	pF
$t_{VD;DAT}$	Data valid time			0.45	us
$t_{VD;ACK}$	Data valid acknowledge time			0.45	us

Characteristics of the SDA and SCL Bus Lines for Standard and Fast Mode Devices

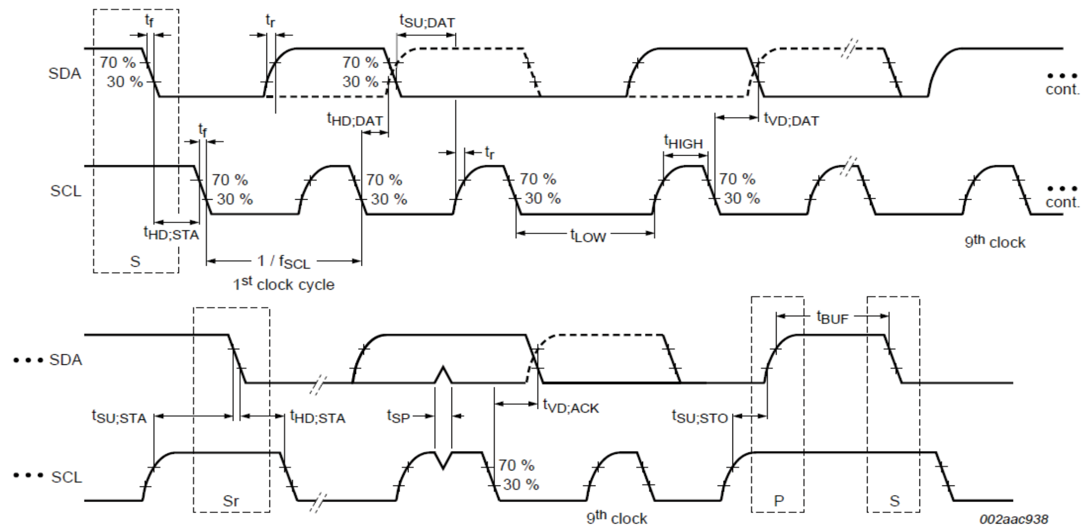
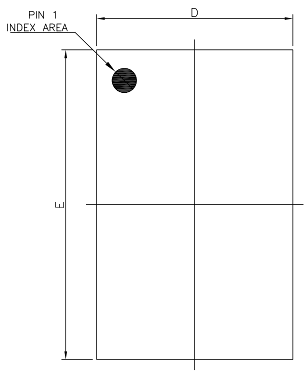
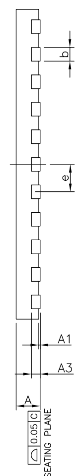


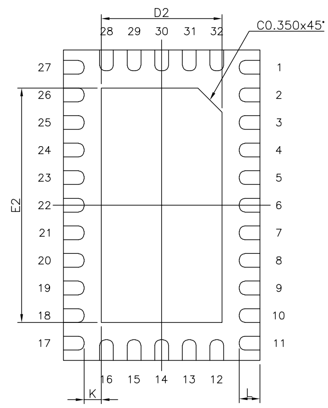
Figure 11. Definition of timing for F/S-mode devices on the I2C bus

Mechanical/Packaging Information

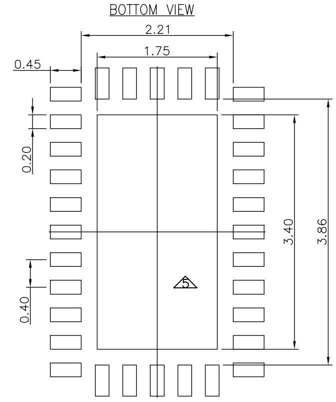


TOP VIEW





BOTTOM VIEW



RECOMMENDED LAND PATTERN

SYMBOLS	MIN.	NOM.	MAX.
A	0.30	0.35	0.40
A1	0.00	0.02	0.05
A3	0.127 REF.		
b	0.15	0.20	0.25
D	2.75	2.85	2.95
E	4.40	4.50	4.60
e	0.40 BSC		
L	0.25	0.30	0.35
D2	1.70	1.75	1.80
E2	3.35	3.40	3.45
K	0.20	—	—

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS
3. REFER JEDEC MO-288
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

PERICOM A PRODUCT LINE OF DIODES INCORPORATED
ENABLING SERIAL CONNECTIVITY

DATE: 10/28/19

DESCRIPTION: 32-Pin, X2QFN 2.85X4.5mm

PACKAGE CODE: XUA (XUA32)

DOCUMENT CONTROL #: PD-2247 **REVISION: --**

19-0420

Part Marking Information

PI2EQX16
924XUAE_
YYYWWXX

1st Y: Die Rev
2nd & 3rd Y: Year
WW: Week
1st X: Assembly Code
2nd X: Fab Code

Tape & Reel Materials and Design

Carrier Tape

The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is 10^6Ohm/sq. maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 3 and 4 for carrier tape dimensions.

Cover Tape

Cover tape is made of Anti-static Transparent Polyester film. The surface resistivity is 10^7Ohm/Sq. Minimum to 10^{11}Ohm sq. maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

Reel

The device loading orientation is in compliance with EIA-481, current version (Figure 2). The loaded carrier tape is wound onto either a 13-inch reel, (Figure 4) or 7-inch reel. The reel is made of Antistatic High-Impact Polystyrene. The surface resistivity 10^7Ohm/sq. minimum to 10^{11}Ohm/sq. max.

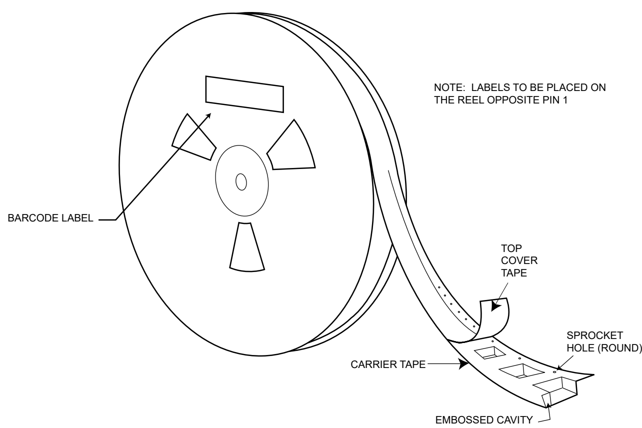


Figure 7-1 Tape & Reel Label Information

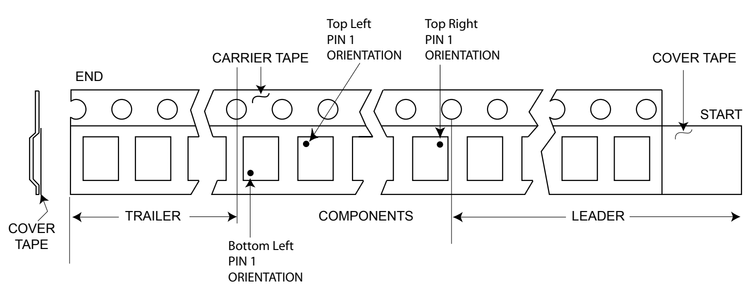


Figure 7-2 Tape Leader and Trailer Pin 1 Orientations

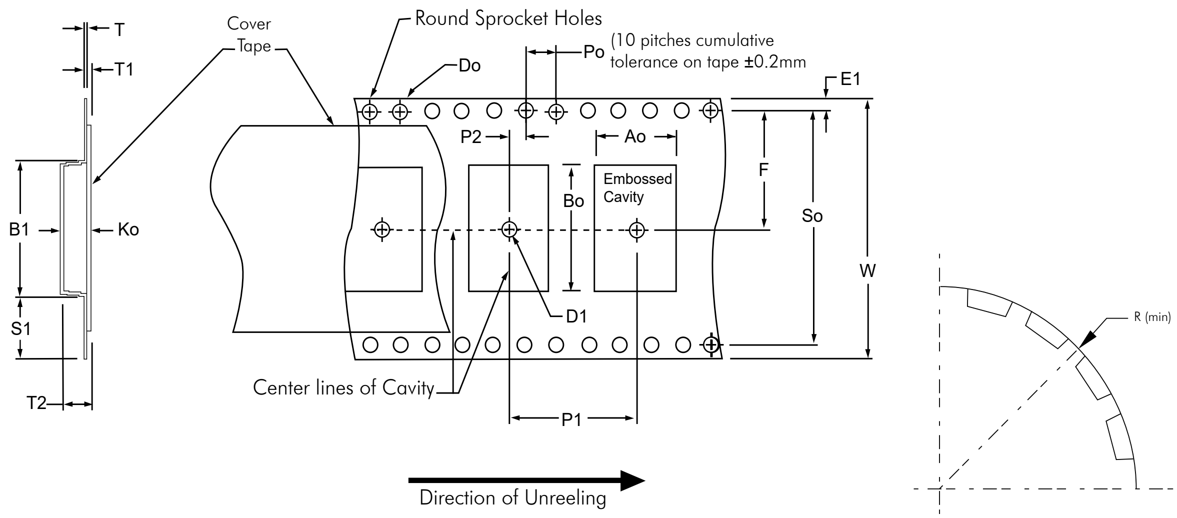


Figure 7-3 Standard Embossed Carrier Tape Dimensions

Table 7-1. Constant Dimensions

Tape Size	D_0	D_1 (Min)	E_1	P_0	P_2	R (See Note 2)	S_1 (Min)	T (Max)	T_1 (Max)
8mm	1.5 +0.1 -0.0	1.0	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	25	0.6	0.6	0.1
12mm		1.5				30			
16mm					2.0 ± 0.1				
24mm									
32mm		2.0				50	N/A (See Note 3)		
44mm					2.0 ± 0.15				

Table 7-2. Variable Dimensions

Tape Size	P_1	B_1 (Max)	E_2 (Min)	F	So	T_2 (Max.)	W (Max)	A_0, B_0, & K_0
8mm	Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information)	4.35	6.25	3.5 ± 0.05	N/A (see note 4)	2.5	8.3	See Note 1
12mm		8.2	10.25	5.5 ± 0.05		6.5	12.3	
16mm		12.1	14.25	7.5 ± 0.1		8.0	16.3	
24mm		20.1	22.25	11.5 ± 0.1		12.0	24.3	
32mm		23.0	N/A	14.2 ± 0.1	28.4± 0.1		32.3	
44mm		35.0	N/A	20.2 ± 0.15	40.4 ± 0.1	16.0	44.3	

Notes:

1. A0, B0, and K0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16 through 44mm.
2. Tape and components will pass around reel with radius "R" without damage.
3. S1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where Do≥S1.
4. So does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.

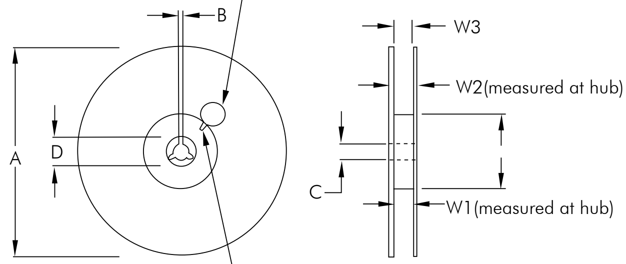


Table 7-3. Reel Dimensions by Tape Size

Tape Size	A	N (Min) See Note A	W_1	W_2(Max)	W_3	B (Min)	C	D (Min)
8mm	178 ±2.0mm or 330±2.0mm	60 ±2.0mm or 100±2.0mm	8.4 +1.5/-0.0 mm	14.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0 mm	18.4 mm				
16mm	330 ±2.0mm	100 ±2.0mm	16.4 +2.0/-0.0 mm	22.4 mm				
24mm			24.4 +2.0/-0.0 mm	30.4 mm				
32mm			32.4 +2.0/-0.0 mm	38.4 mm				
44mm			44.4 +2.0/-0.0 mm	50.4 mm				

Note:

A. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.

Important Notice

1. DIODES INCORPORATED AND ITS SUBSIDIARIES ("DIODES") MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes products. Diodes products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of the Diodes products for their intended applications, (c) ensuring their applications, which incorporate Diodes products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.

3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.

4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.

5. Diodes products are provided subject to Diodes' Standard Terms and Conditions of Sale (https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

6. Diodes products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.

7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.

8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.

www.diodes.com