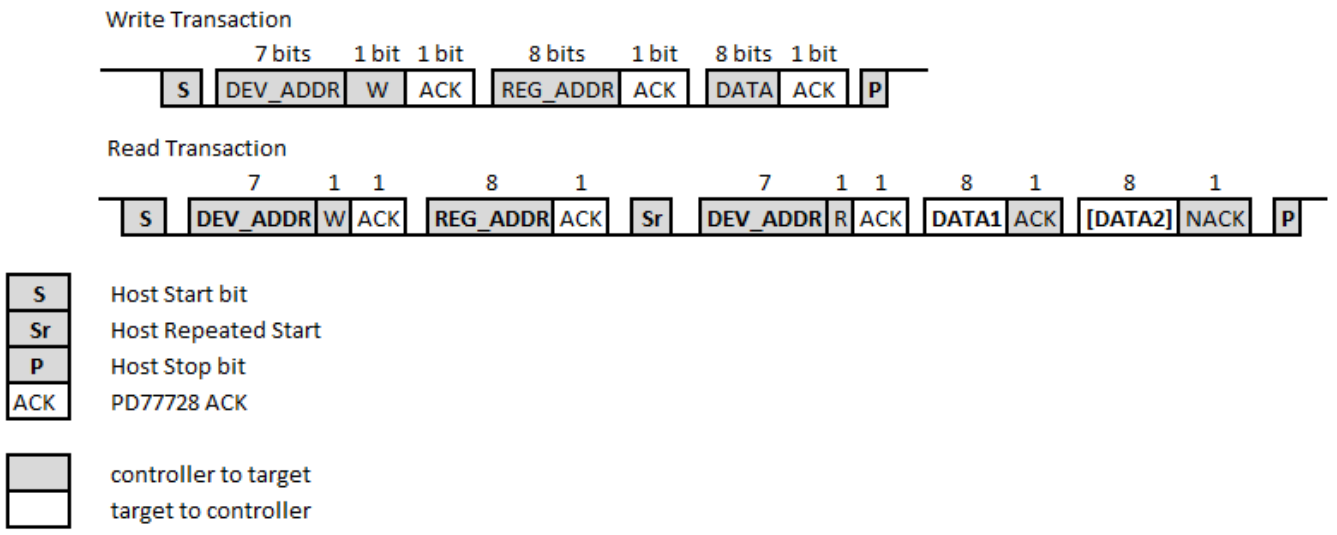
PD77728 Auto Mode Register Map

Introduction

This document describes the PD77728 register map and register functionality. The PD77728 communication method is based on I²C, using register access as shown in Figure 1. Each PD77728 includes two consecutive I²C addresses (a single I²C address controls 4 ports of 2 pairs). The two I²C addresses are set by pins A1–A4, and each address is 7 bits. The PD77728 device does not require clock stretch support from the host. See the I²C section in the PD77728 Datasheet to program the I²C address.

Figure 1. I²C Transactions



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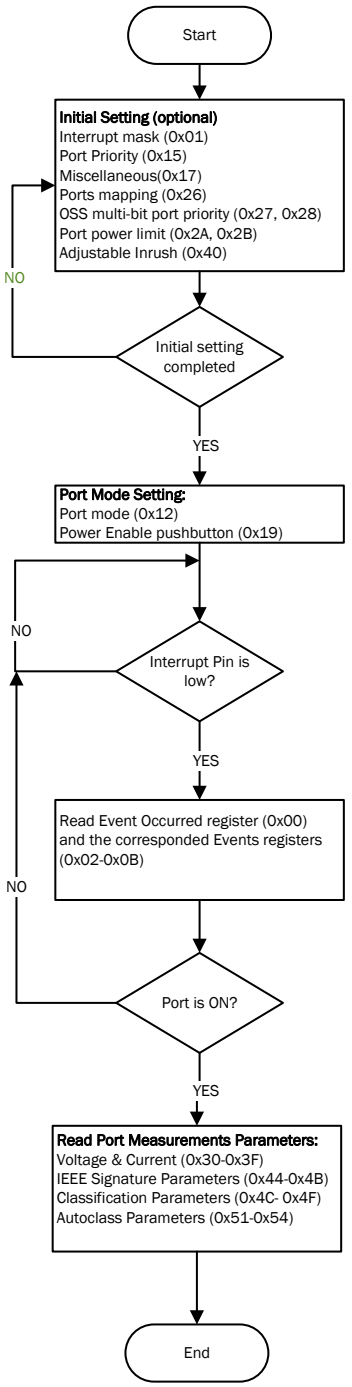
1. Automode Operational Flowchart

The following figure shows the Automode Operational Flowchart of the PD77728 register map.

Figure 1-1. Automode Operational Flowchart



2. Register Map

The following tables list the register map details of the PD77728 device.

Table 2-1. Interrupts

Address	Name	R/W	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
0x00	Interrupt	RO	System	Supply Event	Start Fault	Overload	Class Done	I²C SR/ Cap Meas	Disconnect	Pwr Good Event	Pwr Enable Event	1000, 0000b
0x01	Int Mask	R/W	System	Mask								1000, 0000b

Table 2-2. Event

Address	Name	R/W	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
0x02	Power	RO	4321	Power Good Change				Power Enable Change				0000,0000b
0x03		CoR		Port 4	Port 3	Port 2	Port 1	Port 4	Port 3	Port 2	Port 1	
0x04	Detection/ Classification	RO	4321	Class Done				Detect/CC Done				0000,0000b
0x05		CoR		Port 4	Port 3	Port 2	Port 1	Port 4	Port 3	Port 2	Port 1	
0x06	Fault	RO	4321	Underload				Overload				0000,0000b
0x07		CoR		Port 4	Port 3	Port 2	Port 1	Port 4	Port 3	Port 2	Port 1	
0x08	Start	RO	4321	Current Limit Fault				Power Up Fault				0000,0000b
0x09		CoR		Port 4	Port 3	Port 2	Port 1	Port 4	Port 3	Port 2	Port 1	
0x0A	Supply	RO	4321	Over Temp	VDD UVLO Failure	VDD UVLO Warning	Vpwr UVLO	PCUT34	PCUT12	OSS Event	RAM Fault	00xx,0000b
0x0B		CoR										

Table 2-3. Status

Address	Name	R/W	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
0x0C	Detect/ Class Status	RO	1	Detected Class (see Table 3-8)				Detection Status (see Table 3-7)				0000,0000b
0x0D	Detect/ Class Status	RO	2									0000,0000b
0x0E	Detect/ Class Status	RO	3									0000,0000b
0x0F	Detect/ Class Status	RO	4									0000,0000b
0x10	Power	RO	4321	Power Good				Power Enable				0000,0000b
				Port 4	Port 3	Port 2	Port 1	Port 4	Port 3	Port 2	Port 1	
0x11	Pin	RO	System	AUTO	Client Address					Reserved	Reserved	0,SA[4:0],0,0b

Table 2-4. Configuration

Address	Name	R/W	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
0x12	Port Mode	R/W	4321	Port 4 Mode (see Table 3-9)		Port 3 Mode (see Table 3-9)		Port 2 Mode (see Table 3-9)		Port 1 Mode (see Table 3-9)		0000,0000b
0x15	PWRPR	R/W	4321	Port Power Priority				Disable PCUT				0000,0000b
				Port 4	Port 3	Port 2	Port 1	Port 4	Port 3	Port 2	Port 1	
0x17	Misc	R/W	Global	Interrupt Pin Enable	Port Sig Measure	Reserved	Multi-Bit Priority	Change		Reserved	0x29 Behavior	1100,0000b
								CLASS	DETECT			
0x19	Power Enable	WO	4321	Power Off				Power On				0000,0000b
				Port 4	Port 3	Port 2	Port 1	Port 4	Port 3	Port 2	Port 1	

Table 2-5. General

Address	Name	R/W	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
0x1B	ID	RO	System	Manufacture ID					IC ID			xxxx,x101b (Note 1)
0x1C	AC/CC	RO	4321	AutoClass Detected				Connection Check Results				0000,0000b
				Port 4	Port 3	Port 2	Port 1	Port 3, 4		Port 1, 2		

Note:

1. x = Unknown value

Table 2-6. Specialized

Address	Name	R/W	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
0x24	Power on Fault	RO	4321	Port 4		Port 3		Port 2		Port 1		0000,0000b
0x25		COR										0000,0000b
0x26	Ports Matrix	R/W	4321	Port 4 remap		Port 3 remap		Port 2 remap		Port 1 remap		1110,0100b
0x27	Multi-Bit Power Priority	R/W	21	Resv		Port 2		Resv		Port 1		0000,0000b
0x28		R/W	43	Resv		Port 4		Resv		Port 3		0000,0000b
0x2A	4P Police Config	R/W	21	4P Police Port 1, 2								1111,1111b
0x2B		R/W	43	4P Police Port 3, 4								1111,1111b
0x2C	Temp.	RO	4321	Die Temperature 367 – {2 * (regVal_decimal)} (degrees Celsius)								—
0x2E	V_{PWR}	RO	4321	V_{PWR} LSB								—
0x2F		RO		Reserved		V_{PWR} MSB						—

Table 2-7. Extended Register Set—Port Parametric Measurement

Address	Name	R/W	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
0x30	I-LSB	RO	1	Port 1 Current LSB								0000,0000b
0x31	I-MSB	RO	1	Reserved		Port 1 Current MSB						0000,0000b
0x32	V-LSB	RO	1	Port 1 Voltage LSB								0000,0000b
0x33	V-MSB	RO	1	Reserved		Port 1 Voltage MSB						0000,0000b
0x34	I-LSB	RO	2	Port 2 Current LSB								0000,0000b
0x35	I-MSB	RO	2	Reserved		Port 2 Current MSB						0000,0000b
0x36	V-LSB	RO	2	Port 2 Voltage LSB								0000,0000b
0x37	V-MSB	RO	2	Reserved		Port 2 Voltage MSB						0000,0000b
0x38	I-LSB	RO	2	Port 3 Current LSB								0000,0000b

.....continued												
Address	**Name**	**R/W**	**Type**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset State**
0x39	I-MSB	RO	2	Reserved		Port 3 Current MSB						0000,0000b
0x3A	V-LSB	RO	2	Port 3 Voltage LSB								0000,0000b
0x3B	V-MSB	RO	2	Reserved		Port 3 Voltage MSB						0000,0000b
0x3C	I-LSB	RO	2	Port 4 Current LSB								0000,0000b
0x3D	I-MSB	RO	2	Reserved		Port 4 Current MSB						0000,0000b
0x3E	V-LSB	RO	2	Port 4 Voltage LSB								0000,0000b
0x3F	V-MSB	RO	2	Reserved		Port 4 Voltage MSB						0000,0000b

Table 2-8. Extended Register Set—Configuration 1

Address	Name	R/W	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
0x40	Foldback and Inrush	RW	4321	Not Used				Adjustable Inrush				0000,0000b
								Port 4	Port 3	Port 2	Port 1	
0x41	Firmware	RO	System	Firmware Revision								xxxx,xxxxb (Note 1)
0x43	Device ID	RO	System	Device ID			Silicon revision					Contact Microchip for the most updated firmware.

Note:

1. x = Unknown variable

Table 2-9. Port Signature Measurements

Address	Name	R/W	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
0x44	Detect Resistance	RO	4	Port 1 Detection Signature Resistance								0000,0000b
0x45	Detect Resistance	RO	3	Port 2 Detection Signature Resistance								0000,0000b
0x46	Detect Resistance	RO	2	Port 3 Detection Signature Resistance								0000,0000b
0x47	Detect Resistance	RO	1	Port 4 Detection Signature Resistance								0000,0000b
0x48	Detect Resistance	RO	4	Port 1 Detection Signature Capacitance								0000,0000b
0x49	Detect Resistance	RO	3	Port 2 Detection Signature Capacitance								0000,0000b
0x4A	Detect Resistance	RO	2	Port 3 Detection Signature Capacitance								0000,0000b
0x4B	Detect Resistance	RO	1	Port 4 Detection Signature Capacitance								0000,0000b

Table 2-10. Assigned Class Status

Address	Name	R/W	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
0x4C	Assigned Class	RO	1	Assigned Class Port 1				Requested Class Port 1				0000,0000b
0x4D		RO	2	Assigned Class Port 2				Requested Class Port 2				0000,0000b
0x4E		RO	3	Assigned Class Port 3				Requested Class Port 3				0000,0000b
0x4F		RO	4	Assigned Class Port 4				Requested Class Port 4				0000,0000b

Table 2-11. AutoClass Configuration and Status

Address	Name	R/W	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
0x51	AutoClass Power	RO	1	Done	Calculated AutoClass Power Port 1							0000,0000b
0x52		RO	2	Done	Calculated AutoClass Power Port 2							0000,0000b
0x53		RO	3	Done	Calculated AutoClass Power Port 3							0000,0000b
0x54		RO	4	Done	Calculated AutoClass Power Port 4							0000,0000b

3. Register Functionality

The address of each register represents a byte of data.

The register has the following modes:

- **RO**: Read only, this register can be read by the host (this register cannot be set by the host).
- **R/W**: Read/Write, this register can be read and set by the host.
- **COR**: Clear On Read, this register can be read only by the host (once it is read, its value is reset).
- **Type**:
  - System: The register represents functionality of the whole I^2C address, linked to this register.
  - Port: The register represents functionality of a port or a few ports, the related port number is written in the cell.

3.1 Event Registers (0x00 to 0x0B)

0x00—Interrupt Event

Each bit represents a system event. When the bit is equal to 1, it indicates that an event has occurred.

The following table lists the events associated with the register.

Table 3-1. System Event

Bit	Event Name	Event Description
0	Power Enable	Port has started power-up cycle.
1	Power Good	Port has finished the power-up stage and is delivering power.
2	Disconnect	Port that delivered power has moved from ON to OFF status.
3	I^2C Bus Soft Reset/Legacy Detection Ready	I^2C bus, 50 ms timeout from Start to Stop condition IEEE® detection fail and legacy detection reset is ready to read.
4	Classification Done	Classification and AutoClass completed
5	Overload	Overload or current limit event
6	Start Error	Inrush current too high or insufficient power allocation
7	Supply	Failure related the system supply

0x01—Interrupt Mask

Each bit represents a mask to a system event, described in register 0x00.

When the bit is set by the host to 1, an event is reported in the relative bit of register 0x00.

0x02/0x03—Power Events

These two registers indicate any change in port power good/power enable status.

Register 0x02 is a read only register.

Register 0x03 is a COR register; when it is read, both the registers, 0x02 and 0x03, are cleared.

Register 0x10 (Power Status) provides the actual power status of the port.

Bits 0...3 indicate power enable/disable change:

- 0 = No change
- 1 = Change occurred

Bits 4...7 indicate power good change

- 0 = No change
- 1 = Change occurred

0x04/0x05—Detection, Classification, and Connection Check Events

These two registers indicate changes in Detection, Classification, and Connection Check Events status.

Register 0x04 is a read only register.

Register 0x05 is a COR register; when it is read, both the registers, 0x04 and 0x05, are cleared.

Registers 0x4C to 0x54 provide the full information about the requested class, assigned class, and AutoClass status.

Bits 0...3 indicate detection and connection check change.

- 0 = Detection and connection check not completed yet
- 1 = Detection and connection check have been completed

Bits 4...7 indicate detection and connection check change

- 0 = Classification not completed yet
- 1 = Classification has been completed

0x06/0x07—Underload/Overload Events

These two registers indicate changes in the port status due to underload/disconnect or overload event.

Register 0x06 is a read only register.

Register 0x07 is a COR register; when it is read, both registers 0x06 and 0x07 are cleared.

The port's power limit value can be set in register 0x29.

Bits 0...3 indicate an event of overload

- 0 = No change
- 1 = Power was removed from the ports due to overload

Bits 4...7 indicate an event of underload/PD disconnect/MPS

- 0 = No change
- 1 = Power was removed from the ports due to underload/PD disconnect/MPS

0x08/0x09—Power-up Fault/Current Limit Events

These two registers indicate changes in the port status due to port power-up fault (that is, high inrush), and when port was disconnected due to current limit event longer then T_{LIM} or short circuit.

Register 0x08 is a read only register.

Register 0x09 is a COR register; when it is read, both registers 0x06 and 0x07 are cleared.

Bits 0...3 indicate an event of power-up fault

- 0 = No fault
- 1 = Power up fault on the port

Bits 4...7 indicate an event of underload/PD disconnect/MPS

- 0 = No fault
- 1 = Power was removed from the ports due to current limit event/short

0x0A/0x0B—Supply Events

These two registers indicate failures in the power supply of the system.

Each bit reflects a certain failure.

Register 0x0A is a read only register.

Register 0x0B is a COR register; when it is read, both the registers, 0x06 and 0x07, are cleared.

The following table describes the failure associated with the two registers.

Table 3-2. Supply Failure Event

Bit	Event Name	Event Description
0	NA	Always 0
1	OSS Event	0 = No event 1 = An event occurred (Reg 0x00, bit 2 is also set due to OSS event)
2	4-Pair Port—Over Power Event (Ports 1 and 2)	0 = No event 1 = Over power of event occurred (Reg 0x00, bit 5 is also set)
3	4-Pair Port—Over Power Event (Ports 3 and 4)	0 = No event 1 = Over power of event occurred (Reg 0x00, bit 5 is also set)
4	V_{MAIN} too low	0 = No event 1 = V_{MAIN} is below the minimum threshold
5	V_{DD} too low warning	0 = No event 1 = V_{DD} is below the minimum warning threshold (2.7 V_{DC})
6	V_{DD} too low failure	0 = No event 1 = V_{DD} is below the minimum failure threshold (2.4 V_{DC}, PoE is disabled)
7	Over Temperature	0 = No event 1 = Temperature exceeds the setting

3.2 Status Registers (0x0C to 0x11)

These four registers that provide the port detection status are listed in Table 3-3, and the actual detected classification is listed in Table 3-4. These registers are read only.

- 0x0C: Port 1 Detection Status/Detected Classification
- 0x0D: Port 2 Detection Status/Detected Classification
- 0x0E: Port 3 Detection Status/Detected Classification
- 0x0F: Port 3 Detection Status/Detected Classification

Each register is divided into bits for detection status and requested class status.

Table 3-3. Detection Status (Bits 0...3)

Value Bin/Hex	Detection Status
0000b/0x0	Unknown: POR value
0001b/0x1	Short circuit
0010b/0x2	Port is pre-charged
0011b/0x3	Resistor is too low
0100b/0x4	Valid IEEE® 802.3bt detection
0101b/0x5	Resistor is too high
0110b/0x6	Port is open/empty
0111b/0x7	External voltage is detected on port

.....continued	
Value Bin/Hex	Detection Status
1110b/0x14	MOSFET_FAULT

Table 3-4. Requested Class Status (Bits 4...7)

Value Bin/Hex	Requested Class Status
0000b/0x0	Unknown: POR value
0001b/0x1	Class 1
0010b/0x2	Class 2
0011b/0x3	Class 3
0100b/0x4	Class 4
0101b/0x5	Reserved: Treated as class 0
0110b/0x6	Class 0
0111b/0x7	Over current
1000b/0x8	Class 5 4P SS
1001b/0x9	Class 6 4P SS
1010b/0xA	Class 7 4P SS
1011b/0xB	Class 8 4P SS
1100b/0xC	Class 4 + (PSE port is limited to type 1 power budget)
1101b/0xD	Class 5 4P DS
1110b/0xE	Reserved
1111b/0xF	Classification mismatch

Notes:

- SS = Single Signature
- DS = Dual Signature

0x10—Power Enable/Power Good

The Power Enable bit (bits 0..3, a bit per port) is set when a port is in powered-up process.

The Power Good Status bit (bits 4..7, a bit per port) represents a power delivery port, after it is turned on successfully.

This register is linked to the event registers 0x02/0x03.

Bits 0...3 Power Enable

- 0 = Port is not in power-up process
- 1 = Port is in powered-up process

Bits 4...7 Power Good

- 0 = Port is off
- 1 = Port was powered-up successfully

0x11—I²C Status

Bits 3...6 provide the value of pins A1...A4 (pins 48..51), which set the I²C address of both quads.

3.3 Configuration Registers (0x12 to 0x19 and 0x27/0x28)

0x12—Port Operation Mode Setting

This register is read/write, to set all 4 ports according to Table 3-5.

Each 2 bits set a port according to Table 3-5:

- Bits 0..1 set port 1
- Bits 2..3 set port 2
- Bits 4..5 set port 3
- Bits 6..7 set port 4

Table 3-5. Port Operation Mode

Port Operation Mode	Description	Value
Disable	Any PoE activity is disabled (detection, classification, power).	00b
Autonomous	PSE is enabled. Detection, classification, power-up, and power are preformed automatically.	11b

0x15—Port Priority

This register is read/write.

Bits 0..3 should be set to 0.

Bits 4..7 set if the port are effected by the OSS pin:

- Bit 4 sets port 1
- Bit 5 sets port 2
- Bit 6 sets port 3
- Bit 7 sets port 4

When the bit is set to 0, the port is not disconnected due to OSS level changes.

When the bit is set to 1, the power of that port is removed during OSS changes.

0x17—Misc

This register is read/write, only bit 4 should be set.

Bit 4 set the OSS mode:

- 0 = OSS mode is a single bit
- 1 = OSS is multi-bit

0x19—Power Pushbutton

This register is read/write.

Bits 4..7 are used to disable momentary the PoE activity of the ports, bit per port.

After that the port will continue its activity per register 0x14

- 0 = Performs nothing.
- 1 = Port is momentary turned off. After the action, the bit will be internally cleared. After the action, the bit will be internally cleared.

A bit per port:

- Bit 4 sets port 1
- Bit 5 sets port 2

- Bit 6 sets port 3
- Bit 7 sets port 4

0x27/0x28—Multi-Bit Priority

These 2 registers are read/write, only bit 4 should be set, all other bits should be kept as in the default.

In each register, the priority of two ports can be set, 8 levels of priority, while priority 7 is the highest priority, and priority 0 is the lowest.

Register 0x27 sets the priority of ports 1, 2.

Register 0x28 sets ports 3, 4.

3.4 General Registers (0x1B and 0x1C)

0x1B—Manufacture ID and Chip IC

This register is read only.

The register value is 0x2D (00101101b).

0x1C—AutoClass and Connection Check Result

This register is read only.

Bits 0...1 provide the result of the connection check of the first 4-pair port (ports 1 and 2), per Table 3-6.

Bits 2...3 provide the result of the connection check of the second 4-pair port (ports 3 and 4), per Table 3-6.

Table 3-6. Connection Check Result

Value	Connection Check Result
0x0	Unknown or incomplete.
0x1	4-pair single signature.
0x2	4-pair dual signature.
0x3	Faulty connection check, or invalid signature detected on one of the pair sets.

Bits 4...7 Indicate if the connected PD supports AutoClass:

- 0 = PD does not support AutoClass
- 1 = PD supports AutoClass

A bit per port:

- Bit 4 sets port 1
- Bit 5 sets port 2
- Bit 6 sets port 3
- Bit 7 sets port 4

Note: The result of the AutoClass measurements is read in registers 0x51 to 0x54.

3.5 Specialized Registers (0x24 to 0x2F)

0x24/0x25—Power on Error

These two registers indicate an error during power on sequence (detection, classification, or insufficient power).

Register 0x24 is a read only register.

Register 0x25 is a COR register; when it is read, both registers 0x24 and 0x25 are cleared.

Each port is represented by 2 bits, as seen in Table 3-8:

- Bits 0..1 represent port 1
- Bits 2..3 represent port 2
- Bits 4..5 represent port 3
- Bits 6..7 represent port 4

Table 3-7. Power on Error Result

Value	Power on Failure Description
0x0	No failure
0x1	Invalid detection
0x2	Invalid classification
0x3	Insufficient power

0x26—Ports Matrix (Remap)

This register is read/write, is intended re-arrange the ports matrix differently than the default matrix (0xE4).

If the register is not modified by the user, the default port matrix is shown in Table 3-8.

Each port is represented by 2 bits:

- Bits 0..1 represent logical port 1
- Bits 2..3 represent logical port 2
- Bits 4..5 represent logical port 3
- Bits 6..7 represent logical port 4

Table 3-8. Default Port Matrix

Bits	Value	Logical Port	Physical Port
0..1	0 (00b)	1	1
2..3	1 (01b)	2	2
4..5	2 (10b)	3	3
6..7	3 (11b)	4	4

0x2A/0x2B—4-Pair Police Configuration

These two registers are read/write, to set the power limit of the ports (P_{CUT}).

Register 0x2A sets the 4-pair port based ports 1 and 2.

Register 0x2B sets the 4-pair port based ports 3 and 4.

The following table lists the power level of the 4-pair port.

The power limit is equal to **P_{CUT} = 0.5 * Value**

Table 3-9. P_{CUT} Value

Assigned Class	Value Hex/Dec	Minimum P_{CUT} Setting (0x17 Bit 0 = 0)	Minimum P_{CUT} Setting (0x17 Bit 0 = 1)
Class 0	0x22 (34d)	15.5W	17W
Class 1	0x08 (8d)	4W	17W
Class 2	0x0E (14d)	7W	17W
Class 3	0x22 (34d)	15.5W	17W
Class 4	0x40 (64d)	30W	32W

.....continued			
Assigned Class	**Value Hex/Dec**	**Minimum P_{CUT} Setting (0x17 Bit 0 = 0)**	**Minimum P_{CUT} Setting (0x17 Bit 0 = 1)**
Class 5—4P SS	0x5A (90d)	45W	45W
Class 6—4P SS	0x78 (120d)	60W	60W
Class 7—4P SS	0x96 (150d)	75W	75W
Class 8—4P SS	0xB4 (180d)	90W	90W
Class 4+—Type 1 limited	0x22 (34d)	15.5W	17W
ANY 4P DS PD	0xB4 (180d)	90W	90W

0x2C—Chip Temperature

This is a read-only register provide the die temperature, based on the following formula:

```
367 – {2 * (regVal_decimal)} (degrees Celsius)
```

0x2E/0x2F—V_{MAIN} Measurement

These two registers are read only, and provide the level of V_{MAIN} by 14 bits, with resolution of 64.4 mV per bit.

Register 0x2E represents the 8 LSB bits of the measurement.

Register 0x2F represents the 6 MSB bits, bits 6 and 7 of that register are not used.

The maximum value can be measured is 61V, V_{MAIN} above 61V is reported as 61V (0x3B3).

Example: V_{MAIN} of 55V is provided as `0x356 (55V/64.4 mV = 854)`.

3.6 Port Voltage and Current Measurement Registers (0x30 to 0x3F)

The voltage and current of each port are provided by four registers (two for port voltage and two for current).

- The two current registers per port provide the current level by 14 bits, with resolution of 1 mA per LSB. The maximum value that can be measured is 1020 mA, current above that level is reported as 1020 mA (0x3FC).
- The two voltage registers per port provide the voltage level by 14 bits, with resolution of 64.4 mV per LSB. The maximum value can be measured is 61V, voltage above that level is reported as 61V (0x3B3).

0x30/0x31—Port 1 Current Measurement

Register 0x30 represents the 8 LSB bits of the measurement.

Register 0x31 represents the 6 MSB bits, bits 6 and 7 of that register are not used.

0x32/0x33—Port 1 Voltage Measurement

Register 0x30 represents the 8 LSB bits of the measurement.

Register 0x31 represents the 6 MSB bits, bits 6 and 7 of that register are not used.

0x34/0x35—Port 2 Current Measurement

Register 0x30 represents the 8 LSB bits of the measurement.

Register 0x31 represents the 6 MSB bits, bits 6 and 7 of that register are not used.

0x36/0x37—Port 2 Voltage Measurement

Register 0x30 represents the 8 LSB bits of the measurement.

Register 0x31 represents the 6 MSB bits, bits 6 and 7 of that register are not used.

0x38/0x39—Port 3 Current Measurement

Register 0x30 represents the 8 LSB bits of the measurement.

Register 0x31 represents the 6 MSB bits, bits 6 and 7 of that register are not used.

0x3A/0x3B—Port 3 Voltage Measurement

Register 0x30 represents the 8 LSB bits of the measurement.

Register 0x31 represents the 6 MSB bits, bits 6 and 7 of that register are not used.

0x3C/0x3D—Port 4 Current Measurement

Register 0x30 represents the 8 LSB bits of the measurement.

Register 0x31 represents the 6 MSB bits, bits 6 and 7 of that register are not used.

0x3E/0x3F—Port 4 Voltage Measurement

Register 0x30 represents the 8 LSB bits of the measurement.

Register 0x31 represents the 6 MSB bits, bits 6 and 7 of that register are not used.

3.7 Port Inrush Current Control Register (0x40)

0x40—Inrush Current Control

Only bits 0–3 are active, bits 4–7 are not used.

Each bit sets a port:

- Bit 0 sets port 1
- Bit 1 sets port 2
- Bit 2 sets port 3
- Bit 3 sets port 4
  - 0: If in the end of the start-up period inrush current is still high, port is not powered up.
  - 1: If in the end of the start-up period inrush current is still high, port is powered up normally.

3.8 Firmware Version and Chip ID Registers (0x41 and 0x43)

0x41—Firmware Version

This register is read only.

For the most recent version, contact Microchip.

0x43—Silicon Version and Chip ID

This register is read only.

Bits 0...4 show the chip ID.

Bits 5...7 show the silicon version.

For the most recent version, contact Microchip.

3.9 Port Signature Measurement Registers (0x44 to 0x4B)

0x44–0x47—Signature Measured Resistance

These four registers are read only, and provide the resistance measured during the signature detection.

Register per port, 256Ω per bit (480Ω for short, 65280Ω maximum).

0x48–0x4B—Signature Measured Capacitance

These four registers are read only, and provide the capacitance measured during the signature detection.

Register per port, with a resolution of 64 nF per bit.

3.10 Port Classification Status Registers (0x4C to 0x4F)

These four registers are read only and provide PD's requested class and the port's assigned class. The following table lists both values (requested and assigned).

Table 3-10. Requested and Assigned Values

Value of Requested and Assigned Bits				Class Status
0	0	0	0	Unknown
0	0	0	1	Class 1
0	0	1	0	Class 2
0	0	1	1	Class 3
0	1	0	0	Class 4
0	1	0	1	NA
0	1	1	0	Class 0
0	1	1	1	NA
1	0	0	0	Class 5—4-Pair SS
1	0	0	1	Class 6—4Pair SS
1	0	1	0	Class 7—4-Pair SS
1	0	1	1	Class 8 —4-Pair SS
1	1	0	0	NA
1	1	0	1	Class 5—4-Pair DS
1	1	1	0	NA
1	1	1	1	NA

Notes:

- SS = Single Signature; DS = Dual Signature.
- If PSE has limited power budget and cannot deliver the power that the PD asks for, the port's assigned class might be lower than the PD's requested class.

0x4C—Port 1 Class Status

Bits 0...3 provide PD's requested class.

Bits 4...7 provide the port's assigned class.

0x4D—Port 2 Class Status

Bits 0...3 provide PD's requested class.

Bits 4...7 provide the port's assigned class.

0x4E—Port 3 Class Status

Bits 0...3 provide PD's requested class.

Bits 4...7 provide the port's assigned class.

0x4F—Port 4 Class Status

Bits 0...3 provide PD's requested class.

Bits 4...7 provide the port's assigned class.

3.11 AutoClass Status Registers (0x51 to 0x54)

These four registers are read only and provide the AutoClass measurement and status.

Bits 0...6 provide the power measured during the AutoClass stage, with a resolution of 0.5W per LSB.

Bit 7 provides the AutoClass status:

- 0 = Measurement was not performed.
- 1 = AutoClass measurement was completed.

0x51—Port 1 AutoClass Status

Bits 0...6 are PD's requested class.

Bit 7 is AutoClass status.

0x52—Port 2 AutoClass Status

Bits 0...6 are PD's requested class.

Bit 7 is AutoClass status.

0x53—Port 3 AutoClass Status

Bits 0...6 are PD's requested class.

Bit 7 is AutoClass status.

0x53—Port 3 AutoClass Status

Bits 0...6 are PD's requested class.

Bit 7 is AutoClass status.

4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
B	4/2023	Added section 1. Automode Operational Flowchart and Figure 1-1
A	04/2023	Initial Revision

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