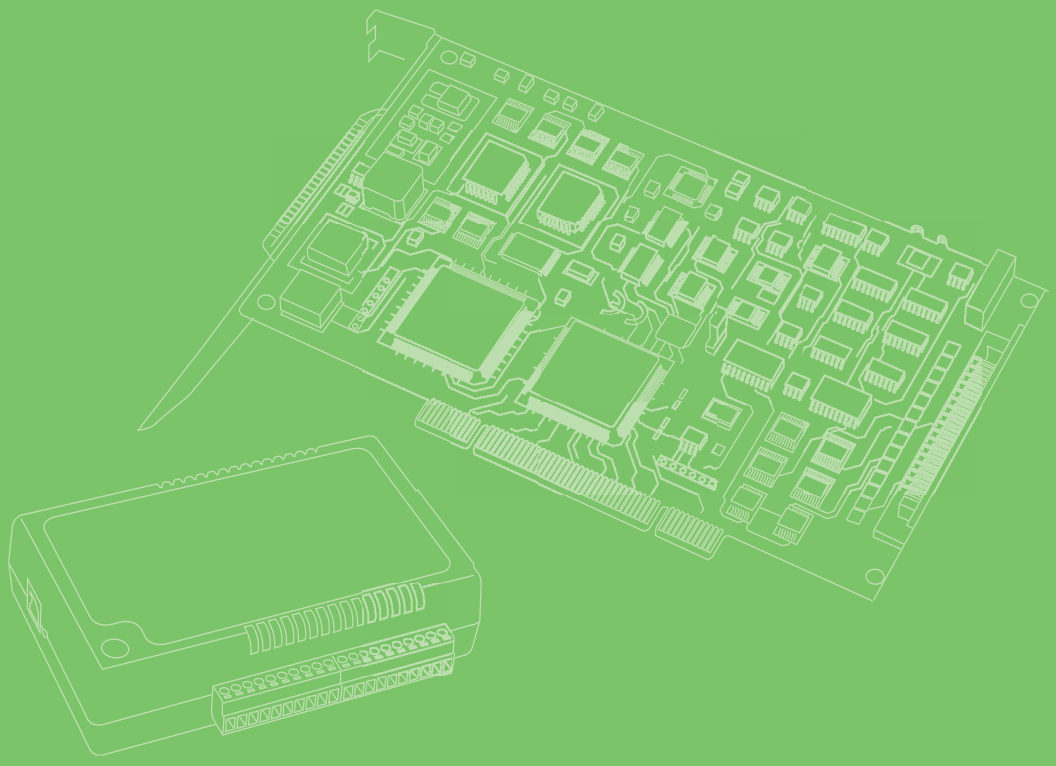

User Manual

PCIE-1812

16-bit Multifunction Card with PCI Express Bus

ADVANTECH

Enabling an Intelligent Planet

Copyright

Acknowledgments

Intel® and Pentium® are trademarks of Intel Corporation.

Microsoft Windows and MS-DOS are registered trademarks of Microsoft Corp.

All other product names or trademarks are properties of their respective owners.

Product Warranty (2 years)

Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced free of charge during the warranty period. For out-of-warranty repairs, customers will be billed according to the cost of replacement materials, service time, and freight. Please consult your dealer for more details.

If you believe your product to be defective, follow the steps outlined below.

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain a return merchandize authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

Part No. 2001181213 Edition 4

Printed in China February 2025

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This type of cable is available from Advantech. Please contact your local supplier for ordering information.

Technical Support and Assistance

1. Visit the Advantech website at www.advantech.com/support to obtain the latest product information.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before calling:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Packing List

Before system installation, check that the items listed below are included and in good condition. If any item does not accord with the list, contact your dealer immediately.

- PCIE-1812 card
- Startup Manual

Safety Precautions - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from the PC chassis before manual handling. Do not touch any components on the CPU card or other cards while the PC is powered on.

3. Disconnect the power before making any configuration changes. A sudden rush of power after connecting a jumper or installing a card may damage sensitive electronic components.

Contents

Chapter 1

Start Using PCIE-1812

1.1 Product Overview

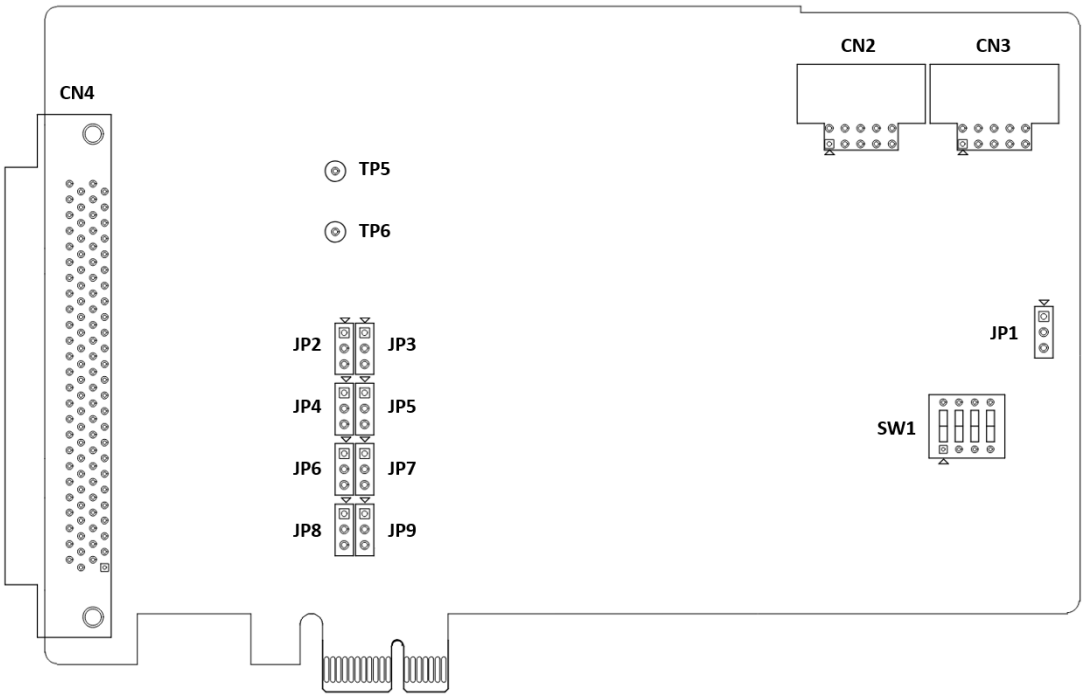

Figure 1.1 Card Layout

Table 1.1: List of connectors and switches

Component	Function
SW1	Board ID
CN2	MDSI IN
CN3	MDSI OUT
CN4	100-pin SCSI Connector
JP1	Power-on Configuration.
JP2 ~ JP9	DI/O Control Selection
TP5	Positive terminal for voltage reference calibration.
TP6	Negative terminal for voltage reference calibration.

1.2 Products Features

1.2.1 Board ID

A board ID can be assigned through the onboard slide switch for the device. The board ID value in the device description of the software is used to map the device in the software to the actual hardware device. Board ID is useful when there are multiple hardware devices with the same model name in the system. Without the board ID, users cannot recognize which device in the software that the hardware device is related to.

When configured as 0, the board ID is automatically assigned by the device driver software. When configured as value other than 0, the configured value is used. Do not configure the same value (except for 0) for hardware devices with the same model name. Refer to the device specifications for the configuration of the board ID.

If changed, the new board ID value takes effect only after a cold reset of the device.

1.3 Driver Installation

The driver package can be found on Advantech Support Portal (https://www.advantech.com/support). Search for PCIE-1812 on the support portal for the corresponding driver/SDK package. The XNavi installer will kick in after the download finishes.

Execute the installer and it will guide you through the session. You can choose the device and software components you'd like to install in the system (Figure 1. 2). After selection, click on "start" to begin the installation.

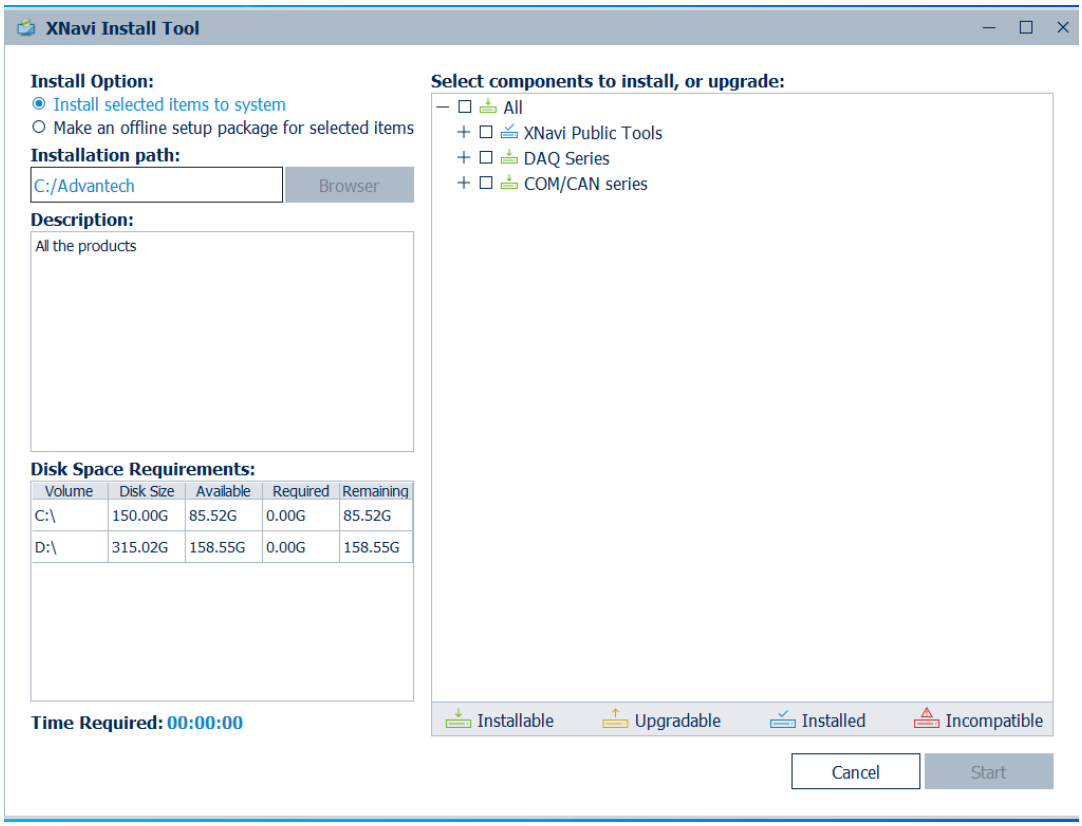

Figure 1.2 XNavi Installation Interface

1.4 Software Utility

Advantech offers device drivers, SDKs, third-party driver support and application software to help fully exploit the functions of your DAQ devices. All these software packages are available on Advantech website: http://www.advantech.com/.

The Advantech Navigator is a utility that allows you to set up, configure and test your device, and later store your settings in a proprietary database.

1. To set up the I/O device for your card, you should first run the Advantech Navigator program (by accessing Start/Programs/Advantech Automation/DAQNavi/Advantech Navigator). The settings could also be saved.
2. You can then view the device(s) already installed on your system (if any) on the Installed Device tree view. If the software and hardware installation are completed, you will see your DAQ devices in the Installed Devices list.

1.5 Software Development Using DAQNavi SDK

DAQNavi SDK is the software development kit for programming applications with Advantech DAQ products. The necessary runtime DLL, header files, software manual and tutorial videos can be installed via the XNavi installer. They can be found under C:\Advantech\DAQNavi (default directory) after finishing the installation.

1.6 FPGA Code Updates

The FPGA can also be updated via the interface in Navigator. However, it is not advised to update FPGA without first doing some research. Advantech strongly suggests you consult your technical support before starting an FPGA update.

Chapter 2

Installation Guide

2.1 Initial Unpacking Check

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

- PCIE-1812 card
- Startup Manual

2.2 Hardware Installation and Configuration

2.2.1 Installation

Before you install your PCIE-1812, please make sure you have the following components:

- PCIE-1812 card
- PCIE-1812 User Manual
- Advantech DAQNavi SDK and its corresponding device driver
- Personal computer or workstation with PCI Express interface
- Accessories (optional)
  - PCL-101100R-1E: 100-pin SCSI shielded cable, ribbon-type to pin-type, 1 m
  - PCL-101100R-2E: 100-pin SCSI shielded cable, ribbon-type to pin-type, 2 m
  - ADAM-39100-BE: 100-pin SCSI DIN-rail wiring board

When the necessary components are prepared, you can begin the installation procedure as follows:

1. Install Advantech DAQNavi SDK and the corresponding device driver. They can be downloaded from Advantech website.
2. Turn off the computer. (for PCI or PCIe cards only)
3. Install the hardware device.
4. Turn on the computer. (for PCI or PCIe cards only)
5. Use Navigator to test the functionality of the hardware.
6. Read software manual and examples.
7. Write your own applications.

2.2.2 Configuration - Board ID (SW1)

Table 2.1: Configuration - Board ID (SW1)

Board ID	Switch Position			
	1	2	3	4
0*	UP	UP	UP	UP
1	UP	UP	UP	DOWN
2	UP	UP	DOWN	UP
3	UP	UP	DOWN	DOWN
4	UP	DOWN	UP	UP
5	UP	DOWN	UP	DOWN
6	UP	DOWN	DOWN	UP
7	UP	DOWN	DOWN	DOWN
8	DOWN	UP	UP	UP
9	DOWN	UP	UP	DOWN
10	DOWN	UP	DOWN	UP
11	DOWN	UP	DOWN	DOWN
12	DOWN	DOWN	UP	UP
13	DOWN	DOWN	UP	DOWN
14	DOWN	DOWN	DOWN	UP
15	DOWN	DOWN	DOWN	DOWN

2.2.3 Configuration - DI/O Control Selection (JP2 ~ JP9)

Table 2.2: Configuration - DI/O Control Selection (JP2 ~ JP9)

Jumper Setting	Description
	DI/O channel direction is software configurable.*
	DI/O channels are fixed at output

* Default setting.

Table 2.3:	
Jumper	**Controlled DI/O channels**
JP2	DI/O 0 ~ DI/O 3
JP3	DI/O 4 ~ DI/O 7
JP4	DI/O 8 ~ DI/O 11
JP5	DI/O 12 ~ DI/O 15
JP6	DI/O 16 ~ DI/O 19
JP7	DI/O 20 ~ DI/O 23
JP8	DI/O 24 ~ DI/O 27
JP9	DI/O 28 ~ DI/O 31

* Default setting.

2.2.4 Multi-Device Synchronization Interface (CN2 ~ CN3)

Table 2.4: Multi-Device Synchronization Interface (CN2 ~ CN3)	
Connector	**Description**
CN2	MDSI input.
CN3	MDSI output.

Note! Refer to “3.7 Synchronize by MDSI Cables/Table 3.1” for description of these connectors.

2.3 Signal Connection and Pin Assignment

2.3.1 Analog Input Signal Connection

An analog input channel measures the voltage (VS) of the external source. The voltage difference between the positive terminal and the negative terminal is being measured.

The voltage is then amplified or attenuated by a programmable gain instrumentation amplifier (PGIA), conditioned by a low-pass filter (LPF), and sampled and converted into a digital form of data by an analog-to-digital converter (ADC). The ADC of every channel samples the signal at the same time, and this architecture is thus called simultaneous sampling.

Analog input signal connection and internal functional block diagram is shown in Figure 2. 1.

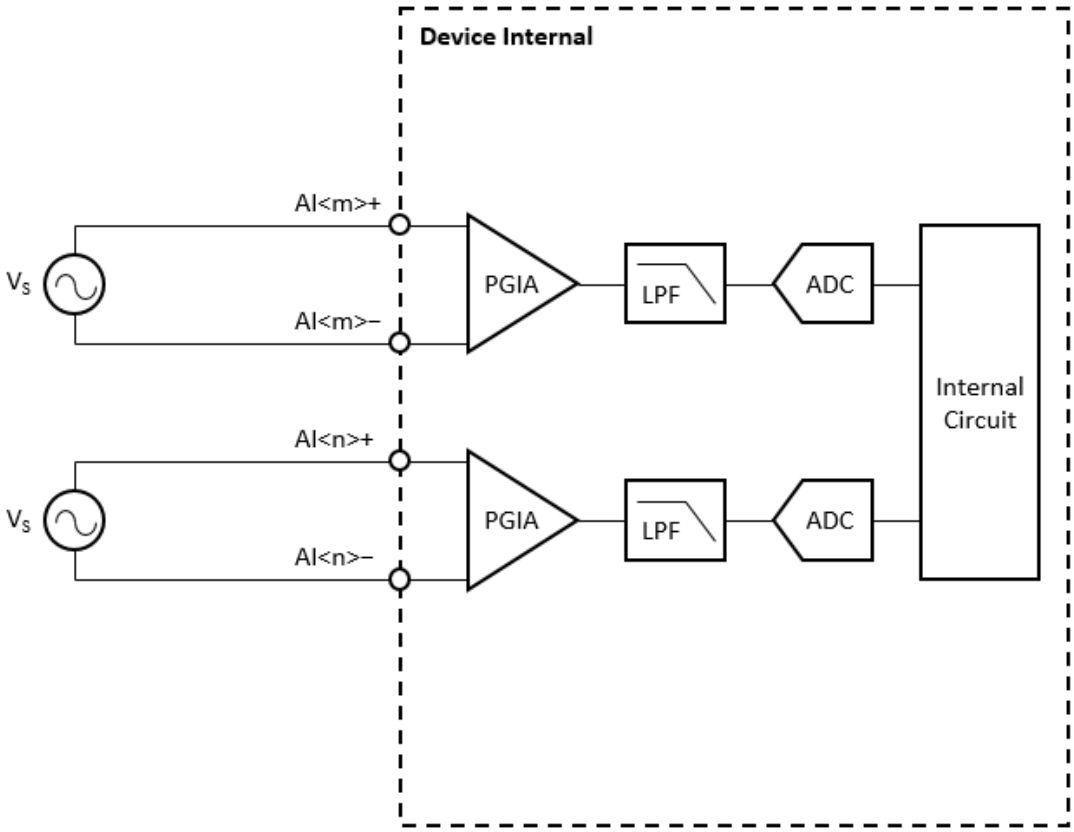

Figure 2.1 Analog input signal connection

2.3.2 Analog Output Signal Connection

An analog output channel generates a voltage output to the load. The voltage to be generated is first sent by the internal controller to the digital-to-analog converter (DAC) in a form of digital data, and the data is converted by the DAC to an analog output voltage. The analog output channel is of single-ended type; hence the load should be connected between the analog output (AO) terminal and the analog ground (AGND) terminal. This is shown in Figure 2. 2.

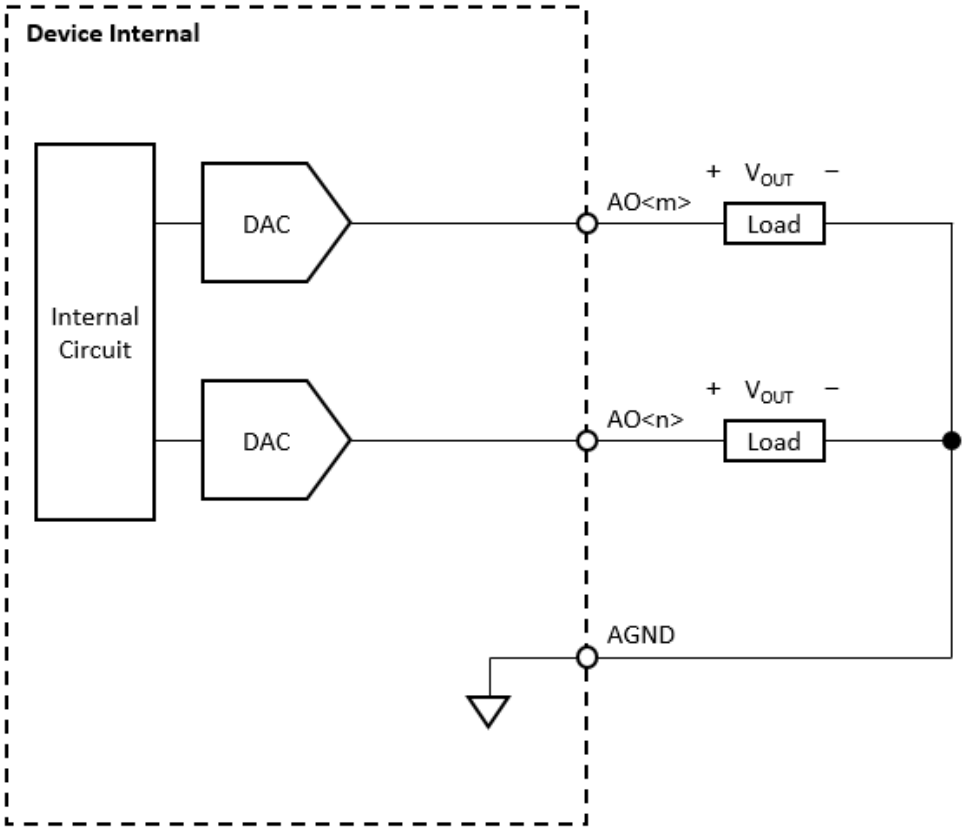

Figure 2.2 Analog output signal connection

Multiple output ranges are supported and can be selected by software for each channel independently. Be sure that the load resistance is within the range of the device specifications, or the output voltage may not reach the specified value due to the limitation of output driving capability.

The output range can also be defined by an external reference voltage which is connected to the analog output reference (AO_REF) terminal. Refer to the device specifications for the relationship between the output range and the external reference voltage. In this configuration, however, the output voltage is not calibrated, and the accuracy of the output voltage depends on the accuracy of the external reference voltage. Users can perform calibration through the calibration utility in the Advantech Navigator by themselves.

2.3.3 Trigger Input Signal Connection

The trigger can come from one of various signal sources. If the signal source is of digital type (logic high or low), it is called a digital trigger. On the other hand, if the signal source is of analog type (voltage level), it is called an analog trigger.

Digital Trigger

A digital trigger can be configured as rising edge active or falling edge active, as shown in Figure 2. 3, Figure 2. 4 respectively.

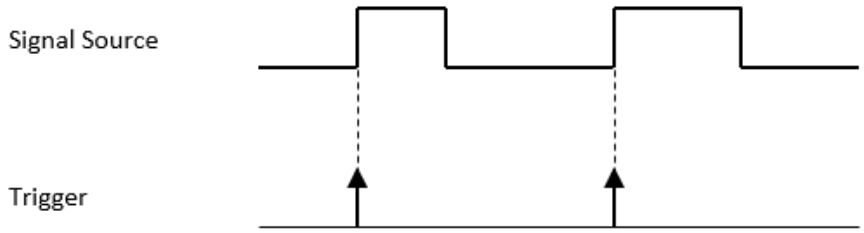

Figure 2.3 Rising edge active digital trigger

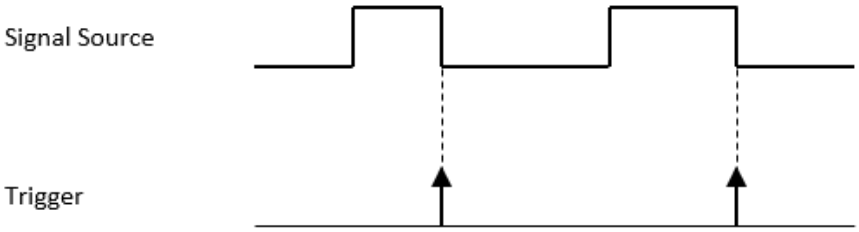

Figure 2.4 Falling edge active digital trigger

Analog Trigger

In addition to active edge, users can configure the threshold level and the hysteresis value for an analog trigger. The threshold level specifies the analog input voltage level where the trigger occurs. The hysteresis value prevents unwanted triggers due to noisy signals.

A rising edge active analog trigger occurs when the signal crosses the threshold level from below. And another trigger occurs only if the signal has crossed the voltage specified by the threshold level minus the hysteresis value from above before it crosses the threshold level from below again. This is shown in Figure 2. 5.

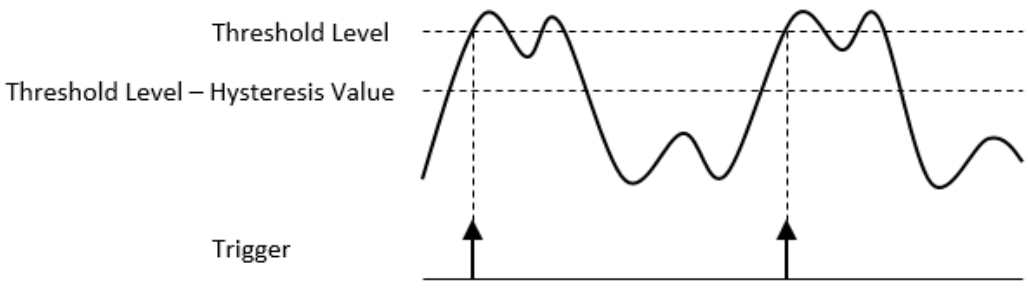

Figure 2.5 Rising edge active analog trigger

A falling edge active analog trigger occurs when the signal crosses the threshold level from above. And another trigger occurs only if the signal has crossed the voltage specified by the threshold level plus the hysteresis value from below before it crosses the threshold level from above again. This is shown in Figure 2. 6.

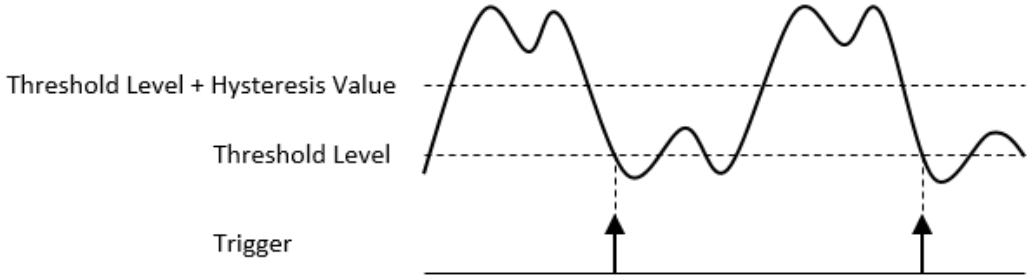

Figure 2.6 Falling edge active analog trigger

2.3.4 Digital Input Signal Connection

A digital input/output (DI/O) channel can be configured by software to perform digital input measurement, which is the power-on default configuration, or digital output generation. When performing digital input measurement, the voltage logic level between the digital input (DI) terminal and the digital ground (DGND) terminal is measured. To prevent undetermined or fluctuating results when input is floating, the digital input channel can be configured as internally pulled-up or pulled-down by software. This is shown in Figure 2. 7.

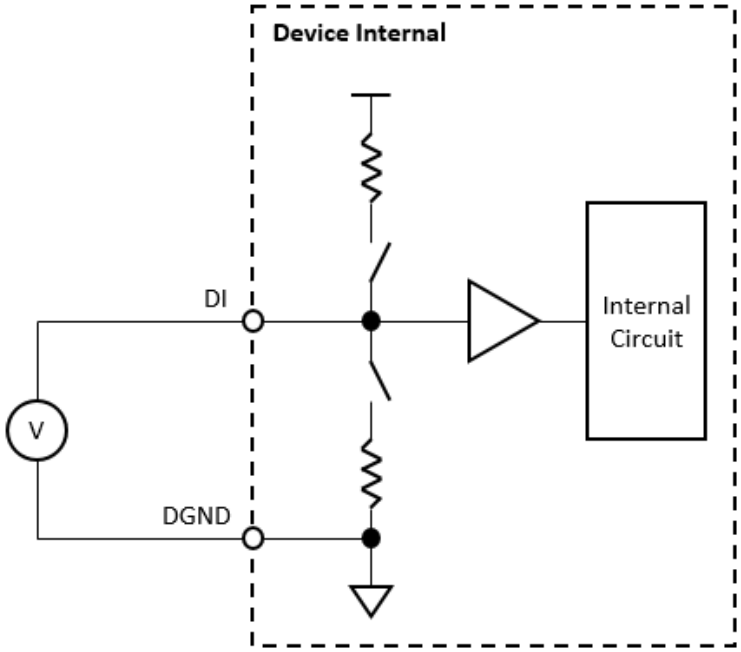

Figure 2.7 Digital input signal connection

The input voltage must be higher than the minimum ON state value or lower than the maximum OFF state value to ensure a predictable outcome. If the input voltage falls between these two values, the result will be indeterminate and could be either ON or OFF. Additionally, avoid applying a voltage that exceeds the maximum allowable ON state value or falls below the minimum allowable OFF state value, as this may cause damage to the device. Please refer to the device specifications for the exact ON and OFF voltage ranges.

The digital input channel can also sense the status of an external switch. When configured as internally pulled-up, the status of an external switch which is connected between the DI terminal and the DGND terminal is sensed as shown in Figure 2. 8. When configured as internally pulled-down, the status of an external switch which is connected between the external source and the DI terminal is sensed as shown in Figure 2. 9. Be sure the voltage of the external source is within the allowable range of the ON state as specified in the device specifications.

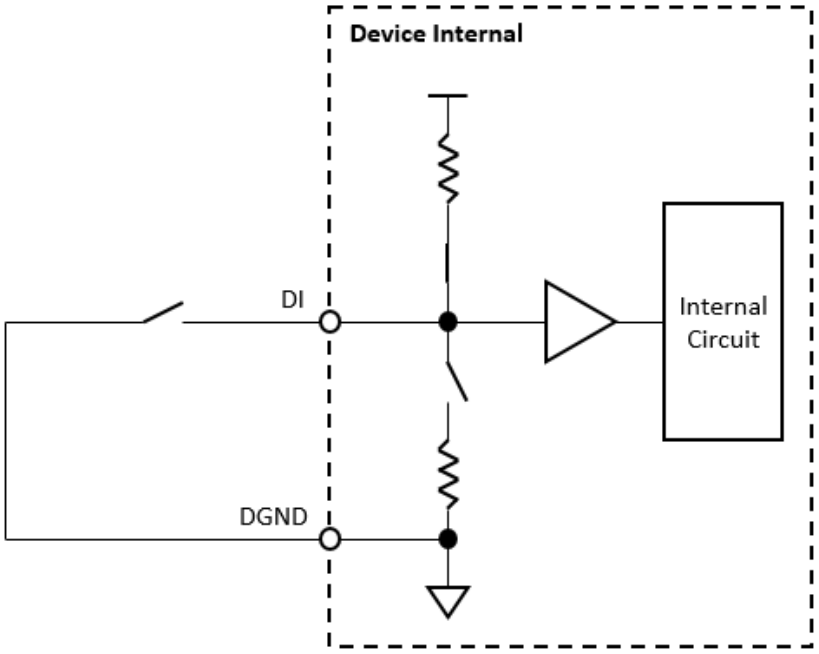

Figure 2.8 Digital input signal connection using a switch with internal pull-up resistor

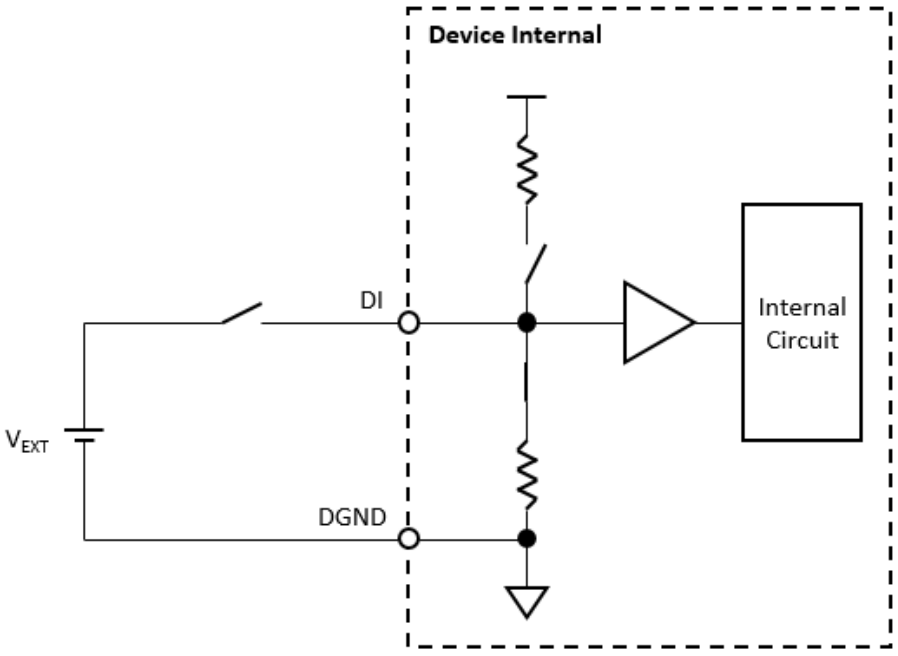

Figure 2.9 Digital input signal connection using a switch with internal pull-down resistor

2.3.5 Digital Output Signal Connection

A digital input/output (DI/O) channel can be configured by software to perform digital input measurement, which is the power-on default configuration, or digital output generation. When performing digital output generation, a voltage logic level is generated between the digital output (DO) terminal and the digital ground (DGND) terminal. This is shown in Figure 2. 10.

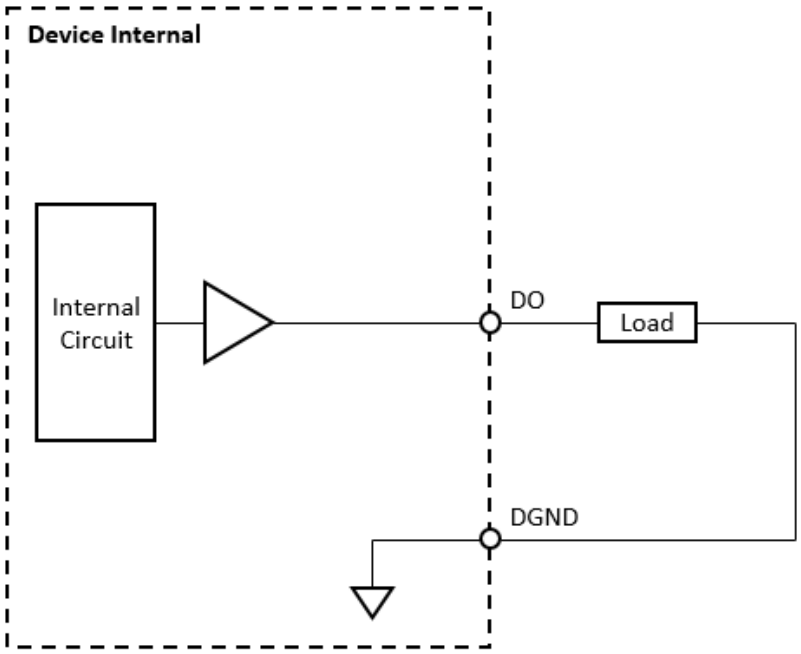

Figure 2.10 Digital output signal connection

Each digital output channel can source or sink only finite amount of current. If this limit is exceeded, the output voltage will not stay in the specified voltage logic level. Refer to the device specifications for the maximum source and skin current values.

2.3.6 Counter Input Signal Connection

The voltage logic level between the counter input (counter clock, counter gate, counter arm, and sample clock) terminals and the digital ground (DGND) terminal is measured. To prevent undetermined or fluctuating results when input is floating, the counter input signals are internally pulled-up. This is shown in Figure 2. 11.

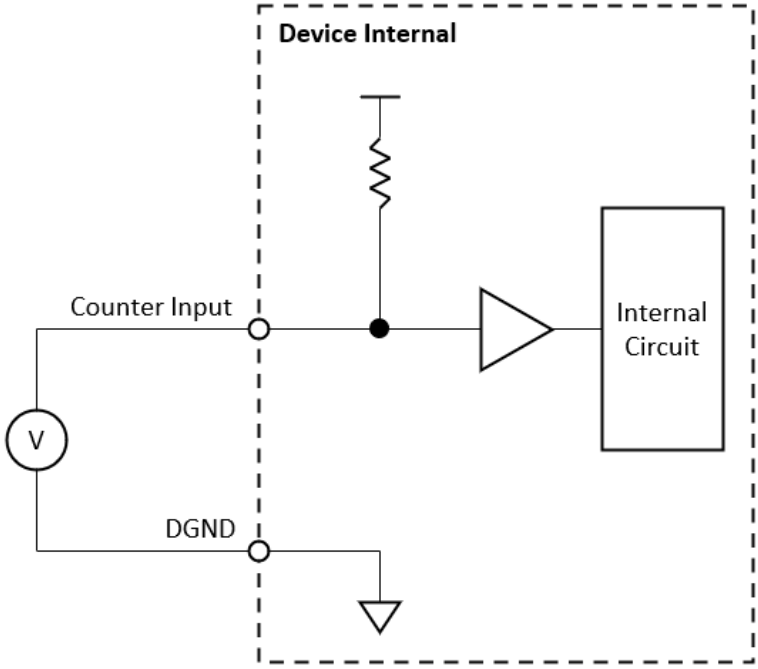

Figure 2.11 Counter input signal connection

The input voltage must be either higher than the minimum value of ON state or lower than the maximum value of OFF state for a deterministic result. If the input voltage is between these two values, the result is undetermined, which may be ON or OFF. In addition, do not input a voltage higher than the maximum allowable value of the ON state or lower than the minimum allowable value of the OFF state. The device may be damaged under such circumstance. Refer to the device specifications for ON and OFF state voltage ranges.

The counter input signals can also sense the status of an external switch. The status of an external switch which is connected between the counter input terminals and the DGND terminal is sensed as shown in Figure 2. 12.

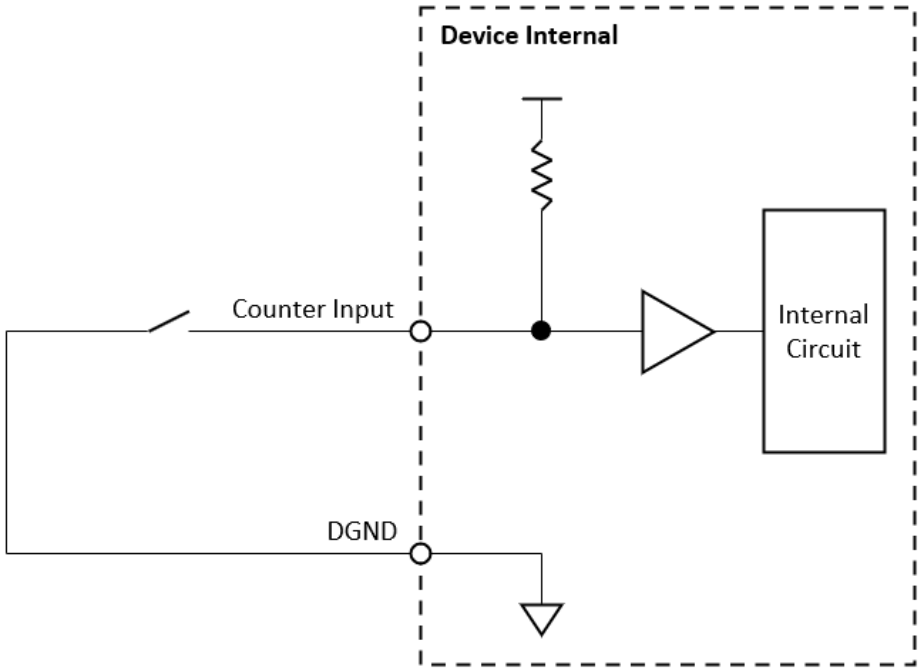

Figure 2.12 Counter input signal connection using a switch with internal pull-up resistor

2.3.7 Counter Output Signal Connection

A voltage logic level is generated between the counter output terminal and the digital ground (DGND) terminal. This is shown in Figure 2. 13.

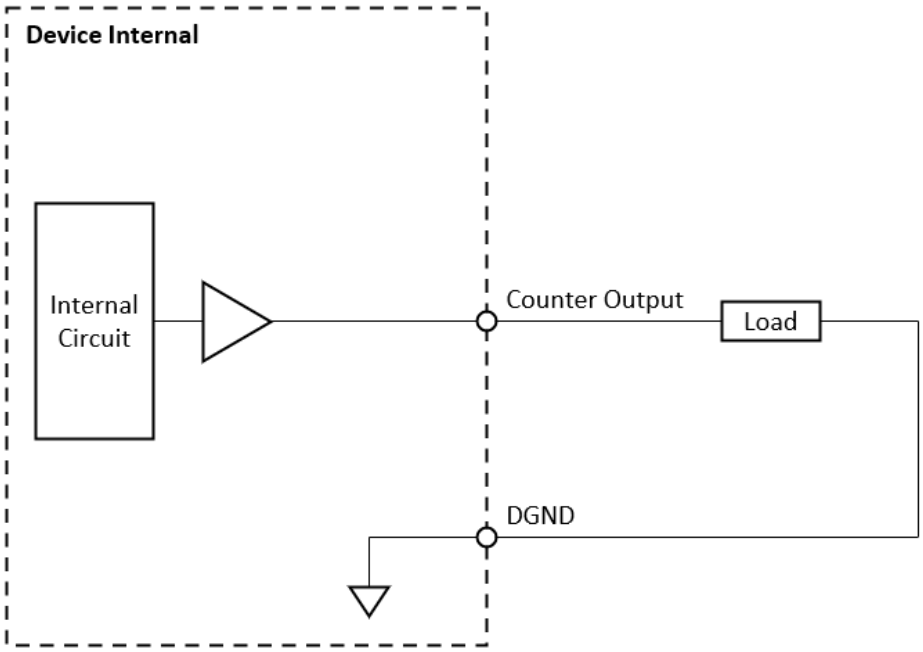

Figure 2.13 Counter output signal connection

Each counter output channel can source or sink only finite amount of current. If this limit is exceeded, the output voltage will not stay in the specified voltage logic level. Refer to the device specifications for the maximum source and skin current values.

2.3.8 Pin Assignment (CN4)

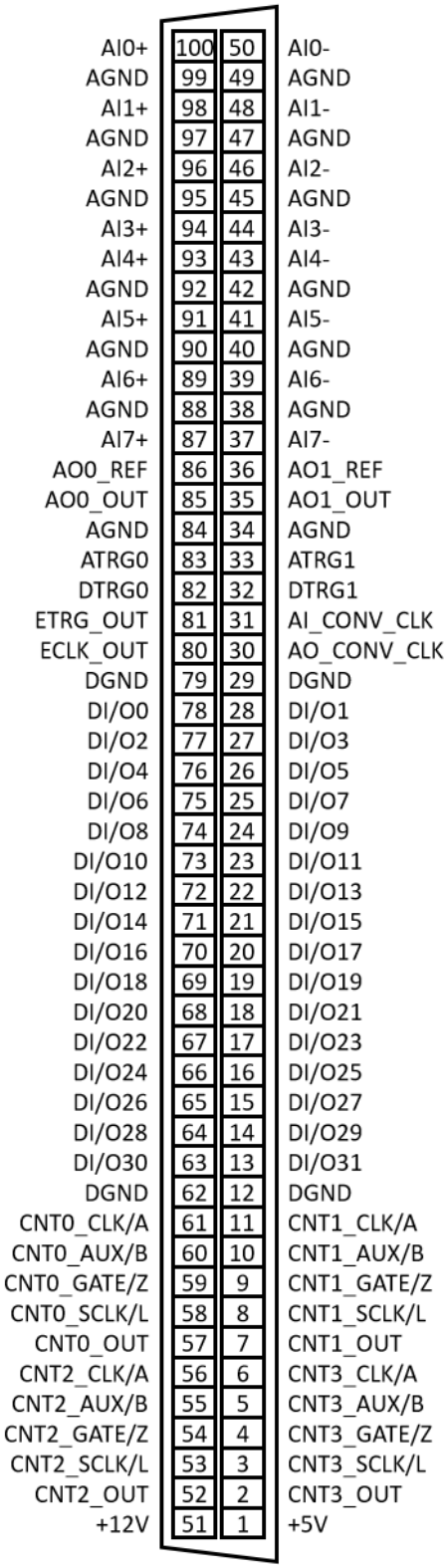

Figure 2.14 Pin assignment

Table 2.5: Pin assignment			
Pin Name	**Direction**	**Description**	**Pin Number**
AI<0..7>+	I	Analog input positive terminals.	87, 89, 91, 93, 94, 96, 98, 100
AI<0..7>-	I	Analog input negative terminals.	37, 39, 41, 43, 44, 46, 48, 50
AO<0..1>_REF	I	Analog output reference voltage input terminals.	36, 86
AO<0..1>_OUT	O	Analog output terminals.	35, 85
ATRG<0..1>	I	Analog trigger input terminals.	33, 83
AGND	-	Ground terminals for analog signals.	34, 38, 40, 42, 45, 47, 49, 84, 88, 90, 92, 95, 97, 99
DTRG<0..1>	I	Digital trigger input terminals.	32, 82
AI_CONV_CLK	I	Analog input conversion clock.	31
AO_CONV_CLK	I	Analog output conversion clock.	30
ETRG_OUT	O	External trigger output.	81
ECLK_OUT	O	External clock output.	80
DI/O<0..31>	I/O	Digital input/output terminals.	13 ~ 28, 63 ~ 78
CNT<0..3>_CLK/A	I	Counter clock/channel A input terminals.	6, 11, 56, 61
CNT<0..3>_AUX/B	I	Counter auxiliary/channel B input terminals.	5, 10, 55, 60
CNT<0..3>_GATE/Z	I	Counter gate/channel Z input terminals.	4, 9, 54, 59
CNT<0..3>_SCLK/L	I	Counter sample clock/latch input terminals.	3, 8, 53, 58
CNT<0..3>_OUT	O	Counter output terminals.	2, 7, 52, 57
DGND	-	Ground terminals for digital signals.	12, 29, 62, 79
+12V	O	+12 V supply output.	51
+5V	O	+5 V supply output.	1

2.4 Grounding Considerations

2.4.1 Signal Source Type

Signal sources can be categorized as grounded (ground-referenced) signal source or ungrounded (floating) signal source. This is shown in Figure 2. 15

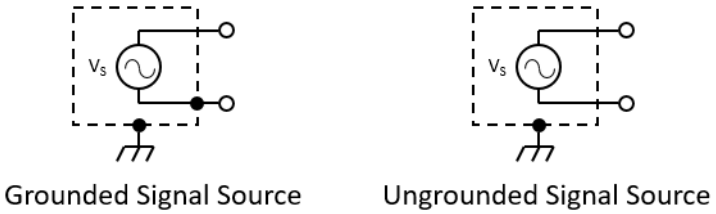

Figure 2.15 Signal source type

The voltage of a grounded signal source is referenced to a system ground, such as earth or building ground. That is, the negative terminal of the signal source is connected to the system ground. Examples of grounded signal source are devices that are plugged into the building ground through a wall outlet. The grounds of two independently grounded devices may not be at the same potential.

An ungrounded signal source is that in which the voltage is not referenced to a system ground. Examples of grounded signal source are battery powered devices, thermocouples, and isolated devices.

2.4.2 Measuring a Grounded Signal Source

For a grounded signal source, it is recommended to measure the signal using differential input configuration.

As described in the previous section, the grounds of two grounded devices may not be at the same potential. If single-ended (grounded) input configuration is used to measure a grounded signal source, a ground loop is formed and there will be current flowing between two grounds, which generates common-mode noise for the measurement. This is shown in Figure 2. 16.

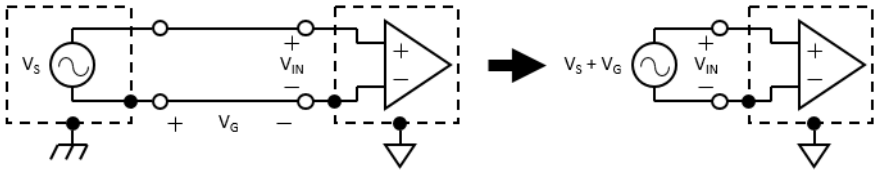

Figure 2.16 Ground loop effect

If differential (ungrounded) input configuration is used instead, the high input impedance of the negative input terminal prevents ground loop current from flowing, and therefore rejects the common-mode noise.

2.4.3 Measuring an Ungrounded (Floating) Signal Source

For an ungrounded (floating) signal source, both differential input configuration and single-ended input configuration are suitable.

When using differential input configuration, however, care must be taken to ensure the input common-mode voltage level remains in the allowable range of the measuring device. Due to the lack of DC path to the ground, the input bias current of input stage amplifier may move the common-mode voltage level of the ungrounded signal source out of the allowable range of the measuring device. When this happens, the measured result will be incorrect or saturated (positive full-scale or negative full-scale). Resistors with equal resistance value connecting between each input terminal and ground can be used to alleviate this issue as shown in Figure 2. 17. These resistors are called bias resistors.

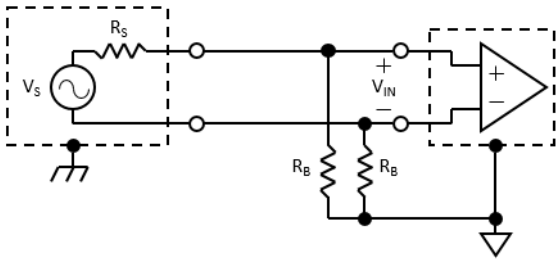

Figure 2.17 Differential input configuration with bias resistors

The resistance value should be large enough that it does not load the signal source and keep it remain floating, but small enough to make input common-mode voltage level stay in the allowable range. Typically, resistance value between 10 kΩ to 100 kΩ work well with low-impedance sources such as thermocouples and signal conditioning module outputs. When using bias resistor, the measured voltage will be attenuated by the voltage divider formed by source resistance of the signal source and bias resistors. This is shown in the following equation.

$$V_{IN} = \frac{2 \times R_B}{R_S + 2 \times R_B} V_S$$

If the source impedance of the signal source is low, only one resistor connecting between the negative input terminal and the ground is required to prevent input common-mode voltage level issues. However, this will lead to an unbalanced system if the source impedance is relatively high. A balanced system is desirable from a noise immunity point of view.

2.5 Field Wiring Considerations

When measuring a signal using the device, noise in the environment might significantly affect the performance of the measurement if some cautions are not taken. Follow these recommendations to avoid degradation of the measurement result.

- Make signal lines as short as possible.
- Use shielded, twisted-pair cables.
- Keep signal lines from noisy environments, high-voltage/current cables, or equipment which generates large electromagnetic interference, such as power lines, motors, breakers, or welding equipment.
- Route signal lines at right angles to noise generating cables.
- Use differential input configuration to reduce common-mode noise.
- For externally powered modules, use separate power sources for modules and other noise generating equipment.

Chapter 3

Functions Details

3.1 Analog Input

The device supports both instant (software-timed) and buffered (hardware-timed) analog input acquisitions.

3.1.1 Instant (Software-Timed) Analog Input Acquisition

With instant acquisition, the software controls the rate and time of acquisition, which is thus also called software-timed acquisition. Whenever the software sends a read command, the current value of analog input channel is returned as shown in Figure 3. 1.

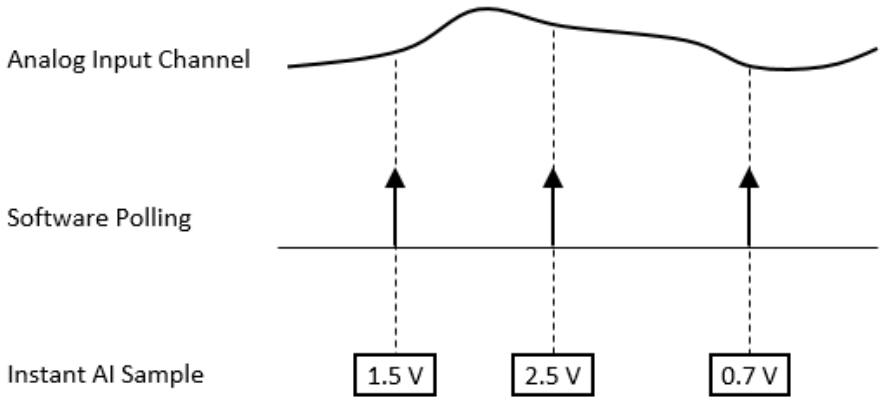

Figure 3.1 Instant (software-timed) analog input acquisition

The advantage of instant acquisition is low latency. It is typically used for reading a single sample of analog input.

3.1.2 Buffered (Hardware-Timed) Analog Input Acquisition

With buffered acquisition, a hardware signal called sample clock controls the rate and time of acquisition. The ADCs of all buffered acquisition enabled channels simultaneously begin to convert the analog input voltage at each rising edge of the sample clock. Figure 3. 2 shows an example of analog input buffered acquisition which AI0, AI1, and AI2 are enabled.

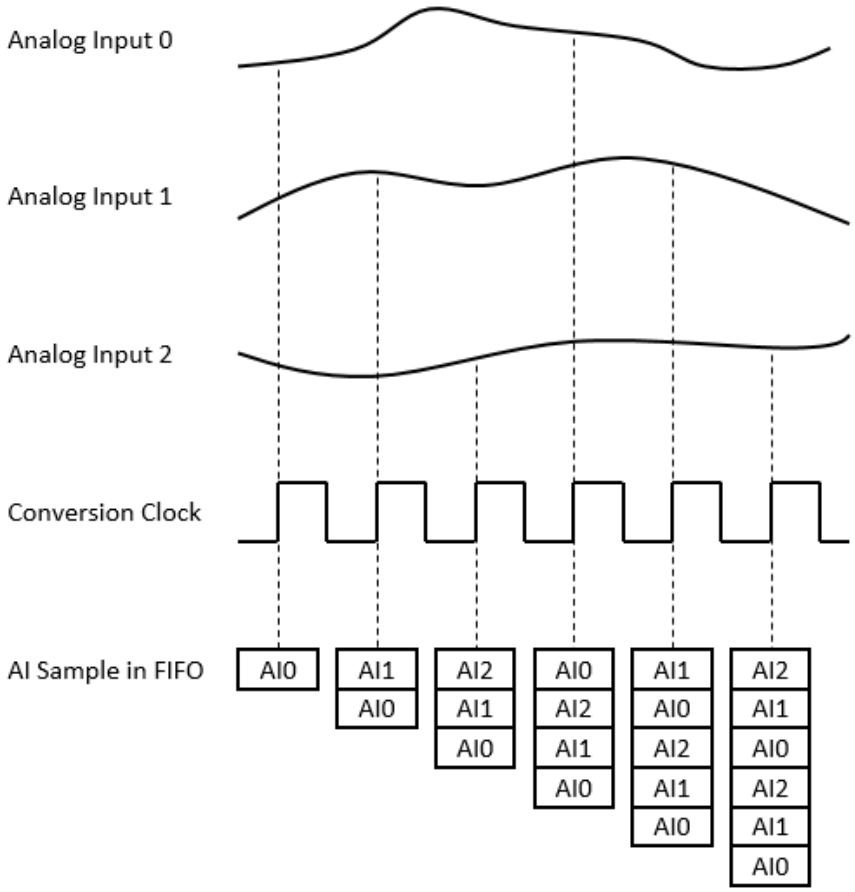

Figure 3.2 Buffered (hardware-timed) analog input acquisition

The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

The acquired samples are first accumulated in the onboard first-in-first-out (FIFO) memory, and then moved to the buffer in the PC by a direct memory access (DMA) engine. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the application memory. Because the data is moved in large blocks instead of one point at a time, buffered acquisition typically allow much higher transfer rates. Buffered acquisition is also called hardware-timed acquisition.

The advantages of buffered acquisition over instant acquisition include:

- The sample rate can be much higher.
- The time of sample is deterministic.
- Hardware triggers can be used.

3.2 Analog Output

The device supports both static (software-timed) analog output update and buffered (hardware-timed) analog output generation.

3.2.1 Static (Software-Timed) Analog Output Update

With static update, the software controls the rate and time of date, which is thus also called software-timed update. Whenever the software sends a write command, the value of analog output channel is updated as shown in Figure 3. 3.

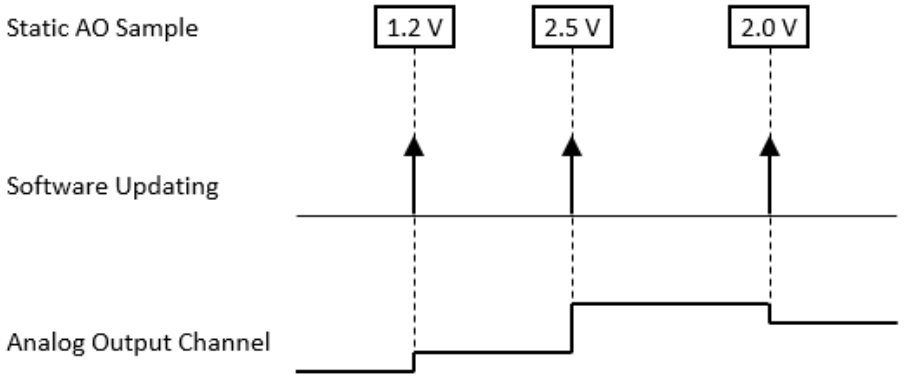

Figure 3.3 Static (software-timed) analog output update

The advantage of state update is low latency. It is typically used for writing a single value of analog output. When updating multiple analog output channels, they can be updated asynchronously or synchronously. For asynchronous update, each the analog output channel is updated immediately when the value to be updated is written to the device as shown in Figure 3. 4. For synchronous update, however, the values to be updated are first stored in the device, and all analog output channels are updated synchronously when the synchronous write command is sent. This is shown in Figure 3. 5.

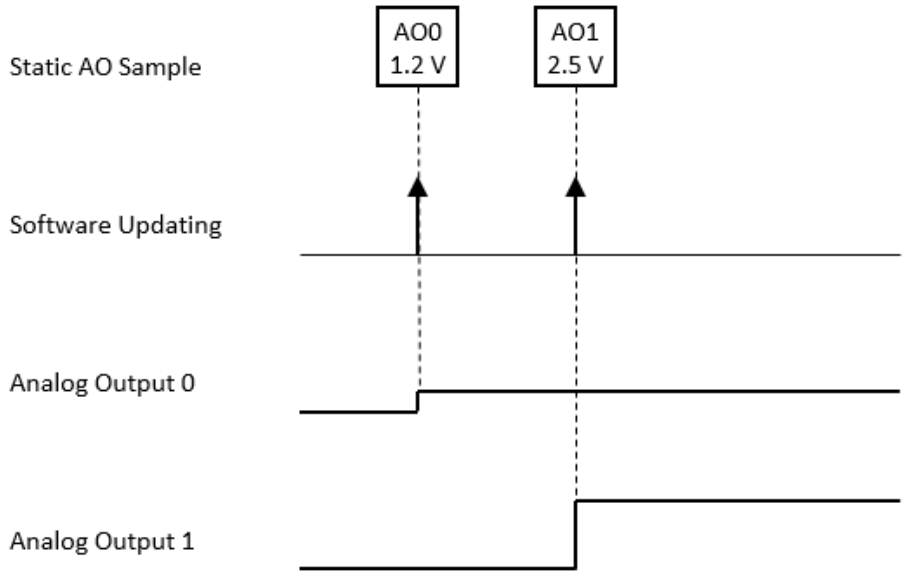

Figure 3.4 Analog output asynchronous update

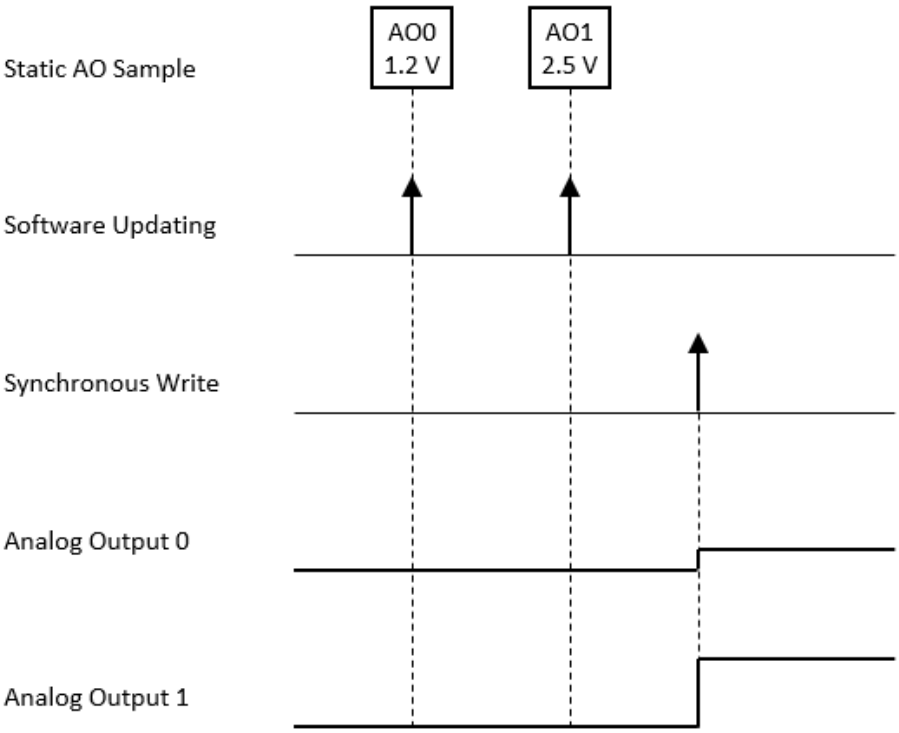

Figure 3.5 Analog output synchronous update

3.2.2 Buffered (Hardware-Timed) Analog Output Generation

With buffered generation, a hardware signal called sample clock controls the rate and time of generation as shown in Figure 3. 6. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

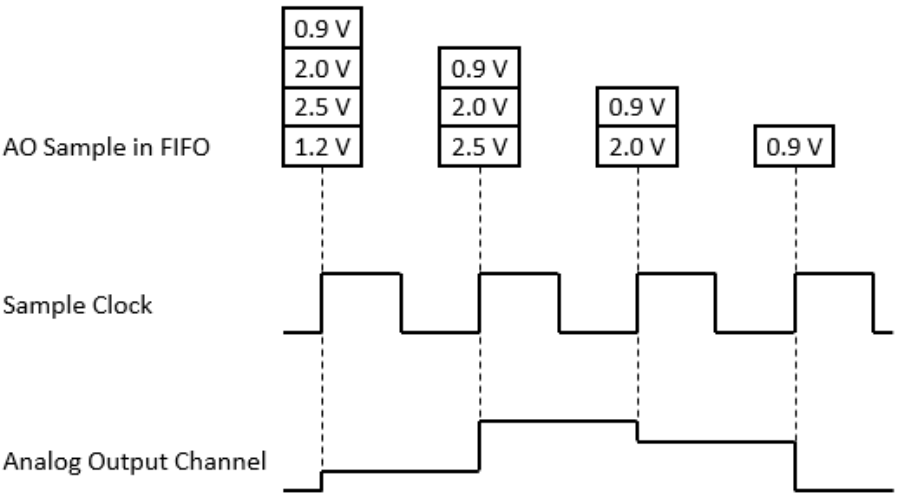

Figure 3.6 Buffered (hardware-timed) analog output generation

The samples to be generated are provided by the application. They are first stored in the buffer of the PC, moved to the onboard first-in-first-out (FIFO) memory of the device by a direct memory access (DMA) engine, and converted by the DAC one sample at a time. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the onboard FIFO. Because the data is moved in large

blocks instead of one point at a time, buffered generation typically allow much higher transfer rates. Buffered generation is also called hardware-timed generation.

The advantages of buffered generation over static update include:

- The generation (update) rate can be much higher.
- The time of sample is deterministic.
- Hardware triggers can be used.

3.3 Digital Input

The device supports both instant (software-timed) and buffered (hardware-timed) digital input acquisitions.

3.3.1 Instant (Software-Timed) Digital Input Acquisition

With instant acquisition, the software controls the rate and time of acquisition, which is thus also called software-timed acquisition. Whenever the software sends a read command, the current status of digital input ports is returned as shown in Figure 3. 7.

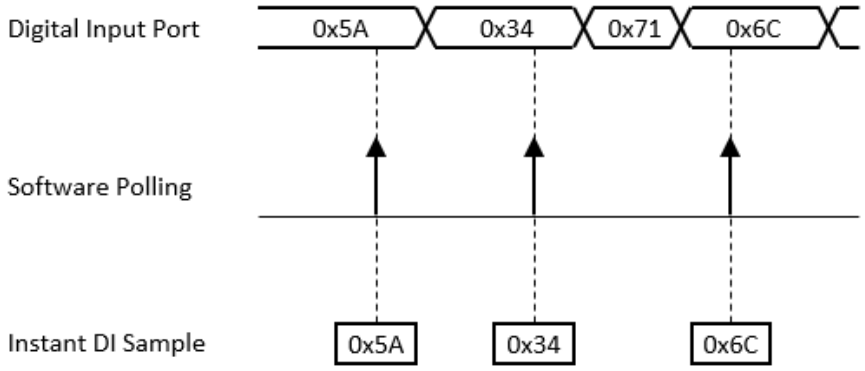

Figure 3.7 Instant (software-timed) digital input acquisition

The advantage of instant acquisition is low latency. It is typically used for reading a single sample of digital input.

3.3.2 Buffered (Hardware-Timed) Digital Input Acquisition

With buffered acquisition, a hardware signal called sample clock controls the rate and time of acquisition as shown in Figure 3. 8. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

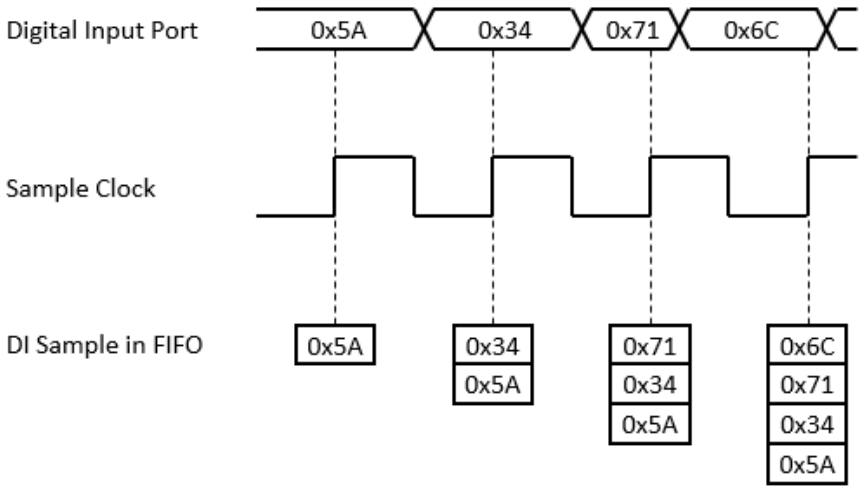

Figure 3.8 Buffered (hardware-timed) digital input acquisition

The acquired samples are first accumulated in the onboard first-in-first-out (FIFO) memory of the device, and then moved to the buffer in the PC by a direct memory access (DMA) engine. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the application memory. Because the data is moved in large blocks instead of one point at a time, buffered acquisition typically allow much higher transfer rates. Buffered acquisition is also called hardware-timed acquisition.

The advantages of buffered acquisition over instant acquisition include:

- The sample rate can be much higher.
- The time of sample is deterministic.
- Hardware triggers can be used.

3.4 Digital Output

The device supports both static (software-timed) digital output update and buffered (hardware-timed) digital output generation.

3.4.1 Static (Software-Timed) Digital Output Update

With static update, the software controls the rate and time of date, which is thus also called software-timed update. Whenever the software sends a write command, the state of digital output ports is updated as shown in Figure 3. 9.

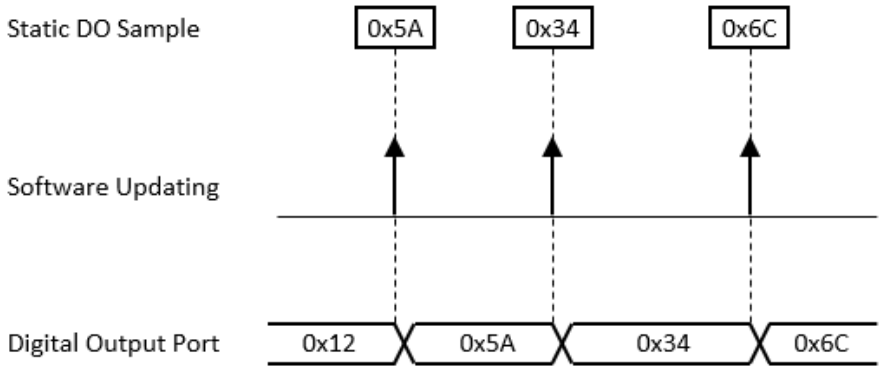

Figure 3.9 Static (software-timed) digital output update

The advantage of state update is low latency. It is typically used for writing a single value of digital output.

3.4.2 Buffered (Hardware-Timed) Digital Output Generation

With buffered generation, a hardware signal called sample clock controls the rate and time of generation as shown in Figure 3. 10 The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

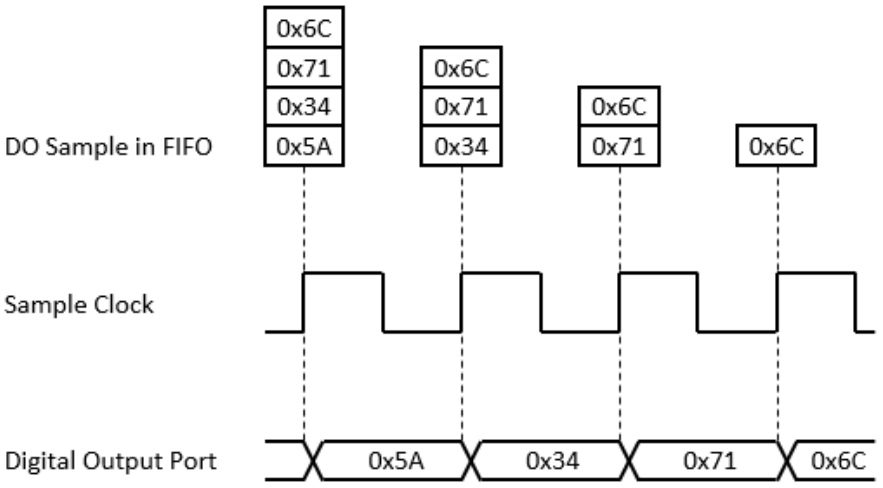

Figure 3.10 Buffered (hardware-timed) digital output generation

The samples to be generated are provided by the application. They are first stored in the buffer of the PC, moved to the onboard first-in-first-out (FIFO) memory of the

device by a direct memory access (DMA) engine, and placed on the digital output channels one sample at a time. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the onboard FIFO. Because the data is moved in large blocks instead of one point at a time, buffered generation typically allow much higher transfer rates. Buffered generation is also called hardware-timed generation.

The advantages of buffered generation over static update include:

- The generation (update) rate can be much higher.
- The time of sample is deterministic.
- Hardware triggers can be used.

3.5 Counter

3.5.1 Event Counting

In event counting mode, the counter counts the number of edges the counter clock signal generates. It can be configured as rising edge active or falling edge active, as shown in Figure 3. 11 and Figure 3. 12, respectively.

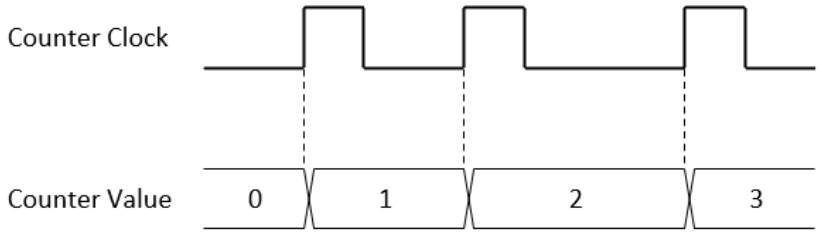

Figure 3.11 Rising edge event counting

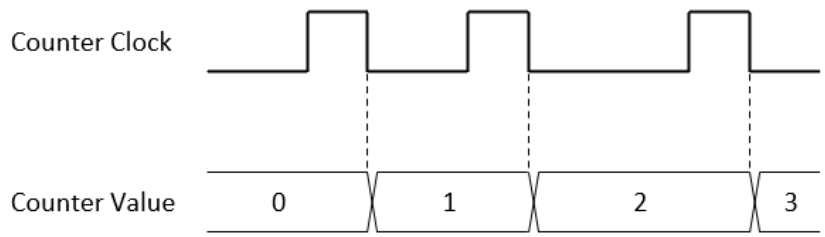

Figure 3.12 Falling edge event counting

Counting may be temporarily paused by the counter gate signal as shown in Figure 3. 13.

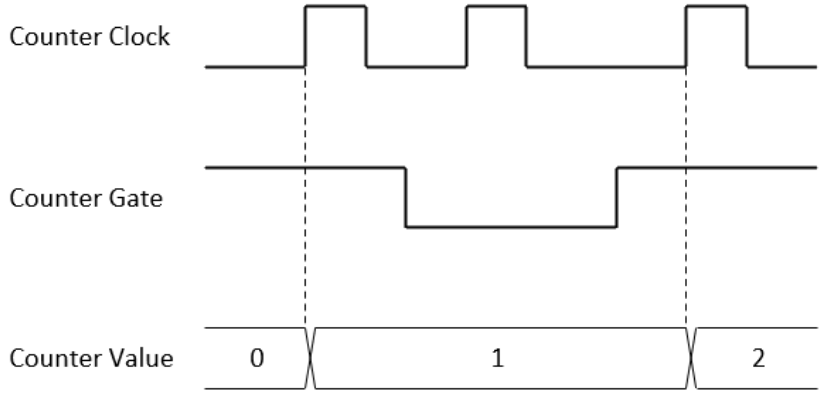

Figure 3.13 Event counting with pause gate

Instant (Software-Timed) Event Counting

With instant event counting, the software controls the rate and time of reading counter value, which is thus also called software-timed event counting. Whenever the software sends a read command, the current value of the counter is returned as shown in Figure 3. 14.

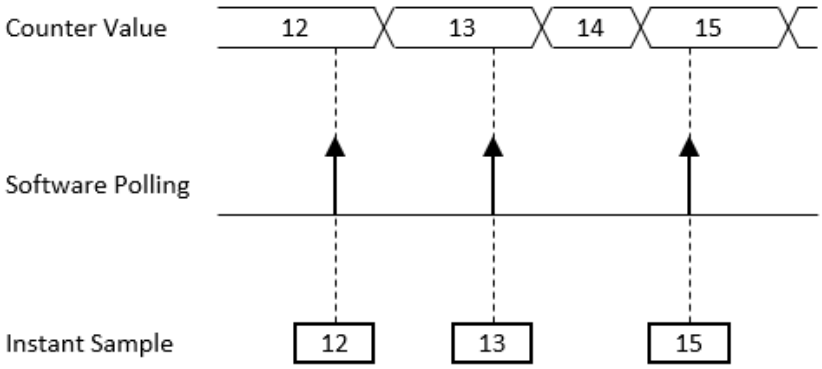

Figure 3.14 Instant (software-timed) event counting

The advantage of instant event counting is low latency. It is typically used for reading a single sample of counter value.

Buffered (Hardware-Timed) Event Counting

With buffered event counting, a hardware signal called sample clock controls the rate and time of reading counter value as shown in Figure 3. 15.The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

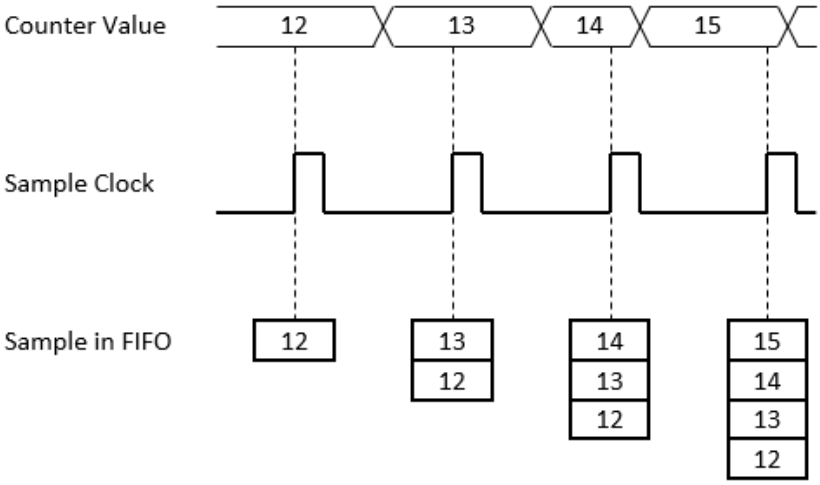

Figure 3.15 Buffered (hardware-timed) event counting

3.5.2 Frequency Measurement

In frequency measurement mode, the frequency of the counter clock signal is measured by one of the two measuring methods: Period inversion or counting number of pulses in fixed duration.

Period Inversion

In this method, the period of the counter clock signal is first measured by an internal high frequency clock. The frequency of the signal is then calculated by inverting the period value. This is shown in Figure 3. 16 and by the following equation.

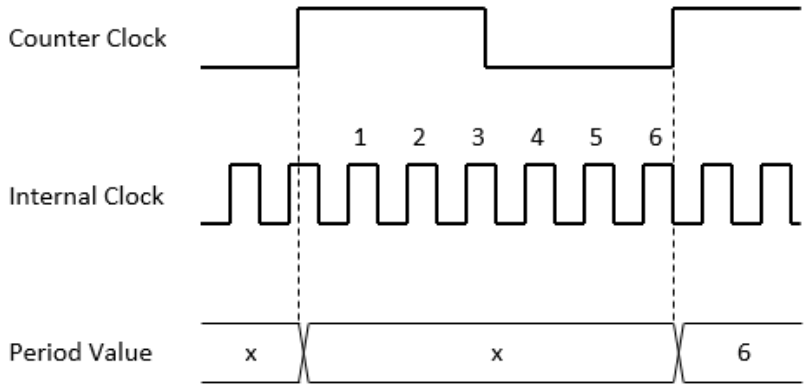

Figure 3.16 Frequency measurement by period inversion

$$Frequency = \frac{1}{Period} = \frac{1}{InternalClockCount \times InternalClockPeriod}$$

This method is suitable if the counter clock signal frequency is much smaller (< 0.1%) than the internal clock frequency. Measuring accuracy degrades as the counter clock signal frequency increases.

Counting Number of Pulses in Fixed Duration

In this method, the pulse number of the counter clock signal is measured in a fixed time duration. The frequency of the signal is then calculated by dividing this number by the time duration. This is shown in Figure 3. 17 and by the following equation.

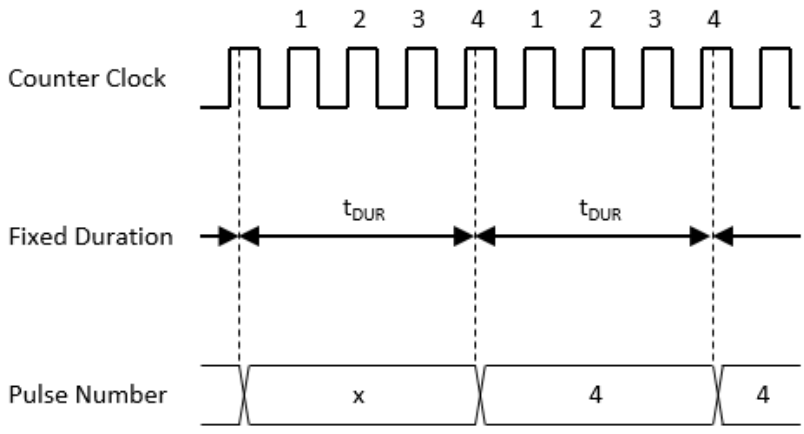

Figure 3.17 Frequency measurement by counting number of pulses in fixed duration

$$Frequency = \frac{PulseNumber}{t_{DUR}}$$

For counter clock signal frequency higher than that specified in the previous section, this method gives a more accurate result.

Instant (Software-Timed) Frequency Measurement

With instant frequency measurement, the software controls the rate and time of reading frequency value, which is thus also called software-timed frequency measurement. Whenever the software sends a read command, the current value of the frequency is returned as shown in Figure 3. 18.

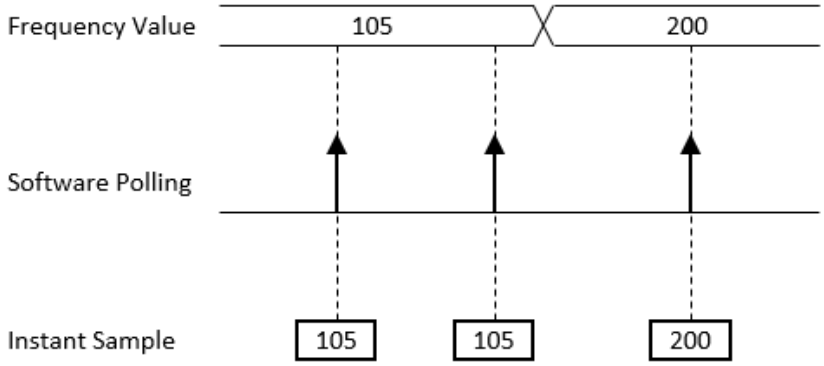

Figure 3.18 Instant (software-timed) frequency measurement

The advantage of instant frequency measurement is low latency. It is typically used for reading a single sample of frequency value.

Buffered (Hardware-Timed) Frequency Measurement

With buffered frequency measurement, a hardware signal called sample clock controls the rate and time of reading frequency value as shown in Figure 3. 19. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

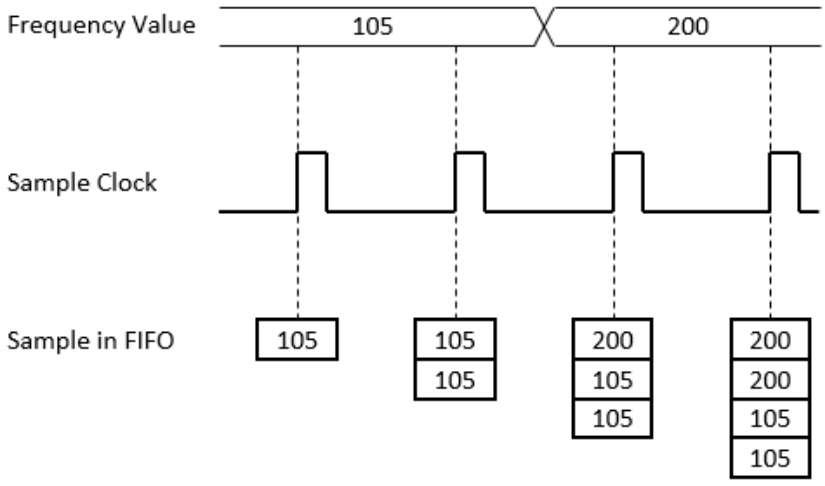

Figure 3.19 Buffered (hardware-timed) frequency measurement

The read samples are first accumulated in the onboard first-in-first-out (FIFO) memory, and then moved to the buffer in the PC by a direct memory access (DMA) engine. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the application memory. Because the data is moved in large blocks instead of one point at a time, buffered frequency measurement typically allow much higher transfer rates. Buffered frequency measurement is also called hardware-timed frequency measurement.

The advantages of buffered frequency measurement over instant frequency measurement include:

- The sample rate can be much higher.
- The time of samples is deterministic.

3.5.3 Pulse Width Measurement

In pulse width measurement mode, both the high period and the low period of the counter clock signal are measured. The measured values are updated when a pulse is completed. This is shown in Figure 3. 20.

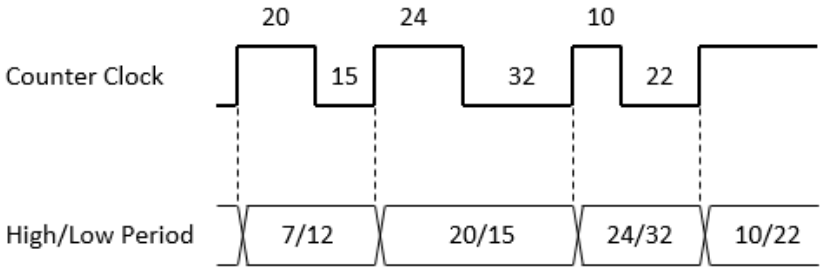

Figure 3.20 Pulse width measurement

Instant (Software-Timed) Pulse Width Measurement

With instant pulse width measurement, the software controls the rate and time of reading counter value, which is thus also called software-timed pulse width measurement. Whenever the software sends a read command, the current value of the counter is returned as shown in Figure 3. 21.

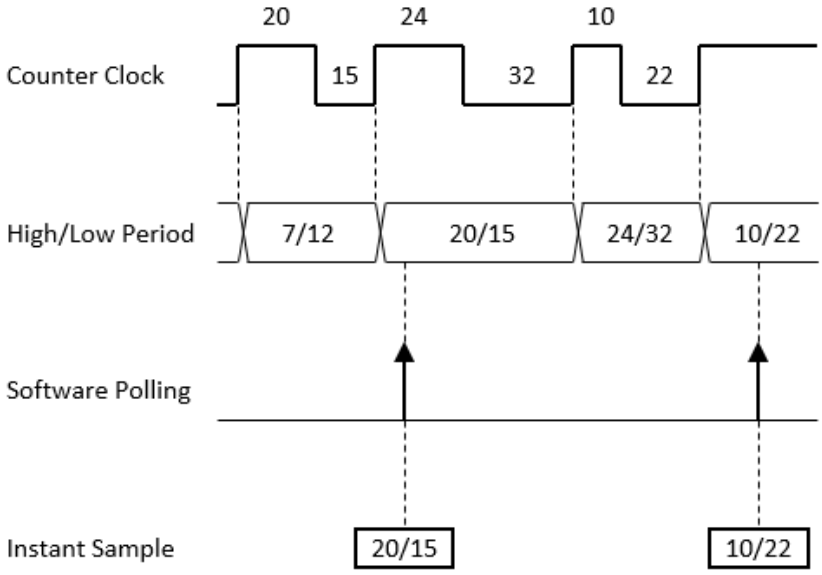

Figure 3.21 Instant (software-timed) pulse width measurement

The advantage of instant pulse width measurement is low latency. It is typically used for reading a single sample of counter value.

Sample Clock Buffered (Hardware-Timed) Pulse Width Measurement

With sample clock buffered pulse width measurement, a hardware signal called sample clock controls the rate and time of reading counter value as shown in Figure 3. 22. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

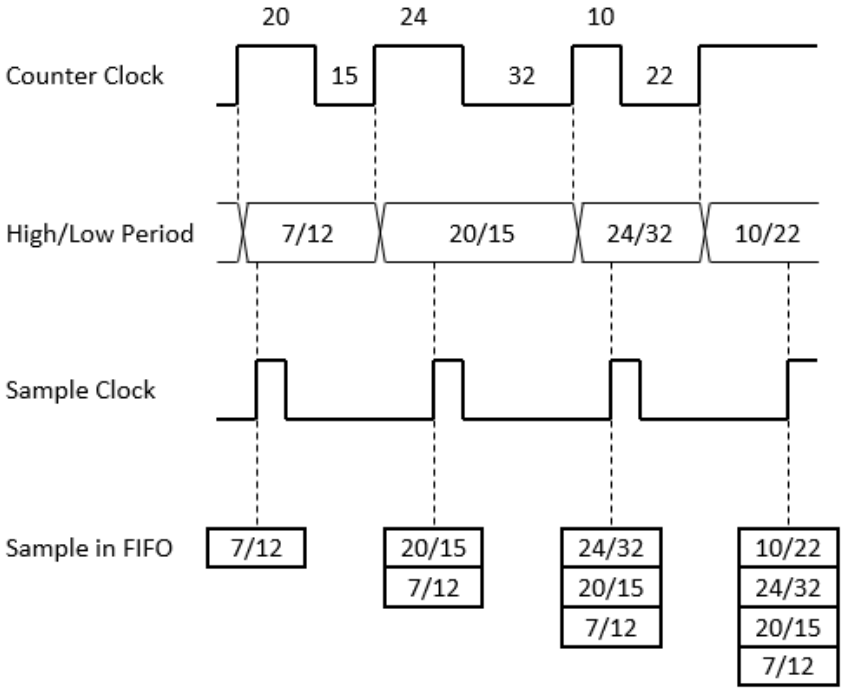

Figure 3.22 Sample clock buffered (hardware-timed) pulse width measurement

The read samples are first accumulated in the onboard first-in-first-out (FIFO) memory, and then moved to the buffer in the PC by a direct memory access (DMA) engine. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the application memory. Because the data is moved in large blocks instead of one point at a time, buffered pulse width measurement typically allow much higher transfer rates. Buffered pulse width measurement is also called hardware-timed pulse width measurement.

The advantages of buffered pulse width measurement over instant pulse width measurement include:

- The sample rate can be much higher.
- The time of sample is deterministic.

Implicit Buffered Pulse Width Measurement

With implicit buffered pulse width measurement, width of every completed pulse will be written to the onboard FIFO memory automatically as shown in Figure 3. 23

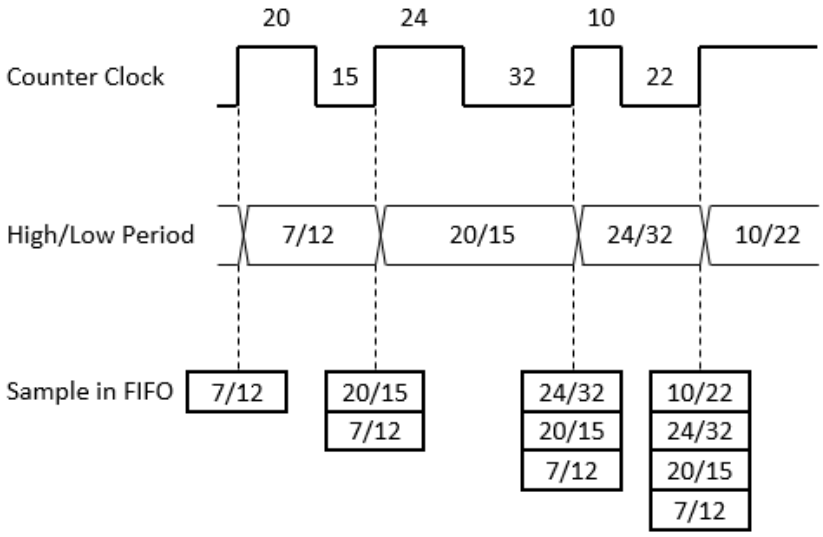

Figure 3.23 Implicit buffered (hardware-timed) pulse width measurement

3.5.4 Position Measurement

In position measurement mode, the condition for increasing or decreasing of the counter value depends on the input mode.

Quadrature x1 Mode

In quadrature x1 mode, if counter A signal leads counter B signal by 90 degrees, the counter value is increased by 1 for each pulse period. If counter B signal leads counter A signal by 90 degrees, the counter value is decrease by 1 for each pulse period. They are shown in Figure 3. 24 and Figure 3. 25, respectively.

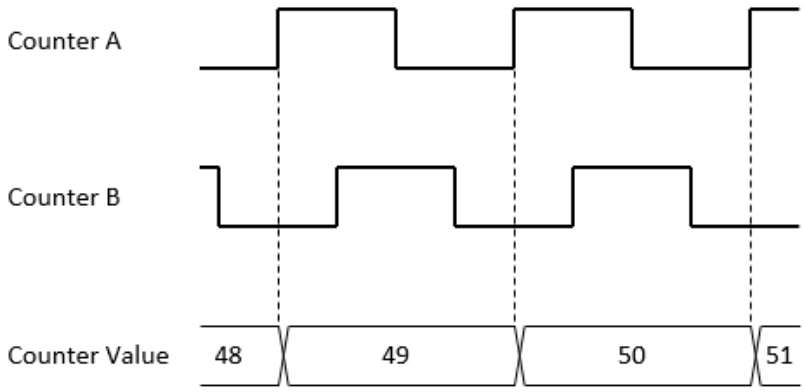

Figure 3.24 Quadrature x1 mode, counter A leads counter B

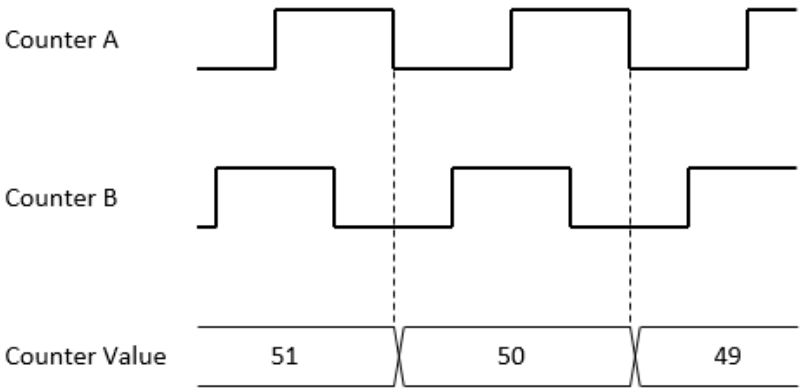

Figure 3.25 Quadrature x1 mode, counter B leads counter A

Quadrature x2 Mode

In quadrature x2 mode, if counter A signal leads counter B signal by 90 degrees, the counter value is increased by 2 for each pulse period. If counter B signal leads counter A signal by 90 degrees, the counter value is decrease by 2 for each pulse period. They are shown in Figure 3. 26 and Figure 3. 27, respectively.

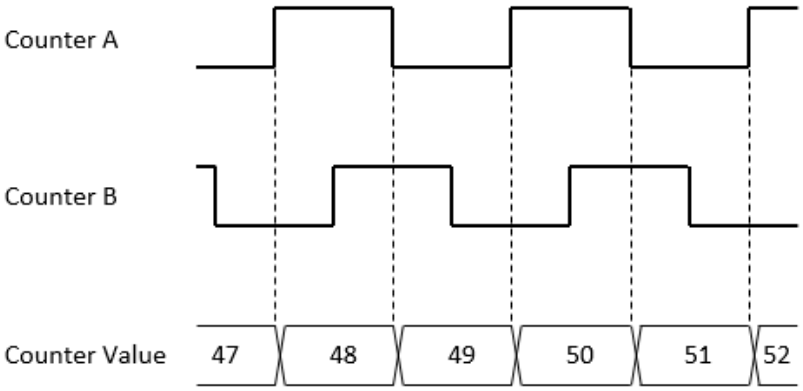

Figure 3.26 Quadrature x2 mode, counter A leads counter B

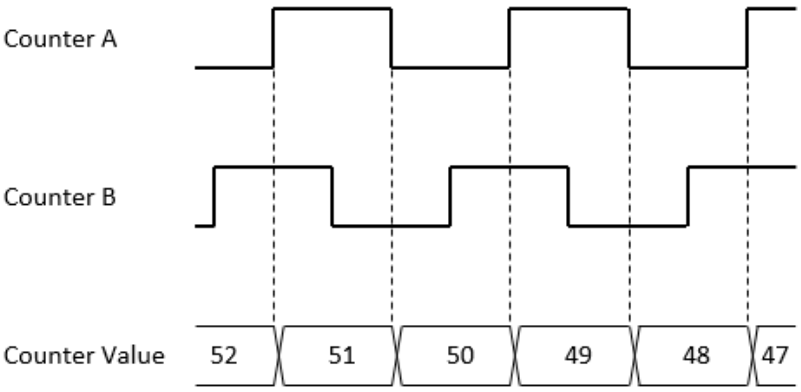

Figure 3.27 Quadrature x2 mode, counter B leads counter A

Quadrature x4 Mode

In quadrature x4 mode, if counter A signal leads counter B signal by 90 degrees, the counter value is increased by 4 for each pulse period. If counter B signal leads counter A signal by 90 degrees, the counter value is decrease by 4 for each pulse period. They are shown in Figure 3. 28 and Figure 3. 29, respectively.

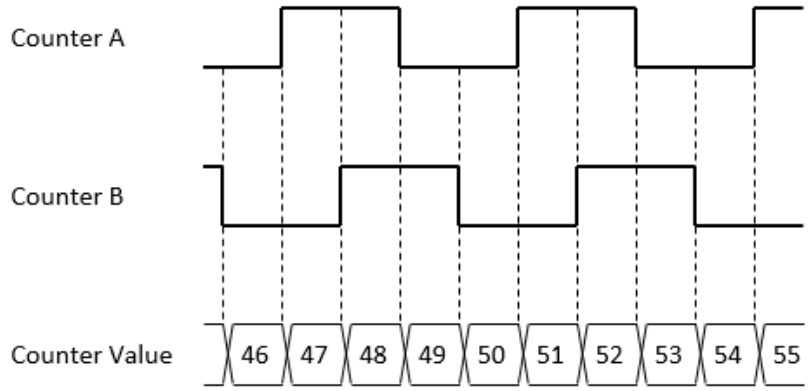

Figure 3.28 Quadrature x4 mode, counter A leads counter B

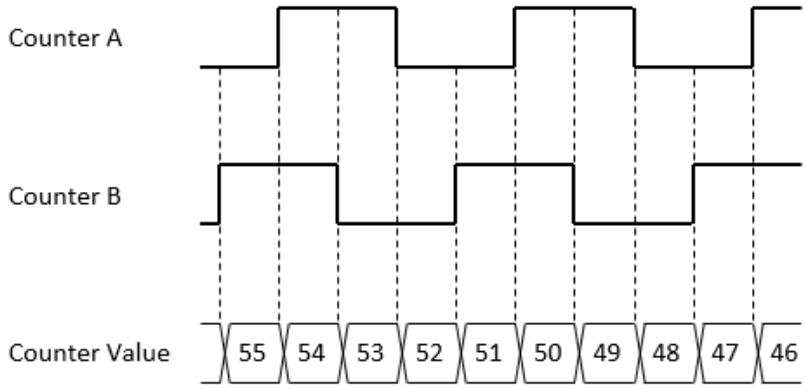

Figure 3.29 Quadrature x4 mode, counter B leads counter A

Two Pulse (Clockwise/Counter-Clockwise) Mode

In two pulse (or clockwise/counter-clockwise) mode, the counter value is increased by 1 for each pulse of counter A signal, and is decreased by 1 for each pulse of counter B signal. This is shown in Figure 3. 30.

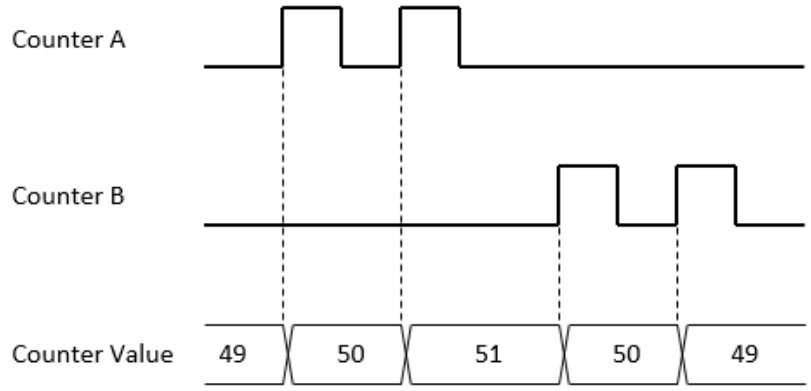

Figure 3.30 Two pulse (clockwise/counter-clockwise) mode

Signed Pulse (Pulse/Direction) Mode

In signed pulse (or pulse/direction) mode, the counting direction is controlled by counter B signal. The counter value is increased by 1 for each pulse of counter A signal when counter B signal is low. It is decreased by 1 for each pulse of counter A signal when counter B signal is high. This is shown in Figure 3. 31.

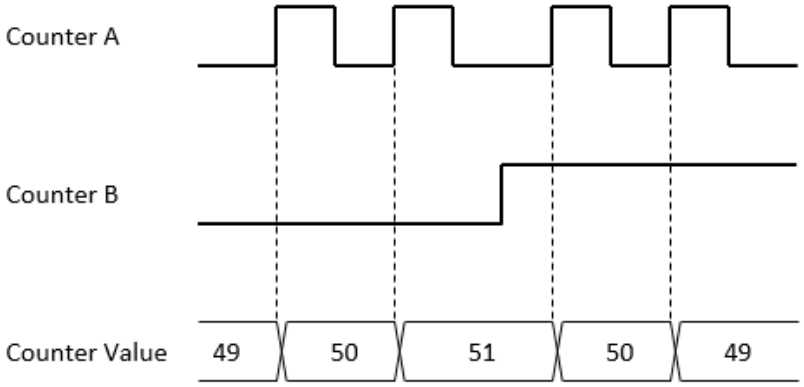

Figure 3.31 Signed pulse (pulse/direction) mode.

Position Reset

In position measurement, the counter value can be reset to a specified value either by the software or by the counter Z signal. Figure 3. 32 shows an example of reset by counter Z signal.

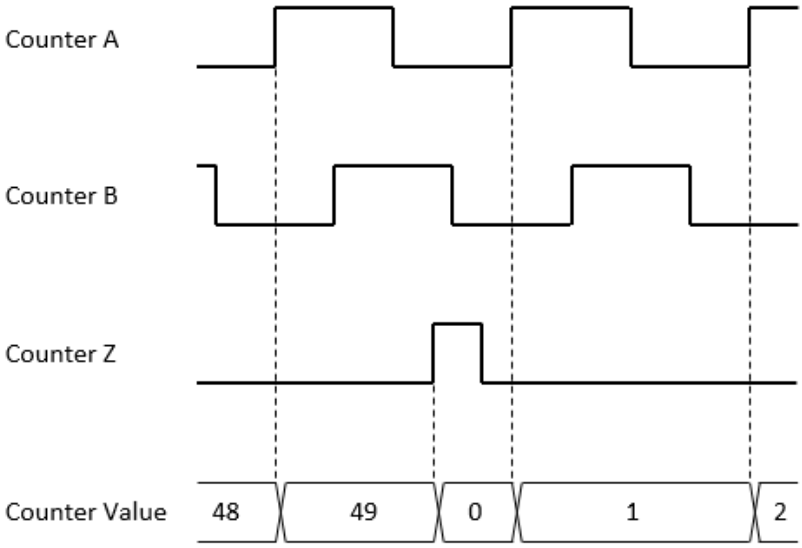

Figure 3.32 Position reset to 0 by counter Z signal

Instant (Software-Timed) Position Measurement

With instant position measurement, the software controls the rate and time of reading counter value, which is thus also called software-timed position measurement. Whenever the software sends a read command, the current value of the counter is returned as shown in Figure 3. 33.

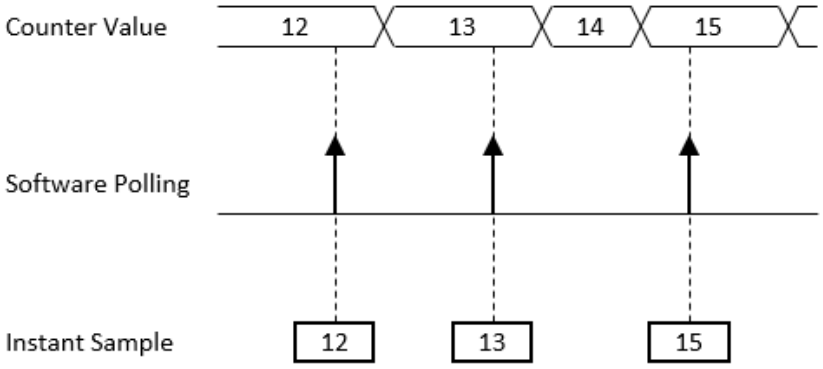

Figure 3.33 Instant (software-timed) position measurement

The advantage of instant position measurement is low latency. It is typically used for reading a single sample of counter value.

Buffered (Hardware-Timed) Position Measurement

With buffered position measurement, a hardware signal called sample clock controls the rate and time of reading counter value as shown in Figure 3. 34. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

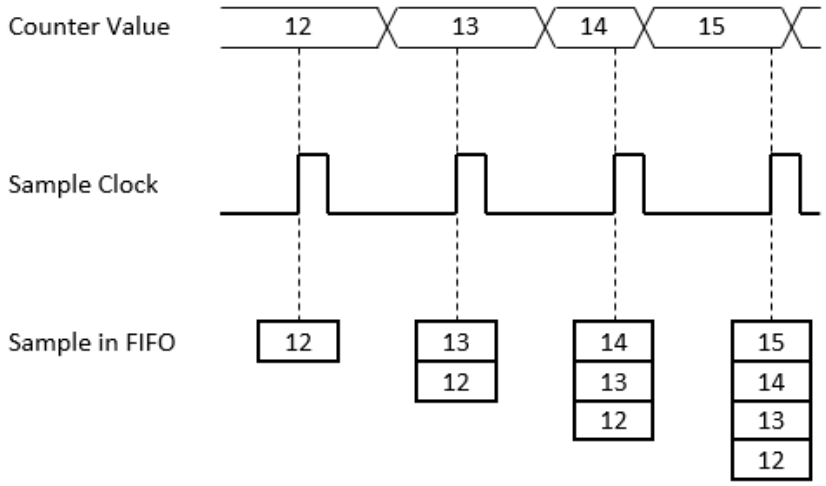

Figure 3.34 Buffered (hardware-timed) position measurement

The read samples are first accumulated in the onboard first-in-first-out (FIFO) memory, and then moved to the buffer in the PC by a direct memory access (DMA) engine. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the application memory. Because the data is moved in large blocks instead of one point at a time, buffered position measurement typically allow much higher transfer rates. Buffered position measurement is also called hardware-timed position measurement.

The advantages of buffered position measurement over instant position measurement include:

- The sample rate can be much higher.
- The time of sample is deterministic.

3.5.5 Position Comparison

An output pulse can be generated at the counter output terminal when the position value matches the specified compare value. This is shown in Figure 3. 35. The width of the output pulse is configurable.

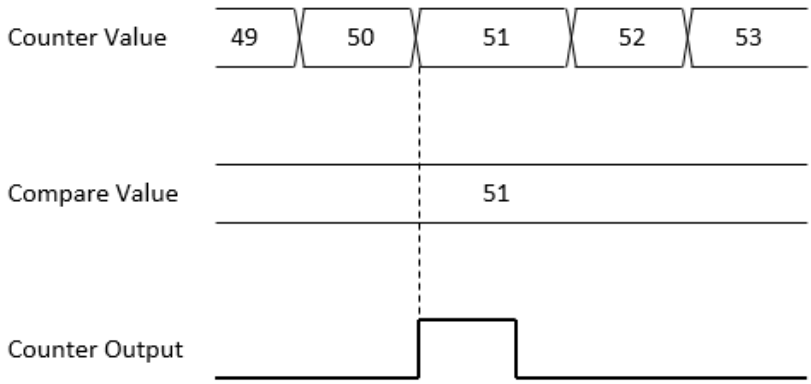

Figure 3.35 Position Comparison

Instant Position Comparison

With instant position comparison, software controls the update of the compare value. A software interrupt will be generated when a compare match occurs, and the software can update the compare value accordingly. This is shown in Figure 3. 36.

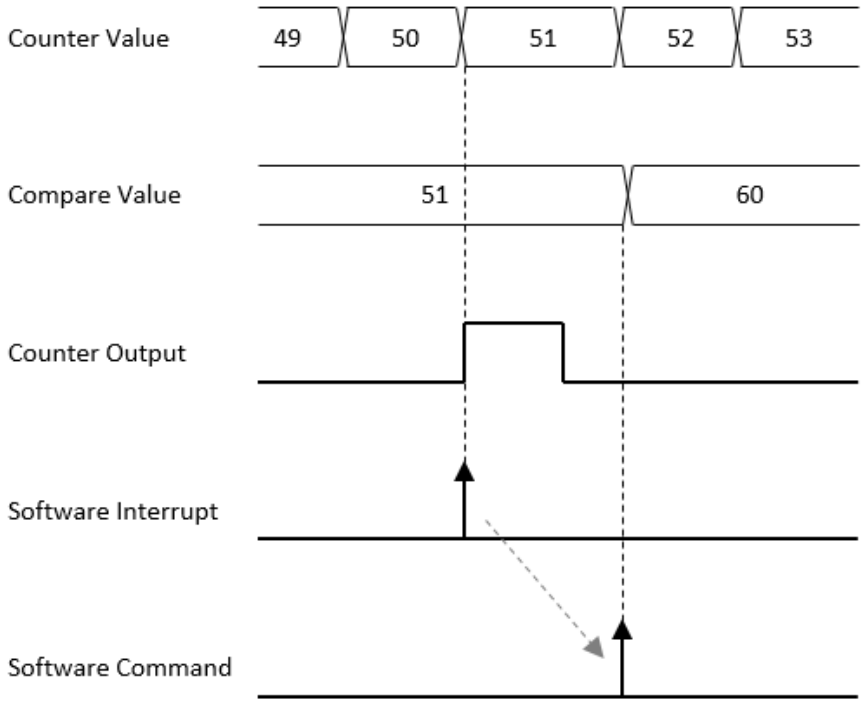

Figure 3.36 Instant position comparison

The advantage of instant position comparison is that the next compare value can be decided on the fly.

Buffered Position Comparison

With buffered position comparison, the compare values are pre-programmed by the software and then stored in the on-board FIFO. When a value match occurs, the next compare value will be automatically loaded by the hardware as shown in Figure 3. 37.

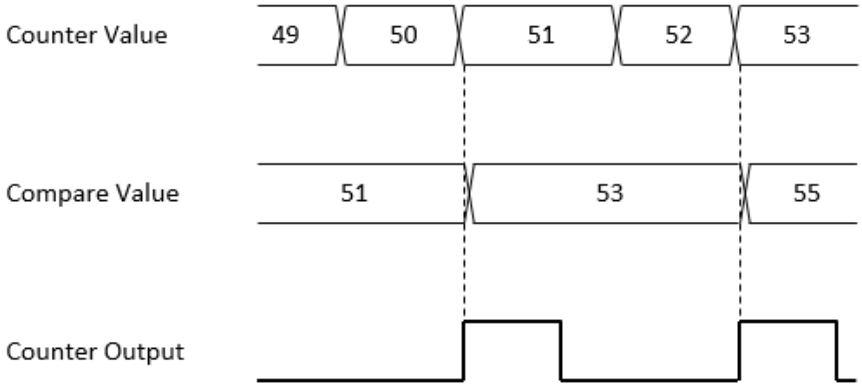

Figure 3.37 Buffered position comparison

Due to the low latency of hardware operation, buffered position comparison supports much higher update rate of the compare value over instant position comparison.

Offset Position Comparison

With offset position comparison, the compare value is generated by the counter sample clock. When the counter sample clock rises, the counter value at that time is latched, offset by a specified value, and stored as the next compare value. An example is shown in Figure 3. 38.

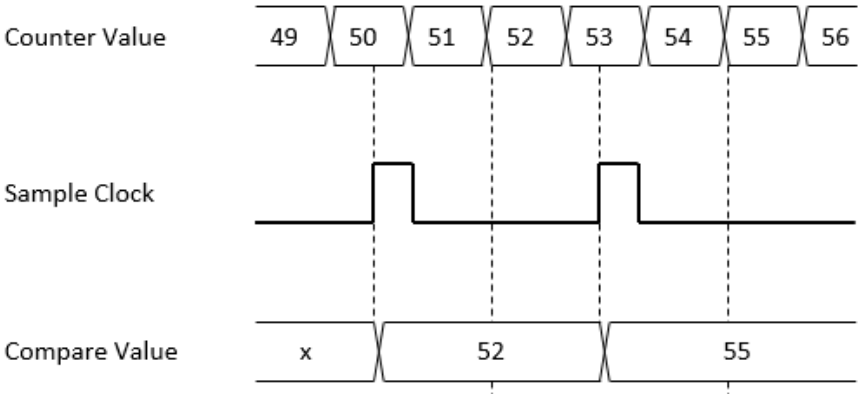

Figure 3.38 Offset position comparison with offset value of "+2"

3.5.6 One-Shot (Delayed Pulse Generation)

In one-shot mode, when an active edge of gate signal is detected, a pulse will be generated after the specified number source clock counts. The pulse width is one period of source clock. Figure 3. 39 shows an example of high-pulse, 5-clock delay one-shot output.

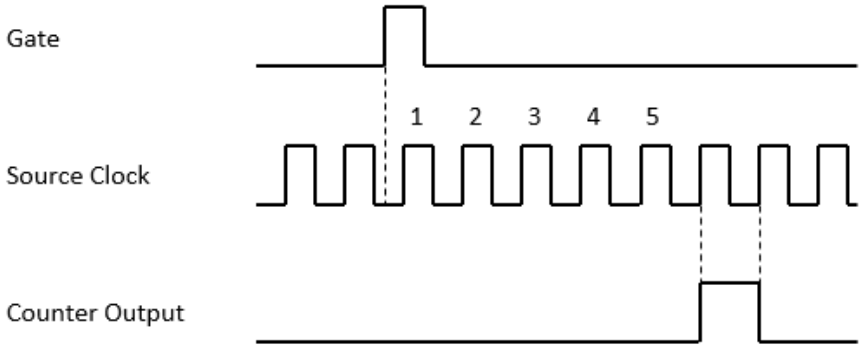

Figure 3.39 One-shot operation

3.5.7 Timer/Pulse

In timer/pulse mode, continuous pulses with specified frequency are generated at counter output terminal, and an interrupt is also generated with each pulse as shown in Figure 3. 40.

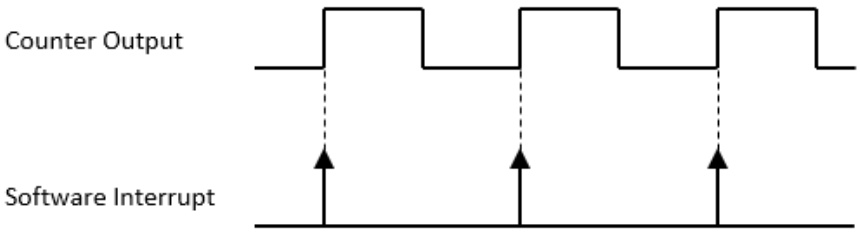

Figure 3.40 Pulse output and timer interrupt

The output can be gated. If counter gate is in active level, pulses are output normally. On the other hand, if counter gate is in inactive level, output is disabled. Figure 3. 41 shows an example of active high gate.

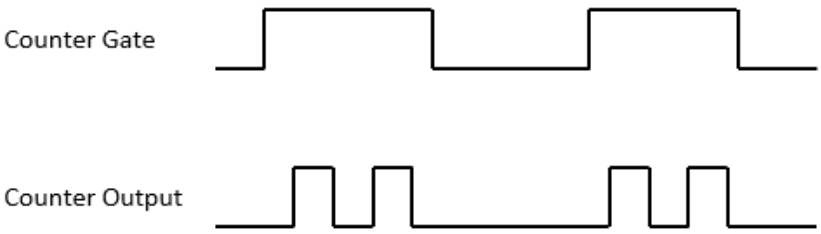

Figure 3.41 Gated timer/pulse output

Static (Software-Timed) Timer/Pulse

With static timer/pulse, the software controls the time of updating output pulse frequency, which is thus also called software-timed timer/pulse. Whenever the software sends an update command, the frequency of output pulse is updated to the specified value after current pulse is completed as shown in Figure 3. 42.

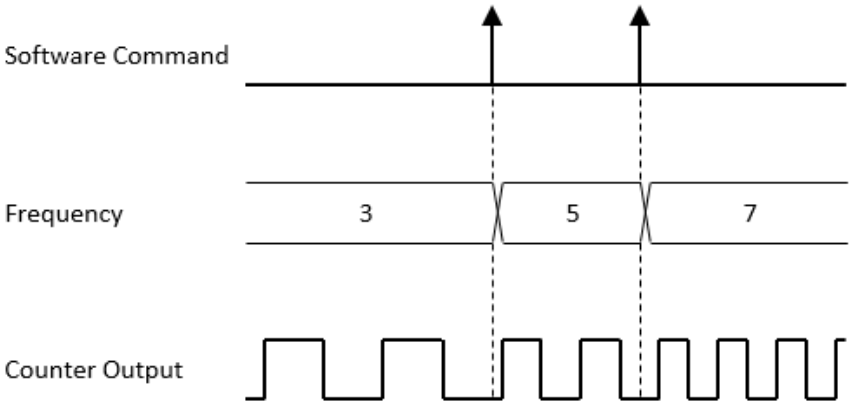

Figure 3.42 Static (software-timed) timer/pulse

Buffered (Hardware-Timed) Timer/Pulse

With buffered timer/pulse, a hardware signal called sample clock controls the time of updating output pulse frequency as shown in Figure 3. 43. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

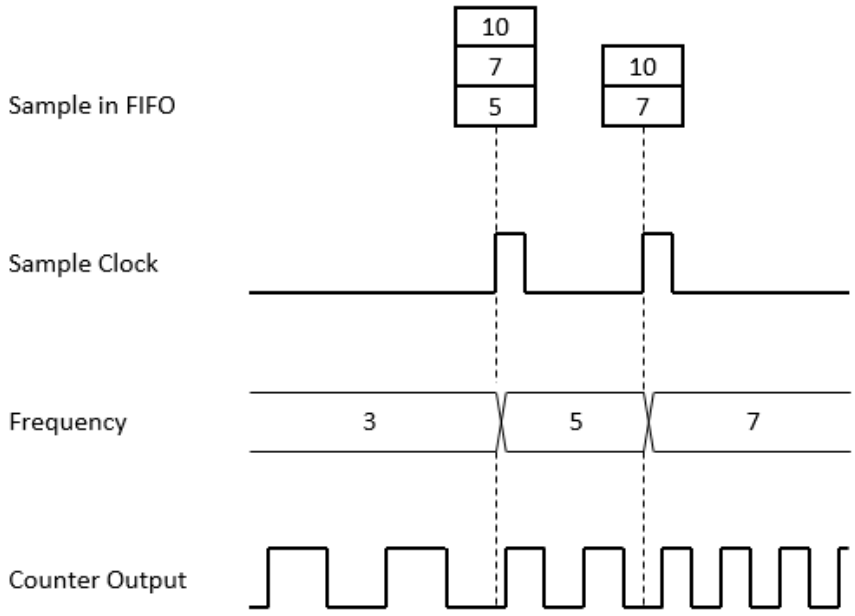

Figure 3.43 Buffered (hardware-timed) timer/pulse

The samples to be updated are first written to the onboard first-in-first-out (FIFO) memory by software. Each time a rising edge of sample clock is detected, the first sample in the FIFO is used to update the output pulse frequency, and then the sample is discarded. Buffered timer/pulse is also called hardware-timed timer/pulse.

The advantages of buffered timer/pulse over static timer/pulse include:

- The time of sample is deterministic.
- The time of sample can be controlled by an external signal.

3.5.8 Pulse Width Modulation Output

In pulse width modulation (PWM) output mode, a pulse waveform with specified high period (tHIGH) and low period (tLOW) is output at counter output terminal as shown in Figure 3. 44.

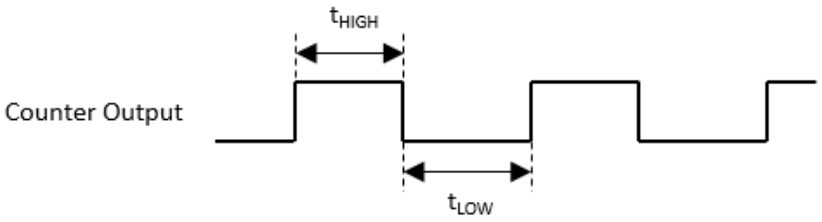

Figure 3.44 Pulse width modulation output

The number of pulses generated can be finite or infinite. For finite pulse generation, the counter output starts generating pulses when armed, and automatically stops after the specified number of pulses has completed. The counter can be re-armed after the previous generation is completed. This is shown in Figure 3. 45.

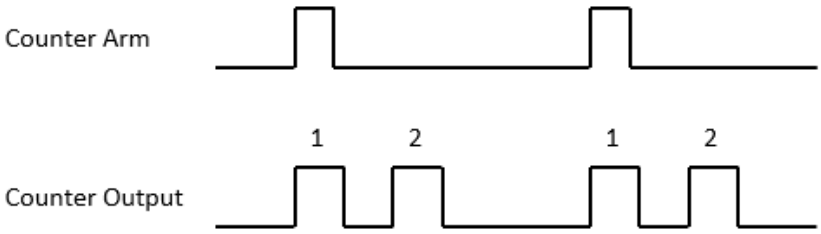

Figure 3.45 Finite pulse generation

For infinite pulse generation, the counter output starts generating pulses when armed and continues until stopped by software. This is shown in Figure 3. 46.

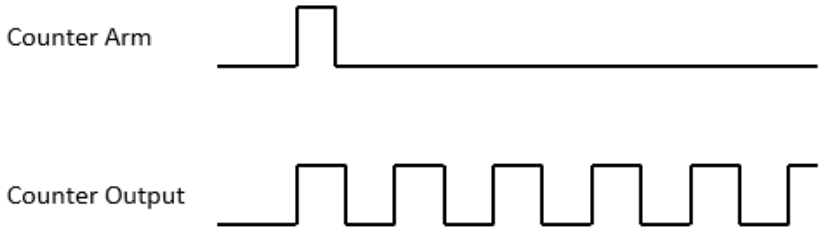

Figure 3.46 Infinite pulse generation

The output can be gated. If counter gate is high, pulses are output normally. On the other hand, if counter gate is low, output is disabled. This is shown in Figure 3. 47.

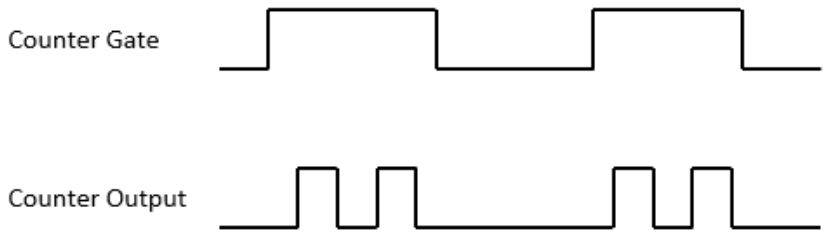

Figure 3.47 Gated pulse width modulation output

Static (Software-Timed) PWM Output

With static PWM output, the software controls the time of updating output pulse width, which is thus also called software-timed timer/pulse. Whenever the software sends an update command, the width of output pulse is updated to the specified value after current pulse is completed as shown in Figure 3. 48.

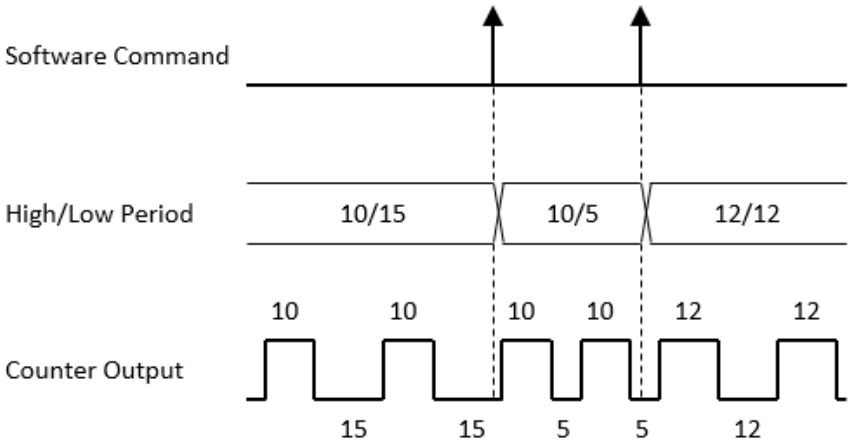

Figure 3.48 Static (software-timed) timer/pulse

Sample Clock Buffered (Hardware-Timed) PWM Output

With sample clock buffered PWM output, a hardware signal called sample clock controls the time of updating output pulse width as shown in Figure 3. 49. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

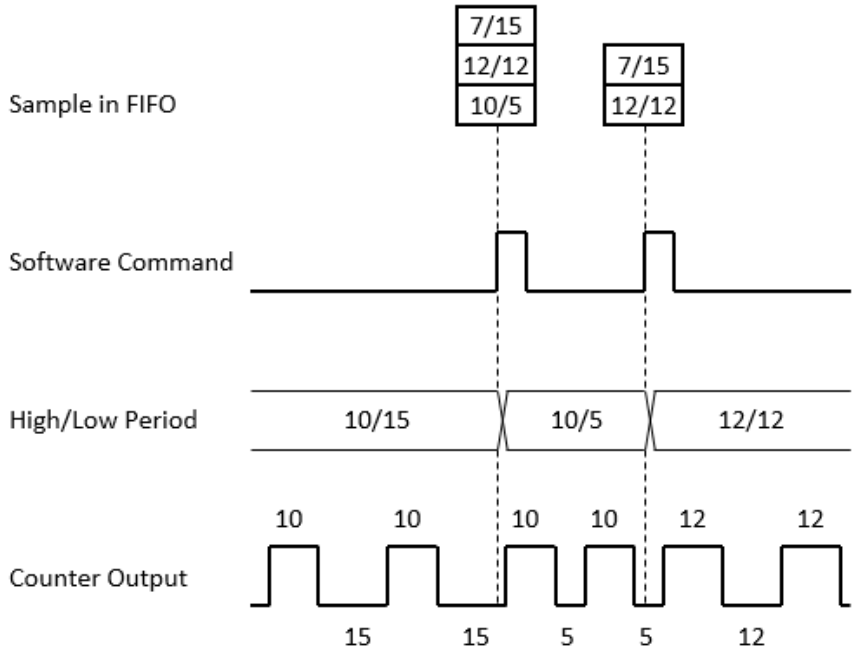

Figure 3.49 Sample clock buffered pulse width modulation output

The samples to be updated are first written to the onboard first-in-first-out (FIFO) memory by software. Each time a rising edge of sample clock is detected, the first sample in the FIFO is used to update the output pulse width, and then the sample is discarded. Buffered PWM output is also called hardware-timed PWM output.

The advantages of buffered PWM output over static PWM output include:

- The time of sample is deterministic.
- The time of sample can be controlled by an external signal.

Implicit Buffered PWM Output

With implicit buffered PWM output, width of every pulse is set by a sample. All samples are first written to the onboard first-in-first-out (FIFO) memory by software. Whenever an output pulse (a high period and a low period) is completed, the first sample in the FIFO is used to set width of the next pulse, and then the sample is discarded. This is shown in Figure 3.50.

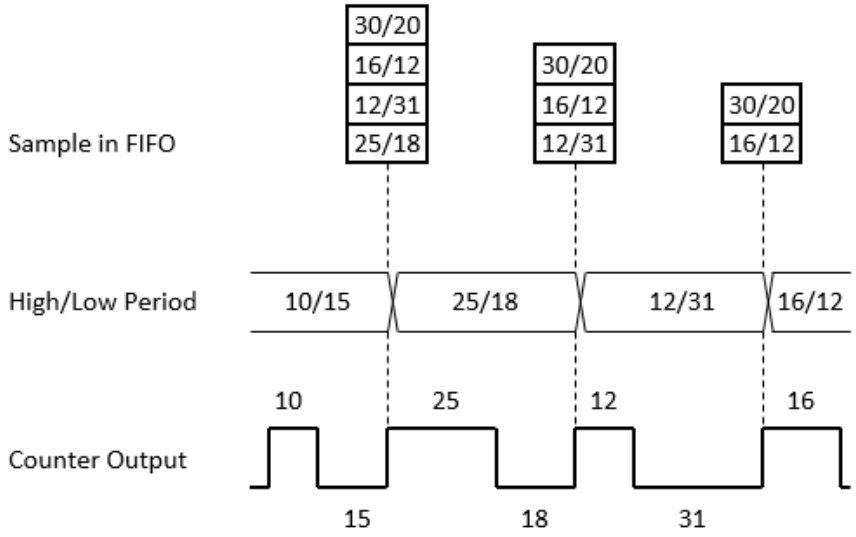

Figure 3.50 Implicit buffered pulse width modulation output

3.6 Timing Signals

Trigger Signal

The trigger can come from one of various signal sources. If the signal source is of digital type (logic high or low), it is called a digital trigger. On the other hand, if the signal source is of analog type (voltage level), it is called an analog trigger.

Digital Trigger

A digital trigger can be configured as rising edge active or falling edge active, as shown in Figure 3. 51 and Figure 3. 52, respectively.

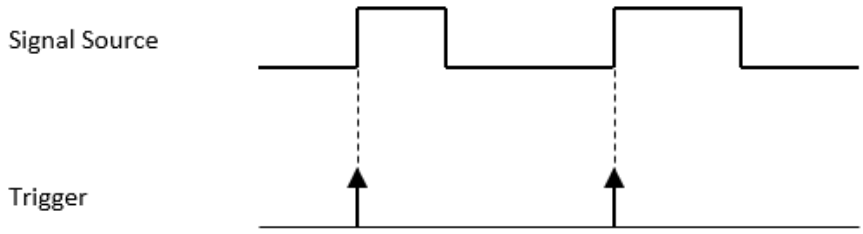

Figure 3.51 Rising edge active digital trigger

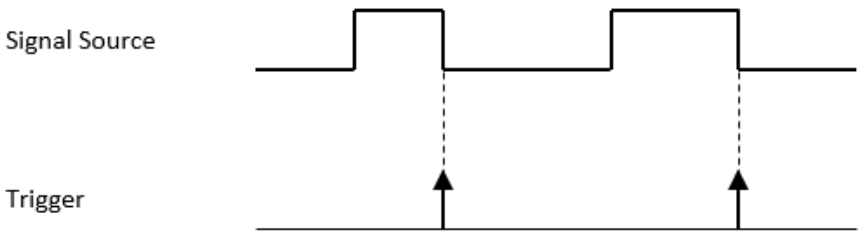

Figure 3.52 Falling edge active digital trigger

Analog Trigger

In addition to active edge, user can configure the threshold level and the hysteresis value for an analog trigger. The threshold level specifies the analog input voltage level where the trigger occurs. The hysteresis value prevents unwanted triggers due to noisy signals.

A rising edge active analog trigger occurs when the signal crosses the threshold level from below. And another trigger occurs only if the signal has crossed the voltage specified by the threshold level minus the hysteresis value from above before it crosses the threshold level from below again. This is shown in Figure 3. 53.

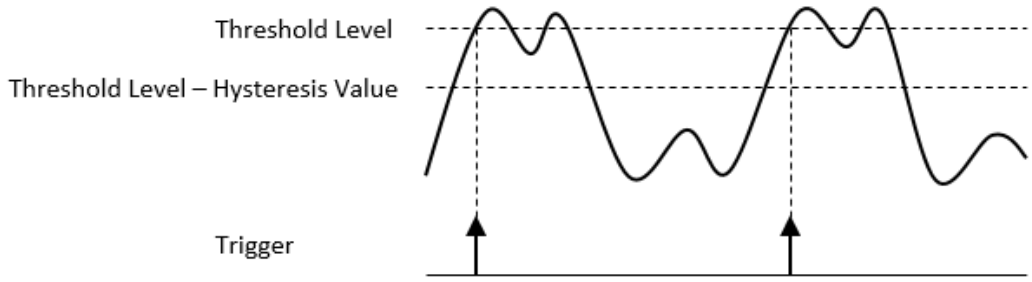

Figure 3.53 Rising edge active analog trigger

A falling edge active analog trigger occurs when the signal crosses the threshold level from above. And another trigger occurs only if the signal has crossed the voltage specified by the threshold level plus the hysteresis value from below before it crosses the threshold level from above again. This is shown in Figure 3. 54.

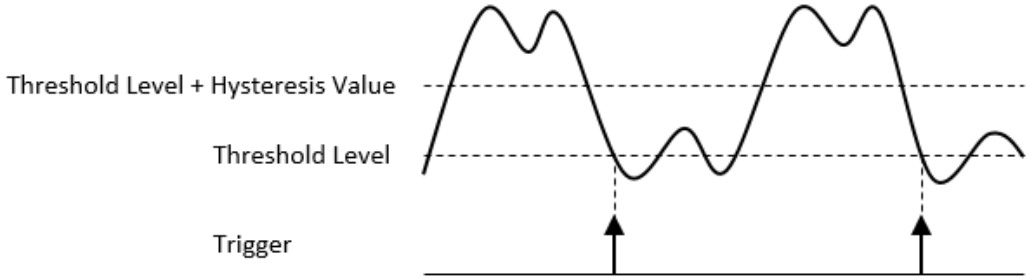

Figure 3.54 Falling edge active analog trigger

Clock Signal

The clock signal can be generated internally or provided from external source. For internal clock, when configuration is done, the clock frequency cannot be changed on the fly during the acquisition or generation operation. For external clock, on the other hand, clock frequency can be controlled by the external source in real time.

3.7 Synchronization

3.7.1 MDSI (Multi-Device Synchronization Interface) Introduction

To achieve synchronization of the Analog Input signals across multiple units of the same product and to provide users with a convenient wiring method, we offer the MDSI signal synchronization feature.

Figure 3.55 shows the location of the MDSI on the product as a reference. There are two on-board 10-pin box headers (MDSI IN, MDSI OUT), along with a 10-pin flat cable (This cable is optional and not included with the product).

To synchronize the acquisition of multiple devices, the required timing signals must be wired correctly. All devices must use the same sample clock for equal sample rate and be start triggered at the same time. One of the devices is selected as the primary device, and others as secondary devices. The primary device sends the required timing signals to all the secondary devices for synchronized acquisition.

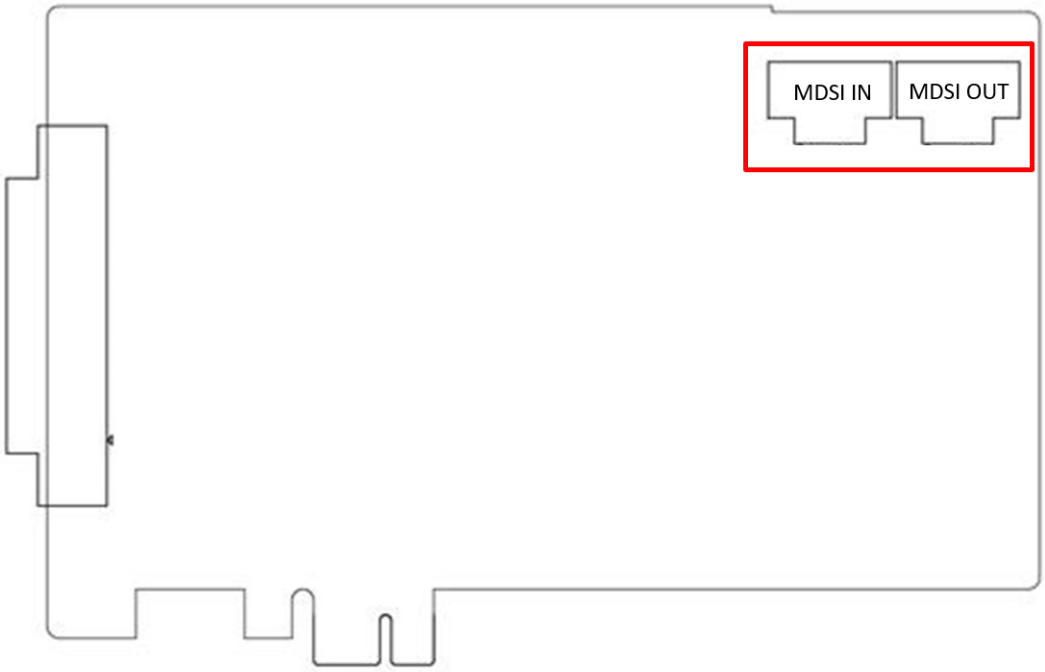

Figure 3.55 MDSI Layout

3.7.2 MDSI Wiring

The timing signals can be wired externally through cables, or internally by the Multi-Device Synchronization Interface (MDSI) 10-pin flat cables.

3.7.2.1 Synchronize by External Cables

Signal synchronization can be achieved through external wiring as shown in Figure 3.56 and Figure 3.57. This method requires additional wiring boards for the connections.

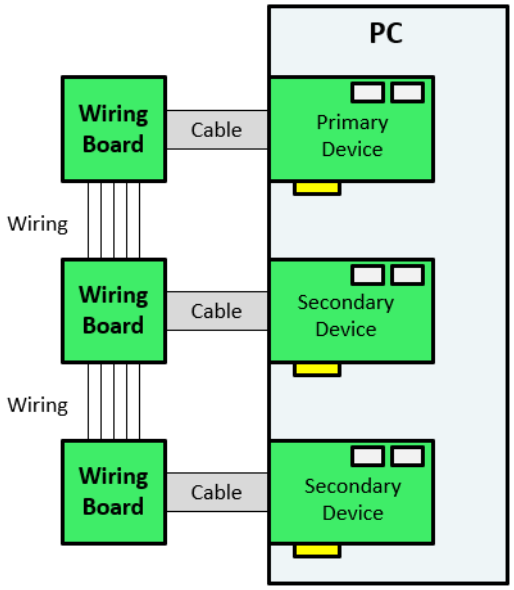

Figure 3.56 Synchronize by External Cables

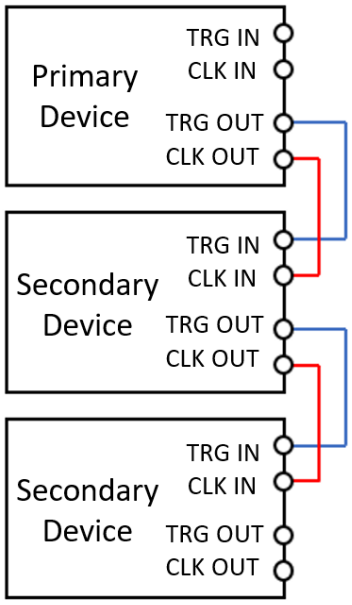

Figure 3.57 Signal Connection Synchronize by External Cables

3.7.2.2 Synchronize by MDSI Cables

To use MDSI cable for synchronization, connect each cable between MDSI OUT of one device to MDSI IN of the next device as shown in Figure 3.58 and Figure 3.59.

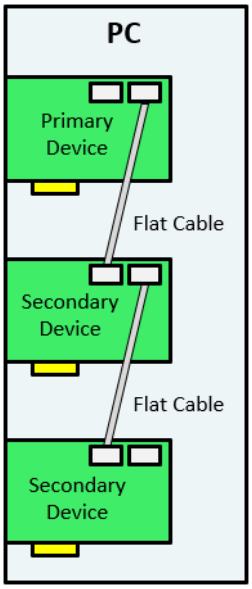

Figure 3.58 Synchronize by MDSI Cables

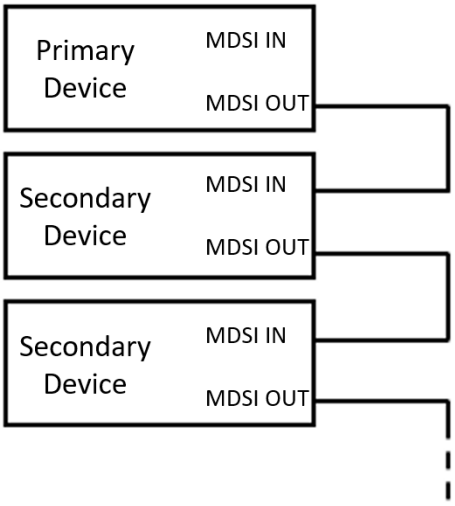

Figure 3.59 Signal Connection of MDSI Synchronize by MDSI Cables

3.7.3 Types of MDSI

Depending on the design characteristics of different products, the MDSI modes can be divided into two types: Synchronized-MDSI and Scanned-MDSI.

3.7.3.1 Synchronized-MDSI

With Synchronized-MDSI acquisition, The ADCs of all acquisition enabled channels simultaneously begin to convert the analog input voltage at each rising edge of the sample clock. Figure 3.60 shows an example of Synchronized-MDSI acquisition which AI0, AI1, and AI2 are enabled. PCIE-1812 adopts Synchronized-MDSI.

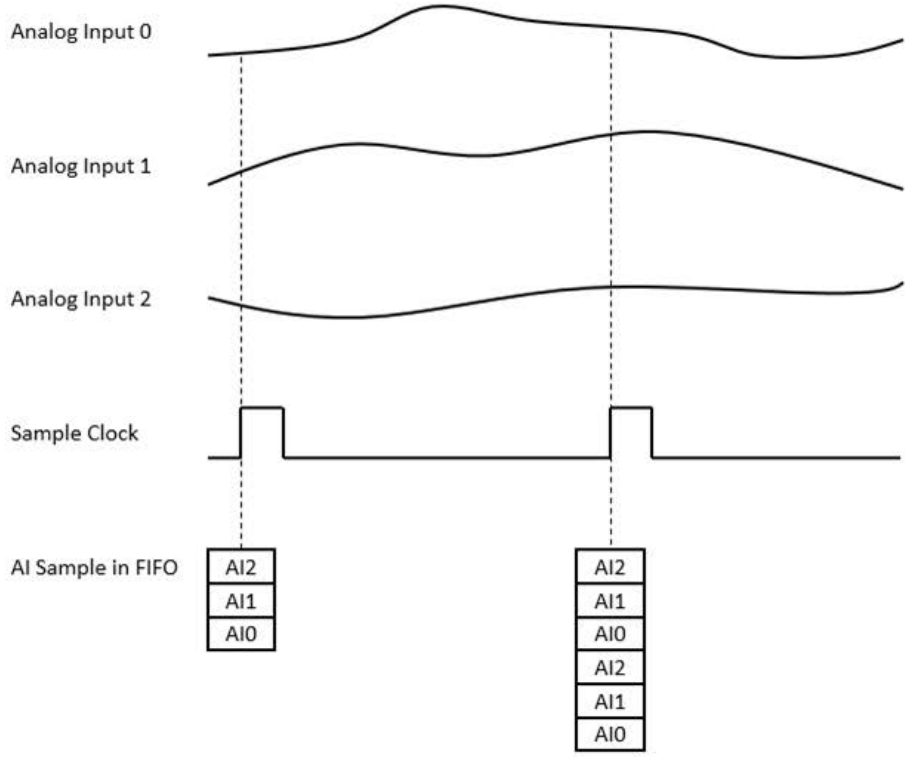

Figure 3.60 Synchronized-MDSI

3.7.3.2 Scanned-MDSI

In Scanned-MDSI products, a multiplexer (MUX) is used to switch between multiple input channels to a single ADC. It allows the ADC to sample different analog signals one at a time by selecting one input channel through control signals. The multiplexer then routes the chosen signal to the ADC for conversion. Figure 3.61 shows an example of Scanned-MDSI.

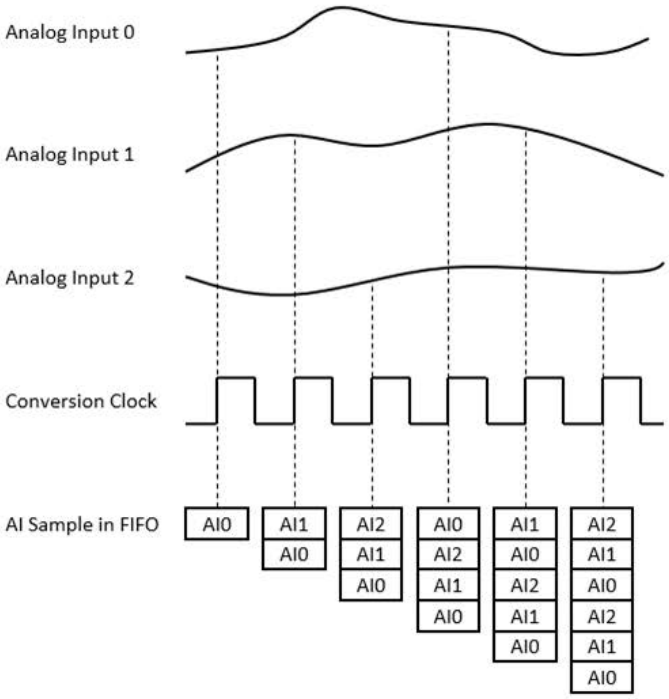

Figure 3.61 Scanned-MDSI

3.7.4 MDSI Setting

To use MDSI cable for synchronization, the primary and secondary devices must be set up differently. The following sections will explain the setup for both the primary and secondary devices.

3.7.4.1 Primary Device

In the Navigator, click on 'Settings,' then select 'Conversion.' Choose 'Internal Clock' as the conversion clock source.

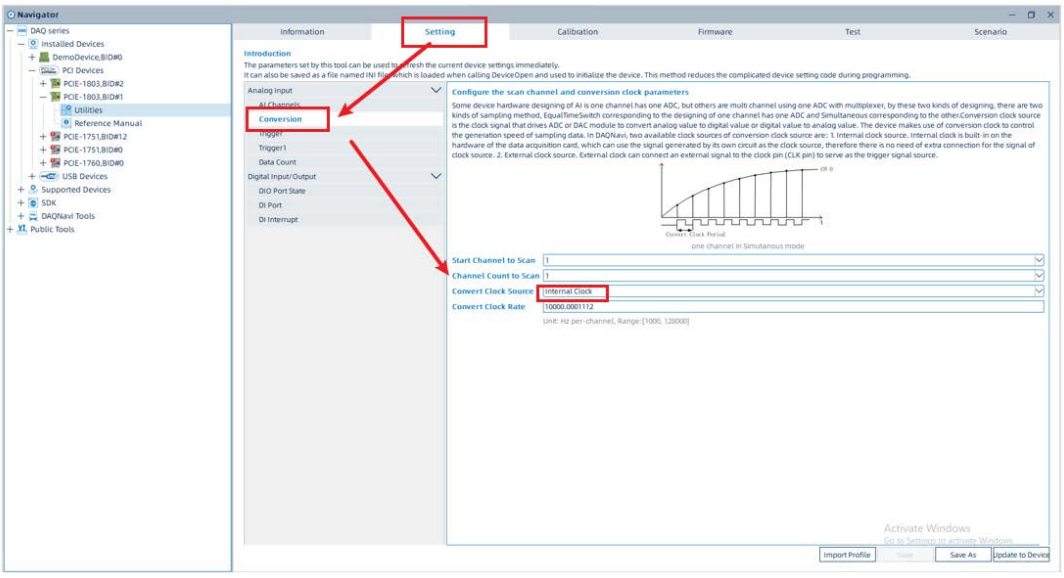

Figure 3.62 Setting for Primary Device

3.7.4.2 Secondary Device

First, click on 'Settings,' then click on 'Conversion.' To synchronize with the primary device, select 'MDSI Clock' as the conversion clock source.

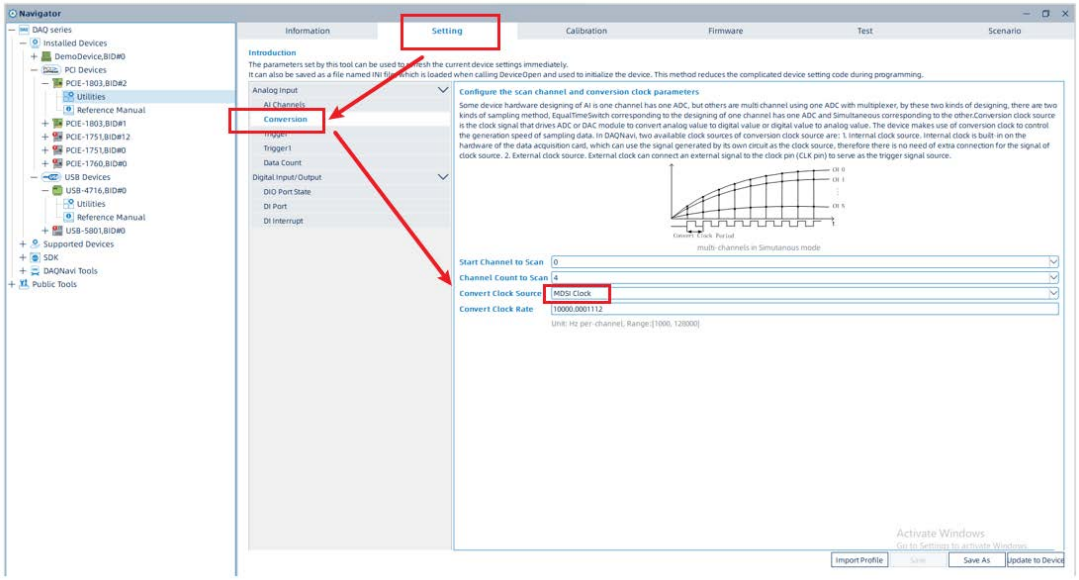

Figure 3.63 Conversion Setting for Secondary Device

Secondly, click on 'Trigger.' To ensure all cards start simultaneously, set 'MDSI Trigger0' as the source.

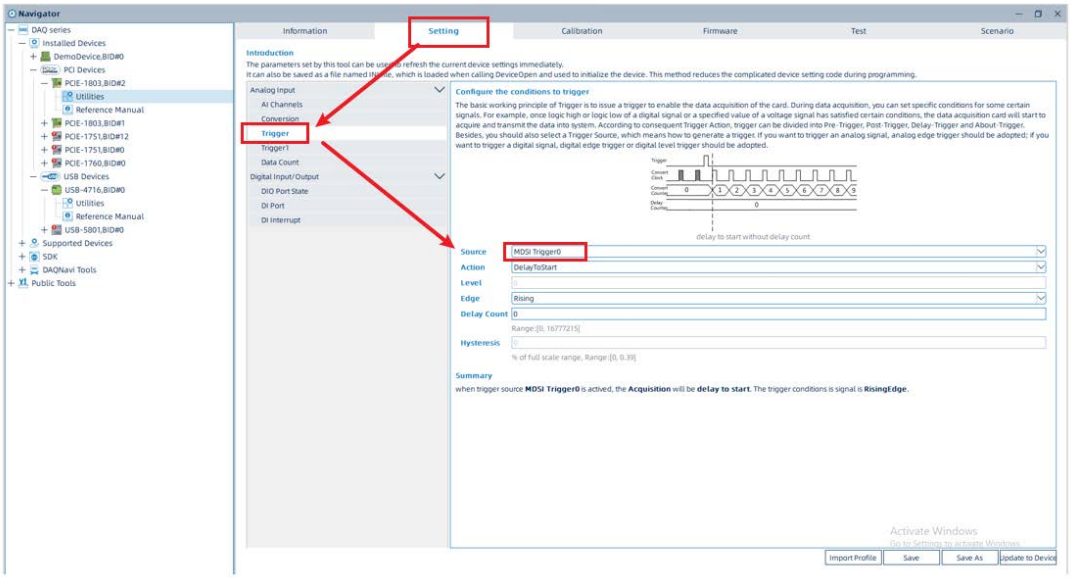

Figure 3.64 Trigger Setting for Secondary Device

Once all the settings are completed, the primary and secondary devices will operate synchronously. Use the Data Logger to verify whether MDSI is functioning properly. Figure 3.65 illustrates an example of synchronization.

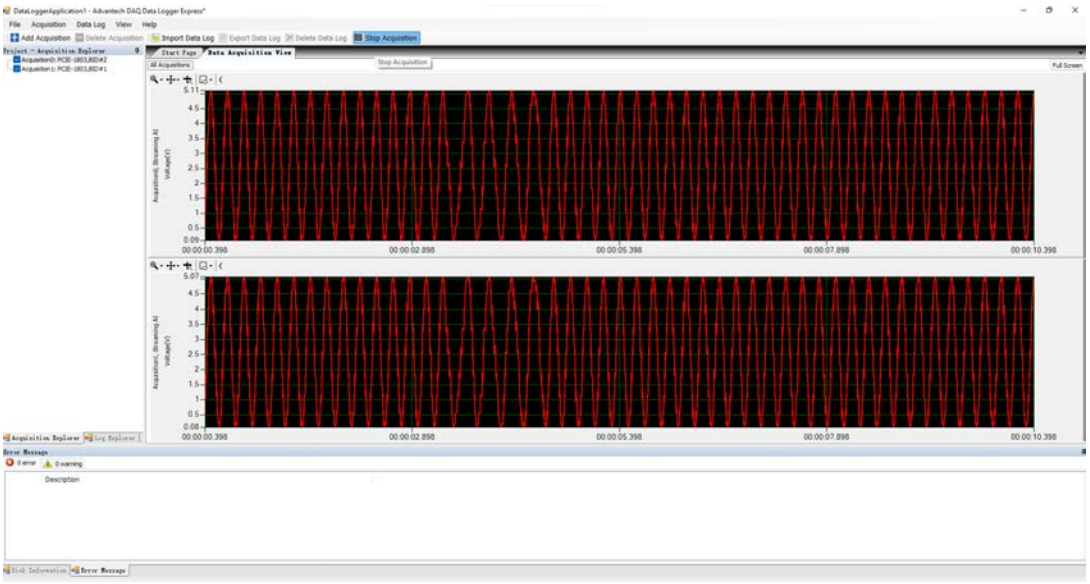

Figure 3.65 Data Logger for synchronization

3.8 Calibration

The Navigator of Advantech DAQNavi provides the calibration utility to calibrate the analog input and analog output circuitry of the device. Figure 3. 66 shows the interface of the calibration utility. Follow the instructions shown to calibration the device. For a multi-function device, which contains both analog input and analog output functions, analog input calibration must be performed before analog output calibration.

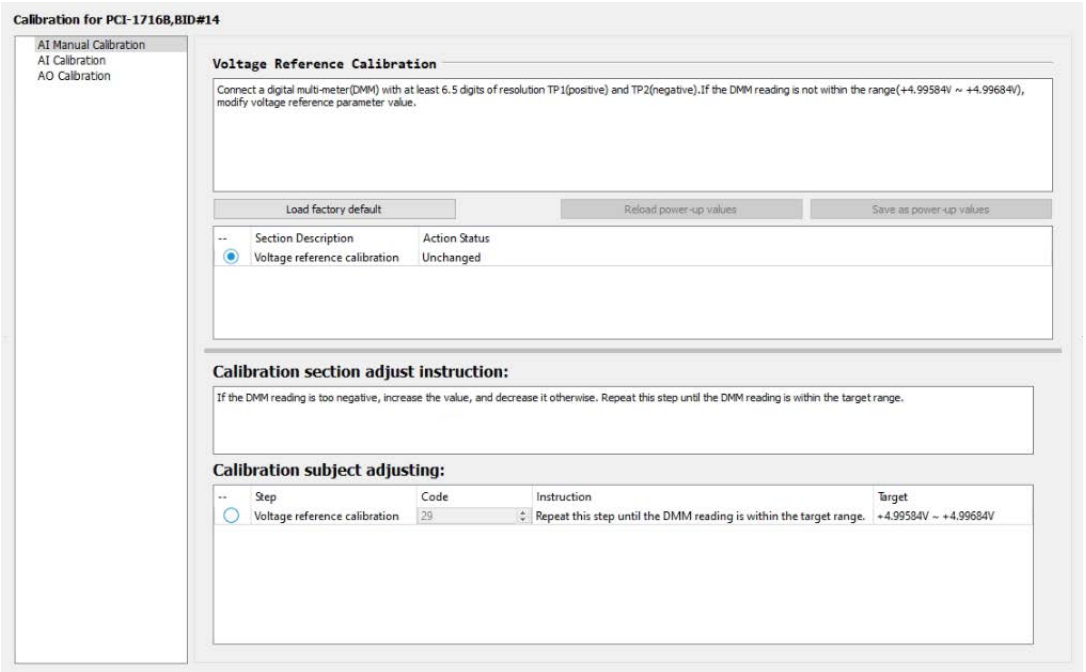

Figure 3.66 Calibration utility

When any of the calibration parameters is changed, user can save the change by clicking “Save as power-up values” button, or can reload power-up value by clicking “Reload power-up values” button. The status of the calibration parameters is shown

in “Action Status” column. If required, user can also load factory default calibration parameters by clicking “Load factory default” button.

3.9 Firmware/FPGA Code Update

The Navigator of Advantech DAQNavi provides the firmware/FPGA code download utility. User can use this utility to update the firmware/FPGA code of the device.

Figure 3. 67 shows the interface of the firmware/FPGA code download utility. To update the firmware/FPGA code, first click “Browser” button to choose the new firmware/FPGA code file. Both file version currently in the device and that of the chosen file will be shown. Then click “Download” button to start file download operation. After download is finished, device must be power cycled. For a PCI/PCIe device, power off the system and then powered on again. For a USB device, disconnect both the USB cable and the external power and then reconnect them again.

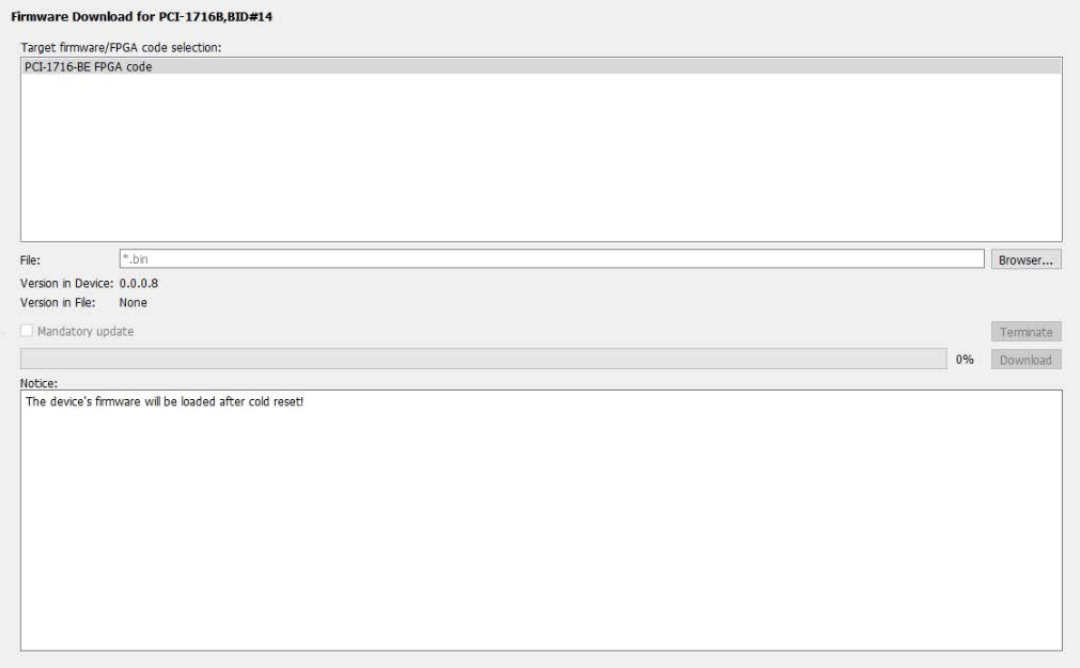

Figure 3.67 Firmware/FPGA code download utility

Ensure that do not turn off system power during download operation, or download operation will fail and current firmware/FPGA code on the device will be corrupted. If this happens, a golden pattern firmware/FPGA code will be loaded when device is powered on next time. The golden pattern may not be the latest version file, user should still update to the latest version using the utility.

Appendix A

Specifications

A.1 Function Block Diagram

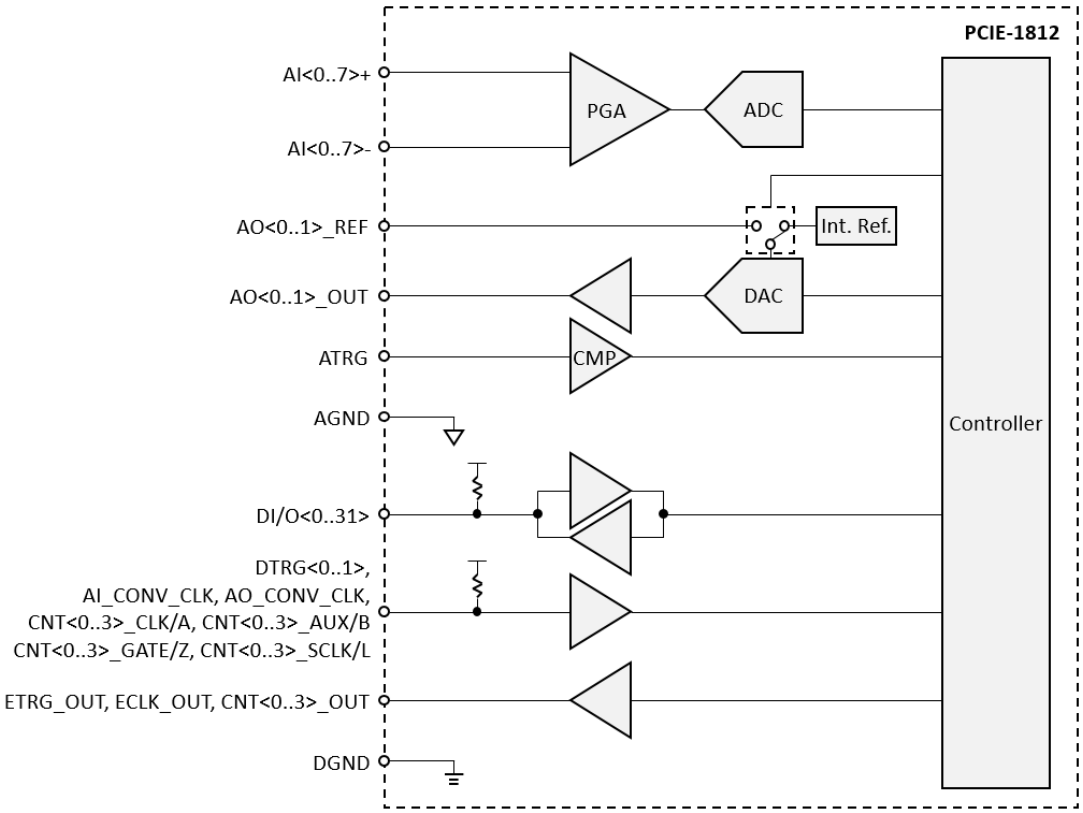

Figure A.1 Function Block

A.2 Analog Input

- **Channels:** 8 differential
- **Analog-to-digital converter (ADC) resolution:** 16 bits
- **Input coupling:** DC
- **Input range:** ±10 V, ±5 V, ±2.5 V, ±1.25 V, ±0.625 V, 0 ~ 10 V, 0 ~ 5 V, 0 ~ 2.5 V, or 0 ~ 1.25 V, software configurable per channel
- **Maximum input voltage:** ±11 V
- **Input common-mode voltage range:** ±11 V
- **Over-voltage protection:** ±15 V
- **Input impedance:** 1 GΩ
- **-3 dB bandwidth**

Table A.1: -3 dB Bandwidth

Range	±10 V	±5 V	±2.5 V	±1.25 V	±0.625 V
		0 ~ 10 V	0 ~ 5 V	0 ~ 2.5 V	0 ~ 1.25 V
BW	1.5 MHz	1.5 MHz	1.2 MHz	1 MHz	1 MHz

- **Linearity**
  - Integral non-linearity (INL): ±2LSB max.
  - Differential non-linearity (DNL): ±1.2LSB max.
- **Absolute accuracy**
  - Operating temperature within ±5°C of last auto-calibration temperature

Table A.2: Accuracy

Range	±10 V	±5 V	±2.5 V	±1.25 V	±0.625 V
Accuracy	±0.01 %	±0.01 %	±0.01 %	±0.01 %	±0.01 %
Range		0 ~ 10 V	0 ~ 5 V	0 ~ 2.5 V	0 ~ 1.25 V
Accuracy		±0.01 %	±0.01 %	±0.01 %	±0.01 %

  - Over full operating temperature range

Table A.3: Accuracy

Range	±10 V	±5 V	±2.5 V	±1.25 V	±0.625 V
Accuracy	±0.05 %	±0.05 %	±0.05 %	±0.05 %	±0.05 %
Range		0 ~ 10 V	0 ~ 5 V	0 ~ 2.5 V	0 ~ 1.25 V
Accuracy		±0.05 %	±0.05 %	±0.05 %	±0.05 %

- **Common-mode rejection ratio (CMRR):** 70 dB

- **DC performance:**

Table A.4: Idle Channel Noise

Range	50 kS/s		200 kS/s		250 kS/s	
	Noise (μV_{RMS})	Effective Resolution (bits)	Noise (μV_{RMS})	Effective Resolution (bits)	Noise (μV_{RMS})	Effective Resolution (bits)
±10 V	191	16	192	16	188	16
±5 V	107	16	103	16	102	16
±2.5 V	59	16	58	16	55	16
±1.25 V	36	16	36	16	35	16
±0.625 V	0	15.684	0	15.675	0	15.655
0 ~ 10 V	158	15.949	160	15.927	160	15.934
0 ~ 5 V	85	15.841	84	15.856	84	15.862
0 ~ 2.5 V	47	15.701	47	15.707	46	15.734
0 ~ 1.25 V	28	45.424	28	15.451	28	15.438

- **AC performance:**

Table A.5: Signal-to-Noise Ratio (SNR, 1 kHz Input Tone, -1 dBFS Amplitude)

Range	10 kS/s	50 kS/s	100 kS/s	250 kS/s
±10 V	81.16 dB	81.18 dB	80.70 dB	81.72 dB
±5 V	75.49 dB	74.36 dB	74.01 dB	74.15 dB
±2.5 V	67.92 dB	68.52 dB	68.53 dB	68.68 dB
±1.25 V	65.22 dB	65.25 dB	65.44 dB	65.66 dB
±0.625 V	61.85 dB	62.03 dB	62.41 dB	65.59 dB

Table A.6: Total Harmonic Distortion (THD, 1 kHz Input Tone, -1 dBFS Amplitude)

Range	10 kS/s	50 kS/s	100 kS/s	250 kS/s
±10 V	-97.69 dB	-94.57 dB	-94.47 dB	-93.31 dB
±5 V	-94.09 dB	-89.36 dB	-89.39 dB	-89.95 dB
±2.5 V	-87.96 dB	-85.20 dB	-82.90 dB	-82.78 dB
±1.25 V	-84.11 dB	-82.33 dB	-80.11 dB	-81.45 dB
±0.625 V	-81.16 dB	-77.97 dB	-77.25 dB	-77.64 dB

Table A.7: Total Harmonic Distortion Plus Noise (THD+N, 1 kHz Input Tone, -1 dBFS Amplitude)				
Range	**10 kS/s**	**50 kS/s**	**100 kS/s**	**250 kS/s**
±10 V	-81.07 dB	-80.98 dB	-80.52 dB	-81.43 dB
±5 V	-75.43 dB	-74.22 dB	-73.88 dB	-74.04 dB
±2.5 V	-67.88 dB	-68.43 dB	-68.37 dB	-67.55 dB
±1.25 V	-65.17 dB	-65.17 dB	-65.29 dB	-65.55 dB
±0.625 V	-61.80 dB	-61.92 dB	-62.27 dB	-62.46 dB

Table A.8: Spurious-Free Dynamic Range (SFDR, 1 kHz Input Tone, -1 dBFS Amplitude)				
Range	**10 kS/s**	**50 kS/s**	**100 kS/s**	**250 kS/s**
±10 V	96.31 dB	97.68 dB	97.07 dB	96.43 dB
±5 V	91.55 dB	90.04 dB	85.17 dB	88.04 dB
±2.5 V	82.81 dB	81.20 dB	80.98 dB	79.59 dB
±1.25 V	78.71 dB	79.27 dB	79.80 dB	76.00 dB
±0.625 V	78.22 dB	77.46 dB	75.14 dB	79.10 dB

Table A.9: Effective Number of Bits (ENOB, 1 kHz Input Tone, -1 dBFS Amplitude)				
Range	**10 kS/s**	**50 kS/s**	**100 kS/s**	**250 kS/s**
±10 V	13.17 dB	13.16 dB	13.08 dB	13.23 dB
±5 V	12.23 dB	12.03 dB	11.98 dB	12.00 dB
±2.5 V	10.98 dB	11.07 dB	11.06 dB	10.93 dB
±1.25 V	10.53 dB	10.53 dB	10.55 dB	10.59 dB
±0.625 V	9.97 dB	9.99 dB	10.05 dB	10.14 dB

Table A.10: Signal to Noise and Distortion (SINAD, 1 kHz Input Tone, -1 dBFS Amplitude)				
Range	**10 kS/s**	**50 kS/s**	**100 kS/s**	**250 kS/s**
±10 V	81.07 dB	80.98 dB	80.52 dB	81.43 dB
±5 V	75.43 dB	74.22 dB	73.88 dB	74.04 dB
±2.5 V	67.88 dB	68.43 dB	68.37dB	67.55 dB
±1.25 V	65.17 dB	65.17 dB	65.29 dB	65.55 dB
±0.625 V	61.80 dB	61.92 dB	62.27 dB	62.46 dB

- **Acquisition type:** Instant or buffered, software configurable
- **Buffered acquisition:**
  - Enable channel combination: Each channel can be enabled/disabled independently by software
  - Scan clock source: Internal or external
  - Sample clock rate: 250 kHz max., for all channels, simultaneous sampling, software configurable
- **Convert clock source:** Internal or external
- **Internal data buffer (FIFO) size:** 8,192 samples

A.3 Analog Output

- **Channels:** 2
- **Digital-to-analog converter (DAC) resolution:** 16-bits
- **Output configuration:** Single-ended
- **Output coupling:** DC
- **Output range**
  - **Reference source:** Internal or external, software configurable per channel
  - **Internal reference:** ±10 V, ±5 V, 0 ~ 10 V, or 0 ~ 5 V, software configurable per channel
  - **External reference:** ±x V or 0 ~ +x V @ +x V reference (-10 ≤ x ≤ +10), software configurable per channel
- **Power-on state:** 0 V @ 0~5 V output range
- **Driving capability:** ±20 mA max.
- **Output impedance:** 0.1 Ω max.
- **Linearity:**
  - Integral non-linearity (INL): ±1 LSB max.
  - Differential non-linearity (DNL): ±1 LSB max.
- **Absolute accuracy:**
  - Operating temperature within ±5°C of last auto-calibration temperature: ±0.01% of full-scale range max.
  - Over full operating temperature range: ±0.05% of full-scale range max.
- **Power-on glitch:** 50 mV
- **DC performance:**
  - Output noise: 100 μVRMS
  - Effective resolution: 16 bits
  - Channel-to-channel DC crosstalk: -140 dB
- **AC performance:**
  - Slew rate: 20 V/μs
  - Settling time: 5 μs (to 4 LSBs of FSR)
- **Update type:** Static or buffered, software configurable
- **Buffered generation:**
  - Enable channel combination: Each channel can be enabled/disabled independently by software
  - Update clock rate: 3 MHz max. per channel, software configurable
  - Update clock source: Internal or external
  - Internal data buffer (FIFO) size: 8,192 samples

A.4 Bi-directional Digital Input/Output

- **Channels:** 32
- **Direction control:** Each channel can be configured independently by software, or can be fixed as output by on-board jumpers
- **Power-on state:** Input when controlled by software, output when set by jumpers

A.4.1 Digital Input

- **Input type:** 5 V TTL
- **Input logic level**:
  - Logic high: 3.5 V min.
  - Logic low: 1.5 V max.
  - Working voltage: -0.25 V ~ 5.25 V
- **Input protection voltage:** -0.5 V ~ 6.5 V
- **Pull-up/down resistor:** Pull-up 10 kΩ (default) or pull-down 10 kΩ, software configurable
- **Response time:** 100 ns max.
- **Debounce filter:** 128 ns ~ 134.2 ms, software configurable
- **Acquisition type:** Instant or buffered, software configurable
- **Buffered acquisition:**
  - Enabled channel combination: Each port can be enabled/disabled independently by software
  - Sample clock rate: 250kHz max. per channel, software configurable
  - Sample clock source: Internal or external, software configurable
  - Internal data buffer (FIFO) size: 4,096 samples, each sample contains state of 1 port
- **Interrupt:**
  - Edge detection: Rising edge, falling edge, or both edges, software configurable per channel
  - Pattern match detection: By port detection, each channel can be enabled or disabled by software independently
  - State latch: Latch port state when interrupt occurs

A.4.2 Digital Output

- **Output type:** 5 V TTL
- **Power-on state:** Logic low
- **Output logic level:**
  - Logic high: 4.5 V min. @ 20 mA source
  - Logic low: 0.5 V max. @ 20 mA sink
- **Load current:**
  - One channel: 20 mA max.
  - Per port summed: 20 mA max.
  - Response time: 100 ns max.
  - Update type: Static or buffered, software configurable
- **Buffered generation:**
  - Enabled channel combination: Each port can be enabled/disabled independently by software
  - Update clock rate: 250 kHz max. for all ports, simultaneous updating
  - Update clock source: Internal or external, software configurable
  - Internal data buffer (FIFO) size: 4,096 samples
- **Initial output value:** Configurable by software

A.5 Trigger

- **Number of triggers:** 2
- **Trigger action:** Start, delay to start, stop, or delay to stop
- **Trigger delay range:** 0 ~ 16,777,215 samples
- **Sample number:** 0 ~ 16,777,215 samples
- **Analog trigger:**
  - Source: 2 external pin
  - Input range: ±10 V
    - Resolution: 16 bits
    - Accuracy: ±0.5% of full-scale range max.
    - Polarity: Rising edge or falling edge, software configurable
    - Input protection voltage: ±15 V
    - Minimum width: 100 ns
- **Digital trigger:**
  - Source: 2 external pins
  - Input logic level:
    - Logic high: 3.5 V min.
    - Logic low: 1.5 V min.
    - Working voltage: -0.25 V ~ 5.25 V
    - Polarity: Rising edge or falling edge, software configurable
    - Input protection voltage: -0.5 V ~ 6.5 V
  - Pull-up/down resistor: Pull-up 10 kΩ
  - Minimum width: 100 ns

A.6 External Clock Input

- **Channels:** 2 conversion clocks/1 scan clock
- **Input type:** 5 V TTL
- **Input logic level:**
  - Logic high: 3.5 V min.
  - Logic low: 1.5 V max.
  - Working voltage: -0.25 V ~ 5.25 V
- **Polarity:** Rising edge
- **Input protection voltage:** -0.5 V ~ 6.5 V
- **Pull-up/down resistor:** Pull-up 50 kΩ
- **Minimum width:**100 ns

A.7 Clock Output

- **Channels:** 1
- **Output type:** 5 V TTL
- **Output logic level:**
  - Logic high: 4.0 V min. @ 2 mA source/5.2 V max.
  - Logic low: 0.4 V max. @ 2 mA sink
- **Load current:** 8 mA max.

A.8 Multi-Device Synchronization Interface (MDSI)

- **Multi-device synchronization interface (MDSI):** Yes, connected by 10-pin flat cable

A.9 Counter

- **Channels:** 4
- **Resolution:** 32 bits
- **Input type:** 5 V TTL
- **Input logic level:**
  - Logic high: 3.5 V min.
  - Logic low: 1.5 V max.
  - Working voltage: -0.25 V ~ 5.25 V
- **Input protection voltage:** -0.5 V ~ 6.5 V
- **Pull-up/down resistor:** Pull-up 50 kΩ
- **Debounce filter:** 128 ns ~ 67 ms, software configurable
- **Output type:** 5 V TTL
- **Output logic level:**
  - Logic high: 4.5 V min. @ 15 mA source
  - Logic low: 0.5 V max. @ 15 mA sink
- **Load current:** 15 mA max.
- **Counter measurement function:**
  - Event counting:
    - Input frequency: 10 MHz max.
    - Clock polarity: Rising edge or falling edge, software configurable
    - Gate function: Enabled or disabled, software configurable
    - Gate polarity: High active or low active, software configurable
    - Measuring type: Instant
  - Frequency measurement:
    - Measuring method: Counting pulse by system time, period inverse, or auto adaptive, software configurable
    - Input frequency: 0.1 Hz ~ 10 MHz
    - Accuracy: 0.1%
    - Measuring type: Instant or sample clock buffered, software configurable
  - Pulse width measurement:
    - Pulse width range: 100 ns ~ 1 s
    - Pulse width resolution: 25 ns
    - Accuracy: 50 ppm
    - Measuring type: Instant or sample clock buffered, software configurable
  - Position measurement:
    - Input frequency:10 MHz max.
    - Measuring mode: Quadrature (A/B phase) x1, x2, x4, two-pulse (clockwise/counter-clockwise), signed-pulse
    - Reload value: Any value
    - Counter reload by Z signal: Enabled or disabled, software configurable
    - Measuring type: Instant or sample clock buffered, software configurable
- **Counter output function:**
  - One shot
    - Internal clock source frequency: 40 MHz
    - Internal clock accuracy: 50 ppm
    - External clock source frequency: 10 MHz max.

- Delay count: 1 ~ 4,294,967,295
- Gate source: External
- Gate polarity: Rising edge or falling edge, software configurable
- Output signal type: Positive pulse or negative pulse, software configurable
- Generation type: Static

– Timer/pulse:
- Timebase clock frequency: 40 MHz
- Timebase clock accuracy: 50 ppm
- Output frequency: 0.1 Hz ~ 10 MHz
- Gate function: Enabled or disabled, software configurable
- Gate polarity: High active or low active, software configurable
- Interrupt generation: Enabled or disabled, software configurable
- Generation type: Static

– Pulse width modulation:
- Timebase clock frequency: 40 MHz
- Timebase clock accuracy: 50 ppm
- Pulse width: 100 ns ~ 1 s
- Pulse width resolution: 25 ns
- Number of pulses: 1 ~ 4,294,967,295 or infinite, software configurable
- Gate function: Enabled or disabled, software configurable
- Gate polarity: High active or low active, software configurable
- Generation type: Static

– Position compare:
- Compare value: Instant or buffered, software configurable
- Output signal type: Positive pulse or negative pulse, software configurable
- Output Pulse width: 100 ns ~ 1 s
- Compare frequency: 5 MHz max.

■ **Buffered counter:**

– Internal data buffer (FIFO) size
- For measurement functions: 128 samples for each counter
- For output functions: 1,024 samples for each counter

– Trigger source: None, analog trigger, digital trigger, digital input edge detection event, or digital input pattern match event, software configurable

– Sample clock rate: 250 kHz max.

– Sample clock source: External or analog input sample clock, software configurable

A.10 FPGA Code Update

■ **FPGA code update function:** Yes, through Advantech Navigator utility

A.11 General Specifications

A.11.1 Power Requirements

■ **Power consumption:**

– +3.3 V: 500 mA typ., 700 mA max.

– +12 V: 400 mA typ., 450 mA max.

A.11.2 Power Supply Output

■ **+5 V (±5%):** 200 mA max.

■ **+12 V (±5%):** 100 mA max.

A.11.3 Physical

- **Form factor:** PCIe x1
- **Dimensions:** 175 x 100 x 18 mm3 (6.9 x 3.9 x 0.7 in.3)
- **Weight:** 122 g
- **I/O connector:** 100-pin SCSI (ribbon type)

A.11.4 Environmental

- **Operating temperature:** 0 °C to 60 °C (32 °F to 140 °F)
- **Storage temperature:** -40°C to 70°C (-40°F to 158°F)
- **Operating humidity:** 10% to 90% RH, non-condensing
- **Storage humidity:** 5% to 95% RH, non-condensing

ADVANTECH

Enabling an Intelligent Planet

www.advantech.com

Please verify specifications before quoting. This guide is intended for reference purposes only.