PCI11101C

PCIe Switch with Integrated USB 3.2 Gen 2 Host Controller and Programmable I/O

Highlights

- PCIe (8GT/s) switch fabric
- 2-lane PCIe (8 GT/s) expansion port
- USB 3.2 Gen 2 (10 Gbps) xHCI host
- I/O Multiplexer (SMBus/SPI/UART/GPIO)
- I/O optimized for M.2 interface breakouts

Target Applications

- Math offload
- Vision intelligence / cameras / machine vision
- Servers with NG BMC & no PCH

Features

- Integrated PCI switching fabric
  - 512 byte maximum payload size
- Integrated PCIe physical interfaces
  - 4-lane (4x 8 GT/s) upstream port
    - Allowing single, dual, or four lane links
  - 2-lane (2x 8 GT/s) downstream port
- Integrated USB 3.2 Gen 2 (10 Gbps) physical interfaces
- Integrated xHCI USB 3.2 Gen 2 (10 Gbps) USB host controller
  - 10 Gbps Gen 2 PHY
  - USB HS/FS/LS PHY
- Two external power supplies: +3.3V and +1.1V
- Comprehensive power management features
  - PCIe 3.1 LPSS (Low Power Sub States): L2 (with aux. power supply) LPSS L1.1 (snooze), L1.2 (off)
- Power and I/O
  - Integrated power-on reset circuit with configurable under/over-voltage protection
  - Latch-up performance exceeds 150 mA per EIA/JESD78, Class II
  - JEDEC Class 2 ESD performance
- UARTs
  - RS232/RS422/RS485
  - Auto-direction control
  - Standard and advanced speed support
  - Basic or comprehensive signal support
- Additional features
  - Multifunction GPIOs
  - Programmable pin multiplexer
  - Ability to use low-cost 25 MHz crystal or clock for reduced BOM
  - PCIe Precision Time Measurement (PTM)
  - Support for Common Reference Clock and Separate Reference Clocks (SRNS and SRIS)
  - SPI peripheral interface
  - SMBus target interface
  - SMBus controller interface
  - JTAG TAP
  - PVT sensor
- Packaging
  - Pb-free RoHS compliant 132-pin VQFN-DR package
- Environmental
  - Available in commercial, industrial, and AEC-Q100 Grade 3 temperature ranges

This document is a truncated version of the full PCI11101C datasheet. The comprehensive version may be obtained by contacting your Microchip sales representative.

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
AFE	Analogue Front End (AFE)
Bandwidth	Bandwidth is defined as the rate of data transfer, bit rate or throughput.
CC	CC is an abbreviation for Configuration Channel. This is used in the discovery, configuration and management of connections across a [USBTYPEC] cable.
CDM	CDM is an abbreviation for Charge Device Model. This is a Model of ESD caused by mechanical handling. See [JS-002-2014].
Completion	In PCIe Completion refers to the Packet used to terminate, or to partially terminate, a transaction sequence. A Completion always corresponds to a preceding Request, and, in some cases, includes data. See [PCIe5].
Configuration Request Retry Status	For PCI Configuration Requests only, following reset it is possible for a device to terminate the request but indicate that it is temporarily unable to process the Request, but will be able to process the PCI Configuration Request in the future - in this case, the Configuration Request Retry Status (CRS) Completion Status is used. See [PCIe5].
Configuration Space	One of the four address spaces within the PCI Express architecture. Packets with a Configuration Space address are used to configure Physical Functions. See [PCIe5].
CPU	CPU is an abbreviation for Central Processing Unit. This is the main processor for the system. **Note:** In this case, the CPU is located on the Host system and not in the device itself which has no CPU.
CRS	CRS is an abbreviation for Configuration Request Retry Status.
DFP	DFP is an abbreviation for Downward Facing Port. This is a Port typically used to connect devices/peripherals (e.g. for USB or PCIe).
Debouncer	A Debouncer is a piece of hardware where the signal is passed through if it is stable for longer than a Debouncer period.
Direct Memory Access	Direct Memory Access is a feature of computer systems that allows certain hardware subsystems to access main system memory (RAM) independently of the central processing unit (CPU). With DMA, the CPU first initiates the transfer, then it does other operations while the transfer is in progress, and it finally receives an interrupt from the DMA Controller (DMAC) when the operation is done.
DMA	DMA is an abbreviation for Direct Memory Access.
DMAC	DMAC is an abbreviation for DMA Controller.
DMA Controller	A DMA Controller is a hardware device that allows I/O devices to directly access memory with less participation from the processor.
EEPROM	EEPROM is an abbreviation for Electrically Erasable Programmable Read-only Memory.
EEPROM I²C Controller	The EEPROM I²C Controller is used to read and write EEPROMs via I²C.
ESD	ESD is an abbreviation for Electro-static Discharge.
FET	FET is an abbreviation for Field Effect Transistor. This is typically used to switch on/off power.
GPIO	GPIO is an abbreviation for General Programmable I/O. It is used to refer to PIO accessible externally to the part. Since there is no internal PIO used in the device the terms PIO and *GPIO* have been used interchangeably.
HBM	HBM is an abbreviation for Human Body Model. The HBM simulates ESD from humans. See [JESD22-A115C].
Hot-Plug	In PCI Hot-Plug is the insertion and removal of add-in cards without powering down the Platform or restarting the operating system from a specific Hot-Plug slot. See [PCIHotPlug].

TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
I²C	Inter-integrated Circuit: multi-Controller/multi-Target architecture. I²C is a 2-wire bus consisting of: I²C SDA, I²C SCL. Defined in [I2CBus].
I²C SCL	I²C SCL is an abbreviation for the I²C Serial Clock line.
I²C SDA	I²C SDA is an abbreviation for the I²C Serial Data line.
I²C Controller	An I²C Controller refers to any device that initiates I²C transactions and drives the clock as defined in [I2CBus].
I²C Controller Core	The I²C Controller Core implements both an I²C Controller and I²C Target.
I²C Target	An I²C Target is the Target of an I²C transaction which is driven by an I²C Controller as defined in [I2CBus].
In-Band	In-Band refers to signaling sent using the main communication channel. See also Out-Of-Band.
IRQ	IRQ is an abbreviation for the Interrupt Request Line.
MAC	The Medium Access Control (MAC) forms part of the Data Link Layer as defined in OSI. The MAC is responsible for controlling how devices in a network gain access to a medium and permission to transmit data.
MFD	MFD is an abbreviation for Multi-Function Device.
Multi-Function Device	A Multi-Function Device is a PCI Device with more than one Physical Function. Physical Functions in an MFD are numbered PF0, PF1, PF2 etc.
N/A	N/A is an abbreviation for Not Applicable.
NC	NC is an abbreviation for Not Connected.
OCS	OCS is an abbreviation for Over-Current Sense.
OEM	OEM is an abbreviation for Original Equipment Manufacturer.
OTP	OTP is an abbreviation for One Time Programmable Memory.
Out-Of-Band	Out-Of-Band refers to signaling sent outside of the main communication channel. See also In-Band.
PCB	PCB is an abbreviation for Printed Circuit Board.
PCI Bridge	The PCI Bridge is one of several PCI defined System Elements. A Function that connects a PCI/PCI-X segment or PCI Express Port with an internal component interconnect or with another PCI/PCI-X bus segment or PCI Express Port. A virtual PCI Bridge in a Root Complex or PCI Switch must use the software configuration interface described in [PCIe5].
PCI Switch	A PCI Switch *is a* [PCIe5] System Element that connects two or more Ports to allow Packets to be routed from one Port to another. To configuration software, a PCI Switch appears as a collection of virtual PCI Bridges.
PCI Configuration Request	A PCI Configuration Request PCI Packet targeted at the Configuration Space. See [PCIe5]. **Note:** This is not the same as a System Configuration Request.
PD	PD is an abbreviation for USB Power Delivery as defined in [USBPD3].
PF	PF is an abbreviation for Physical Function.
PHY	PHY is an abbreviation for “physical layer”, an electronic circuit required to implement physical layer functions of OSI in a network interface controller.
Physical Function	Within a Device, the Physical Function, is an addressable entity in Configuration Space associated with a single Function Number. Used to refer to one Function of a Multi-Function Device, or to the only Function in a Single-Function Device.
Pin	A Pin is an external connection on the package enabling connection to the PCB.
PIO	*PIO* is an abbreviation for Programmable I/O. These are fully programmable input/output lines.
PLL	PLL is an abbreviation for Phase-Locked Loop.
Port Partner	Port Partner refers to a remote port which is connected to the device’s local port.
PVT Sensor	PVT Sensor is an abbreviation for Process-Voltage-Temperature Sensor.
QFN	QFN is an abbreviation for a Quad-Flat No-leads package.
RAM	RAM is an abbreviation for Random-access Memory (read/write).
RFE	RFE is an abbreviation for Receive Filtering Engine.
ROM	ROM is an abbreviation for Read-only Memory.

TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
Root Complex	A Root Complex is a PCI defined System Element that includes at least one Host PCI Bridge, Root Port, or Root Complex Integrated Endpoint. The Host PCI Bridge connects a host CPU or CPUs to a PCI Hierarchy connected to the Root Port or Root Complex Integrated Endpoint. See [PCIe5].
Side-Band	In this document, Side-Band is used to refer to Registers or control paths accessed via any of the Side-Band options (SMBus/SPI).
Sink Role	A USB Type-C Port in Sink Role is sinking power from its Port Partner.
SMBus	SMBus is an abbreviation for System Management Bus, a two-wire bus derived from I²C. Defined in [SMBus3].
SMBus Controller	An SMBus Controller refers to any device that initiates SMBus transactions and drives the clock as defined in [SMBus3].
SMBus Target	An SMBus Target is the Target of an SMBus transaction which is driven by a SMBus Controller as defined in [SMBus3].
Source Role	USB Type-C Port is in Source Role when it is sourcing power to its Port Partner as defined in [USBTYPEC] and [USBPD3].
Source-only Operation	Source-only Operation refers to a USB Type-C Port which operates exclusively in USB Type-C/ Power Delivery Source Role as defined in [USBTYPEC] and [USBPD3].
SPI	SPI is an abbreviation for Serial Peripheral Interface bus: a full-duplex bus utilizing a single-Controller/multi-Peripheral architecture. SPI is a 4-wire bus consisting of: SPI CLK, SPI COPI, SPI CIPO, SPI CS.
SPI CLK	SPI CLK *refers to the* SPI clock line.
SPI CIPO	SPI CIPO is an abbreviation for Controller In Peripheral Out for SPI connections.
SPI Controller	A SPI Controller is any device that initiates SPI transactions and drives the clock.
SPI COPI	SPI COPI is an abbreviation for Controller Out Peripheral In for SPI connections.
SPI Peripheral	Target of an SPI transaction which is driven by an SPI Controller.
SPI CS	SPI CS *is* an abbreviation for SPI Peripheral Chip Select used to select each individual SPI Peripheral on the bus.
SRIS	Separate Reference Clock with Independent SSC.
SRNS	Separate Reference Clock With No SSC.
SSC	Spread Spectrum Clocking
System Configuration Request	A System Configuration Request is a request initiated by setting bits in the GENERAL_SYS_CONFIG_REQ_REG Register indicating that part of the device needs to be configured from OTP/EEPROM and/or via SPI/SMBus. **Note:** This is not the same as a *PCI Configuration Request*.
UART	UART is an abbreviation for Universal Asynchronous Receiver Transmitter.
UFP	UFP is an abbreviation for Upward Facing Port: a Port typically taking the Device role.
USB Host Controller	A USB Host Controller provides a means for a computer system to manage USB Peripherals connected to the USB. The USB Host Controller provides an interface conforming with either [xHCI] for SuperSpeed USB or [eHCI] for low, full and high speed USB.
USB Power Delivery Operation	USB Power Delivery Operation refers to a Port which is operating using USB Power Delivery protocols in conformance to [USBPD3].
USB Type-C Operation	USB Type-C Operation refers to a Port which is operating without using USB Power Delivery protocols and in conformance to [USBTYPEC].
UUID	UUID is an abbreviation for Universally Unique Identifier.
V_{BUS}	V_{BUS} is the USB main power supply which operates as defined in [USB3.2], [USBTYPEC] and [USBPD3].
V_{CONN}	V_{CONN} is the USB Supplementary power supply defined for the USB Type-C Connector in [USBTYPEC].
VQFN-DR	VQFN-DR is an abbreviation for a Dual-row Quad-Flat No-leads package.
V_{SAFE0V}	V_{safe0V} is the V_{BUS} “0 Volt” level as defined by [USBPD3].
V_{SAFE5V}	V_{safe5V} is the V_{BUS} “5 Volt” level as defined by [USBPD3].

1.2 Buffer Types

The pin buffer type definitions are detailed in Table 1-2. Refer to Chapter 3.0, "Pin Descriptions and Configuration" for details on individual pin buffer type assignments.

TABLE 1-2: BUFFER TYPE DESCRIPTIONS

Buffer	Description
AI	Analog input.
AIO	Analog bidirectional.
DB	Debouncer available on input pin (refer to Section 3.4, "Debouncers").
I	Input.
I/O-P	Analog input/output defined per the [PCIe3.1a] Specification.
I/O-U	Analog input/output defined per the USB 2.0 Specification.
ICLK	Crystal oscillator input pin.
IS	Input with Schmitt trigger in the **VDD33** power domain.
LVDS	Low Voltage Differential Signaling.
O_V10	Fixed voltage output with programmable output buffer up to 10 mA (2/4/8/10 mA) in the **VDD33** power domain.
OD_V10	Fixed voltage open drain output with programmable output buffer up to 10 mA (2/4/8/10 mA) in the **VDD33** power domain.
OCLK	Crystal oscillator output pin.
P	Power pin.
PD	Internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
VIS	Variable voltage Schmitt-triggered input in the **VDDVARIO** power domain.
VO_V10	Variable voltage output with programmable output buffer up to 10 mA (2/4/8/10 mA) in the **VDDVARIO** power domain.
VOD_V10	Variable voltage open drain output with programmable output buffer up to 10 mA (2/4/8/10 mA) in the **VDDVARIO** power domain.
VO-R_5	Variable voltage output with 5 mA sink and 5 mA source in the **VDDVARIO** power domain.

1.3 Pin Reset States

The pin reset state definitions are detailed in Table 1-3. Refer to Table 3-1 for details on individual pin reset states.

TABLE 1-3: PIN RESET STATE LEGEND

Symbol	Description
AI	Analog input
AO	Analog output
P	Power
PD	Hardware enables pull-down
Y	Hardware enables function
Z	Hardware disables output driver (high impedance)

1.4 Reference Documents

TABLE 1-4: REFERENCE DOCUMENTS

Reference	Document Name	Revision/Version Date
[ACPI]	Advance Configuration and Power Interface (ACPI) Specification. https://uefi.org/sites/default/files/resources/ACPI_6_3_May16.pdf	6.3 2019-01
[AEC-Q100-002E]	AEC - Q100-002, Human Body Model Electrostatic Discharge Test. http://www.aecouncil.com/Documents/AEC_Q100-002E.pdf	E August 20, 2013
[AEC-Q100-003E]	AEC - Q100-003, Machine Model (MM) Electrostatic Discharge Test (decommissioned specification). http://www.aecouncil.com/AECDocuments.html	E
[AEC-Q100-011C1]	AEC - Q100-011, Charged Device Model (CDM) Electrostatic Discharge Test. http://www.aecouncil.com/Documents/AEC_Q100-011C1.pdf	C1 2013-03-12
[AN4255]	AN4255 PCI12000/PCI11xxx Register Map Contact your Microchip representative for more information.	Rev. A (02-21-22)
[ASME-Y14.5M]	ASME Y14.5M-2018, Dimensioning and Tolerancing. https://www.asme.org/products/codes-standards/y145-2018-dimensioning-and-tolerancing	14.5-2018
[eHCI]	Enhanced Host Controller for USB 2.0 specification. https://www.intel.com/content/www/us/en/products/docs/io/universal-serial-bus/ehci-specification-for-usb.html	R1.0 2002-03-12
[I2CBus]	I^2C bus specification and user manual. https://www.nxp.com/docs/en/user-guide/UM10204.pdf	V.6 2014-04-04
[I2SBus]	I^2S bus specification. https://web.archive.org/web/20070102004400/http://www.nxp.com/acrobat_download/various/I2SBUS.pdf	N/A 1996-06-05
[IEC61000-4-2]	IEC 61000-4-2:2008, Electromagnetic Compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test. https://webstore.iec.ch/publication/4189	2.0 2008-12-09
[JEP106]	JEDEC Standard, JEP106, Standard Manufacturer's Identification Code. https://www.jedec.org/system/files/docs/JEP106BB.pdf	BB 2020-06
[JESD22-A115C]	JEDEC, JESD22-A114F, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM). https://www.jedec.org/sites/default/files/docs/22A115C_0.pdf	5C 2010-11
[JESD78D]	JEDEC, IC Latch-Up Test, JESD78D. https://www.jedec.org/sites/default/files/docs/JESD78D.pdf	D 2011-11
[JS-001-2017]	ANSI/ESDA/JEDEC JS-001-2017, for Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM) - Component Level. https://www.jedec.org/system/files/docs/JS-001-2017.pdf	2017-05-12
[JS-002-2014]	ANSI/ESDA/JEDEC JS-002-2014, for Electrostatic Discharge Sensitivity Testing, Charged Device Model (CDM) - Device Level. https://www.jedec.org/system/files/docs/JS-002-2014.pdf	2015-04-07
[M.2]	PCI Express M.2 Specification. https://pcisig.com/specifications/pciexpress/	Rev 3.0 v1.2 2019-06-26
[PCICode]	PCI Code and ID Assignment Specification. https://pcisig.com/specifications/pciexpress/	Rev 1.11 2019-01-24
[PCIHotPlug]	PCI Hot-Plug Specification. https://pcisig.com/specifications/pciexpress/	1.1 2001-06-20
[PCIe3.1a]	PCI Express Base Specification Revision 3.1a. https://pcisig.com/specifications/pciexpress/	R3.1a 2015-12-07
[PCIe4]	PCI Express Base Specification Revision 4.0. https://pcisig.com/specifications/pciexpress/	R4.0, V1.0 2017-09-27
[PCIe5]	PCI Express Base Specification Revision 5.0. https://pcisig.com/specifications/pciexpress/	R5.0 V1.0 2019-05-22

TABLE 1-4: REFERENCE DOCUMENTS (CONTINUED)

Reference	Document Name	Revision/Version Date
[SMBus2]	System Management Bus (SMBus) Specification. http://www.smbus.org/specs/smbus20.pdf	2.0 2000-08-03
[SMBus3]	System Management Bus (SMBus) Specification. http://www.smbus.org/specs/SMBus_3_0_20141220.pdf	3.0 2014-12-20
[USB2]	Universal Serial Bus Revision 2.0 Specification. https://www.usb.org/document-library/usb-20-specification	2.0 + errata + ECNs, 2019-05-24
[USB3.2]	Universal Serial Bus Revision 3.2 Specification + ECNs. https://www.usb.org/document-library/usb-32-specification-released-september-22-2017-and-ecns	3.2 + ECNs 2018-09-12
[USBHID1_11]	USB Device Class Definition for Human Interface Devices (HID). https://www.usb.org/document-library/device-class-definition-hid-111	1.11 2001-06-27
[USBPD3]	USB Power Delivery Specification. https://www.usb.org/document-library/usb-power-delivery	3.0 Version 1.2 + ECNs 2018-12-03
[USBTYPEC]	USB Type-C Specification. https://www.usb.org/document-library/usb-type-cr-cable-and-connector-specification-revision-20	R2.1 2021-05
[xHCI]	Intel eXtensible Host Controller Interface for Universal Serial Bus (xHCI). https://www.intel.com/content/dam/www/public/us/en/documents/technical-specifications/extensible-host-controler-interface-usb-xhci.pdf	1.2 2019-05

2.0 INTRODUCTION

2.1 General Description

The Microchip PCI11101C is a single-chip PCIe switch with an integrated USB 3.2 Gen 2 host controller and programmable I/O. The integrated PCIe physical interfaces provide a 4-lane (4x8 GT/s) upstream port and a 2-lane (2x8GT/s) downstream port. The device is targeted to address customer requests for higher bandwidth PCIe subsystems within embedded applications, with a maximum line rate of 8 GT/s. PCIe upstream can be delivered across a single or multiple lanes to accommodate best system architecture. The PCI11101C includes a compliant PCIe implementation from external facing physical interfaces through to switch fabric and endpoint controllers.

PCIe PTM communicates precise timing information between components for scenarios where the time difference between the PCIe Host clock and the device clock needs to be determined, per PCI Express Base Specification R5.0 V1.0. PTM enables components to calculate the relationship between their local times and a shared, independent time domain called PTM Master Time.

The PCI11101C includes a USB-IF and xHCI compliant USB 3.2 Gen 2 host controller with one USB 3.2 Gen 2 port. USB 3.2 Gen 2 10 Gbps support is provided for USB Type-A/C, M.2 breakout, or embedded connections. Overcurrent Sense (OCS) and Port Control are provided for control of Vbus.

A programmable pin multiplexer is used to map I/O functions to package pins. This enables designers to work with either a default configuration or modify signals to best fit their application. Example signals include those associated with USB operation, through to GPIO or SMBus, which are accessed via a dedicated PCIe Endpoint Controller.

Though many clocks are required for PCI11101C operation, these are generated within an integrated clock farm. Only a single-ended 25 MHz clock or crystal is required externally together with a PCIe reference clock.

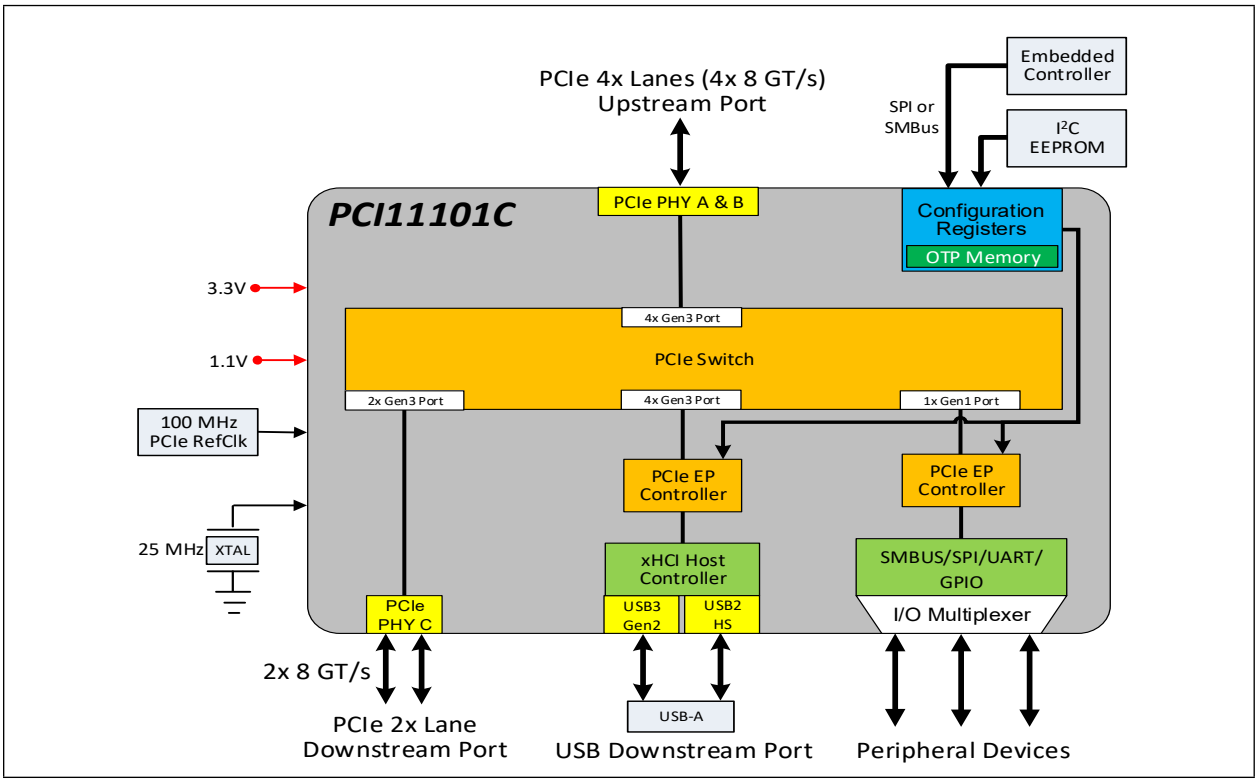
PCI11101C software presentation is enabled using standard abstractions to major operating systems.

The PCI11101C is available in a 132-pin VQFN-DR package in commercial (0°C to +70°C), industrial (-40°C to +85°C), or automotive Grade 3 (-40°C to +85°C) temperature ranges.

Note: This document is for PCI11101C silicon revision C0 or newer only. For information on older PCI11101 silicon revisions A0 or B0, contact your Microchip sales representative.

An internal block diagram of the PCI11101C is shown in Figure 2-1.

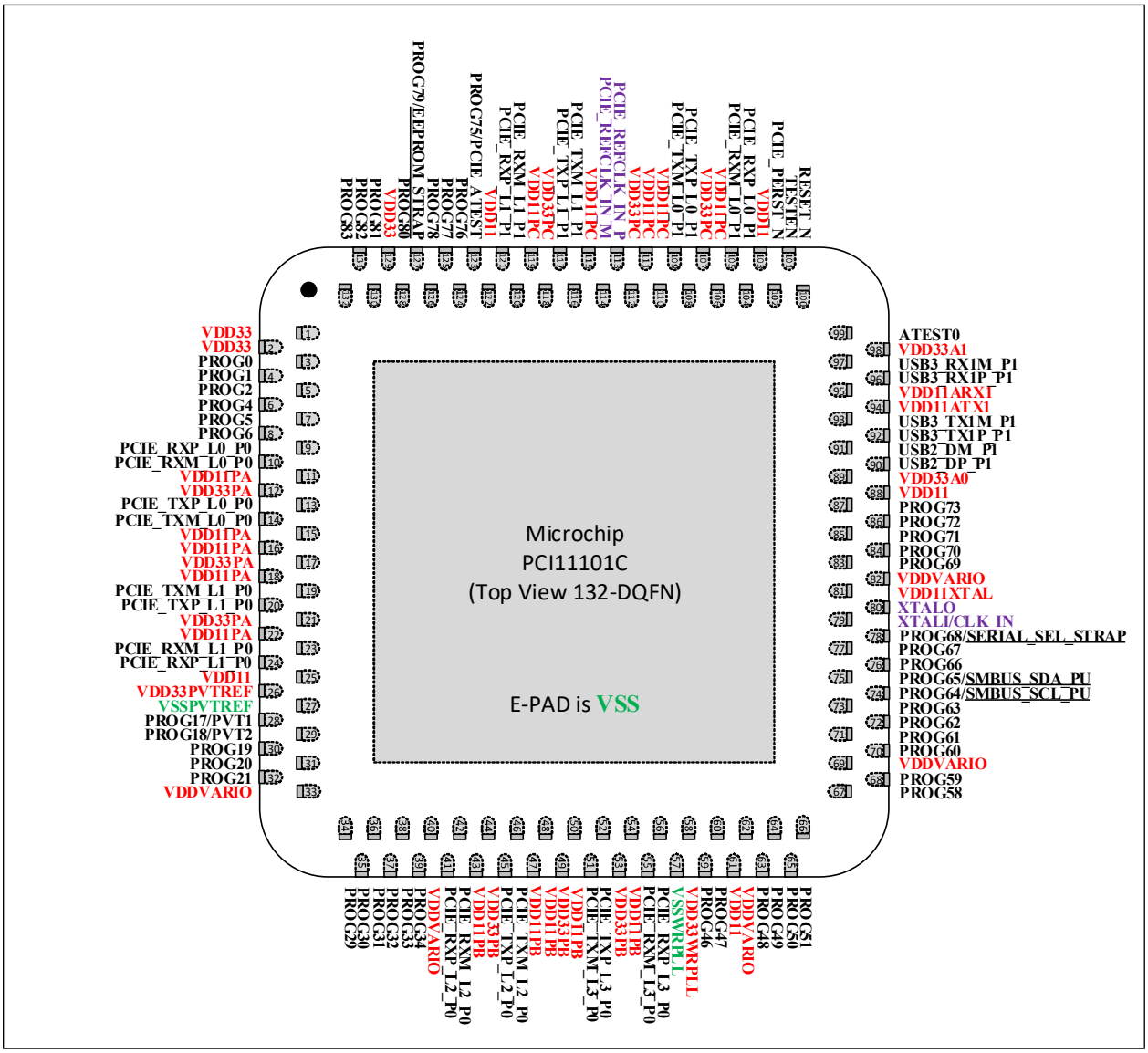
FIGURE 2-1: INTERNAL BLOCK DIAGRAM



3.0 PIN DESCRIPTIONS AND CONFIGURATION

The device pin diagram for the PCI11101C can be seen in Figure 3-1. Table 3-1 provides a PCI11101C pin assignments table with reset states. Pin descriptions are detailed in Section 3.1, "Pin Descriptions". Configuration strap descriptions are detailed in Section 3.2, "Configuration Straps". Programmable function pin descriptions are detailed in Section 3.3, "Programmable Function Pins". Buffer type and pin reset state definitions are provided in Section 1.2, "Buffer Types" and Section 1.3, "Pin Reset States", respectively.

FIGURE 3-1: PIN ASSIGNMENTS



Note: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load.

TABLE 3-1: PIN ASSIGNMENTS

Pin	Pin Name	Reset	Pin	Pin Name	Reset
1	VDD33	P	67	PROG58	Z
2	VDD33	P	68	PROG59	Z
3	PROG0	Z	69	VDDVARIO	P
4	PROG1	Z	70	PROG60	Z
5	PROG2	Z	71	PROG61	Z
6	PROG4	Z	72	PROG62	Z
7	PROG5	Z	73	PROG63	Z
8	PROG6	Z	74	PROG64/SMBUS_SCL_PU	Z
9	PCIE_RXP_L0_P0	Z	75	PROG65/SMBUS_SDA_PU	Z
10	PCIE_RXM_L0_P0	Z	76	PROG66	Z
11	VDD11PA	P	77	PROG67	Z
12	VDD33PA	P	78	PROG68/SERIAL_SEL_STRAP	Z
13	PCIE_TXP_L0_P0	Z	79	XTALI/CLK_IN	AI
14	PCIE_TXM_L0_P0	Z	80	XTALO	AO
15	VDD11PA	P	81	VDD11XTAL	P
16	VDD11PA	P	82	VDDVARIO	P
17	VDD33PA	P	83	PROG69	Z
18	VDD11PA	P	84	PROG70	Z
19	PCIE_TXM_L1_P0	Z	85	PROG71	Z
20	PCIE_TXP_L1_P0	Z	86	PROG72	Z
21	VDD33PA	P	87	PROG73	Z
22	VDD11PA	P	88	VDD11	P
23	PCIE_RXM_L1_P0	Z	89	VDD33A0	P
24	PCIE_RXP_L1_P0	Z	90	USB2_DP_P1	Z
25	VDD11	P	91	USB2_DM_P1	Z
26	VDD33PVTREF	P	92	USB3_TX1P_P1	Z
27	VSSPVTREF	P	93	USB3_TX1M_P1	Z
28	PROG17/PVT1	Z	94	VDD11ATX1	P
29	PROG18/PVT2	Z	95	VDD11ARX1	P
30	PROG19	Z	96	USB3_RX1P_P1	Z
31	PROG20	Z	97	USB3_RX1M_P1	Z
32	PROG21	Z	98	VDD11A1	P
33	VDDVARIO	P	99	ATEST0	Z
34	PROG29	Z	100	RESET_N	Z/Y
35	PROG30	Z	101	TESTEN	PD
36	PROG31	Z	102	PCIE_PERST_N	Z
37	PROG32	Z	103	VDD11	P

TABLE 3-1: PIN ASSIGNMENTS (CONTINUED)

Pin	Pin Name	Reset	Pin	Pin Name	Reset
38	PROG33	Z	104	PCIE_RXP_L0_P1	Z
39	PROG34	Z	105	PCIE_RXM_L0_P1	Z
40	VDDVARIO	P	106	VDD11PC	P
41	PCIE_RXP_L2_P0	Z	107	VDD33PC	P
42	PCIE_RXM_L2_P0	Z	108	PCIE_TXP_L0_P1	Z
43	VDD11PB	P	109	PCIE_TXM_L0_P1	Z
44	VDD33PB	P	110	VDD11PC	P
45	PCIE_TXP_L2_P0	Z	111	VDD11PC	P
46	PCIE_TXM_L2_P0	Z	112	VDD33PC	P
47	VDD11PB	P	113	PCIE_REFCLK_IN_P	Z
48	VDD11PB	P	114	PCIE_REFCLK_IN_M	Z
49	VDD33PB	P	115	VDD11PC	P
50	VDD11PB	P	116	PCIE_TXM_L1_P1	Z
51	PCIE_TXM_L3_P0	Z	117	PCIE_TXP_L1_P1	Z
52	PCIE_TXP_L3_P0	Z	118	VDD33PC	P
53	VDD33PB	P	119	VDD11PC	P
54	VDD11PB	P	120	PCIE_RXM_L1_P1	Z
55	PCIE_RXM_L3_P0	Z	121	PCIE_RXP_L1_P1	Z
56	PCIE_RXP_L3_P0	Z	122	VDD11	P
57	VSSWRPLL	P	123	PROG75	Z
58	VDD33WRPLL	P	124	PROG76	Z
59	PROG46	Z	125	PROG77	Z
60	PROG47	Z	126	PROG78	Z
61	VDD11	P	127	PROG79/EEPROM_STRAP	Z
62	VDDVARIO	P	128	PROG80	Z
63	PROG48	Z	129	VDD33	P
64	PROG49	Z	130	PROG81	Z
65	PROG50	Z	131	PROG82	Z
66	PROG51	Z	132	PROG83	Z
Exposed Pad (VSS) must be connected to ground.					

3.1 Pin Descriptions

TABLE 3-2: PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
USB 3.2 Data Interface Pins			
USB 3.2 Port 1 TX1+	**USB3_TX1P_P1**	I/O-U	USB 3.2 Port 1 TX1+
USB 3.2 Port 1 TX1-	**USB3_TX1M_P1**	I/O-U	USB 3.2 Port 1 TX1-
USB 3.2 Port 1 RX1+	**USB3_RX1P_P1**	I/O-U	USB 3.2 Port 1 RX1+
USB 3.2 Port 1 RX1-	**USB3_RX1M_P1**	I/O-U	USB 3.2 Port 1 RX1-
USB 2.0 Data Interface Pins			
USB 2.0 Port 1 D+	**USB2_DP_P1**	I/O-U	USB 2.0 Port 1 D+
USB 2.0 Port 1 D-	**USB2_DM_P1**	I/O-U	USB 2.0 Port 1 D-
PCIe Common Pins			
PCIe REFCLK+ Input	**PCIE_REFCLK_IN_P**	LVDS	Common PCIe REFCLK+ input from host
PCIe REFCLK- Input	**PCIE_REFCLK_IN_M**	LVDS	Common PCIe REFCLK- input from host
PCIe Reset# Input	**PCIE_PERST_N**	IS	Power and Clock Good Indication The PERST# signal indicated that both PCIe power and clock are available. This active low signal is used by the system to reset the chip. The active low pulse should be at least 1 µs wide. **Note:** When the device is powered down, this pin is isolated from the PCIe bus and does not present any significant loading or provide any drive.
PCIe Port 0 (Upstream) Pins			
PCIe TX+ Lane 0 Port 0	**PCIE_TXP_L0_P0**	I/O-P	Upstream PCIe Port 0 Lane 0 TX+
PCIe TX- Lane 0 Port 0	**PCIE_TXM_L0_P0**	I/O-P	Upstream PCIe Port 0 Lane 0 TX-
PCIe RX+ Lane 0 Port 0	**PCIE_RXP_L0_P0**	I/O-P	Upstream PCIe Port 0 Lane 0 RX+
PCIe RX- Lane 0 Port 0	**PCIE_RXM_L0_P0**	I/O-P	Upstream PCIe Port 0 Lane 0 RX-

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
PCIe TX+ Lane 1 Port 0	**PCIE_TXP_L1_P0**	I/O-P	Upstream PCIe Port 0 Lane 1 TX+
PCIe TX- Lane 1 Port 0	**PCIE_TXM_L1_P0**	I/O-P	Upstream PCIe Port 0 Lane 1 TX-
PCIe RX+ Lane 1 Port 0	**PCIE_RXP_L1_P0**	I/O-P	Upstream PCIe Port 0 Lane 1 RX+
PCIe RX- Lane 1 Port 0	**PCIE_RXM_L1_P0**	I/O-P	Upstream PCIe Port 0 Lane 1 RX-
PCIe TX+ Lane 2 Port 0	**PCIE_TXP_L2_P0**	I/O-P	Upstream PCIe Port 0 Lane 2 TX+
PCIe TX- Lane 2 Port 0	**PCIE_TXM_L2_P0**	I/O-P	Upstream PCIe Port 0 Lane 2 TX-
PCIe RX+ Lane 2 Port 0	**PCIE_RXP_L2_P0**	I/O-P	Upstream PCIe Port 0 Lane 2 RX+
PCIe RX- Lane 2 Port 0	**PCIE_RXM_L2_P0**	I/O-P	Upstream PCIe Port 0 Lane 2 RX-
PCIe TX+ Lane 3 Port 0	**PCIE_TXP_L3_P0**	I/O-P	Upstream PCIe Port 0 Lane 3 TX+
PCIe TX- Lane 3 Port 0	**PCIE_TXM_L3_P0**	I/O-P	Upstream PCIe Port 0 Lane 3 TX-
PCIe RX+ Lane 3 Port 0	**PCIE_RXP_L3_P0**	I/O-P	Upstream PCIe Port 0 Lane 3 RX+
PCIe RX- Lane 3 Port 0	**PCIE_RXM_L3_P0**	I/O-P	Upstream PCIe Port 0 Lane 3 RX-
PCIe Port 1 (Downstream) Pins			
PCIe TX+ Lane 0 Port 1	**PCIE_TXP_L0_P1**	I/O-P	Downstream PCIe Port 1 Lane 0 TX+
PCIe TX- Lane 0 Port 1	**PCIE_TXM_L0_P1**	I/O-P	Downstream PCIe Port 1 Lane 0 TX-
PCIe RX+ Lane 0 Port 1	**PCIE_RXP_L0_P1**	I/O-P	Downstream PCIe Port 1 Lane 0 RX+
PCIe RX- Lane 0 Port 1	**PCIE_RXM_L0_P1**	I/O-P	Downstream PCIe Port 1 Lane 0 RX-
PCIe TX+ Lane 1 Port 1	**PCIE_TXP_L1_P1**	I/O-P	Downstream PCIe Port 1 Lane 1 TX+
PCIe TX- Lane 1 Port 1	**PCIE_TXM_L1_P1**	I/O-P	Downstream PCIe Port 1 Lane 1 TX-
PCIe RX+ Lane 1 Port 1	**PCIE_RXP_L1_P1**	I/O-P	Downstream PCIe Port 1 Lane 1 RX+

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
PCIe RX- Lane 1 Port 1	**PCIE_RXM_L1_P1**	I/O-P	Downstream PCIe Port 1 Lane 1 RX-
Programmable Function Pins			
Programmable Pins 0-2	**PROG[0:2]**	IS/O_V10/ OD_V10 DB	Programmable pins 0-2. Refer to Section 3.3, Programmable Function Pins for additional information.
Programmable Pins 4-6	**PROG[4:6]**	IS/O_V10/ OD_V10 DB	Programmable pins 4-6. Refer to Section 3.3, Programmable Function Pins for additional information.
Programmable Pins 17-21	**PROG[17:21]**	VIS/ VO_V10/ VOD_V10 DB	Programmable pins 17-21. Refer to Section 3.3, Programmable Function Pins for additional information.
Programmable Pins 29-34	**PROG[29:34]**	VIS/ VO_V10/ VOD_V10 DB	Programmable pins 29-34. Refer to Section 3.3, Programmable Function Pins for additional information.
Programmable Pins 46-51	**PROG[46:51]**	VIS/ VO_V10/ VOD_V10 DB	Programmable pins 46-51. Refer to Section 3.3, Programmable Function Pins for additional information.
Programmable Pins 58-63	**PROG[58:63]**	VIS/ VO-R_5 DB	Programmable pins 58-63. Refer to Section 3.3, Programmable Function Pins for additional information.
Programmable Pins 64-73	**PROG[64:73]**	VIS/ VO_V10/ VOD_V10 DB	Programmable pins 64-73. Refer to Section 3.3, Programmable Function Pins for additional information.
Programmable Pins 75-83	**PROG[75:83]**	IS/O_V10/ OD_V10 DB	Programmable pins 75-83. Refer to Section 3.3, Programmable Function Pins for additional information.
Miscellaneous Pins			
Reset Input	**RESET_N**	IS	This active low signal is used by the system to reset the chip. The active low pulse should be at least 1 µs wide.
PVT Input 1	**PVT1**	AI	PVT thermal monitor input 1
PVT Input 2	**PVT2**	AI	PVT thermal monitor input 2
25 MHz Crystal/Clock Input	**XTALI/CLK_IN**	ICLK	25 MHz crystal or external clock input. This pin can be connected to one terminal of the crystal. The device may alternatively be driven by a single-ended clock oscillator. When this method is used, **XTALO** should be left unconnected.
25 MHz Crystal Output	**XTALO**	OCLK	25 MHz crystal output.

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Test Enable	**TESTEN**	I	This pin is used to enter test mode (JTAG) and is read during the negation of reset. 1: Test Mode enabled 0: Test Mode disabled **Note:** This pin should be pulled down to ground for normal operation.
Analog Test Point	**ATEST0**	AIO	Analog test point 0. **Note:** This pin should be pulled down to ground for normal operation.
Configuration Strap Pins			
EEPROM Configuration Strap	**EEPROM_STRAP**	I	This configuration strap defines whether a device configuration should be read from EEPROM. See Note 3-1. Refer to Section 3.2, "Configuration Straps" for additional information. **Note:** When enabled, the EEPROM interface must also be enabled via the **PROG*xx*** pins. Refer to Section 3.3, "Programmable Function Pins" for additional information.
Serial Interface Configuration Strap	**SERIAL_SEL_STRAP**	I	This configuration strap defines whether a configuration will be written via a serial interface (SMBus or SPI). See Note 3-1. Refer to Section 3.2, "Configuration Straps" for additional information. **Note:** When enabled, the SMBus or SPI interface must be also enabled via the **PROG*xx*** pins. Refer to Section 3.3, "Programmable Function Pins" for additional information.
SMBus SCL Pull-Up Configuration Strap	**SMBUS_SCL_PU**	I	This configuration strap defines whether an external pull-up on the SCL line is used for normal operation (typically 10 kΩ). When the **SERIAL_SEL_STRAP** is present, this pull-up is used together with the **SMBUS_SDA_PU** to determine whether SMBus or SPI has been configured as the serial configuration mechanism. See Note 3-1. Refer to Section 3.2, "Configuration Straps" for additional information. **Note:** When both **SMBUS_SDA_PU** and **SMBUS_SCL_PU** are present, the SMBus interface must also be enabled via the **PROG*xx*** pins. Otherwise, the SPI interface must be enabled via the **PROG*xx*** pins. Refer to Section 3.3, "Programmable Function Pins" for additional information.

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
SMBus SDA Pull-Up Configuration Strap	**SMBUS_SDA_PU**	I	This configuration strap defines whether an external pull-up on the SDA line is used for normal operation (typically 10 kΩ). When the **SERIAL_SEL_STRAP** is present, this pull-up is used together with the **SMBUS_SCL_PU** to determine whether SMBus or SPI has been configured as the serial configuration mechanism. See Note 3-1. Refer to Section 3.2, "Configuration Straps" for additional information. **Note:** When both **SMBUS_SDA_PU** and **SMBUS_SCL_PU** are present, the SMBus interface must also be enabled via the **PROG*xx*** pins. Otherwise, the SPI interface must be enabled via the **PROG*xx*** pins. Refer to Section 3.3, "Programmable Function Pins" for additional information.
Power/Ground Pins			
+3.3V Power Supply Input	**VDD33**	P	+3.3V power supply input. Provides +3.3V supply to the I/O rail. Connect to an external +3.3V supply. See Note 3-3.
+1.1V Core Supply Input	**VDD11**	P	+1.1V power supply input. Provides +1.1V supply to the core. Connect to an external +1.1V supply. See Note 3-2.
+3.3V USB AFE Power Supply Input 0	**VDD33A0**	P	+3.3V power supply input to USB AFE. Provides +3.3V supply to the USB AFE. Connect to an external +3.3V supply. See Note 3-3.
+3.3V USB AFE Power Supply Input 1	**VDD33A1**	P	+3.3V power supply input to USB AFE. Provides +3.3V supply to the USB AFE. Connect to an external +3.3V supply. See Note 3-3.
+1.1V USB AFE Core Transmit Supply Input 1	**VDD11ATX1**	P	+1.1V power supply input to USB AFE core. Provides +1.1V supply to the USB AFE. Connect to an external +1.1V supply. See Note 3-2.
+1.1V USB AFE Core Receive Supply Input 1	**VDD11ARX1**	P	+1.1V power supply input to USB AFE core. Provides +1.1V supply to the USB AFE. Connect to an external +1.1V supply. See Note 3-2.
+1.8V to +3.3V Variable I/O Supply Input	**VDDVARIO**	P	+1.8V to +3.3V variable I/O supply input. Provides variable +1.8/2.5/3.3V supply to the I/O rail. Connect to an external +1.8/2.5/3.3V supply.
+3.3V Wide-Range PLL Supply Input	**VDD33WRPLL**	P	+3.3V wide-range PLL supply input. Provides +3.3V supply to the wide-range PLL. See Note 3-3.

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Wide-Range PLL Ground	**VSSWRPLL**	P	Wide-Range PLL ground. This is the analog ground reference for the **VDD33WRPLL** power input pin. The **VSSWRPLL** pin must not be connected to any other signals or ground references external to the ASIC.
+1.1V PCIe PHY A Supply Input	**VDD11PA**	P	+1.1V PCIe PHY A supply input. Provides +1.1V supply to PCIe PHY A. See Note 3-2.
+1.1V PCIe PHY B Supply Input	**VDD11PB**	P	+1.1V PCIe PHY B supply input. Provides +1.1V supply to PCIe PHY B. See Note 3-2.
+1.1V PCIe PHY C Supply Input	**VDD11PC**	P	+1.1V PCIe PHY C supply input. Provides +1.1V supply to PCIe PHY C. See Note 3-2.
+3.3V PCIe PHY A Supply Input	**VDD33PA**	P	+3.3V PCIe PHY A supply input. Provides +3.3V supply to PCIe PHY A. See Note 3-3.
+3.3V PCIe PHY B Supply Input	**VDD33PB**	P	+3.3V PCIe PHY B supply input. Provides +3.3V supply to PCIe PHY B. See Note 3-3.
+3.3V PCIe PHY C Supply Input	**VDD33PC**	P	+3.3V PCIe PHY C supply input. Provides +3.3V supply to PCIe PHY C. See Note 3-3.
+3.3V PVT Supply Input	**VDD33PVTREF**	P	+3.3V PVT thermal monitor power supply. See Note 3-3.
PVT Ground	**VSSPVTREF**	P	PVT thermal monitor ground. This is the analog ground reference for the **VDD33PVTREF** power input pin. The **VSSPVTREF** pin must not be connected to any other signals or ground references external to the ASIC.
+1.1V 25 MHz XTAL Clock Supply Input	**VDD11XTAL**	P	+1.1V 25 MHz XTAL clock supply input. See Note 3-2.
25 MHz XTAL Clock Ground	**VSSXTAL**	P	25 MHz XTAL clock ground.
Ground	**VSS**	P	Ground (e-pad).

Note 3-1: Configuration strap values are latched on Power-On Reset (POR) and the rising edge of **RESET_N** (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load.

Note 3-2: All +1.1V power supplies must be powered from a common +1.1V source and cannot be powered separately.

Note 3-3: All +3.3V power supplies must be powered from a common +3.3V source and cannot be powered separately.

3.2 Configuration Straps

Configuration straps are multi-function pins that are used during Power-On Reset (POR) or external chip reset (**RESET_N**) to determine the default configuration of a particular feature. The state of the signal is latched following de-assertion of the reset. Configuration straps are identified by an underlined symbol name. This section details the various device configuration straps.

Note: The system designer must ensure that configuration straps meet the timing requirements specified in the device data sheet. If configuration straps are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

3.2.1 EEPROM CONFIGURATION STRAP (EEPROM_STRAP)

The **EEPROM_STRAP** configuration strap is used to define whether a device configuration should be read from EEPROM.

Note: When enabled, the EEPROM interface must also be enabled via the **PROG*xx*** pins.

3.2.2 SERIAL CONFIGURATION STRAP (SERIAL_SEL_STRAP)

The **SERIAL_SEL_STRAP** configuration strap is used to define whether a configuration will be written via a serial interface (SMBus or SPI).

Note: When enabled, the SMBus or SPI interface must be enabled via the **PROG*xx*** pins.

3.2.3 SMBUS SCL PULL-UP CONFIGURATION STRAP (SMBUS_SCL_PU)

The **SMBUS_SCL_PU** configuration strap is used to define whether an external pull-up on the SCL line is used for normal operation (typically 10 kΩ). When the **SERIAL_SEL_STRAP** is present, this pull-up is used together with the **SMBUS_SDA_PU** to determine whether SMBus or SPI has been configured as the serial configuration mechanism.

Note: When both **SMBUS_SDA_PU** and **SMBUS_SCL_PU** are present, the SMBus interface must also be enabled via the **PROG*xx*** pins. Otherwise, the SPI interface must be enabled via the **PROG*xx*** pins.

3.2.4 SMBUS SDA PULL-UP CONFIGURATION STRAP (SMBUS_SDA_PU)

The **SMBUS_SDA_PU** configuration strap is used to define whether an external pull-up on the SDA line is used for normal operation (typically 10 kΩ). When the **SERIAL_SEL_STRAP** is present, this pull-up is used together with the **SMBUS_SCL_PU** to determine whether SMBus or SPI has been configured as the serial configuration mechanism.

Note: When both **SMBUS_SDA_PU** and **SMBUS_SCL_PU** are present, the SMBus interface must also be enabled via the **PROG*xx*** pins. Otherwise, the SPI interface must be enabled via the **PROG*xx*** pins.

3.3 Programmable Function Pins

The PCI11101C provides 48 individually programmable function pins **PROG*x***. Each **PROG*x*** pin can be configured in firmware to 15 different functions. When the system is in reset, the pins revert to func0 until the device configuration is completed. Table 3-3 provides a list of default and typical values for each **PROG*x*** pin. The programmable function definitions are detailed in Table 3-5.PCI11101C

Note: The buffer type of a given programmable function depends on which programmable pin the function has been selected on. The buffer type will be the same as that of the associated **PROG*x*** pin, as defined in Table 3-2.

TABLE 3-3: PROGRAMMABLE PIN VOLTAGE DOMAIN AND DEFAULT/TYPICAL FUNCTION VALUES

Pin	Voltage I/O Domain	Default Function	Typical Application Function
PROG0	VDD33	GPIO0	EE_CTLR_SCL
PROG1	VDD33	GPIO1	EE_CTLR_SDA
PROG2	VDD33	GPIO2	GPIO2
PROG4	VDD33	PCIE_CLKREQ0_N	PCIE_CLKREQ0_N
PROG5	VDD33	PCIE_WAKE_N	PCIE_WAKE_N
PROG6	VDD33	VAUX_DET	VAUX_DET
PROG17 (Note 3-4)	VDDVARIO	GPIO17 (Note 3-4)	GPIO17
PROG18 (Note 3-4)	VDDVARIO	GPIO18 (Note 3-4)	GPIO18
PROG19	VDDVARIO	GPIO19	GPIO19
PROG20	VDDVARIO	GPIO20	GPIO20
PROG21	VDDVARIO	GPIO21	GPIO21
PROG29	VDDVARIO	GPIO29	GPIO29
PROG30	VDDVARIO	GPIO30	GPIO30
PROG31	VDDVARIO	GPIO31	GPIO31
PROG32	VDDVARIO	GPIO32	SMBUS_CTLR_SCL
PROG33	VDDVARIO	GPIO33	SMBUS_CTLR_SDA
PROG34	VDDVARIO	GPIO34	SMBUS_CTLR_ALERT_N
PROG46	VDDVARIO	GPIO46	GPIO46
PROG47	VDDVARIO	GPIO47	GPIO47
PROG48	VDDVARIO	GPIO48	GPIO48
PROG49	VDDVARIO	GPIO49	GPIO49
PROG50	VDDVARIO	GPIO50	GPIO50
PROG51	VDDVARIO	GPIO51	GPIO51
PROG58	VDDVARIO	GPIO58	GPIO58
PROG59	VDDVARIO	GPIO59	GPIO59
PROG60	VDDVARIO	GPIO60	GPIO60
PROG61	VDDVARIO	GPIO61	GPIO61
PROG62	VDDVARIO	GPIO62	GPIO62
PROG63	VDDVARIO	GPIO63	GPIO63
PROG64	VDDVARIO	GPIO64	GPIO64
PROG65	VDDVARIO	GPIO65	GPIO65
PROG66	VDDVARIO	GPIO66	GPIO66

TABLE 3-3: PROGRAMMABLE PIN VOLTAGE DOMAIN AND DEFAULT/TYPICAL FUNCTION VALUES (CONTINUED)

Pin	Voltage I/O Domain	Default Function	Typical Application Function
PROG67	VDDVARIO	GPIO67	GPIO67
PROG68	VDDVARIO	GPIO68	GPIO68
PROG69	VDDVARIO	UART0_TXD	GPIO69
PROG70	VDDVARIO	UART0_RXD	GPIO70
PROG71	VDDVARIO	UART0_CTS_N	GPIO71
PROG72	VDDVARIO	UART0_RTS_N	GPIO72
PROG73	VDDVARIO	GPIO73	GPIO73
PROG75	VDD33	GPIO75	GPIO75
PROG76	VDD33	GPIO76	GPIO76
PROG77	VDD33	GPIO77	GPIO77
PROG78	VDD33	GPIO78	GPIO78
PROG79	VDD33	GPIO79	GPIO79
PROG80	VDD33	GPIO80	GPIO80
PROG81	VDD33	GPIO81	GPIO81
PROG82	VDD33	GPIO82	GPIO82
PROG83	VDD33	GPIO83	GPIO83

Note 3-4: In order to use the PVT functions PVT1 and PVT2, shared on the **PROG17** and **PROG18** pins respectively, GPIO functions must be selected on **PROG17** and **PROG18** with the GPIOs disabled, which ensures that they are tri-stated.

TABLE 3-4: M.2 INTERFACE FUNCTIONS (VDD33 = 3.3V, VDDVARIO = 1.8V)

	Pin	M.2 Key A	M.2 Key B	M.2 Key C	M.2 Key E	M.2 Key A+E	M.2 Key M
3.3V I/O	PROG0	EE_CTLR_SCL	EE_CTLR_SCL	EE_CTLR_SCL	EE_CTLR_SCL	EE_CTLR_SCL	EE_CTLR_SCL
	PROG1	EE_CTLR_SDA	EE_CTLR_SDA	EE_CTLR_SDA	EE_CTLR_SDA	EE_CTLR_SDA	EE_CTLR_SDA
	PROG2	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
	PROG4	PCIE_CLKREQ0_N	PCIE_CLKREQ0_N	PCIE_CLKREQ0_N	PCIE_CLKREQ0_N	PCIE_CLKREQ0_N	PCIE_CLKREQ0_N
	PROG5	PCIE_WAKE_N	PCIE_WAKE_N	PCIE_WAKE_N	PCIE_WAKE_N	PCIE_WAKE_N	PCIE_WAKE_N
	PROG6	VAUX_DET	VAUX_DET	VAUX_DET	VAUX_DET	VAUX_DET	VAUX_DET
1.8V I/O	PROG17	GPIO	GPIO	GPIO (GPIO_0)	GPIO	GPIO	GPIO
	PROG18	GPIO	GPIO	GPIO (GPIO_1)	GPIO	GPIO	GPIO
	PROG19	GPIO	GPIO	GPIO (GPIO_2)	GPIO	GPIO	GPIO
	PROG20	GPIO	GPIO	GPIO (GPIO_3)	GPIO	GPIO	GPIO
	PROG21	GPIO	GPIO	GPIO (VENDOR_PORT_A_0)	GPIO	GPIO	GPIO
	PROG29	GPIO	GPIO	GPIO (VENDOR_PORT_A_1)	GPIO (Vendor Defined)	GPIO	GPIO
	PROG30	GPIO	GPIO	GPIO (VENDOR_PORT_A_2)	GPIO (Vendor Defined)	GPIO	GPIO
	PROG31	GPIO	GPIO	GPIO (VENDOR_PORT_A_3)	GPIO (Vendor Defined)	GPIO	GPIO
	PROG32	SMBUS_CTLR_SCL	GPIO (GPIO_0 [SMBUS_CTLR_SCL])	GPIO (VENDOR_PORT_B_0 [SMBUS_CTLR_SCL])	SMBUS_CTLR_SCL	SMBUS_CTLR_SCL	SMBUS_CTLR_SCL
	PROG33	SMBUS_CTLR_SDA	GPIO (GPIO_1 [SMBUS_CTLR_SDA])	GPIO (VENDOR_PORT_B_1 [SMBUS_CTLR_SDA])	SMBUS_CTLR_SDA	SMBUS_CTLR_SDA	SMBUS_CTLR_SDA
	PROG34	SMBUS_CTLR_ALERT_N	GPIO (GPIO_2 [SMBUS_CTLR_ALERT#])	GPIO (VENDOR_PORT_B_2 [SMBUS_CTLR_ALERT#])	SMBUS_CTLR_ALERT_N	SMBUS_CTLR_ALERT_N	SMBUS_CTLR_ALERT_N
	PROG46	GPIO	GPIO (GPIO_3)	GPIO (VENDOR_PORT_B_3)	GPIO	GPIO	GPIO
	PROG47	GPIO	GPIO (GPIO_4)	GPIO (VENDOR_PORT_B_4)	GPIO	GPIO	GPIO
	PROG48	GPIO	GPIO (GPIO_5)	GPIO (VENDOR_PORT_B_5)	GPIO	GPIO	GPIO
	PROG49	GPIO	GPIO (GPIO_6)	GPIO (VENDOR_PORT_C_0)	GPIO	GPIO	GPIO
	PROG50	GPIO	GPIO (GPIO_7)	GPIO (VENDOR_PORT_C_1)	GPIO	GPIO	GPIO
	PROG51	GPIO	GPIO (GPIO_8)	GPIO (RESET#)	GPIO	GPIO	GPIO
	PROG58	GPIO	GPIO (GPIO_9)	GPIO (FULL_CARD_POWER_OFF#)	GPIO	GPIO	GPIO
	PROG59	GPIO	GPIO (GPIO_10)	GPIO (VENDOR_PORT_C_2)	GPIO	GPIO	GPIO
	PROG60	GPIO	GPIO (GPIO_11)	GPIO (VENDOR_PORT_C_3)	GPIO	GPIO	GPIO
	PROG61	GPIO	GPIO (W_DISABLE2#)	GPIO (PERST#)	GPIO	GPIO	GPIO
	PROG62	GPIO	GPIO (FULL_CARD_POWER_OFF#)	GPIO	GPIO	GPIO	GPIO
	PROG63	GPIO	GPIO (WAKE_ON_WAN#)	GPIO	GPIO	GPIO	GPIO
	PROG64	SMBUS_TGT_SCL	SMBUS_TGT_SCL	SMBUS_TGT_SCL	SMBUS_TGT_SCL	SMBUS_TGT_SCL	SMBUS_TGT_SCL
	PROG65	SMBUS_TGT_SDA	SMBUS_TGT_SDA	SMBUS_TGT_SDA	SMBUS_TGT_SDA	SMBUS_TGT_SDA	SMBUS_TGT_SDA
	PROG66	SMBUS_TGT_ALERT#	SMBUS_TGT_ALERT#	SMBUS_TGT_ALERT#	SMBUS_TGT_ALERT#	SMBUS_TGT_ALERT#	SMBUS_TGT_ALERT#
	PROG67	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
	PROG68	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
	PROG69	GPIO	GPIO (ANTCTL0)	UART0_TXD	UART0_TXD	GPIO	GPIO
	PROG70	GPIO	GPIO (ANTCTL1)	UART0_RXD	UART0_RXD	GPIO	GPIO
	PROG71	GPIO	GPIO (ANTCTL2)	UART0_CTS_N	UART0_CTS_N	GPIO	GPIO
	PROG72	GPIO	GPIO (ANTCTL3)	UART0_RTS_N	UART0_RTS_N	GPIO	GPIO
	PROG73	GPIO	GPIO (RESET#)	GPIO	GPIO	GPIO	GPIO

TABLE 3-4: M.2 INTERFACE FUNCTIONS (VDD33 = 3.3V, VDDVARIO = 1.8V) (CONTINUED)

	Pin	M.2 Key A	M.2 Key B	M.2 Key C	M.2 Key E	M.2 Key A+E	M.2 Key M
3.3V I/O	PROG75	GPIO (W_DISABLE1#)	GPIO (W_DISABLE1#)	GPIO	GPIO (W_DISABLE1#)	GPIO (W_DISABLE1#)	GPIO
	PROG76	GPIO (W_DISABLE2#)	GPIO (GPIO_9/DAS/DSS/ LED_1#)	GPIO	GPIO (W_DISABLE2#)	GPIO (W_DISABLE2#)	GPIO
	PROG77	GPIO (PERST#)	GPIO (PERST#)	GPIO	GPIO (PERST#)	GPIO (PERST#)	GPIO
	PROG78	GPIO	GPIO (PEWAKE#)	GPIO	UART0_WAKE_N	GPIO	GPIO
	PROG79	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
	PROG80	GPIO (Vendor Defined)	GPIO (CONFIG_0)	GPIO	GPIO (Vendor Defined)	GPIO	GPIO
	PROG81	GPIO (Vendor Defined)	GPIO (CONFIG_1)	GPIO	GPIO (Vendor Defined)	GPIO	GPIO
	PROG82	GPIO (Vendor Defined)	GPIO (CONFIG_2)	GPIO	GPIO (Vendor Defined)	GPIO	GPIO
	PROG83	GPIO	GPIO (CONFIG_3)	GPIO	GPIO	GPIO	GPIO

Note 3-5: Although listed in the map, this specific function is disabled in the device.

TABLE 3-5: PROGRAMMABLE FUNCTIONS DESCRIPTIONS

Programmable Function	Description
USB Port Control Functions	
VB_PRT_CTL_P1/ VB_OCS_P1	VBUS Port Control/OCS Port 1 Active high control signal to enable VBUS power to the downstream Port 1: **1:** Enable VBUS power and disable VBUS discharge **0:** Disable VBUS power and enable VBUS discharge **Note:** This pin also serves as the overcurrent sense for Port 1.
VB_PRT_CTL_P2/ VB_OCS_P2	VBUS Port Control/OCS Port 2 Active high control signal to enable VBUS power to the downstream Port 2: **1:** Enable VBUS power and disable VBUS discharge **0:** Disable VBUS power and enable VBUS discharge **Note:** This pin also serves as the overcurrent sense for Port 2.
VB_PRT_CTL_P3/ VB_OCS_P3	VBUS Port Control/OCS Port 3 Active high control signal to enable VBUS power to the downstream Port 3: **1:** Enable VBUS power and disable VBUS discharge **0:** Disable VBUS power and enable VBUS discharge **Note:** This pin also serves as the overcurrent sense for Port 3.
VB_PRT_CTL_P4/ VB_OCS_P4	VBUS Port Control/OCS Port 4 Active high control signal to enable VBUS power to the downstream Port 4: **1:** Enable VBUS power and disable VBUS discharge **0:** Disable VBUS power and enable VBUS discharge **Note:** This pin also serves as the overcurrent sense for Port 4.
VCONN1_EN_P1	CC1 Port 1 VCONN enable signal to external FET
VCONN1_EN_P2	CC1 Port 2 VCONN enable signal to external FET
VCONN2_EN_P1	CC2 Port 1 VCONN enable signal to external FET
VCONN2_EN_P2	CC2 Port 2 VCONN enable signal to external FET
VBUS_DIS_P1	Port 1 VBUS discharge signal to external FET
VBUS_DIS_P2	Port 2 VBUS discharge signal to external FET
CC_ATTACH_P1	Port 1 USB Type-C CC attach signal output
CC_ATTACH_P2	Port 2 USB Type-C CC attach signal output
CC_ORIENT_P1	Port 1 USB Type-C orientation signal output
CC_ORIENT_P2	Port 2 USB Type-C orientation signal output

TABLE 3-5: PROGRAMMABLE FUNCTIONS DESCRIPTIONS (CONTINUED)

Programmable Function	Description
PCIe Functions	
PCIE_WAKE_N	Common PCIe Wake This signal is driven low when the device detects a wakeup. In OBFF mode, OBFF events are signaled using the WAKE# pin as an input. **Note:** When the device is powered down, these pins are isolated from the PCIe bus and do not present any significant loading or provide any drive. **Note:** Open drain pin; requires an external pull-up.
VAUX_DET	Auxiliary voltage detection The VAUX_DET is used to indicate when PME from D3cold is supported. When tied to VSS, PME from D3cold is not supported. The weak pull-down will create a logic low when plugged into a system board that does not support the delivery of the auxiliary voltage (the auxiliary voltage connection is floating). When the device is powered exclusively from auxiliary voltage, this is tied to the auxiliary voltage (3.3V) to indicate PME from D3cold is supported. When the device is powered from a multiplexed main voltage/auxiliary voltage, this is tied to the auxiliary voltage (3.3V) to indicate PME from D3cold is supported and to monitor presence of the auxiliary voltage. **Note:** This function enables an internal pull-down (PD). If alternate usage of this pin is enabled, the pull-down is disabled and the input value of the pin is overridden to a low value. Because this pin is shared with GPIOs, a series resistor is recommended to prevent an accidental conflict with the auxiliary voltage. This resistor must be low enough in value to override the on-chip pull-down.
PCIE_CLKREQ0_N	Port 0 PCIe Clock Request input/output **Note:** When the device is powered down, these pins are isolated from the PCIe bus and do not present any significant loading or provide any drive. **Note:** Open drain pin; requires an external pull-up.
PCIE_CLKREQ1_N	Port 1 PCIe Clock Request input/output **Note:** When the device is powered down, these pins are isolated from the PCIe bus and do not present any significant loading or provide any drive. **Note:** Open drain pin; requires an external pull-up.
SPI Peripheral Interface Functions	
SPI_PERI_CLK	SPI Peripheral Clock This is the SPI clock input from the SPI controller. If the SPI interface is enabled, this pin must be driven low during reset.
SPI_PERI_DO	SPI Peripheral Data Out This is the data out for the SPI port when configured for SPI operation (MISO).

TABLE 3-5: PROGRAMMABLE FUNCTIONS DESCRIPTIONS (CONTINUED)

Programmable Function	Description
SPI_PERI_DI	SPI Peripheral Data In This is the SPI data in to the controller from the SPI controller (MOSI). This pin must have a weak pull-down applied at all times to prevent floating if configured for SPI operation.
SPI_PERI_CE_N	SPI Peripheral Chip Enable This is an active low SPI chip enable input. If the SPI interface is enabled, this pin must be pulled high in power-down states.
SPI_PERI_ALERT_N	SPI Peripheral Alert
SPI Controller Interface 0 Functions	
SPI_CTRL0_CLK	SPI Controller 0 Clock This is the SPI clock output from the SPI controller. If the SPI interface is enabled, this pin must be driven low during reset.
SPI_CTRL0_DO	SPI Controller 0 Data Out This is the data out for the SPI port when configured for SPI operation (MOSI).
SPI_CTRL0_DI	SPI Controller 0 Data In This is the SPI data in to the controller from the SPI controller (MISO). This pin must have a weak pull-down applied at all times to prevent floating if configured for SPI operation.
SPI_CTRL0_CE0_N	SPI Controller 0 Chip Enable 0 This is an active low SPI chip enable output 0. If the SPI interface is enabled, this pin must be pulled high in power-down states.
SPI_CTRL0_CE1_N	SPI Controller 0 Chip Enable 1 This is an active low SPI chip enable output 1. If the SPI interface is enabled, this pin must be pulled high in power-down states.
SPI_CTRL0_CE2_N	SPI Controller 0 Chip Enable 2 This is an active low SPI chip enable output 2. If the SPI interface is enabled, this pin must be pulled high in power-down states.
SPI_CTRL0_CE3_N	SPI Controller 0 Chip Enable 3 This is an active low SPI chip enable output 3. If the SPI interface is enabled, this pin must be pulled high in power-down states.
SPI_CTRL0_CE4_N	SPI Controller 0 Chip Enable 4 This is an active low SPI chip enable output 4. If the SPI interface is enabled, this pin must be pulled high in power-down states.

TABLE 3-5: PROGRAMMABLE FUNCTIONS DESCRIPTIONS (CONTINUED)

Programmable Function	Description
SPI_CTRL0_CE5_N	SPI Controller 0 Chip Enable 5 This is an active low SPI chip enable output 5. If the SPI interface is enabled, this pin must be pulled high in power-down states.
SPI_CTRL0_CE6_N	SPI Controller 0 Chip Enable 6 This is an active low SPI chip enable output 6. If the SPI interface is enabled, this pin must be pulled high in power-down states.
SPI_CTRL0_ALERT_N	SPI Peripheral Alert Active low SPI chip input. This pin enables a Debouncer (DB).
SPI Controller Interface 1 Functions	
SPI_CTRL1_CLK	SPI Controller 1 Clock This is the SPI clock output from the SPI controller. If the SPI interface is enabled, this pin must be driven low during reset.
SPI_CTRL1_DO	SPI Controller 1 Data Out This is the data out for the SPI port when configured for SPI operation (MOSI).
SPI_CTRL1_DI	SPI Controller 1 Data In This is the SPI data in to the controller from the SPI controller (MISO). This pin must have a weak pull-down applied at all times to prevent floating if configured for SPI operation.
SPI_CTRL1_CE0_N	SPI Controller 1 Chip Enable 0 This is an active low SPI chip enable output 0. If the SPI interface is enabled, this pin must be pulled high in power-down states.
SPI_CTRL1_CE1_N	SPI Controller 1 Chip Enable 1 This is an active low SPI chip enable output 1. If the SPI interface is enabled, this pin must be pulled high in power-down states.
SPI_CTRL1_CE2_N	SPI Controller 1 Chip Enable 2 This is an active low SPI chip enable output 2. If the SPI interface is enabled, this pin must be pulled high in power-down states.
SPI_CTRL1_CE3_N	SPI Controller 1 Chip Enable 3 This is an active low SPI chip enable output 3. If the SPI interface is enabled, this pin must be pulled high in power-down states.
SPI_CTRL1_CE4_N	SPI Controller 1 Chip Enable 4 This is an active low SPI chip enable output 4. If the SPI interface is enabled, this pin must be pulled high in power-down states.

TABLE 3-5: PROGRAMMABLE FUNCTIONS DESCRIPTIONS (CONTINUED)

Programmable Function	Description
SPI_CTRL1_CE5_N	SPI Controller 1 Chip Enable 5 This is an active low SPI chip enable output 5. If the SPI interface is enabled, this pin must be pulled high in power-down states.
SPI_CTRL1_CE6_N	SPI Controller 1 Chip Enable 6 This is an active low SPI chip enable output 6. If the SPI interface is enabled, this pin must be pulled high in power-down states.
SPI_CTRL1_ALERT_N	SPI Peripheral Alert Active low SPI chip input. This pin enables a Debouncer (DB).
SMBus Controller Functions	
SMBUS_CTLR_SCL	SMBus Controller 1 MHz Clock
SMBUS_CTLR_SDA	SMBus Controller Data This pin enables an internal pull-down (PD).
SMBUS_CTL-R_ALERT_N	SMBus Controller Alert This pin enables a Debouncer (DB).
SMBus Target Functions	
SMBUS_TGT_SCL	SMBus Target Clock
SMBUS_TGT_SDA	SMBus Target Data This pin enables an internal pull-down (PD).
SMBUS_T-GT_ALERT_N	SMBus Target Alert
UART0 Functions	
UART0_TXD	UART0 Transmit Data
UART0_RXD	UART0 Receive Data
UART0_RTS_N	UART0 Ready To Send
UART0_CTS_N	UART0 Clear To Send
UART0_DTR_N	UART0 Data Terminal Ready
UART0_DSR_N	UART0 Data Set Ready
UART0_DCD_N	UART0 Data Carrier Detect
UART0_RI_N	UART0 Ring Indicator

TABLE 3-5: PROGRAMMABLE FUNCTIONS DESCRIPTIONS (CONTINUED)

Programmable Function	Description
UART0_WAKE_N	UART0 Wake Out-of-band signaling used to wake up the platform. This signal is open drain, active low, and enables a Debouncer (DB). A pull-up is required on the host side (100 kΩ recommended).
UART1 Functions	
UART1_TXD	UART1 Transmit Data
UART1_RXD	UART1 Receive Data
UART1_RTS_N	UART1 Ready To Send
UART1_CTS_N	UART1 Clear To Send
UART1_DTR_N	UART1 Data Terminal Ready
UART1_DSR_N	UART1 Data Set Ready
UART1_DCD_N	UART1 Data Carrier Detect
UART1_RI_N	UART1 Ring Indicator
UART1_WAKE_N	UART1 Wake Out-of-band signaling used to wake up the platform. This signal is open drain, active low, and enables a Debouncer (DB). A pull-up is required on the host side (100 kΩ recommended).
UART2 Functions	
UART2_TXD	UART2 Transmit Data
UART2_RXD	UART2 Receive Data
UART2_RTS_N	UART2 Ready To Send
UART2_CTS_N	UART2 Clear To Send
UART2_DTR_N	UART2 Data Terminal Ready
UART2_DSR_N	UART2 Data Set Ready
UART2_DCD_N	UART2 Data Carrier Detect
UART2_RI_N	UART2 Ring Indicator
UART2_WAKE_N	UART2 Wake Out-of-band signaling used to wake up the platform. This signal is open drain, active low, and enables a Debouncer (DB). A pull-up is required on the host side (100 kΩ recommended).

UART3 Functions	
UART3_TXD	UART3 Transmit Data
UART3_RXD	UART3 Receive Data

TABLE 3-5: PROGRAMMABLE FUNCTIONS DESCRIPTIONS (CONTINUED)

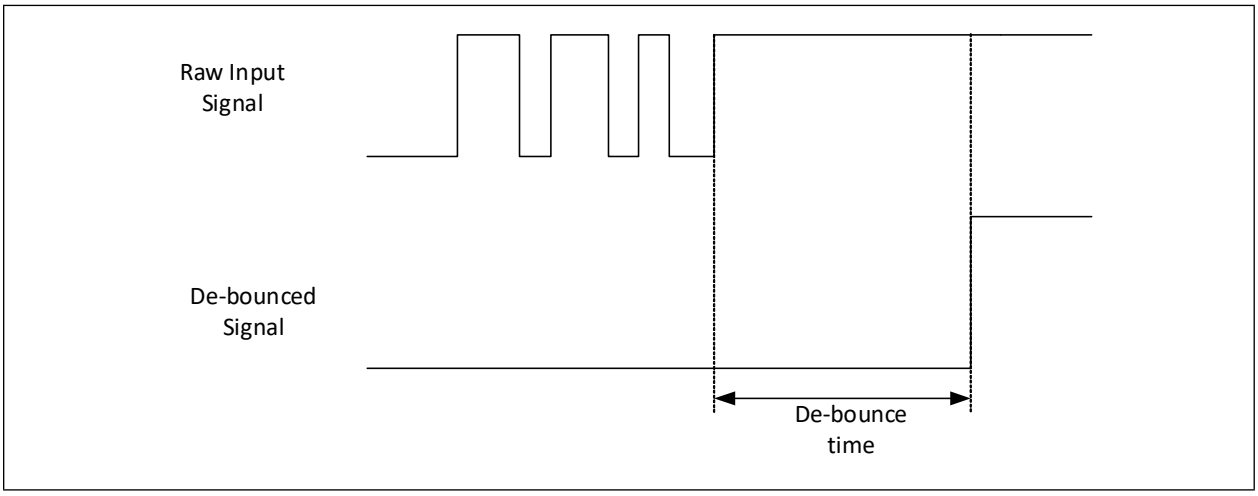
Programmable Function	Description
UART3_RTS_N	UART3 Ready To Send
UART3_CTS_N	UART3 Clear To Send
UART3_DTR_N	UART3 Data Terminal Ready
UART3_DSR_N	UART3 Data Set Ready
UART3_DCD_N	UART3 Data Carrier Detect
UART3_RI_N	UART3 Ring Indicator
UART3_WAKE_N	UART3 Wake Out-of-band signaling used to wake up the platform. This signal is open drain, active low, and enables a Debouncer (DB). A pull-up is required on the host side (100 kΩ recommended).
EEPROM Interface Functions	
EE_CTLR_SCL	1 MHz EEPROM SMBus Controller Clock
EE_CTLR_SDA	1 MHz EEPROM SMBus Controller Data This pin enables an internal pull-down (PD).
General Purpose Input/Output (GPIO) Functions	
GPIO[0:2]	General Purpose Input/Output pins 0-2.
GPIO[4:6]	General Purpose Input/Output pins 4-6.
GPIO[17:21]	General Purpose Input/Output pins 17-21.
GPIO[29:34]	General Purpose Input/Output pins 29-34.
GPIO[46:51]	General Purpose Input/Output pins 46-51.
GPIO[58:73]	General Purpose Input/Output pins 58-73.
GPIO[75:83]	General Purpose Input/Output pins 75-83.

3.4 Debouncers

Some pins have associated Debouncers (indicated by a DB buffer type) which can be enabled or disabled as needed. The pins may be connected to pushbuttons that require debouncing, or they may be connected to digital outputs from other chips which are perfectly clean (and may even be signaling something at a very high rate higher than the minimum period resolution of the debounce timer). Via static (or even dynamic software driven) configuration, the system designer can decide whether a Debouncer is needed and the associated timer value.

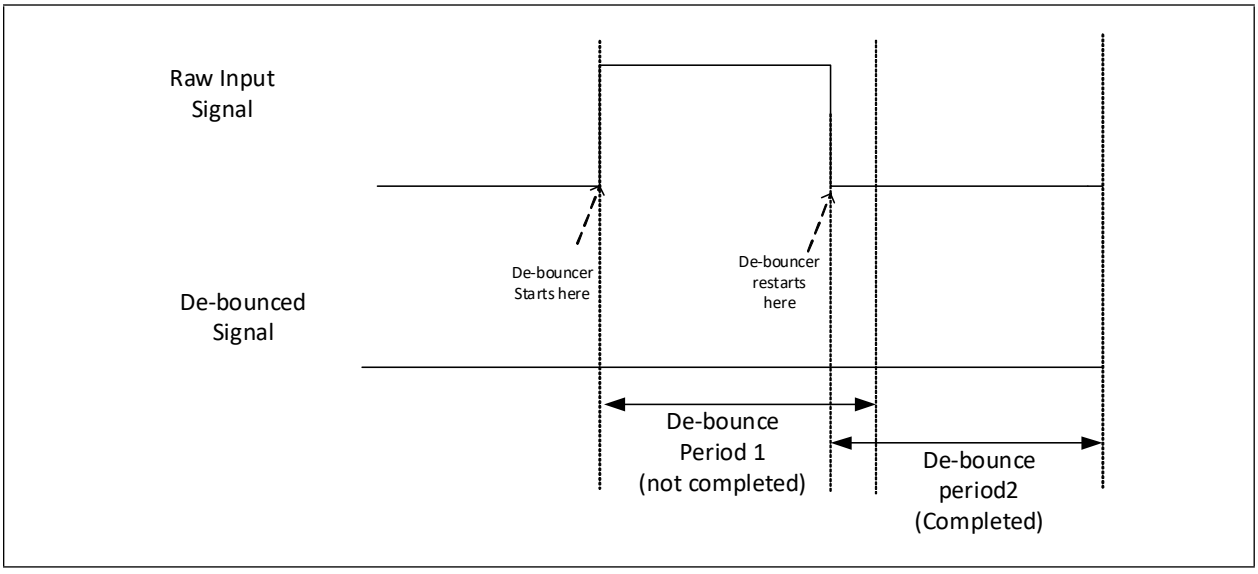
When the Debouncer is disabled, the raw input is used as the pin input. When the Debouncer is enabled, it will start to debounce if there is a change in the value on the pin. The debounce will continue for the specified period of debounce time. Once the debounce is complete, the signal is passed through (see Figure 3-2).

FIGURE 3-2: DEBOUNCED RAW PIN INPUT



If the pin value changes within the debounce time, then the debouncing is restarted for the new input value. This behavior is shown in Figure 3-3.

FIGURE 3-3: DEBOUNCER RESTART



4.0 OPERATIONAL CHARACTERISTICS

4.1 Absolute Maximum Ratings*

+3.3V Supply Voltage (**VDD33**, **VDD33A0**, **VDD33PA**, **VDD33PB**, **VDD33PC**, **VDD33A1**, **VDD33WRPLL**, **VDD33PVTREF**) (Note 4-1) . . . . . -0.5V to +3.63V
+1.8V to +3.3V Variable Supply Voltage (**VDDVARIO**) (Note 4-1) . . . . . -0.5V to +3.63V
+1.1V Supply Voltage (**VDD11**, **VDD11ATX1**, **VDD11ARX1**, **VDD11PA**, **VDD11PB**, **VDD11PC**, **VDD11XTAL**) (Note 4-1) -0.5V to +1.21V
Positive voltage on **PROGx** signal pins, with respect to ground . . . . . +3.63V
Positive voltage on **XTALI/CLK_IN** pins, with respect to ground . . . . . +3.63V
Positive voltage on USB 2.0 DP/DM signal pins, with respect to ground . . . . . +3.63V
Positive voltage on USB 3.0 TX/RX signal pins, with respect to ground. . . . . +1.21V
Positive voltage on PCIe TX/RX signal pins, with respect to ground . . . . . +1.21V
Positive voltage on **PCIE_REFCLK_IN_x** signal pins, with respect to ground. . . . . +2.75V
Negative voltage on input signal pins, with respect to ground . . . . . -0.5V
Storage Temperature . . . . . -55°C to +150°C
Junction Temperature . . . . . +125°C
Lead Temperature Range . . . . . Refer to JEDEC Spec. J-STD-020
HBM ESD Performance (Digital Pins). . . . . 3 kV
HBM ESD Performance (Analog Pins) . . . . . 3 kV

Note 4-1: When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested to use a clamp circuit.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 4.2, "Operating Conditions**" or any other applicable section of this specification is not implied.

4.2 Operating Conditions**

+3.3V Supply Voltage (**VDD33**, **VDD33A0**, **VDD33PA**, **VDD33PB**, **VDD33PC**, **VDD33A1**, **VDD33WRPLL**, **VDD33PVTREF**) . . . . . +2.97V to +3.63V
+3.3V Variable Supply Voltage (**VDDVARIO** @ +3.3V) . . . . . +2.97V to +3.63V
+2.5V Variable Supply Voltage (**VDDVARIO** @ +2.5V) . . . . . +2.25V to +2.75V
+1.8V Variable Supply Voltage (**VDDVARIO** @ +1.8V) . . . . . +1.62V to +1.98V
+1.1V Supply Voltage (**VDD11**, **VDD11ATX1**, **VDD11ARX1**, **VDD11PA**, **VDD11PB**, **VDD11PC**, **VDD11XTAL**) +1.09V to +1.21V
PROG*x* Voltage. . . . . -0.30V to +3.63V
XTALI/CLK_IN Voltage . . . . . -0.30V to +3.63V
USB 2.0 DP/DM Voltage . . . . . 0V to +3.63V
USB 3.0 TX/RX Voltage . . . . . 0V to +1.21V
PCIe TX/RX Voltage . . . . . 0V to +1.21V
PCIE_REFCLK_IN_*x* Voltage . . . . . 0V to +2.75V
Ambient Operating Temperature in Still Air (T_A) . . . . . Note 4-2

Note 4-2: (0°C to +70°C) for commercial version, (-40°C to +85°C) for industrial version, or (-40°C to +85°C) for Automotive Grade 3 version.

**Proper operation of the device is guaranteed only within the ranges specified in this section.

Note: Do not drive input signals without power supplied to the device.

4.3 Power Consumption

TABLE 4-1: DEVICE POWER CONSUMPTION

	Typical Current (mA)	
	+1.1V Supplies	**+3.3 Supplies**
Reset Current	187.2	15.48
Sleep Current	329	42.8
Idle	675	112
USB Active Current		
1 SSP	1040	125
1 SS	987	124
1 HS	810	125
Peripheral Active Current		
1 I^2C Controller with 1 MHz speed	174	35
PCIe Active Current		
4 lane UFP + 1 lane DFP at 8GT/s	746	116
4 lane UFP + 2 lane DFP at 8GT/s	805	132
Maximum Current		
USB 1SSP, 1 UART channel, 1 SPI Controller, 1 I2C Controller, 1 PCIe DFP at 8GT/s	1050	135

Note: All active power data is based the maximum UFP lane width (see PCIe Active Current above).

Note: End system integrators should ensure their power design meets the power consumption requirements for their individual systems maximal use-case by taking power measurements during development.

Note: In the USB Active Current sections of Table 4-1, the various port configurations are indicated via the following acronyms:
HS = Hi-Speed
FS = Full-Speed
SS = Super-Speed (5 Gbps)
SSP = Super-Speed Plus (10 Gbps)

Note 4-3: Analog input/output as defined in the *Universal Serial Bus Revision 3.2/2.0 Specifications* or *USB Type-C Specification*.

4.4 AC Specifications

This section details the various AC timing specifications of the device.

4.4.1 POWER SEQUENCE TIMING

Power supplies must adhere to the following rules:

- All power supplies of the same voltage must be powered up/down together.
- There is no power-up sequencing requirement. However all power supplies must reach operational levels within the time periods specified in Table 4-2.
- There is no power-down sequencing or timing requirement, however the device must not be powered for an extended period of time without all supplies at operational levels.
- Following initial power-on, or if a power supply brownout occurs (i.e., one or more supplies drops below operational limits), a power-on reset must be executed once all power supplies reach operational levels.
- Do not drive input signals without power supplied to the device.

Note:	Violation of these specifications may damage the device.

FIGURE 4-1: POWER SEQUENCE TIMING

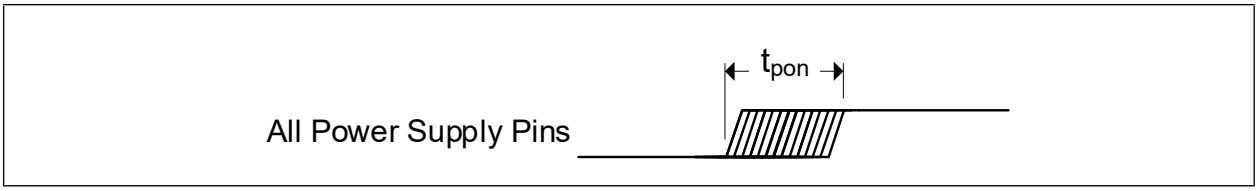


TABLE 4-2: POWER SEQUENCE TIMING

Symbol	Description	Min	Typ	Max	Unit
t_{pon}	Power supply turn-on time	0	—	5	ms

4.4.2 PCIE TIMING

All device PCIe signals (**PCIE_*xx***) conform to the voltage, power, and timing characteristics/specifications as set forth in the *PCI Express Base Specification Revision 3.1a*. Please refer to the *PCI Express Base Specification Revision 3.1a* for additional information.

4.4.3 USB TIMING

4.4.3.1 USB 2.0

All device USB 2.0 signals (**USB2_*xx*** pins) conform to the voltage, power, and timing characteristics/specifications as set forth in the *Universal Serial Bus Revision 2.0 Specification*. Please refer to the *Universal Serial Bus Revision 2.0 Specification* for additional information.

4.4.3.2 USB 3.2

All device USB 3.2 signals (**USB3_*xx*** pins) conform to the voltage, power, and timing characteristics/specifications as set forth in the *Universal Serial Bus Revision 3.2 Specification*. Please refer to the *Universal Serial Bus Revision 3.2 Specification* for additional information.

4.4.4 SMBUS TIMING

All device SMBus signals (**SMBUS_*xx***) conform to the voltage, power, and timing characteristics/specifications as set forth in the *System Management Bus Specification Revision 2.0*. Please refer to the *System Management Bus Specification, Version 2.0* for additional information. Additionally, when operating at 1 MHz, the SMBus signals confirm to the timing characteristics/specifications as set forth in the *System Management Bus Specification Revision 3.0*. Please refer to the *System Management Bus Specification, Version 3.0* for additional information.

4.4.5 UART TIMING

All device UART signals (**UART_*xx***) conform to the timing characteristics/specifications as set forth in the *RS-232, RS-422* and *RS-485* specifications. Please refer to the *RS-232, RS-422* and *RS-485* specifications for additional information.

4.4.6 SPI CONTROLLER TIMING

This section specifies the SPI controller (**SPI_CTRL[0:1]_*xx***) timing requirements for the device. The SPI controllers support operation at 30, 20, 15, 12, 10 or 2 MHz.

FIGURE 4-2: SPI CONTROLLER TIMING

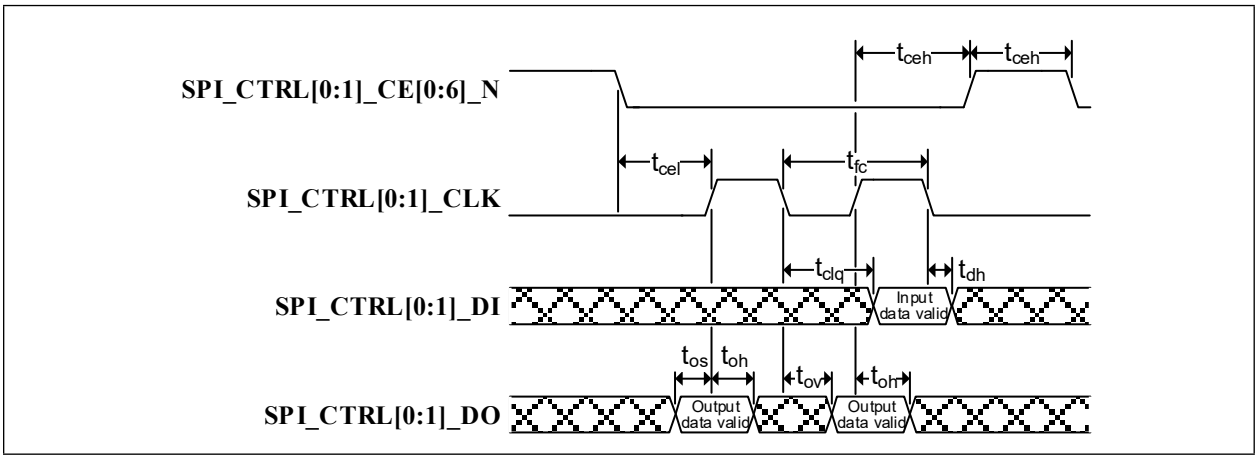


TABLE 4-3: SPI CONTROLLER TIMING

Symbol	Description	Min	Typ	Max	Unit
t_{fc}	Clock frequency	—	—	Note 4-4	MHz
t_{ceh}	Chip enable (**SPI_CTRL[0:1]_CE[0:6]_N**) high time	100	—	—	ns
t_{clq}	Clock to input data	—	—	13	ns
t_{dh}	Input data hold time	0	—	—	ns
t_{os}	Output setup time	5	—	—	ns
t_{oh}	Output hold time	5	—	—	ns
t_{ov}	Clock to output valid	4	—	—	ns
t_{cel}	Chip enable (**SPI_CTRL[0:1]_CE[0:6]_N**) low to first clock	12	—	—	ns
t_{ceh}	Last clock to chip enable (**SPI_CTRL[0:1]_CE[0:6]_N**) high	12	—	—	ns

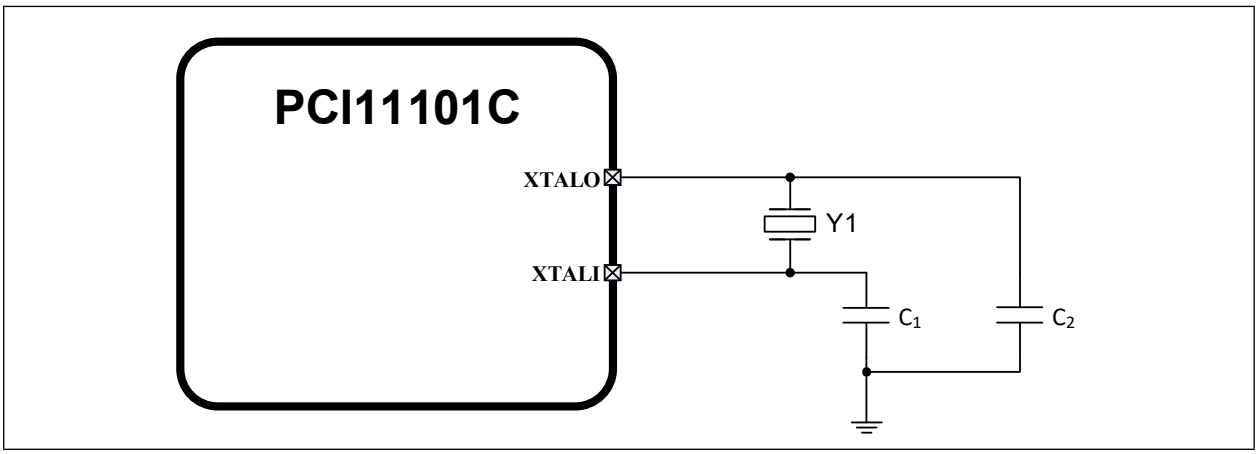
Note 4-4: 30, 20, 15, 12, 10 or 2 MHz, depending on the mode of operation.

4.5 Clock Specifications

The device can accept either a 25 MHz crystal or a 25 MHz single-ended clock oscillator input. If the single-ended clock oscillator method is implemented, **XTALO** should be left unconnected and **XTALI/CLK_IN** should be driven with a nominal 0-3.3V clock signal. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (**XTALI/XTALO**). The following circuit design (Figure 4-3) is required to ensure proper operation.

FIGURE 4-3: 25 MHZ CRYSTAL CIRCUIT



4.5.1 EXTERNAL REFERENCE CLOCK (CLK_IN)

When using an external reference clock, the following clock characteristics are required:

- 25 MHz
- 50% duty cycle ±10%, 25 MHz ±300 ppm
- Jitter < 100 ps pk-pk

4.5.1.1 TX Ref Clocks

The TXREFCLKP/N is an LVDS-based receiver, operating in a VDDHV (2.5V...3.3V) domain.

It has a built in, trimmable 100Ω termination, but does not include any common-mode VCM generation, so it's suitable for DC-coupling. In the case of AC-coupling you will have to add resistors on the board to set the proper VCM outside of the chip.

This receiver can operate with the VCM ranging from 0.2V to (VDDHV-0.2V), with at least 100 mVpp of input swing, regardless of AC vs DC coupling. There is no maximum swing specification, but the pins should not exceed the VDDDHV level by more than 300 mV, to avoid leakage through ESD up diodes.

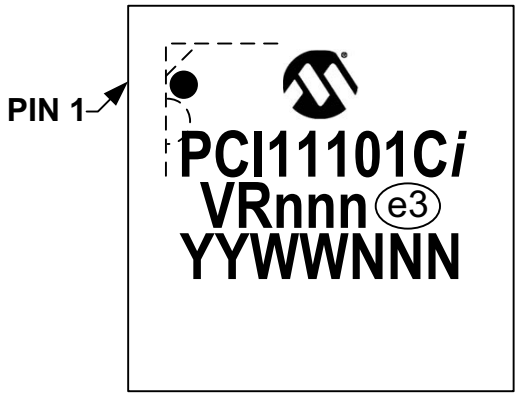
If the host/clock generator output is in HCSL format, then the clock does not need any LVDS conversion or common mode biasing using a resistor; you can directly connect the HCSL clock source to the **REFCLK** pin.

This LVDS RX does not have a build in hysteresis.

5.0 PACKAGE INFORMATION

5.1 Package Marking Information

132-VQFN-DR (11x11 mm)



Legend:	*i*	Temperature range designator (Blank = Commercial, *i* = Industrial/Automotive Grade 3)
	V	Automotive designator (Blank = Commercial/Industrial, V = Automotive)
	R	Product revision
	nnn	Internal code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	YY	Year code (last two digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

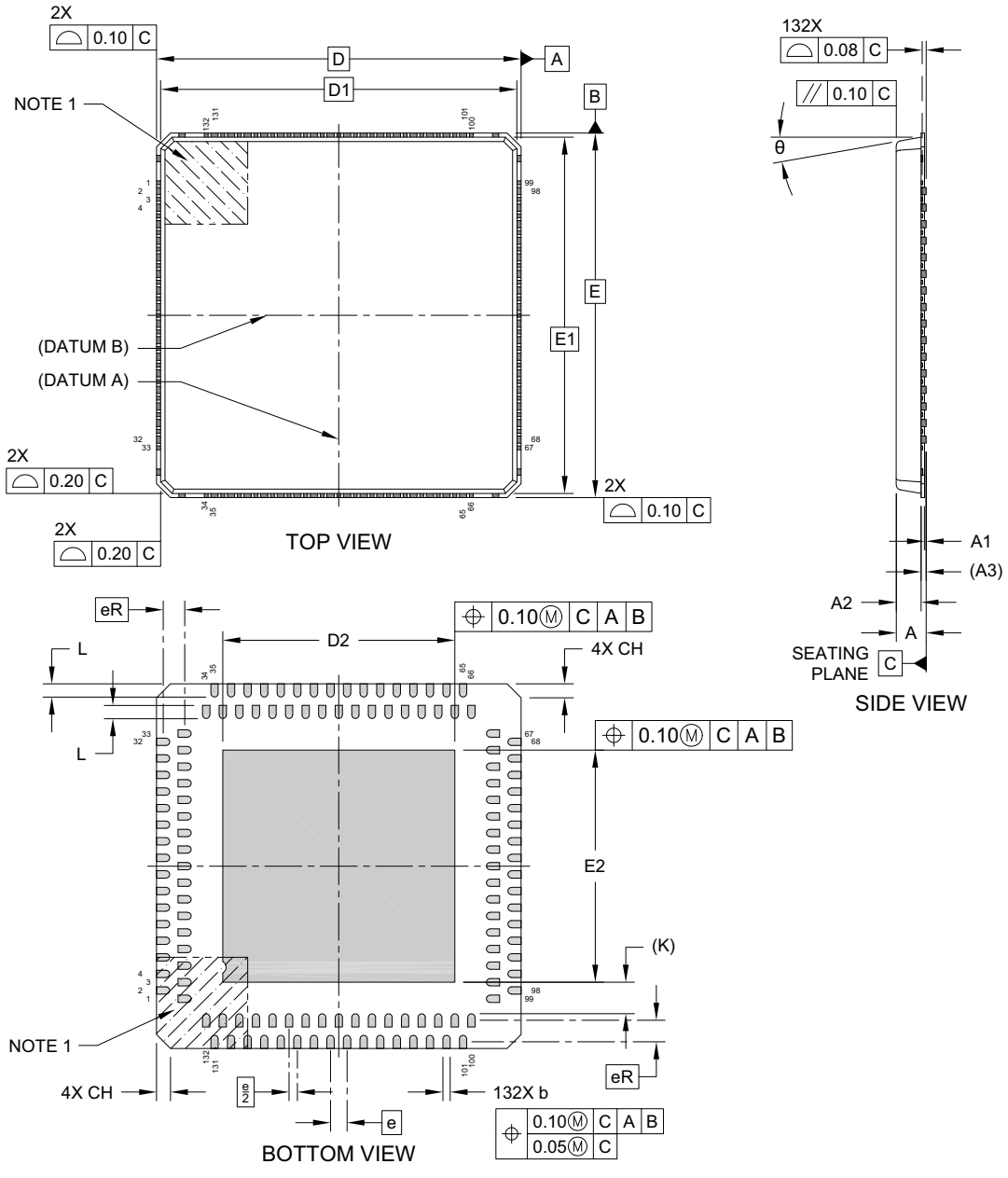
***** Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

5.2 Package Drawings

FIGURE 5-1: 132-VQFN-DR PACKAGE (DRAWING)

132-Lead Very Thin Plastic Quad Flat, No Lead Package (MXX) - 11x11x0.9 mm Body [DVQFN]; Dual Row, Punch Singulated

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

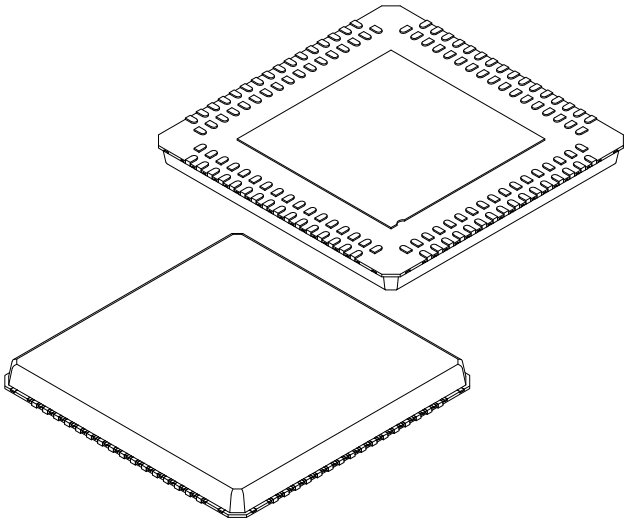


Microchip Technology Drawing C04-517 Rev E Sheet 1 of 2

FIGURE 5-2: 132-VQFN-DR PACKAGE (DIMENSIONS)

132-Lead Very Thin Plastic Quad Flat, No Lead Package (MXX) - 11x11x0.9 mm Body [DVQFN]; Dual Row, Punch Singulated

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		132	
Pitch	e		0.50 BSC	
Overall Height	A	–	–	0.90
Standoff	A1	0.00	0.02	0.05
Molded Package Height	A2	–	0.70	0.75
Terminal Thickness	A3		0.152 REF	
Overall Length	D		11.00 BSC	
Molded Package Length	D1		10.75 BSC	
Exposed Pad Length	D2	6.90	7.00	7.10
Overall Width	E		11.00 BSC	
Molded Package Width	E1		10.75 BSC	
Exposed Pad Width	E2	6.90	7.00	7.10
Spacing Between Rows	eR		0.65 BSC	
Terminal Width	b	0.18	0.22	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K		0.95 REF	
Package Corner Chamfer	CH	–	–	0.60
Mold Draft Angle	θ	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is punch singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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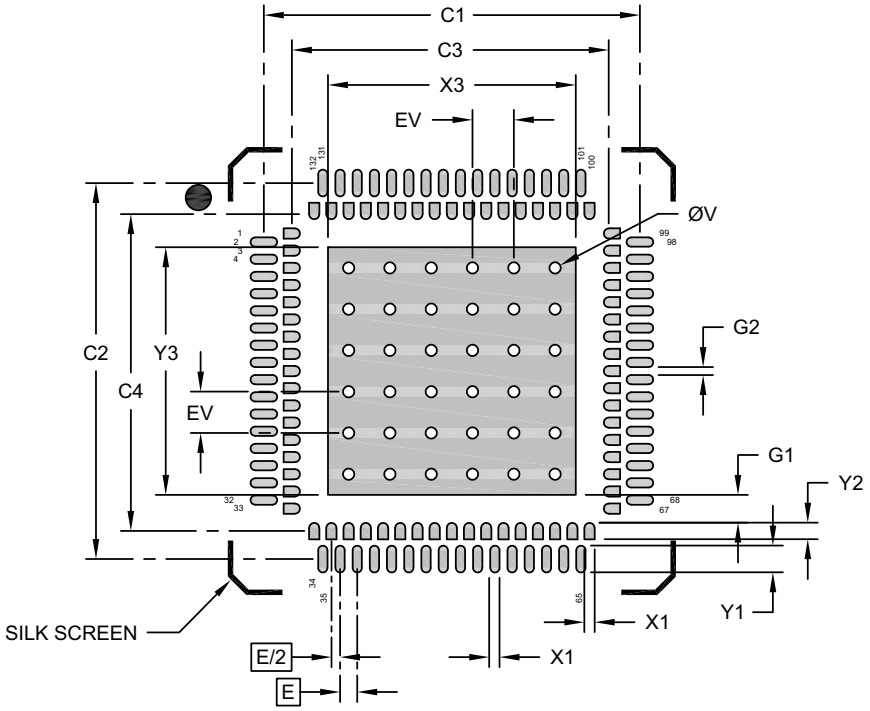
FIGURE 5-3: 132-VQFN-DR PACKAGE (LAND PATTERN)

132-Lead Very Thin Plastic Quad Flat, No Lead Package (MXX) - 11x11x0.9 mm Body [DVQFN]; Dual Row, Punch Singulated

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X3			7.20
Optional Center Pad Length	Y3			7.20
Outer Row Contact Pad Spacing	C1		10.93	
Outer Row Contact Pad Spacing	C2		10.93	
Inner Row Contact Pad Spacing	C3		9.21	
Inner Row Contact Pad Spacing	C4		9.21	
Contact Pad Width (X132)	X1			0.30
Outer Row Contact Pad Length (X64)	Y1			0.78
Inner Row Contact Pad Length (X68)	Y2			0.48
Inner Contact Pad to Center Pad (X68)	G1	0.80		
Contact Pad to Contact Pad (X132)	G2	0.23		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, please refer to current industry standard IPC-7093.

Microchip Technology Drawing C04-2517 Rev E

APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00006233A (11-11-25)	All	Preliminary release.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/	XXX	XXX
Device	Tape and Reel Option		Temperature Range		Package	Automotive Code

Device:	PCI11101C= PCIe with USB Host, Ethernet MAC, Prog. I/O	
Tape and Reel Option:	Blank T	= Standard packaging (tray) = Tape and Reel (Note 1)
Temperature Range:	Blank I	= 0°C to +70°C (Commercial) = -40°C to +85°C (Industrial/Automotive Grade 3)
Package:	MXX	= 132-pin VQFN-DR
Automotive Code:	Vxx	= 3 character code with "V" prefix, specifying automotive product.

Examples:

a) PCI11101C/MXX
Tray, 0°C to +70°C (Commercial),
132-pin VQFN-DR

b) PCI11101CT/MXX
Tape & reel, 0°C to +70°C (Commercial),
132-pin VQFN-DR

c) PCI11101C-I/MXX
Tray, -40°C to +85°C (Industrial),
132-pin VQFN-DR

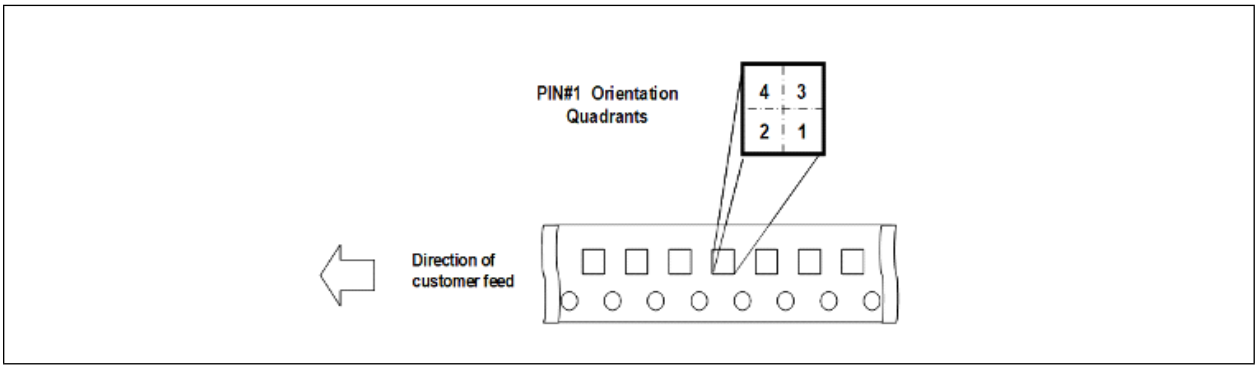
d) PCI11101CT-I/MXX
Tape & reel, -40°C to +85°C (Industrial),
132-pin VQFN-DR

e) PCI11101C-I/MXXVAO
Tray, -40°C to +85°C (Automotive Grade 3),
132-pin VQFN-DR

f) PCI11101CT-I/MXXVAO
Tape & reel, -40°C to +85°C (Automotive Grade 3),
132-pin VQFN-DR

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Pin 1 orientation is in quadrant 1, as detailed in the direction of unreeling diagram below.



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