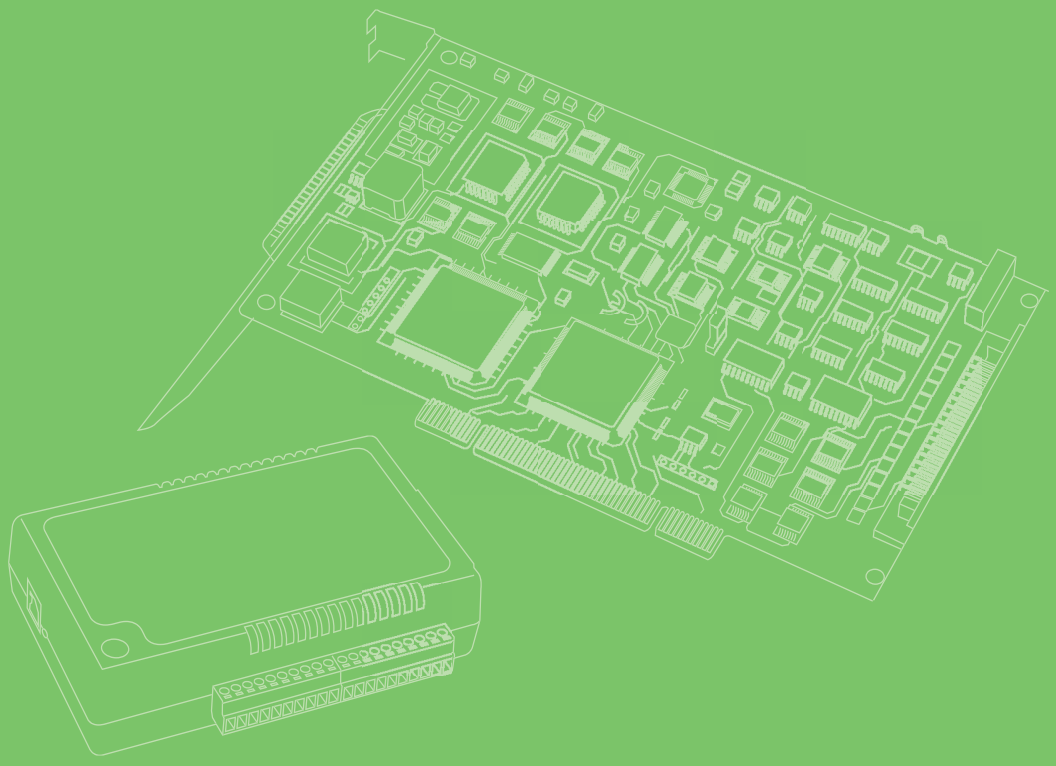

User Manual

PCI-1716/1716H/1716L

16-bit Multi-function Card with PCI Bus

ADVANTECH

Enabling an Intelligent Planet

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Acknowledgments

Product Warranty (2 years)

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Consult your dealer for more details.

If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an RMA (return merchandize authorization) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

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CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from Advantech. Please contact your local supplier for ordering information.

Technical Support and Assistance

1. Visit the Advantech web site at **http://support.advantech.com.tw/** where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, Contact your dealer immediately.

- PCI-1716/1716H/1716L DA&C card
- Startup or User Manual

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

1. To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
2. Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.

Contents

Chapter 1

Introduction

1.1 Introduction

The PCI-1716/1716H/1716L is a multifunction card for IBM x86 or compatible computers. It offers the five most desired measurement and control functions:

- 16-bit AI conversion
- 16-bit AO conversion
- Digital input
- Digital output
- Timer/counter.

A programmable-gain instrument amplifier lets you acquire different input signals without external signal conditioning. An onboard 8k word FIFO buffer provides high-speed data transfer and predictable performance under Windows. Automatic channel scanning circuitry and onboard SRAM lets you perform multiple-channel AI conversion and individual gains for each channel.

The following sections of this chapter will provide further information about features of the multifunction cards, together with some brief information on software and accessories for the PCI-1716/1716H/1716L cards.

1.2 Features

- 16 single-ended or 8 differential or a combination of analog inputs
- 16-bit A/D converter, with up to 1 MS/s or 250 KS/s sampling rate
- FIFO memory (8,192 samples)
- Auto-calibration
- 2 analog output channels (PCI-1716/PCI-1716H only)
- 16-ch digital input and 16-ch digital output
- BoardID switch

PCI-1716/1716H/1716L offers the following main features:

PCI-Bus Plug & Play

The PCI-1716/1716H/1716L card uses a PCI controller to interface the card to the PCI bus. The controller fully implements the PCI bus specification Rev 2.2. All configurations related to the bus, such as base address and interrupt assignment, are automatically controlled by software. No jumper or switch is required for user configuration.

Automatic Channel/Gain Scanning

The PCI-1716/1716H/1716L features an automatic channel/gain scanning circuit. This circuit, instead of your software, controls multiplexer switching during sampling. On-board SRAM stores different gain values for each channel. This combination lets user perform multi-channel high-speed sampling for each channel.

BoardID Switch

The PCI-1716/1716H/1716L has a built-in DIP switch that helps define each card's ID when multiple PCI-1716/1716H/1716L cards have been installed on the same PC chassis. The BoardID setting function is very useful when building a system with multiple PCI-1716/1716H/1716L cards. With the correct BoardID settings, you can easily

identify and access each card during hardware configuration and software programming.

Note! *For detailed specifications and operation of the PCI-1716/1716H/1716L, please refer to Appendix A and B.*

1.3 Applications

- Transducer and sensor measurements
- Waveform acquisition and analysis
- Process control and monitoring
- Vibration and transient analysis

1.4 Installation Guide

Before you install your PCI-1716/1716H/1716L card, please make sure you have the following necessary components:

- PCI-1716/1716H/1716L DA&C card
- PCI-1716/1716H/1716L User Manual
- Driver software Advantech DAQNavi software
- Personal computer or workstation with a PCI interface (running Windows 7, 10 or Linux

Other optional components are also available for enhanced operation:

- DAQ Navi, LabView or other 3rd-party software

After you get the necessary components and maybe some of the accessories for enhanced operation of your multifunction card, you can then begin the installation procedure.

1.5 Software Overview

Advantech offers a rich set of DLL drivers, third-party driver support and application software to help fully exploit the functions of your PCI-1716/1716H/1716L card:

- Device Drivers
- LabVIEW driver
- Advantech DAQNavi
- Data logger

Programming choices for DA&C cards

You may use Advantech application software such as Advantech Device Drivers. On the other hand, advanced users can use register-level programming, although this is not recommended due to its laborious and time-consuming nature.

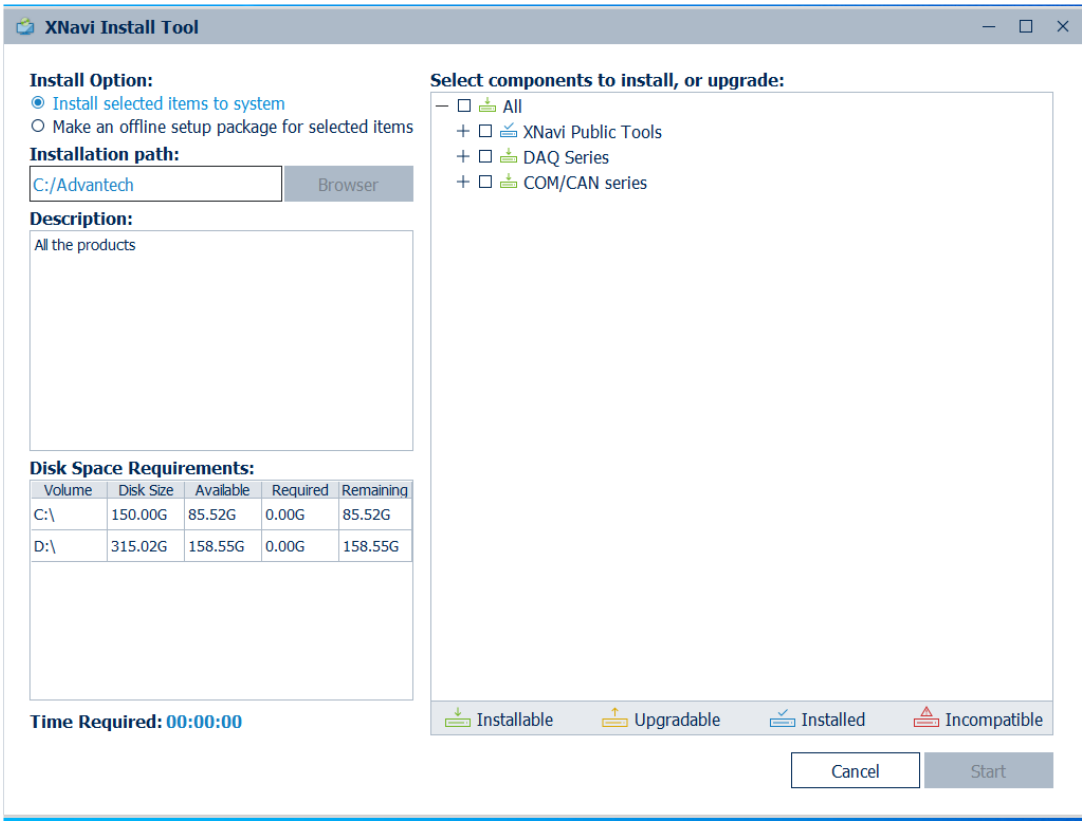
DAQNavi Software

Advantech DAQNavi software includes device drivers and SDK which features a complete I/O function library to help boost your application performance.

The software package could be found on Advantech Support Portal (https://www.advantech.com/support). Search for PCI-1716 on the support portal, then the

corresponding driver/SDK package can be found. You'll get the XNavi installer after the download session finishes.

Execute the installer, then it will guide you through the session. You can choose the device and software components you'd like to install in the system (Figure 1.1). After the selection, click on “start” to begin the installation.



1.6 Software Utility

Advantech offers device drivers, SDKs, third-party driver support and application software to help fully exploit the functions of your iDAQ system. All these software packages are available on the Advantech website: http://www.advantech.com/.

The Advantech Navigator is a utility that allows you to set up, configure and test your device, and later store your settings in a proprietary database.

1. To set up the I/O device, you could first run the Advantech Navigator program (by accessing Start/Programs/Advantech Automation/DAQNavi/Advantech Navigator). The settings could also be saved.
2. You can then view the device(s) already installed on your system (if any) on the Installed Device tree view. Once the software and hardware installation have completed, you will see the iDAQ modules in the Installed Devices list.

1.7 Software Development Using DAQNavi SDK

DAQNavi SDK is the software development kit for programming applications with Advantech DAQ products. The necessary runtime DLL, header files, software manual and tutorial videos could be installed via XNavi installer. They could be found under C:\Advantech\DAQNavi (default directory) after the finishing the installation.

1.8 Accessories

Advantech offers a complete set of accessory products to support the PCI-1716/1716H/1716L card. These accessories include:

Wiring Cables

- **PCL-10168-1E** 68-pin SCSI Shielded Cable, 1 m
- **PCL-10168-2E** 68-pin SCSI Shielded Cable, 2 m
- **PCL-10168H-1E** 68-pin SCSI Shielded Cable with Noise Rejecting, 1 m
- **PCL-10168H-2E** 68-pin SCSI Shielded Cable with Noise Rejecting, 2 m

Wiring Boards

- ADAM-3968 68-pin DIN-rail SCSI Wiring Board
- **PCLD-8710:** DIN-rail wiring board with CJC

Chapter 2

Installation Guide

2.1 Unpacking

After receiving your PCI-1716/1716H/1716L package, inspect the contents first. The package should include the following items:

- PCI-1716/1716H/1716L card
- Startup Manual

The PCI-1716/1716H/1716L card harbor certain electronic components vulnerable to electrostatic discharge (ESD). ESD can easily damage the integrated circuits and certain components if preventive measures are ignored.

Before removing the card from the anti-static plastic bag, you should take following precautions to ward off possible ESD damage:

- Touch the metal part of your computer chassis with your hand to discharge the static electricity accumulated on your body. Alternatively, one can also use a grounding strap.
- Touch the anti-static bag to a metal part of your computer chassis before opening the bag.
- Take hold of the card only by the metal bracket when removing it out of the bag.

After taking out the card, you should first:

- Inspect the card for any possible signs of external damage (loose or damaged components, etc.). If the card is visibly damaged, please notify our service department or our local sales representative immediately. Do not install a damaged card into your system.

Also pay extra attention to the followings to ensure a proper installation:

- Avoid physical contact with materials that could hold static electricity such as plastic, vinyl and Styrofoam.
- Whenever you handle the card, grasp it only by its edges. DO NOT TOUCH the exposed metal pins of the connector or the electronic components.

Note! *Keep the anti-static bag for future use. You might need the original bag to store the card if you have to remove the card from a PC or transport it elsewhere.*

2.2 Switch and Jumper Settings

Please refer to Figure 2.1 for jumper and switch locations on PCI-1716/1716H/1716L.

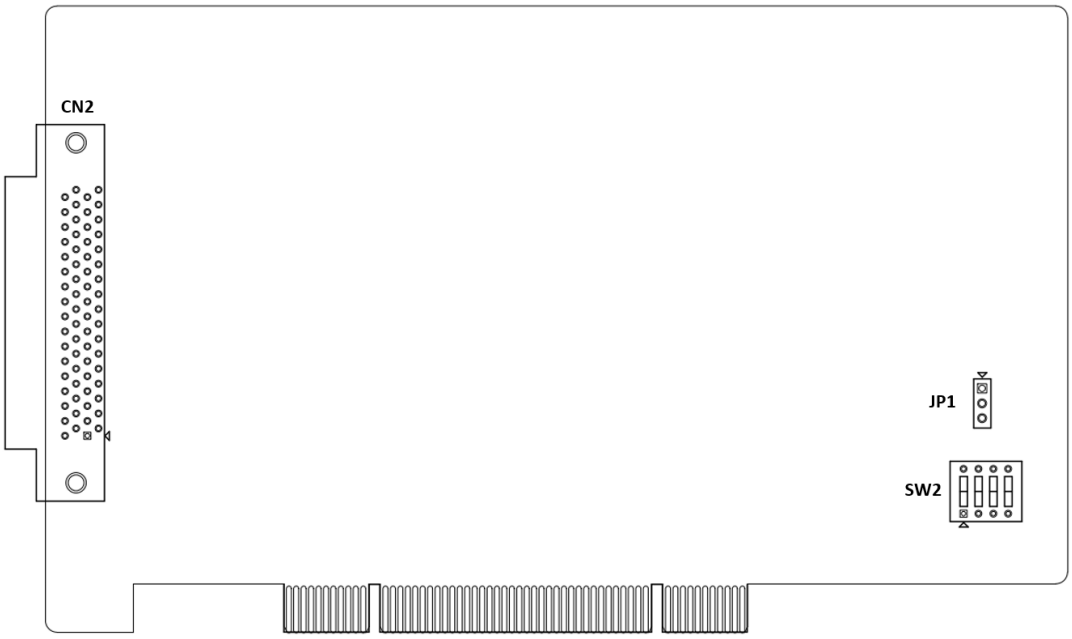


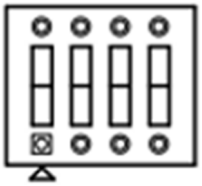
Figure 2.1 Connector and Switch Locations

2.2.1 Board ID (SW1)

The PCI-1716/1716H/1716L has a built-in DIP switch (SW1), which is used to define each card's board ID. When there are multiple cards on the same chassis, this board ID switch is useful for identifying each card's device number.

After setting each PCI-1716/1716H/1716L, you can identify each card in system with different device numbers. The default value of board ID is 0 and if you need to adjust it to other value, please set the SW1 by referring to Table 2.1.

Table 2.1: Board ID Setting (SW2)

SW2	Board ID	Position 1 (ID0)	Position 2 (ID1)	Position 3 (ID2)	Position 4 (ID3)
ON  OFF	0*	ON	ON	ON	ON
	1	ON	ON	ON	OFF
	2	ON	ON	OFF	ON
	3	ON	ON	OFF	OFF
	4	ON	OFF	ON	ON
	5	ON	OFF	ON	OFF
	6	ON	OFF	OFF	ON
	7	ON	OFF	OFF	OFF
	8	OFF	ON	ON	ON
	9	OFF	ON	ON	OFF
	10	OFF	ON	OFF	ON
	11	OFF	ON	OFF	OFF
	12	OFF	OFF	ON	ON
	13	OFF	OFF	ON	OFF
	14	OFF	OFF	OFF	ON
	15	OFF	OFF	OFF	OFF

*Default setting

2.2.2 Power On Configuration(JP1)

Default configuration after power on, and hardware reset is to set all the analog input and analog output channels to open status (the current of the load can't be a sink) so that the external devices will not be damaged when the system starts or resets. When the system is hot reset, then the status of isolated digital output channels are selected by jumper JP1. Table 2.2 shows the configuration of jumper JP1.

Table 2.2: Power on Configuration after Hot Reset (JP1)

JP1	Power on configuration after hot reset
1 	Keep last status after hot reset
1 	Default configuration (Default setting)

2.3 Pin Assignments and Signal Connections

Pin Assignments

The I/O connector on the PCI-1716/1716H/1716L is a 68-pin connector that enable you to connect to accessories with the PCL-10168-1 or PCL-10168H shielded cable.

Figure 2.2 shows the pin assignments for the 68-pin I/O connector on the PCI-1716/1716H/1716L, and Table 2.3 shows its I/O connector signal description.

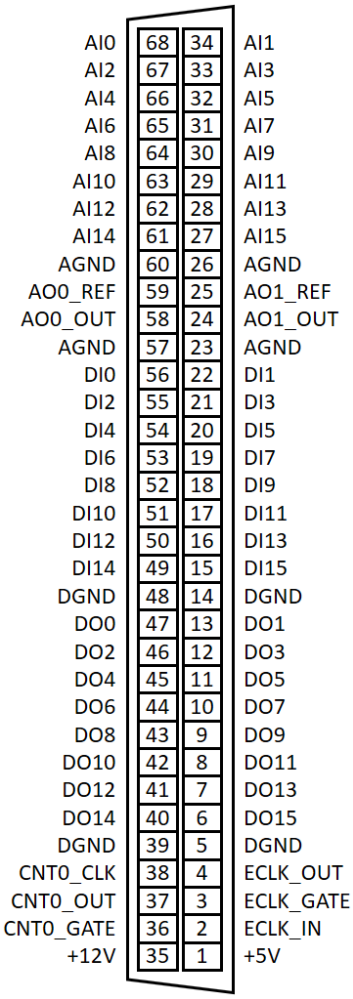


Figure 2.2 68-pin I/O Connector Pin Assignments

Table 2.3: I/O Connector Signal Description			
Signal Name	**Reference**	**Direction**	**Description**
AI<0..15>	AGND	Input	Analog input terminals. Each channel pair (AI0 & AI1, AI2 & AI3, etc.) can be configured as a differential input channel or two single-ended channels.
AO<0..1>_REF*	AGND	Input	Analog output reference voltage input terminals.
AO<0..1>_OUT*	AGND	Output	Analog output terminals.
AGND	-	-	Ground terminals for analog signals.
DI<0..15>	DGND	Input	Digital input terminals.
DO<0..15>	DGND	Output	Digital output terminals.
CNT0_CLK	DGND	Input	Counter 0 clock input terminal.
CNT0_OUT	DGND	Output	Counter 0 output terminal.
CNT0_GATE	DGND	Input	Counter 0 gate input terminal.
ECLK_IN	DGND	Input	External clock input terminal. It is the external conversion/sample/update clock source for various functions.
ECLK_OUT	DGND	Output	External clock output terminal. Analog input conversion clock is routed to this terminal. It can be used to synchronize acquisition among multiple devices.
ECLK_GATE	DGND	Input	External clock gate input terminal.
DGND	-		Ground terminals for digital signals.
+12V	DGND	Output	+12 V supply output.
+5V	DGND	Output	+5 V supply output.

* Not available for PCI-1716L.

2.4 Analog Input Signal Connection

An analog input channel measures the voltage (VS) of the external source. Each two channels, for example, AI0 and AI1, AI2 and AI3, etc., can be configured as a differential input channel, or as two separate single-ended channels. When configured as a differential channel, even number channel is the positive terminal, and odd number channel is the negative terminal. When configured as separate single-ended channels, voltage should be applied between channel terminal and analog ground (AGND) terminal.

The voltage is routed through an analog multiplexer (MUX), amplified or attenuated by a programmable gain instrumentation amplifier (PGIA), and sampled and converted into a digital form of data by an analog-to-digital converter (ADC). Each channel is converted by the ADC in channel by channel order. That is, only one channel at a time is being converted. This architecture is called multiplexed analog input.

Analog input signal connection and internal functional block diagram is shown in Figure 2.3.

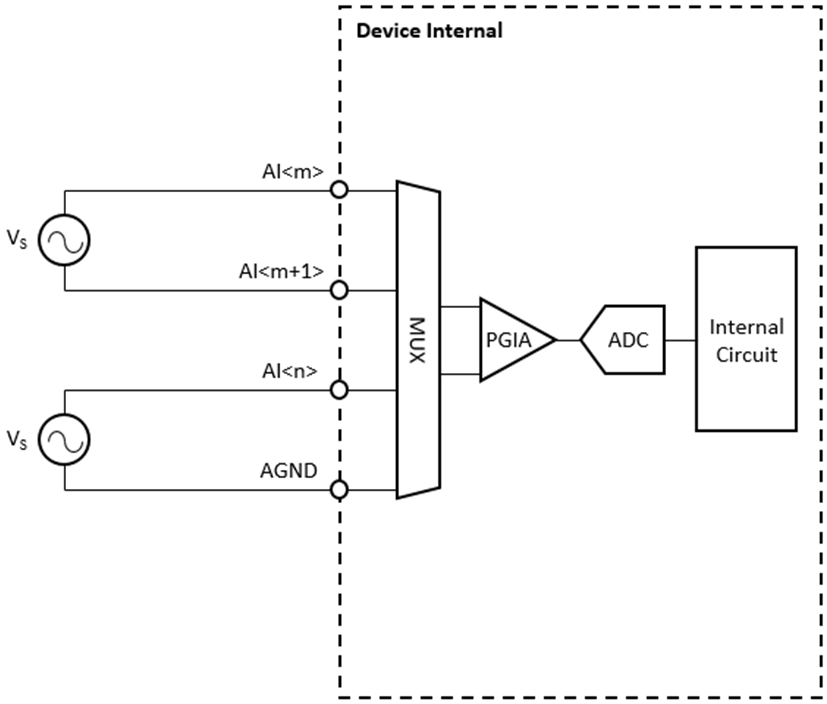


Figure 2.3 Analog input signal connection.

2.4.1 Analog Input Configuration

The input configuration can be either differential or single-ended. For differential configuration, connect the external source between an even number of analog input (AI) terminal and the next odd number of AI terminal. For example, connect between AI0 and AI1, or between AI8 and AI9. Differential configuration rejects common-mode noise picked up from the wiring, which results in better performance. However, it requires two channels to measure one external source.

For single-ended configuration, connect the external source between an AI terminal and the analog ground (AGND) terminal. Only one channel is required to measure the external source. However, it is more vulnerable to ground noise and common-noise picked up from the wiring.

Each analog input channel can be configured as differential or single-ended independently by software. When an even-number channel is configured as differential, the corresponding odd-number channel will be fixed to differential automatically.

2.4.2 Analog Multiplexer

The analog multiplexer routes one of the analog input channels at a time (one for single-ended configuration, and two for differential configuration) to the PGIA and ADC to be measured. This mechanism is called channel scanning. It realizes multiple channel measurement using only one ADC at a cost of sharing ADC sample rate among all scanned channels.

User can select a range of channels to be scanned. The selected channels will be scanned by the order of channel number. After the last channel is scanned, the next channel will be the first channel. For example, if channels 3, 4, 5, 6, and 7 are selected, the scanning sequence is channel 3, 4, 5, 6, 7, 3, 4, 5, 6, 7, 3, etc.

2.4.3 Programmable Gain Instrumentation Amplifier (PGIA)

Multiple input ranges are supported and can be selected by software for each channel independently. The input signal is amplified or attenuated by the PGIA before being sampled by the ADC. The gain of the PGIA differs for different input ranges, so that the signal range at input of the ADC is the same for every input range. Refer to the device specifications for the supported input ranges.

2.4.4 Grounding Considerations

2.4.4.1 Signal Source Type

Signal sources can be categorized as grounded (ground-referenced) signal source or ungrounded (floating) signal source. This is shown in Figure 2.4.

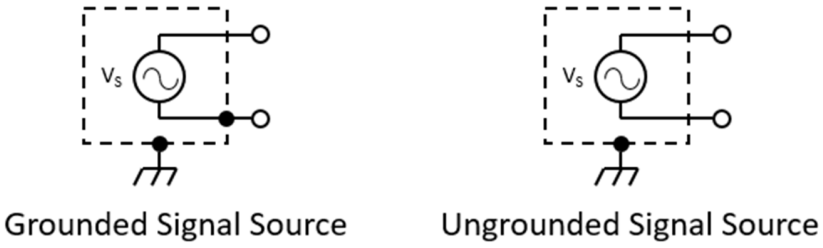


Figure 2.4 Signal source type.

The voltage of a grounded signal source is referenced to a system ground, such as earth or building ground. That is, the negative terminal of the signal source is connected to the system ground. Examples of grounded signal source are devices that are plugged into the building ground through a wall outlet. The grounds of two independently grounded devices may not be at the same potential.

An ungrounded signal source is that in which the voltage is not referenced to a system ground. Examples of grounded signal source are battery powered devices, thermocouples, and isolated devices.

2.4.4.2 Measuring a Grounded Signal Source

For a grounded signal source, it is recommended to measure the signal using differential input configuration. As described in the previous section, the grounds of two grounded devices may not be at the same potential. If single-ended (grounded) input configuration is used to measure a grounded signal source, a ground loop is formed

and there will be current flowing between two grounds, which generates common-mode noise for the measurement. This is shown in Figure 2.5.

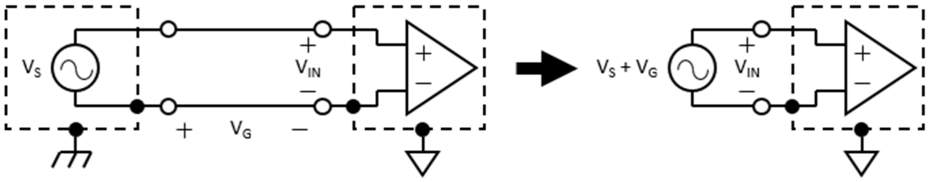


Figure 2.5 Ground loop effect.

If differential (ungrounded) input configuration is used instead, the high input impedance of the negative input terminal prevents ground loop current from flowing, and therefore rejects the common-mode noise.

2.4.4.3 Measuring an Ungrounded (Floating) Signal Source

For an ungrounded (floating) signal source, both differential input configuration and single-ended input configuration are suitable. When using differential input configuration, however, care must be taken to ensure the input common-mode voltage level remains in the allowable range of the measuring device. Due to the lack of DC path to the ground, the input bias current of input stage amplifier may move the common-mode voltage level of the ungrounded signal source out of the allowable range of the measuring device. When this happens, the measured result will be incorrect or saturated (positive full-scale or negative full-scale). Resistors with equal resistance value connecting between each input terminal and ground can be used to alleviate this issue as shown in Figure 2.6. These resistors are called bias resistors.

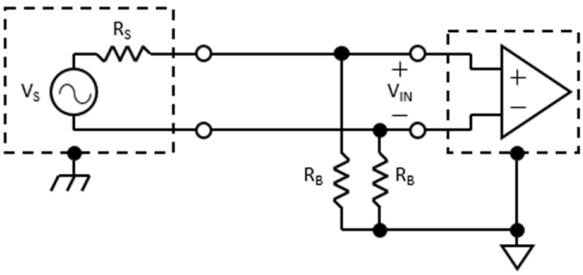


Figure 2.6 Differential input configuration with bias resistors.

The resistance value should be large enough that it does not load the signal source and keep it remain floating, but small enough to make input common-mode voltage level stay in the allowable range. Typically, resistance value between 10 kΩ to 100 kΩ work well with low-impedance sources such as thermocouples and signal conditioning module outputs. When using bias resistor, the measured voltage will be attenuated by the voltage divider formed by source resistance of the signal source and bias resistors. This is shown in the following equation.

$$V_{IN} = \frac{2 \times R_B}{R_S + 2 \times R_B} V_S$$

If the source impedance of the signal source is low, only one resistor connecting between the negative input terminal and the ground is required to prevent input common-mode voltage level issue. However, this will lead to an unbalanced system if the source impedance is relatively high. A balanced system is desirable from a noise immunity point of view.

2.5 Analog Output Signal Connection

An analog output channel generates a voltage output to the load. The voltage to be generated is first sent by the internal controller to the digital-to-analog converter (DAC) in a form of digital data, and the data is converted by the DAC to an analog output voltage. The analog output channel is of single-ended type, hence the load should be connected between the analog output (AO) terminal and the analog ground (AGND) terminal. This is shown in Figure 2.7.

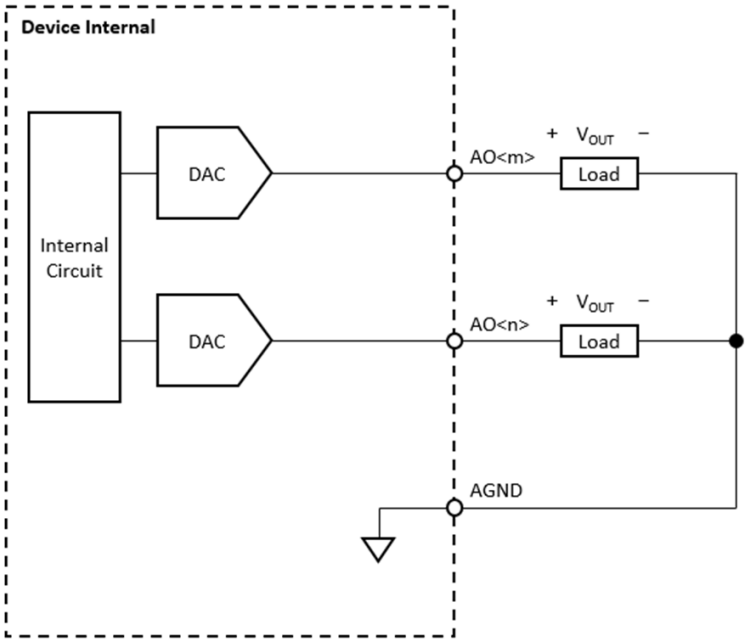


Figure 2.7 Analog output signal connection.

Multiple output ranges are supported and can be selected by software for each channel independently. Be sure that the load resistance is within the range of the device specifications, or the output voltage may not reach the specified value due to the limitation of output driving capability.

The output range can also be defined by an external reference voltage which is connected to the analog output reference (AO_REF) terminal. Refer to the device specifications for the relationship between the output range and the external reference voltage. In this configuration, however, the output voltage is not calibrated, and the accuracy of the output voltage depends on the accuracy of the external reference voltage. Users can perform calibration through the calibration utility in the Advantech Navigator by themselves.

2.5.1 Analog Output Reference Voltage Input

If desired, an external voltage source can be connected to the reference voltage input terminal to use a user-defined output range. When a “x V” voltage is applied, output range can be configured as 0 V ~ x V or –x V ~ x V.

2.6 Digital Input Signal Connection

A digital input channel can perform digital input measurement. The voltage logic level between the digital input (DI) terminal and the digital ground (DGND) terminal is measured. To prevent undetermined or fluctuating results when input is floating, the digital input channel is internally pulled-up. This is shown in Figure 2.8.

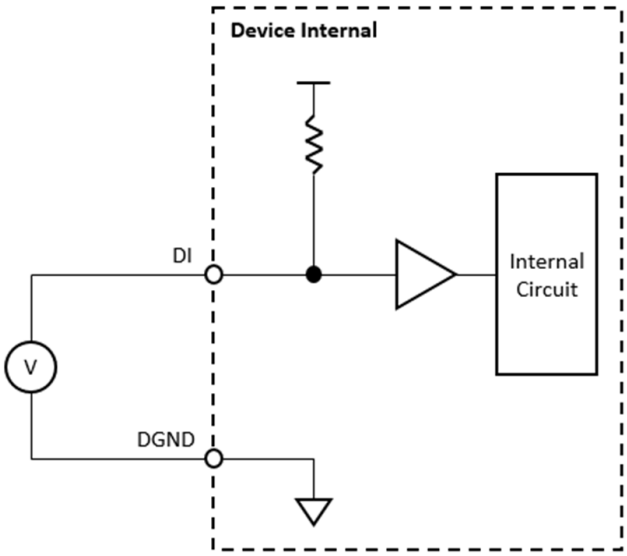


Figure 2.8 Digital input signal connection.

The input voltage must be either higher than the minimum value of ON state or lower than the maximum value of OFF state for deterministic result. If the input voltage is between these two values, the result is undetermined, which may be ON or OFF. In addition, do not input a voltage higher than the maximum allowable value of ON state or lower than the minimum allowable value of OFF state. The device may be damaged under such circumstance. Refer to the device specifications for ON and OFF state voltage ranges.

The digital input channel can also sense the status of an external switch. The status of an external switch which is connected between the DI terminal and the DGND terminal is sensed as shown in Figure 2.9.

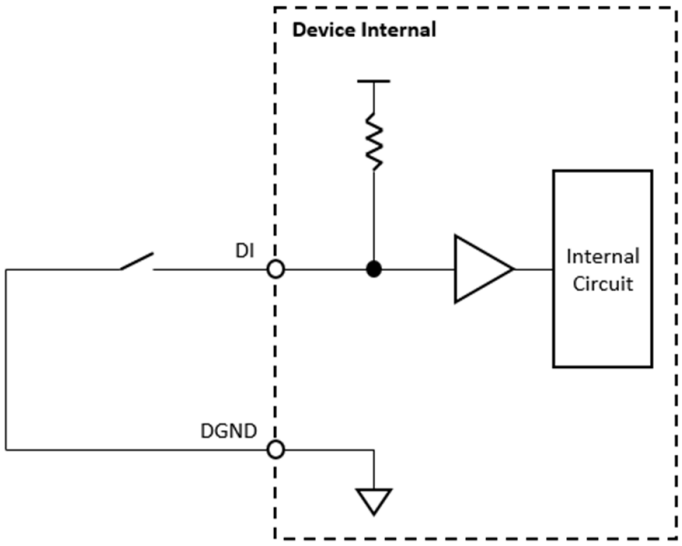


Figure 2.9 Digital input signal connection using a switch with internally pulled-up.

2.7 Digital Output Signal Connection

A digital output (DO) channel can perform digital output generation. A voltage logic level is generated between the digital output (DO) terminal and the digital ground (DGND) terminal. This is shown in Figure 2.10.

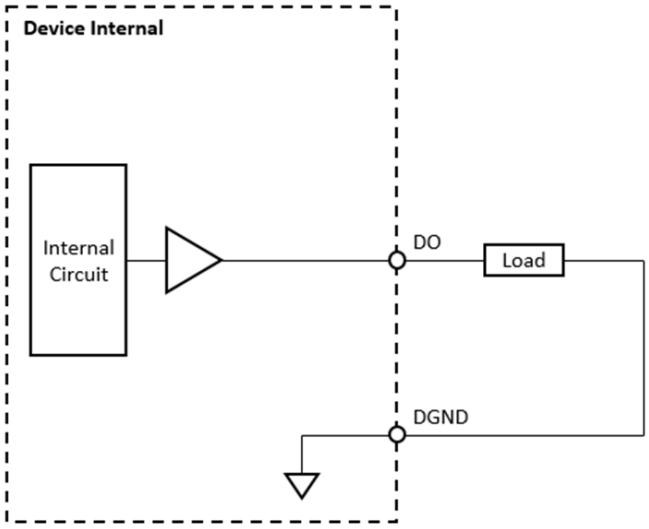


Figure 2.10 Digital output signal connection.

Each digital output channel can source or sink only finite amount of current. If this limit is exceeded, the output voltage will not stay in the specified voltage logic level. Refer to the device specifications for the maximum source and skin current values.

2.8 Counter Input Signal Connection

The voltage logic level between the counter input (counter clock, counter gate, counter arm, and sample clock) terminals and the digital ground (DGND) terminal is measured. To prevent undetermined or fluctuating results when input is floating, the counter input signals are internally pulled-up. This is shown in Figure 2.11.

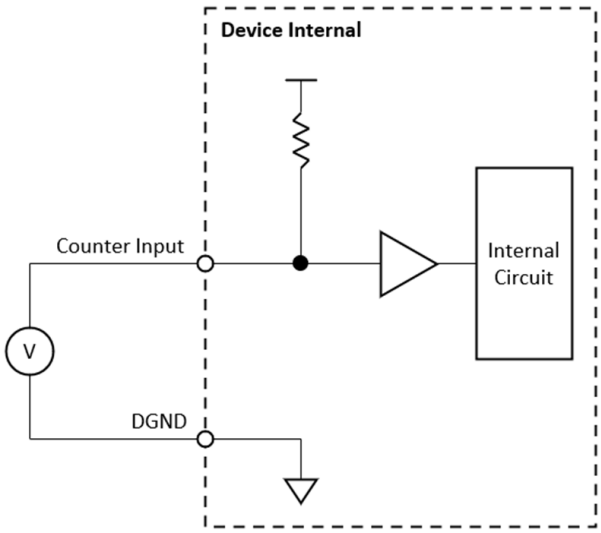


Figure 2.11 Counter input signal connection.

The input voltage must be either higher than the minimum value of ON state or lower than the maximum value of OFF state for deterministic result. If the input voltage is between these two values, the result is undetermined, which may be ON or OFF. In addition, do not input a voltage higher than the maximum allowable value of ON state or lower than the minimum allowable value of OFF state. The device may be damaged under such circumstance. Refer to the device specifications for ON and OFF state voltage ranges.

The counter input signals can also sense the status of an external switch. The status of an external switch which is connected between the counter input terminals and the DGND terminal is sensed as shown in Figure 2.12.

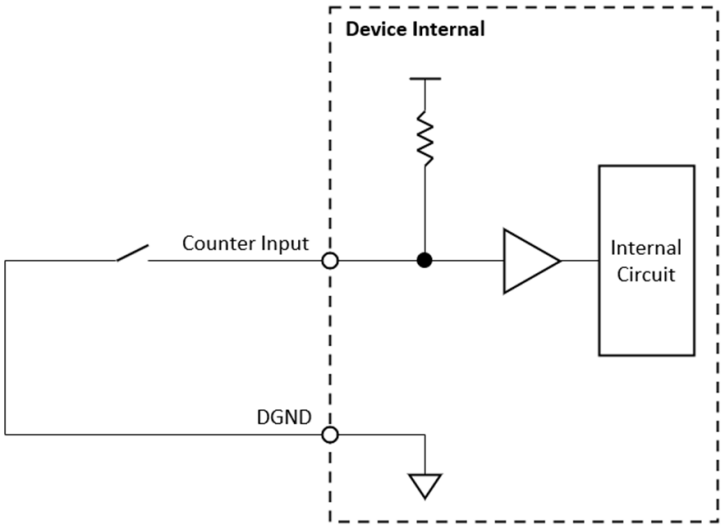


Figure 2.12 Counter input signal connection using a switch with internally pulled-up.

2.9 Counter Output Signal Connection

A voltage logic level is generated between the counter output terminal and the digital ground (DGND) terminal. This is shown in Figure 2.13.

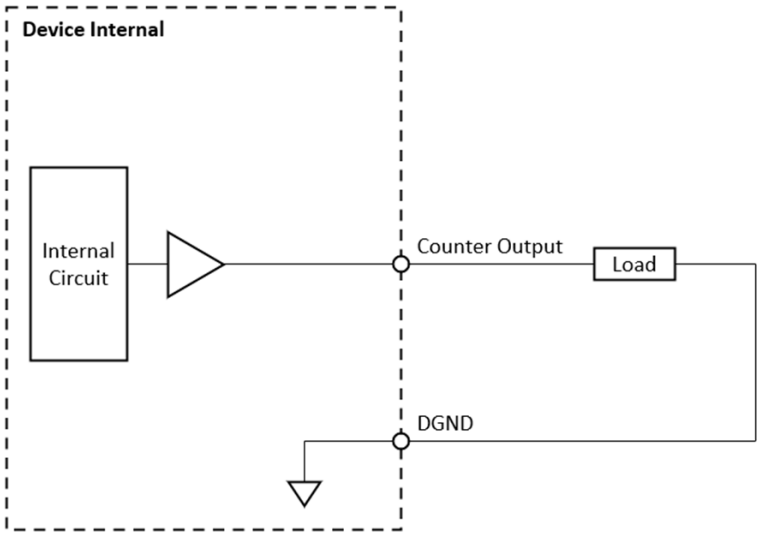


Figure 2.13 Counter output signal connection.

Each counter output channel can source or sink only finite amount of current. If this limit is exceeded, the output voltage will not stay in the specified voltage logic level. Refer to the device specifications for the maximum source and skin current values.

Chapter 3

Function Details

3.1 Analog Input

3.1.1 Analog Input Resolution

Analog input voltage or current is measured by an ADC, which has a finite resolution. For example, a 16-bit ADC divides the input range into 65,536, which is 216, codes. These codes represent input voltage or current which are equally distributed across the input range. If the input range is ±10 V, the resolution is

$$\frac{+10V-(-10V)}{65{,}536}=305\mu V$$

Because resolution depends on input range, as stated in the previous equation, a smaller input range has higher (finer) resolution, and vice versa. Choose an input range that matches the maximum possible range of the input signal. If a larger-than-required range is used, the resolution is reduced; if a smaller-than-required range is used, on the other hand, the required input range cannot be covered.

3.1.2 Analog Input Acquisition Methods

The device supports both instant (software-timed) and buffered (hardware-timed) analog input acquisitions.

3.1.2.1 Instant (Software-Timed) Analog Input Acquisition

With instant acquisition, the software controls the rate and time of acquisition, which is thus also called software-timed acquisition. Whenever the software sends a read command, the current value of analog input channel is returned as shown in Figure 3.1.

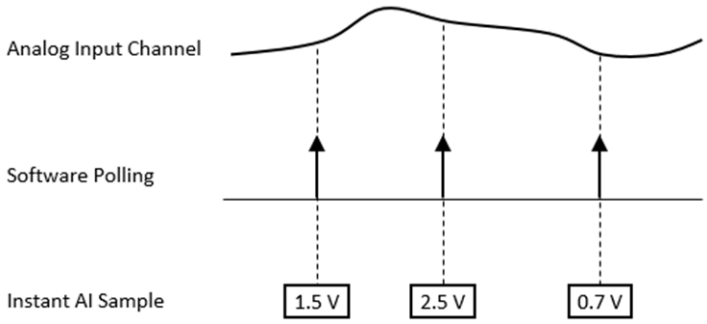


Figure 3.1 Instant (software-timed) analog input acquisition.

The advantage of instant acquisition is low latency. It is typically used for reading a single sample of analog input.

3.1.2.2 Buffered (Hardware-Timed) Analog Input Acquisition

With buffered acquisition, a hardware signal called conversion clock controls the rate and time of acquisition. The ADC begins to convert the analog input voltage at each rising edge of the conversion clock. After the ADC begins conversion, the analog multiplexer routes the next buffered acquisition enabled analog input channel to the ADC, which will be converted at the next rising edge of the conversion clock. Figure 3.2 shows an example of analog input buffered acquisition which AI0, AI1, and AI2 are enabled.

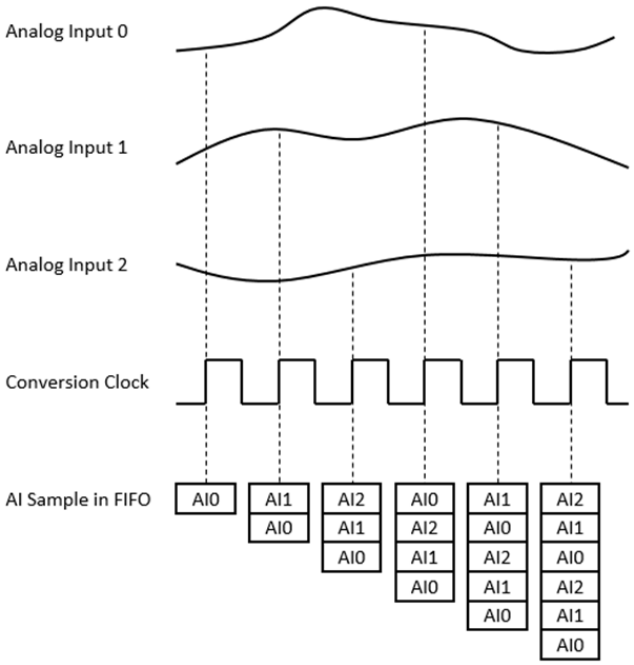


Figure 3.2 Buffered (hardware-timed) analog input acquisition.

The conversion clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported conversion clock sources and the maximum allowable frequency of conversion clock.

The acquired samples are first accumulated in the onboard first-in-first-out (FIFO) memory of the device, and then moved to the buffer in the PC by a direct memory access (DMA) engine. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the application memory. Because the data is moved in large blocks instead of one point at a time, buffered acquisition typically allow much higher transfer rates. Buffered acquisition is also called hardware-timed acquisition.

The advantages of buffered acquisition over instant acquisition include:

- The sample rate can be much higher.
- The time of sample is deterministic.
- Hardware triggers can be used.

3.1.3 Configuration for Buffered Analog Input Acquisition

According to software configurations, buffered analog input acquisition can be classified into two types:

- One-buffered analog input acquisition
- Streaming analog input acquisition

3.1.3.1 One-Buffered Analog Input Acquisition

For one-buffered acquisition, only a specified number of samples is acquired. Both the start and stop of acquisition are controlled by software commands. Only one type of acquisition can be achieved: post-trigger acquisition.

Post-Trigger Acquisition

A post-trigger acquisition acquires a specified number of samples after the start trigger. The acquisition starts when a start trigger is received and automatically stops when the specified number of samples is acquired. An example of 5-sample post-trigger acquisition is shown in Figure 3.3.

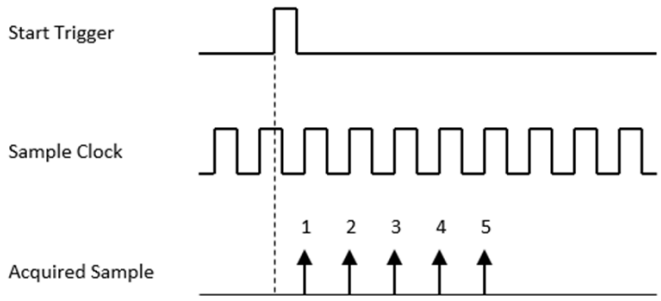


Figure 3.3 Post-trigger acquisition.

3.1.3.2 Streaming Analog Input Acquisition

For a streaming acquisition, the number of samples to be acquired is set to infinite. The acquisition starts when a start trigger is received and continues until a stop trigger is received as shown in Figure 3.4.

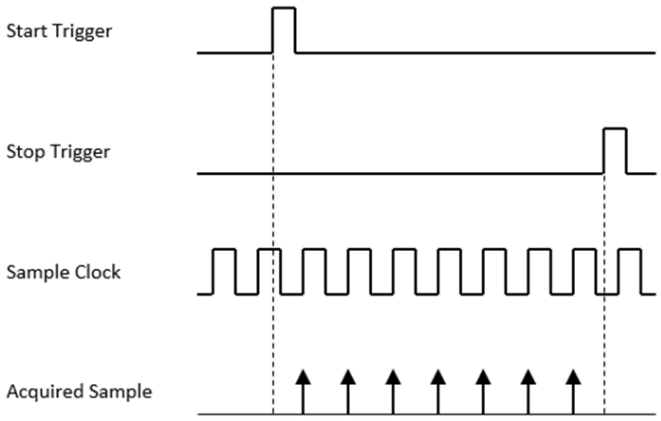


Figure 3.4 Streaming acquisition.

Both the start trigger and the stop trigger can come from a software command or a hardware signal. If a hardware signal is used, the start (for the start trigger) or the stop (for the stop trigger) of the acquisition can also be delayed. Refer to the device specifications for possible signal sources.

3.1.4 External Conversion Clock with Gate

The conversion clock source can be software configured as either internally generated clock or external source. When using external clock, be sure the clock frequency does not exceed the maximum allowable value of the specifications.

An external gate signal can be used to temporarily mask the external clock. Clock is effective only when external gate signal is low, and it is masked when external gate signal is high. This is shown in Figure 3.5.

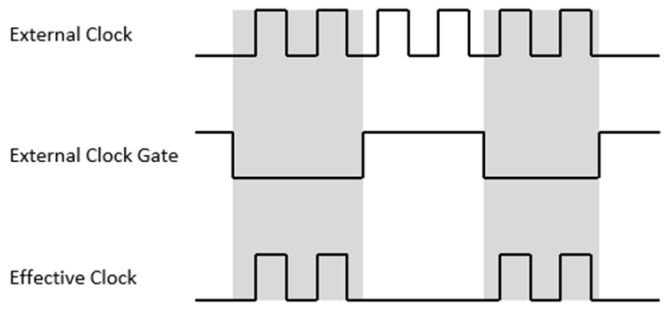


Figure 3.5 External conversion clock with gate.

3.2 Analog Output

3.2.1 Analog Output Resolution

Analog output voltage or current is generated by a DAC, which has a finite resolution. For example, a 16-bit DAC divides the output range into 65,536, which is 216, codes. These codes represent output voltage or current which are equally distributed across the output range. If the output range is ±10 V, the resolution is

$$\frac{+10V-(-10V)}{65{,}536}=305\mu V$$

Because resolution depends on output range, as stated in the previous equation, a smaller output range has higher (finer) resolution, and vice versa. Choose an output range that matches the maximum possible range of the output signal. If a larger-than-required range is used, the resolution is reduced; if a smaller-than-required range is used, on the other hand, the required output range cannot be covered.

3.2.2 Analog Output Signal Glitch

3.2.2.1 DAC Code Change Glitch

When the output voltage or current of an analog output channel changes, glitches may be observed. This is a normal phenomenon due to released charges of the DAC. The largest glitches occur when the most significant bit of the DAC code changes.

To preserve the slew rate and settling time specifications, no further signal conditioning is applied in the device. If the glitches are unacceptable, an external low-pass deglitching filter can be used to reduce the glitches. However, user should verify that the frequency response and distortion of the signal due to the deglitching filter can still meet the requirement of the applications.

3.2.2.2 Power-On Glitch

For other devices which do not have power-on glitch remover, when the device is powered-on, glitches may be observed at the analog output channels. This is because the internal power supplies and the DAC control circuitry are not stable yet.

In this device, however, each analog output channel is equipped with a switch as the power-on glitch remover. The switch is closed only when the internal power supplies and the DAC control circuitry are stable, which result in no power-on glitch. This is shown in Figure 3.6.

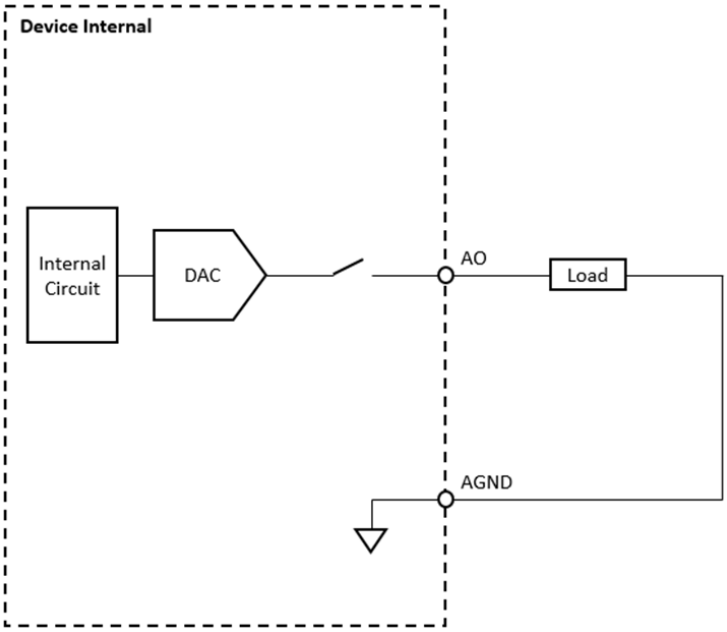


Figure 3.6 Power-on glitch remover of the analog output.

3.2.3 Output Status When Changing Range

When analog output range changes, the DAC setting remains unchanged, and so does the output voltage. The DAC will be updated to the new output range only when a new output value is written. For example, if an analog output channel is at +5 V of ±10 V range, after changing to 0 V to 5 V range, the output voltage still remains at +5 V. If a new output value of +2 V is written, DAC will be updated to 0 V to 5 V range and output voltage will be updated to +2 V at the same time. This is shown in Figure 3.7.

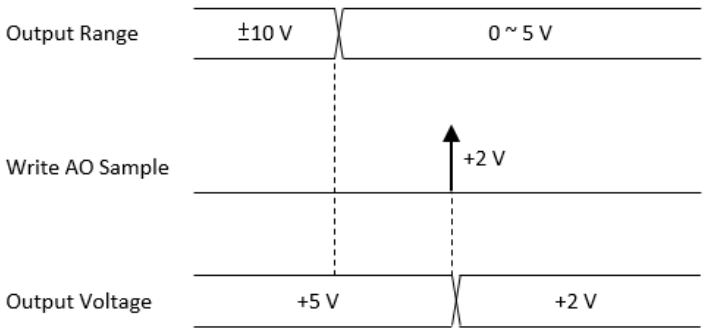


Figure 3.7 Output status when changing range.

3.2.4 Analog Output Data Generation Methods

The device supports both static (software-timed) analog output update and buffered (hardware-timed) analog output generation.

3.2.4.1 Static (Software-Timed) Analog Output Update

With static update, the software controls the rate and time of date, which is thus also called software-timed update. Whenever the software sends a write command, the value of analog output channel is updated as shown in Figure 3.8.

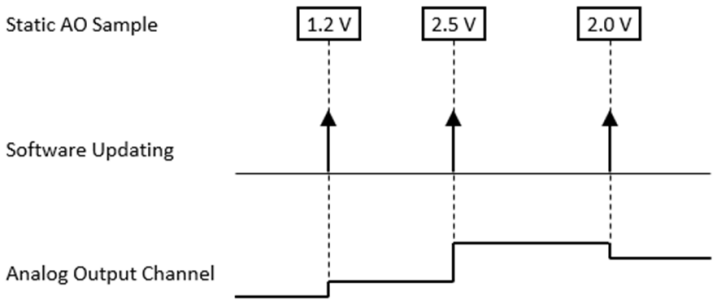


Figure 3.8 Static (software-timed) analog output update.

The advantage of state update is low latency. It is typically used for writing a single value of analog output.

When updating multiple analog output channels, they can be updated asynchronously or synchronously. For asynchronous update, each the analog output channel is updated immediately when the value to be updated is written to the device as shown in Figure 3.9. For synchronous update, however, the values to be updated are first stored in the device, and all analog output channels are updated synchronously when the synchronous write command is sent. This is shown in Figure 3.10.

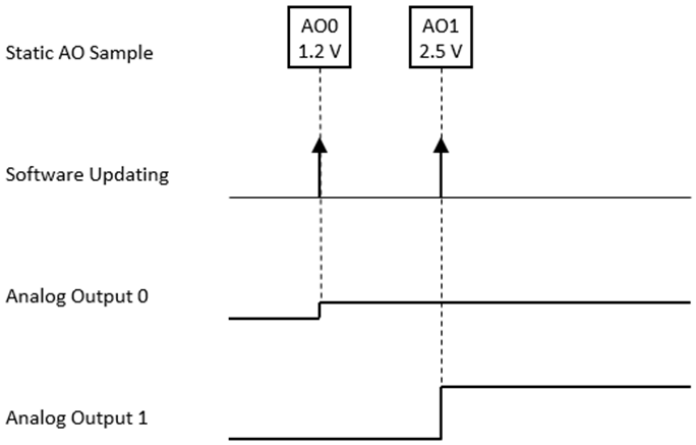


Figure 3.9 Analog output asynchronous update.

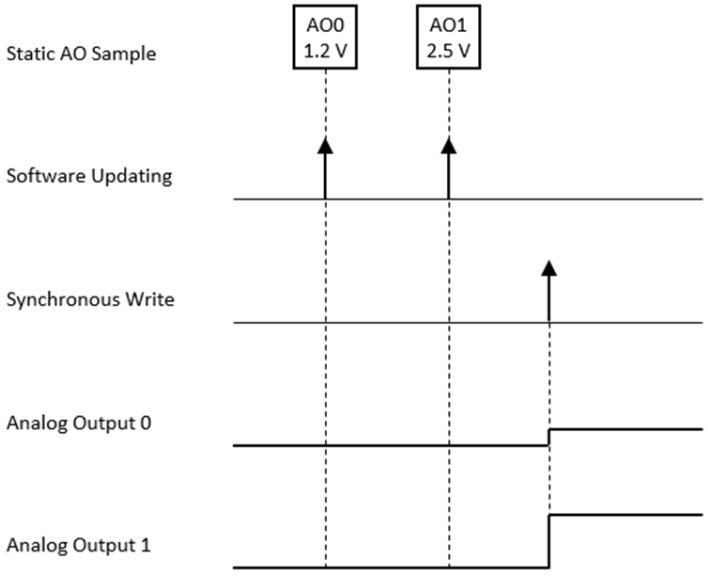


Figure 3.10 Analog output synchronous update.

3.2.4.2 Buffered (Hardware-Timed) Analog Output Generation

With buffered generation, a hardware signal called sample clock controls the rate and time of generation as shown in Figure 3.11. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

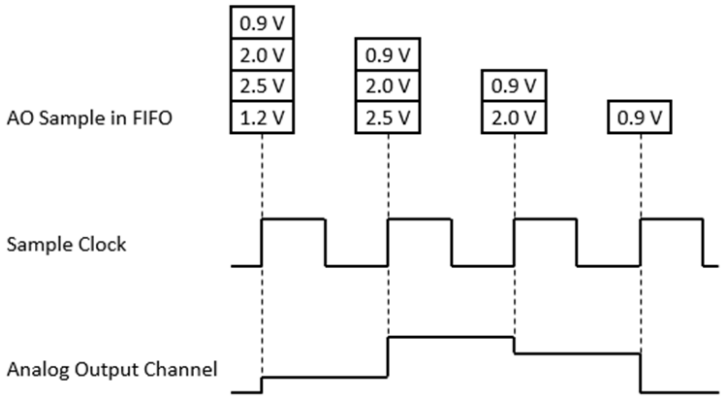


Figure 3.11 Buffered (hardware-timed) analog output generation.

The samples to be generated are provided by the application. They are first stored in the buffer of the PC, moved to the onboard first-in-first-out (FIFO) memory of the device by a direct memory access (DMA) engine, and converted by the DAC one sample at a time. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the onboard FIFO. Because the data is moved in large blocks instead of one point at a time, buffered generation typically allow much higher transfer rates. Buffered generation is also called hardware-timed generation.\

The advantages of buffered generation over static update include:

- The generation (update) rate can be much higher.
- The time of sample is deterministic.
- Hardware triggers can be used.

3.2.5 Configuration for Buffered Analog Output Generation

According to software configurations, buffered analog output generation can be classified into two types:

- One-buffered analog output generation
- Streaming analog output generation

3.2.5.1 One-Buffered Analog Output Generation

For one-buffered generation, only a specified number of samples is generated. The generation starts when a start trigger is received and automatically stops when the specified number of samples is generated. An example of 5-sample generation is shown in Figure 3.12.

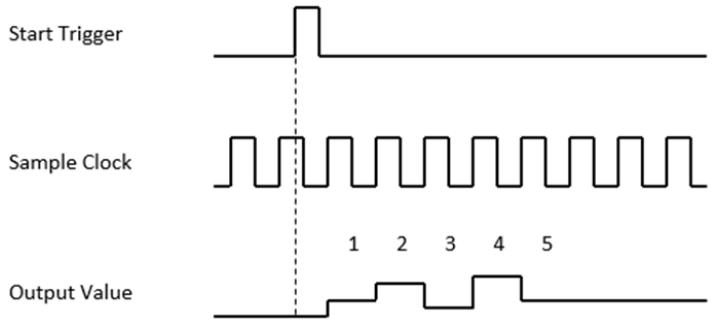


Figure 3.12 One-buffered generation.

The start trigger can be a software command or a hardware signal. If a hardware signal is used as the start trigger, the start of generation can be delayed for a specified number of sample clock cycles after a start trigger is received. Figure 3.13 shows an example of a 2-sample delay post-trigger generation. Refer to the device specifications for possible signal sources.

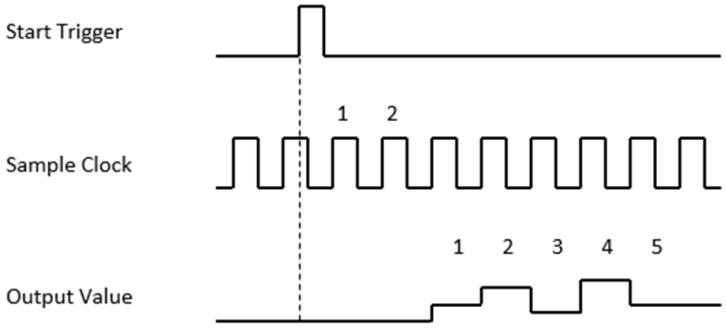


Figure 3.13 One-buffered generation with delay.

3.2.5.2 Streaming Analog Output Generation

For a streaming generation, the number of samples to be generated is set to infinite. The generation starts when a start trigger is received and continues until a stop trigger is received as shown in Figure 3.14.

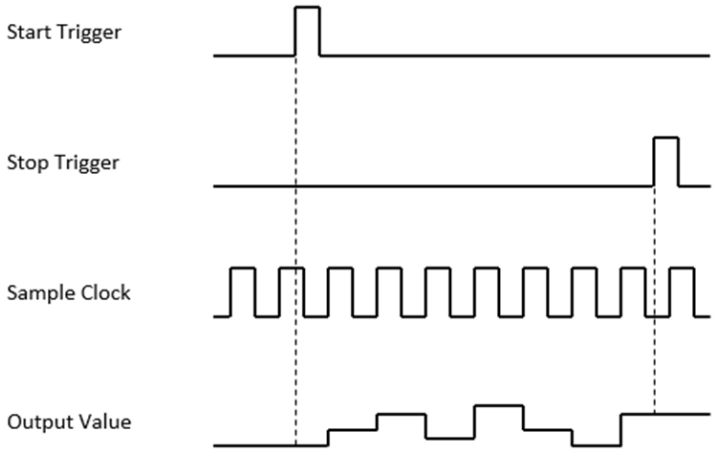


Figure 3.14 Streaming generation.

Both the start trigger and the stop trigger can come from a software command or a hardware signal. If a hardware signal is used, the start (for the start trigger) or the stop (for the stop trigger) of the generation can also be delayed. Refer to the device specifications for possible signal sources.

3.3 Digital Input

3.3.1 Digital Input Acquisition Methods

The device supports both instant (software-timed) and buffered (hardware-timed) digital input acquisitions.

3.3.1.1 Instant (Software-Timed) Digital Input Acquisition

With instant acquisition, the software controls the rate and time of acquisition, which is thus also called software-timed acquisition. Whenever the software sends a read command, the current status of digital input ports is returned as shown in Figure 3.15.

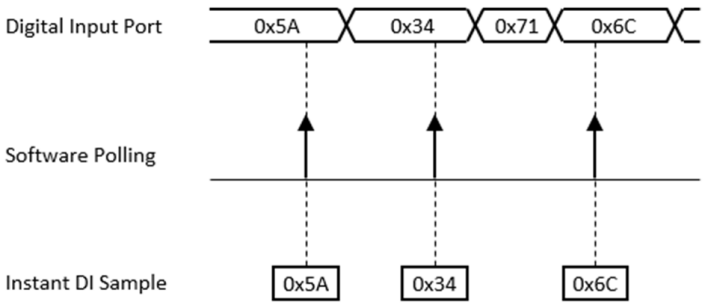


Figure 3.15 Instant (software-timed) digital input acquisition.

The advantage of instant acquisition is low latency. It is typically used for reading a single sample of digital input.

3.3.1.2 Buffered (Hardware-Timed) Digital Input Acquisition

With buffered acquisition, a hardware signal called sample clock controls the rate and time of acquisition as shown in Figure 3.16. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

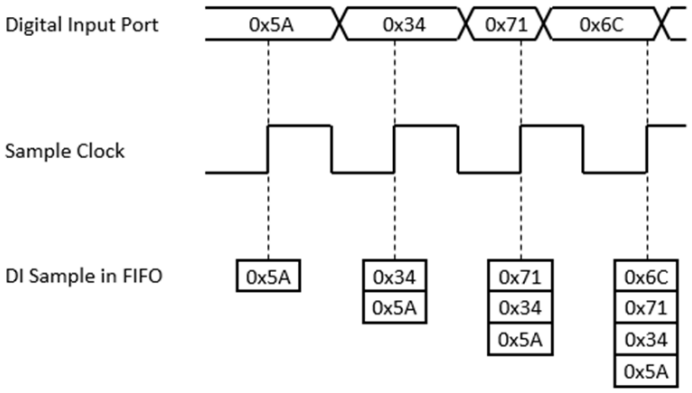


Figure 3.16 Buffered (hardware-timed) digital input acquisition.

The acquired samples are first accumulated in the onboard first-in-first-out (FIFO) memory of the device, and then moved to the buffer in the PC by a direct memory access (DMA) engine. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the application memory. Because the data is moved in large blocks instead of one point at a time, buffered acquisition typically allow much higher transfer rates. Buffered acquisition is also called hardware-timed acquisition.

The advantages of buffered acquisition over instant acquisition include:

- The sample rate can be much higher.
- The time of sample is deterministic.
- Hardware triggers can be used.

3.3.2 Configuration for Buffered Digital Input Acquisition

According to software configurations, buffered digital input acquisition can be classified into two types:

- One-buffered digital input acquisition
- Streaming digital input acquisition

3.3.2.1 One-Buffered Digital Input Acquisition

For one-buffered acquisition, only a specified number of samples is acquired. Both the start and stop of acquisition are controlled by software commands. Only one type of acquisition can be achieved: post-trigger acquisition.

Post-Trigger Acquisition

A post-trigger acquisition acquires a specified number of samples after the start trigger. The acquisition starts when a start trigger is received and automatically stops when the specified number of samples is acquired. An example of 5-sample post-trigger acquisition is shown in Figure 3.17.

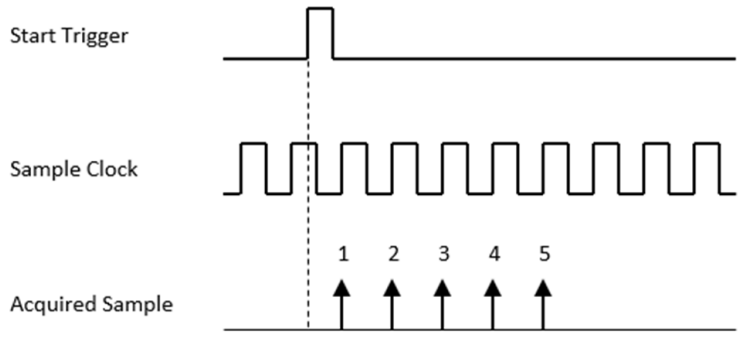


Figure 3.17 Post-trigger acquisition.

3.3.2.2 Streaming Digital Input Acquisition

For a streaming acquisition, the number of samples to be acquired is set to infinite. The acquisition starts when a start trigger is received and continues until a stop trigger is received as shown in Figure 3.18.

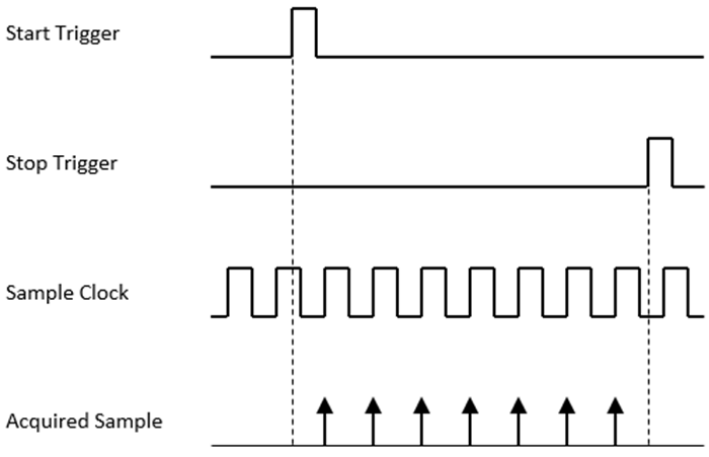


Figure 3.18 Streaming acquisition.

Both the start trigger and the stop trigger can come from a software command or a hardware signal. If a hardware signal is used, the start (for the start trigger) or the stop (for the stop trigger) of the acquisition can also be delayed. Refer to the device specifications for possible signal sources.

3.3.3 Digital Input Interrupt

Some of the digital input channels can generate a software interrupt (or event) to notice the application about the state change of input signals. Interrupts can occur at rising edge, falling edge, or both edges of the digital input signal for selected channels as shown in Figure 3.19, Figure 3.20, and Figure 3.21, respectively. The enable/disable of interrupt generation and the edges for generation can be configured independently for each channel. Refer to the device specifications for the digital input interrupt supported channels.

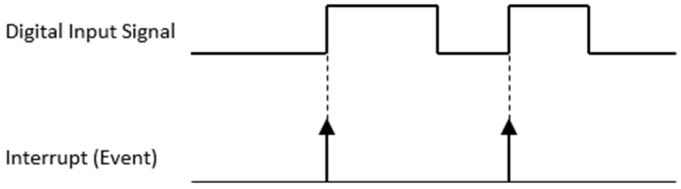


Figure 3.19 Digital input interrupt at rising edges.

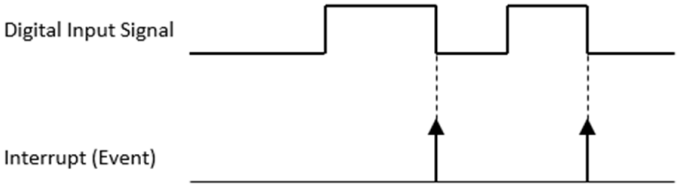


Figure 3.20 Digital input interrupt at falling edges.

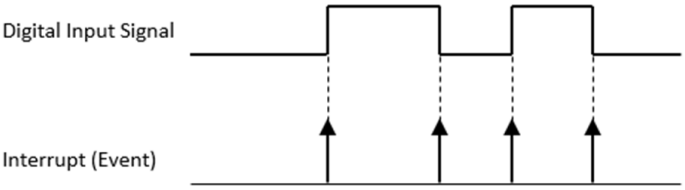


Figure 3.21 Digital input interrupt at both edges.

3.3.4 Digital Input Pattern Match Interrupt

A software interrupt (or event) can be generated by detecting a specific pattern of a digital input port (each port consists of 8 channels). Each channel in the port can be enabled or disabled the detection independently. For example, if channels 0, 1, 2, 3, 6, and 7 of a digital input port is pattern match detect enabled, and the pattern is “10xx0100” (channels 7 through 0, where x indicates a don’t care bit), an interrupt will be generated as shown in Figure 3.22.

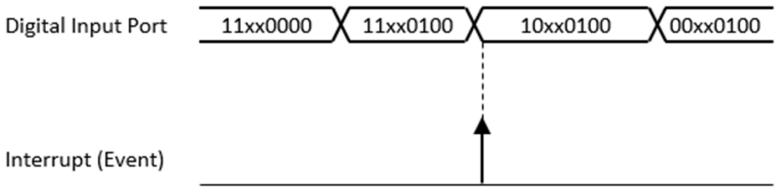


Figure 3.22 Digital input pattern match interrupt for pattern “10xx0100”.

3.3.5 Digital Input Debounce Filter

To prevent false results such as redundant interrupts (as shown in Figure 3.23) due to noise or bouncing in the digital input signal, the digital input debounce filter can be enabled. When enabled, transient pulses with duration shorter than the filter duration will be considered as glitches and will not present in the filtered digital input signal. The transition of the original signal propagates to the filtered signal only after it is stable for at least filter duration. This is shown in Figure 3.24.

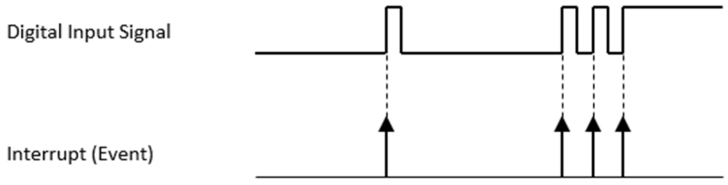


Figure 3.23 Digital input without debounce filter.

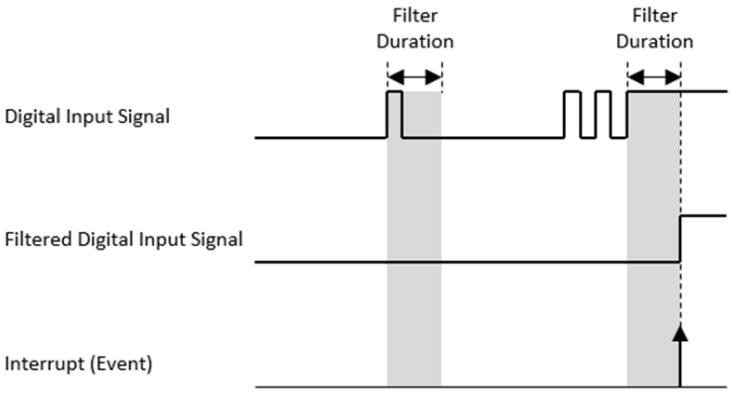


Figure 3.24 Digital input with debounce filter.

When the digital input debounce filter is enabled, an internal filter sample clock is enabled accordingly. The half-period of the filter sample clock is equal to the configured filter duration. The digital input signal is sampled at each rising edge and falling edge of the filter sample clock. The transition of the original signal propagates to the filtered signal only when it is stable for two consecutive filter sample clock edges as shown in Figure 3.25. Due to the uncertainty of relative time between original signal edge and filter sample clock edge, transient pulse of the original signal with width between 1 to 2 times the filter duration may or may not be filtered. However, pulse width which is longer than 2 times the filter duration will not be filtered, and that is shorter than the filter duration will be filtered.

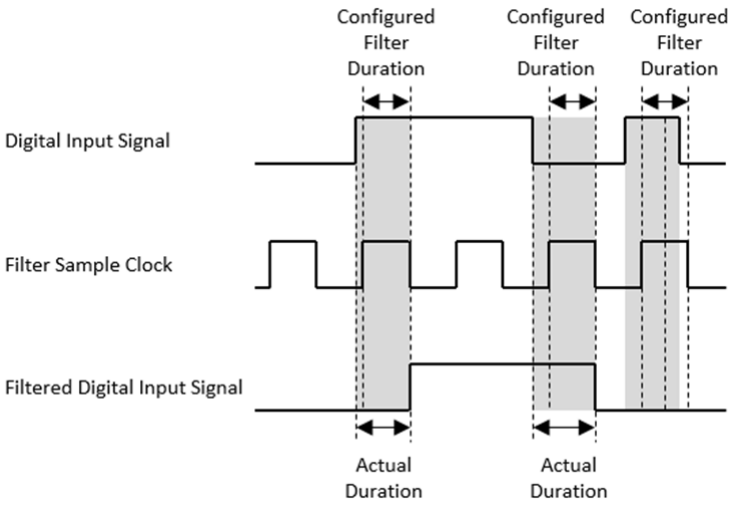


Figure 3.25 Debounce filter sample clock.

Digital input debounce filter can be enabled or disabled independently for each channel, and filter duration can be configured by ports (each port consists of 8 channels). Refer to the device specifications for the allowable filter duration.

3.3.6 Digital Input Status Latch

When a software interrupt (or event) is generated due to digital input status changed detection mentioned above, the status of the corresponding digital input port at that time is latched and can be read back by a software command. This is shown in Figure 3.26.

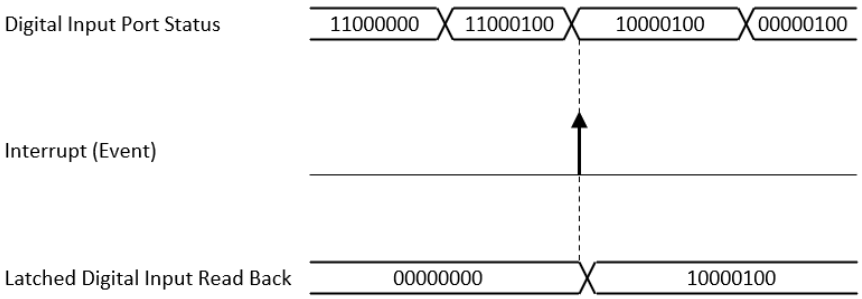


Figure 3.26 Digital input status latch.

3.4 Digital Output

3.4.1 Digital Output Data Generation Methods

The device supports both static (software-timed) digital output update and buffered (hardware-timed) digital output generation.

3.4.1.1 Static (Software-Timed) Digital Output Update

With static update, the software controls the rate and time of date, which is thus also called software-timed update. Whenever the software sends a write command, the state of digital output ports is updated as shown in Figure 3.27.

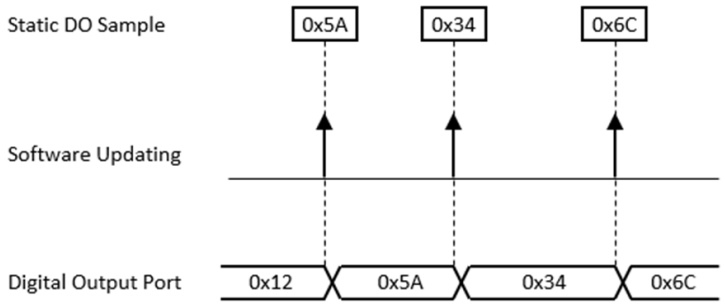


Figure 3.27 Static (software-timed) digital output update.

The advantage of state update is low latency. It is typically used for writing a single value of digital output.

3.4.1.2 Buffered (Hardware-Timed) Digital Output Generation

With buffered generation, a hardware signal called sample clock controls the rate and time of generation as shown in Figure 3.28. The sample clock can be generated internally on the device or be provided externally. Refer to the device specifications for supported sample clock sources and the maximum allowable frequency of sample clock.

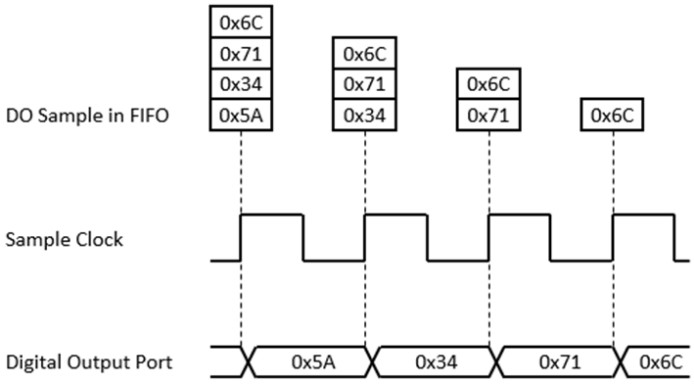


Figure 3.28 Buffered (hardware-timed) digital output generation.

The samples to be generated are provided by the application. They are first stored in the buffer of the PC, moved to the onboard first-in-first-out (FIFO) memory of the device by a direct memory access (DMA) engine, and placed on the digital output channels one sample at a time. A buffer is a block of memory in the PC for temporarily storing the data to be transferred to the onboard FIFO. Because the data is moved in large blocks instead of one point at a time, buffered generation typically allow

much higher transfer rates. Buffered generation is also called hardware-timed generation.

The advantages of buffered generation over static update include:

- The generation (update) rate can be much higher.
- The time of sample is deterministic.
- Hardware triggers can be used.

3.4.2 Configuration for Buffered Digital Output Generation

According to software configurations, buffered digital output generation can be classified into two types:

- One-buffered digital output generation
- Streaming digital output generation

3.4.2.1 One-Buffered Digital Output Generation

For one-buffered generation, only a specified number of samples is generated. The generation starts when a start trigger is received and automatically stops when the specified number of samples is generated. An example of 5-sample generation is shown in Figure 3.29.

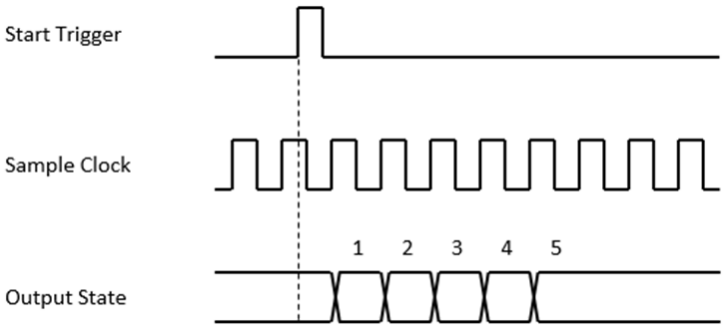


Figure 3.29 One-buffered generation.

The start trigger can be a software command or a hardware signal. If a hardware signal is used as the start trigger, the start of generation can be delayed for a specified number of sample clock cycles after a start trigger is received. Figure 3.30 shows an example of a 2-sample delay post-trigger generation. Refer to the device specifications for possible signal sources.

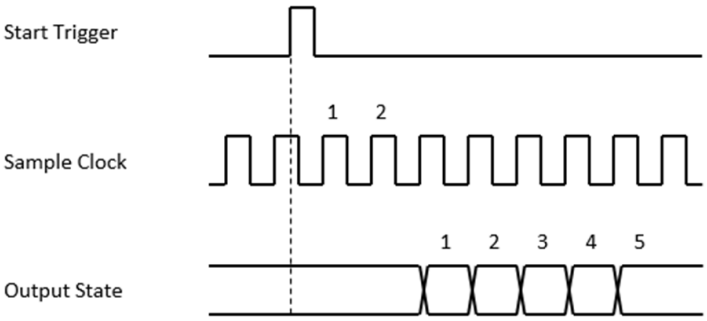


Figure 3.30 One-buffered generation with delay.

3.4.2.2 Streaming Digital Output Generation

For a streaming generation, the number of samples to be generated is set to infinite. The generation starts when a start trigger is received and continues until a stop trigger is received as shown in Figure 3.31.

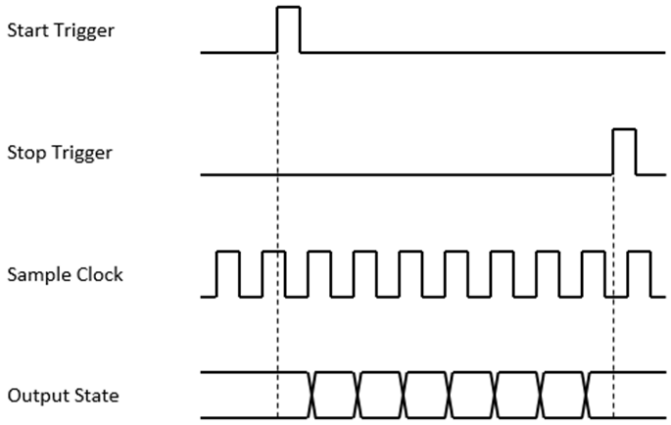


Figure 3.31 Streaming generation.

Both the start trigger and the stop trigger can come from a software command or a hardware signal. If a hardware signal is used, the start (for the start trigger) or the stop (for the stop trigger) of the generation can also be delayed. Refer to the device specifications for possible signal sources.

3.5 Counter

3.5.1 Event Counting

In event counting mode, the counter counts the number of edges the counter clock signal generates. It can be configured as rising edge active or falling edge active, as shown in Figure 3.32 and Figure 3.33, respectively.

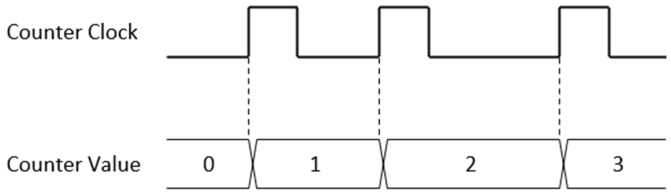


Figure 3.32 Rising edge event counting.

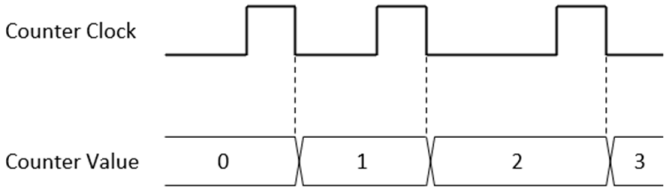


Figure 3.33 Falling edge event counting.

Counting may be temporarily paused by the counter gate signal as shown in Figure 3.34.

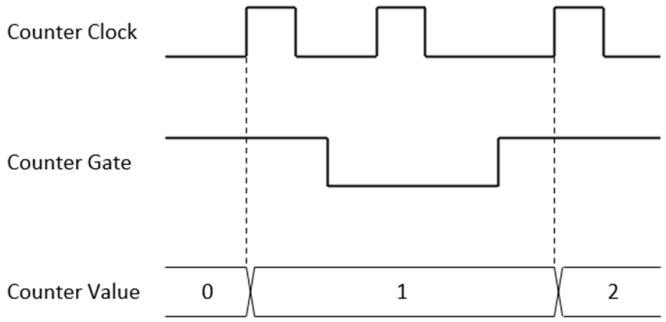


Figure 3.34 Event counting with pause gate.

3.5.1.1 Instant (Software-Timed) Event Counting

With instant event counting, the software controls the rate and time of reading counter value, which is thus also called software-timed event counting. Whenever the software sends a read command, the current value of the counter is returned as shown in Figure 3.35.

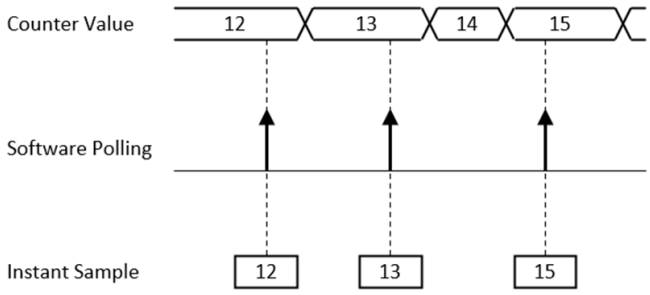


Figure 3.35 Instant (software-timed) event counting.

The advantage of instant event counting is low latency. It is typically used for reading a single sample of counter value.

3.5.2 Frequency Measurement

In frequency measurement mode, the frequency of the counter clock signal is measured by one of the two measuring methods: Period inversion or counting number of pulses in fixed duration.

3.5.2.1 Period Inversion

In this method, the period of the counter clock signal is first measured by an internal high frequency clock. The frequency of the signal is then calculated by inverting the period value. This is shown in Figure 3.36 and by the following equation.

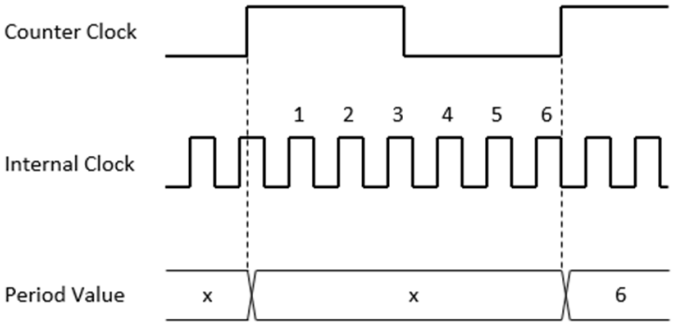


Figure 3.36 Frequency measurement by period inversion.

$$Frequency = \frac{1}{Period} = \frac{1}{InternalClockCount \times InternalClockPeriod}$$

This method is suitable if the counter clock signal frequency is much smaller (< 0.1%) than the internal clock frequency. Measuring accuracy degrades as the counter clock signal frequency increases.

3.5.2.2 Counting Number of Pulses in Fixed Duration

In this method, the pulse number of the counter clock signal is measured in a fixed time duration. The frequency of the signal is then calculated by dividing this number by the time duration. This is shown in Figure 3.37 and by the following equation.

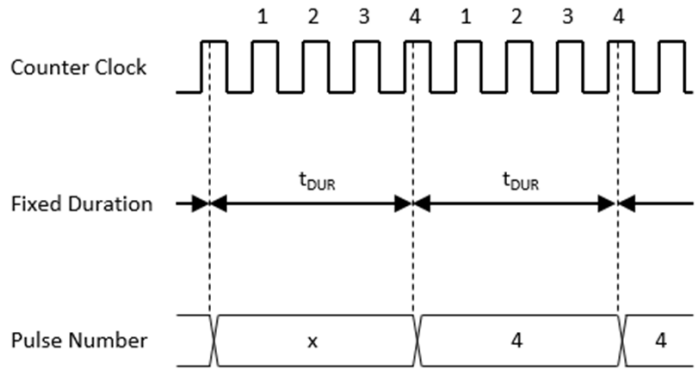


Figure 3.37 Frequency measurement by counting number of pulses in fixed duration.

$$Frequency = \frac{PulseNumber}{t_{DUR}}$$

For counter clock signal frequency higher than that specified in the previous section, this method gives a more accurate result.

3.5.3 One-Shot (Delayed Pulse Generation)

In one-shot mode, when an active edge of gate signal is detected, a pulse will be generated after the specified number source clock counts. The pulse width is one period of the source clock. Figure 3.38 shows an example of high-pulse, 5-clock delay one-shot output.

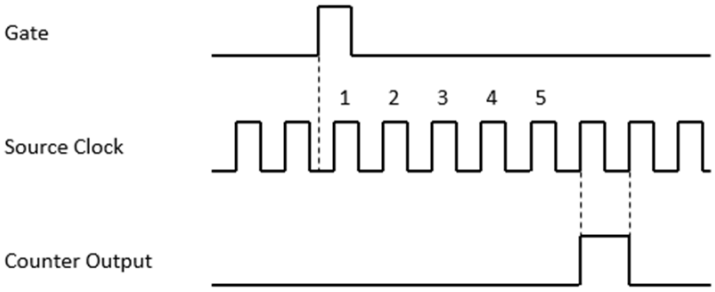


Figure 3.38 One-shot operation.

3.5.4 Timer/Pulse

In timer/pulse mode, continuous pulses with specified frequency are generated at counter output terminal, and an interrupt is also generated with each pulse as shown in Figure 3.39.

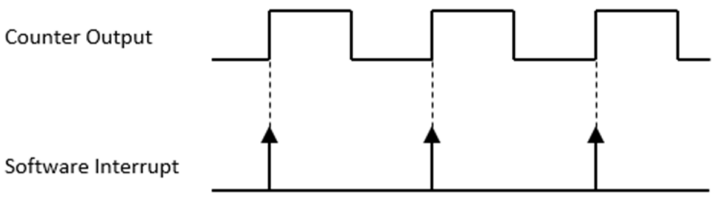


Figure 3.39 Pulse output and timer interrupt.

The output can be gated. If counter gate is in active level, pulses are output normally. On the other hand, if counter gate is in inactive level, output is disabled. Figure 3.40 shows an example of active high gate.

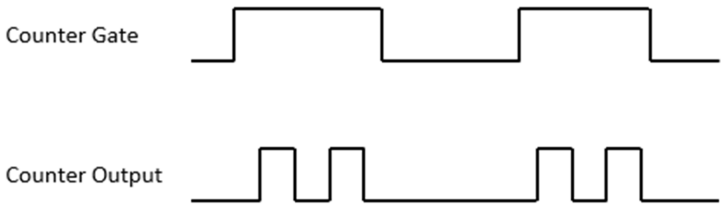


Figure 3.40 Gated timer/pulse output.

3.5.5 Pulse Width Modulation Output

In pulse width modulation output mode, a pulse waveform with specified high period (tHIGH) and low period (tLOW) is output at counter output terminal as shown in Figure 3.41.

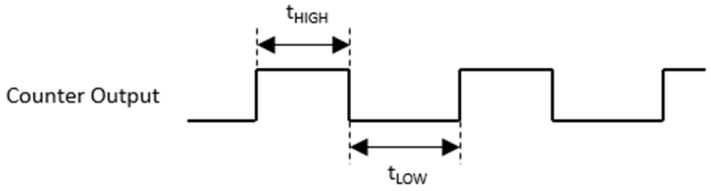


Figure 3.41 Pulse width modulation output.

The output can be gated. If counter gate is high, pulses are output normally. On the other hand, if counter gate is low, output is disabled. This is shown in Figure 3.42.

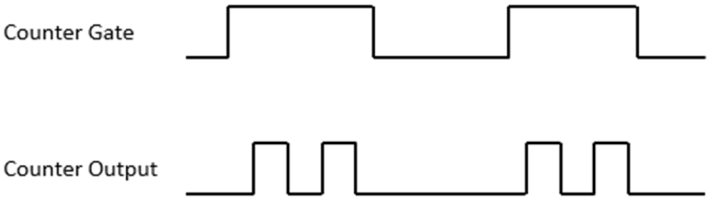


Figure 3.42 Gated pulse width modulation output.

3.6 Timing Signals

3.6.1 Clock Signal

The clock signal can be generated internally or provided from an external source. For the internal clock, when configuration is done, the clock frequency cannot be changed on the fly during the acquisition or generation operation. For the external clock, on the other hand, clock frequency can be controlled by the external source in real time.

3.6.2 Synchronization

To synchronize the acquisition of multiple devices, all the devices must use the same clock signal. One of the devices needs to be selected to be the master device, and others are slave devices. The master device may generate a clock signal internally, or accept them from an external source. It then routes this signal to the output terminal and sends it to all the slave devices through external wirings for synchronized acquisition. To synchronize more than two devices, both daisy-chain and star topology can be used as shown in Figure 3.43 and Figure 3.44, respectively. Star topology reduces intermediate signal delay between devices. However, it also introduces signal degradation if too many loads are present for one signal source. It is recommended to keep a number of loads for one signal source to be three or less.

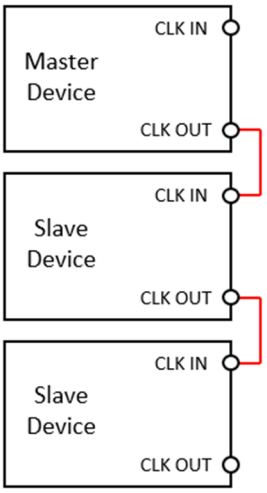


Figure 3.43 Multiple devices synchronization with daisy-chain topology.

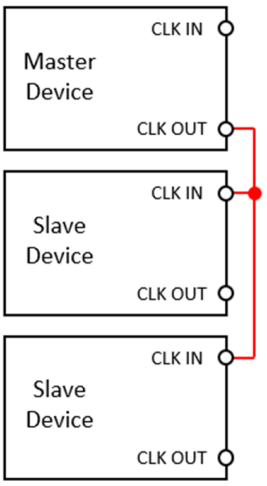


Figure 3.44 Multiple devices synchronization with star topology.

3.7 Calibration

The Navigator of Advantech DAQNavi provides a calibration utility to calibrate the analog input and analog output circuitry of the device. Figure 3.45 shows the interface of the calibration utility. Follow the instructions shown to calibrate the device. For a multi-function device, which contains both analog input and analog output functions, analog input calibration must be performed before analog output calibration.

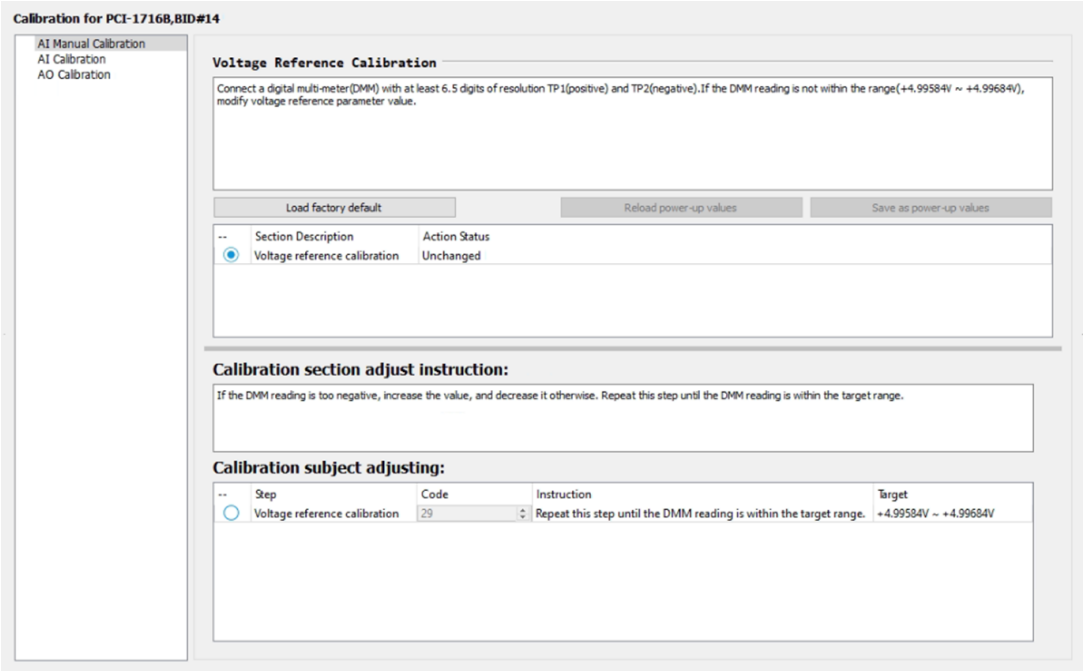


Figure 3.45 Calibration utility.

When any of the calibration parameters is changed, users can save the change by clicking “Save as power-up values” button, or can reload power-up values by clicking “Reload power-up values” button. The status of the calibration parameters is shown in “Action Status” column. If required, user can also load factory default calibration parameters by clicking “Load factory default” button.

3.8 Firmware/FPGA Code Update

The Navigator of Advantech DAQNavi provides the firmware/FPGA code download utility. Users can use this utility to update the firmware/FPGA code of the device.

Figure 3.46 shows the interface of the firmware/FPGA code download utility. To update the firmware/FPGA code, first click “Browser” button to choose the new firmware/FPGA code file. Both file version currently in the device and that of the chosen file will be shown. Then click “Download” button to start file download operation. After the download has finished, the device must be power cycled. For a PCI/PCIe device, power off the system and then power it on again. For a USB device, disconnect both the USB cable and the external power and then reconnect them again.

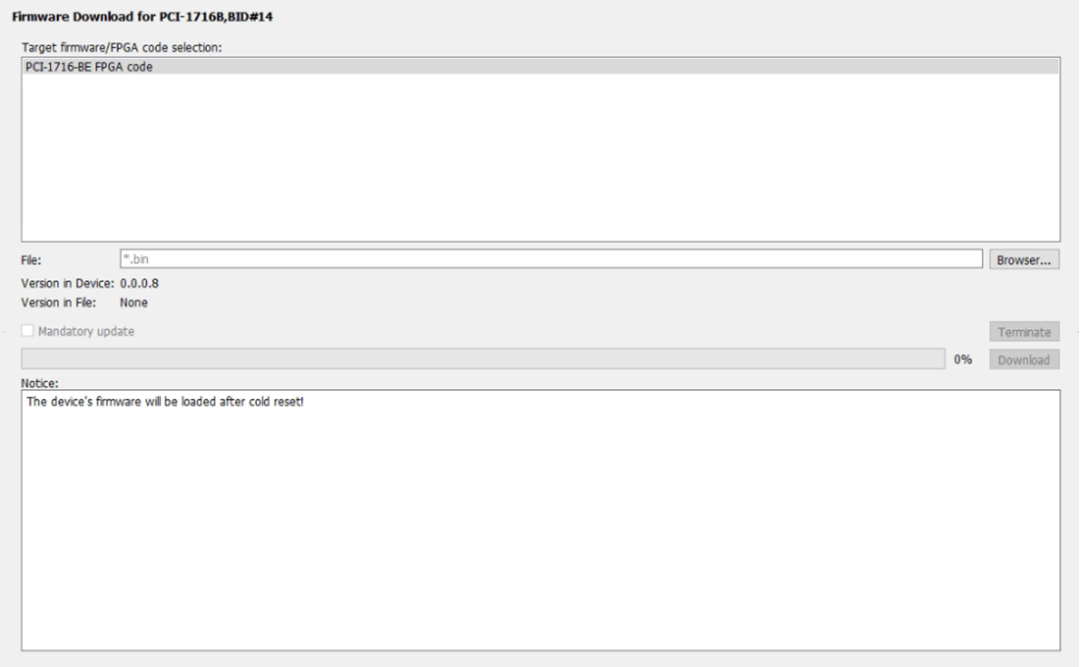


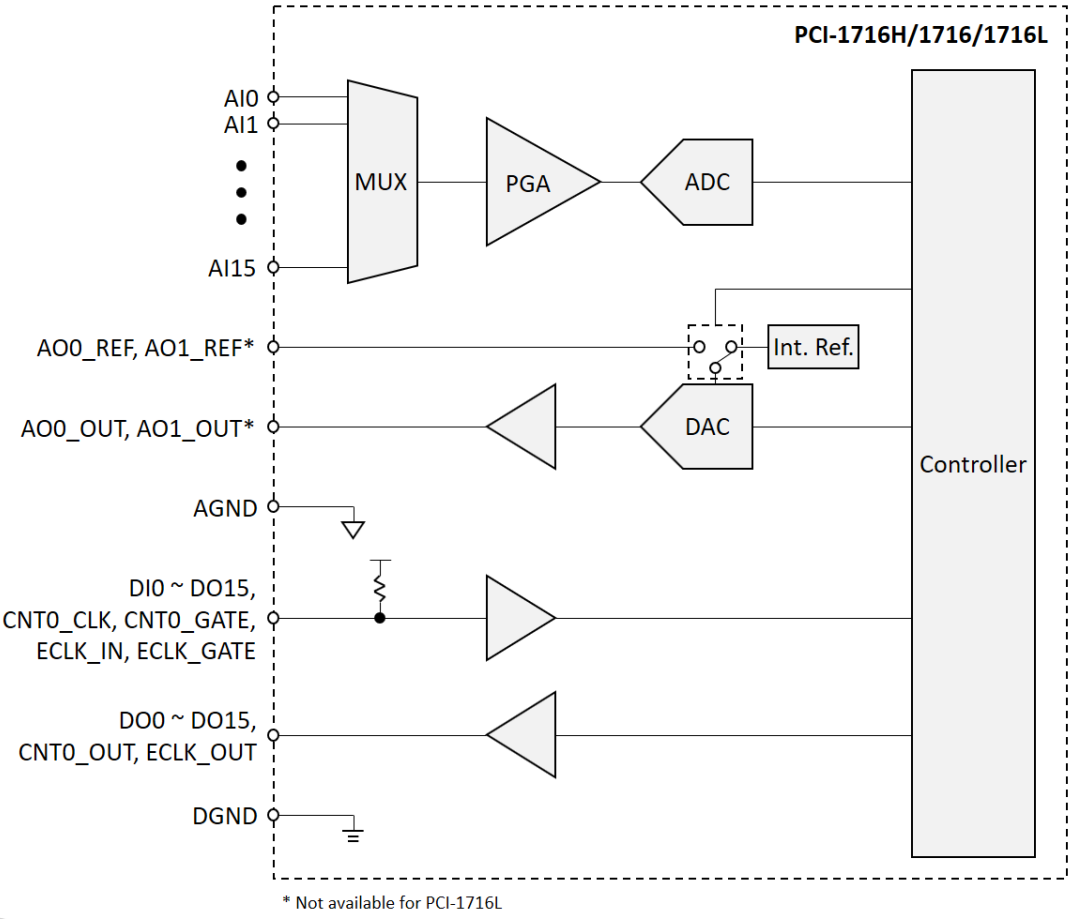
Figure 3.46 Firmware/FPGA code download utility.

Ensure that you do not turn off system power during download operation, or the download operation will fail and the current firmware/FPGA code on the device will be corrupted. If this happens, a golden pattern firmware/FPGA code will be loaded when the device is powered on next time. The golden pattern may not be the latest version file, so the user should still update to the latest version when using the utility.

Appendix A

Specifications

A.1 Function Block



A.2 Analog Input

Channels	16 single-ended, 8 differential, or combination					
Resolution	16 bits					
Convert clock rate	1 MS/s max. for PCI-1716H 250 kS/s max. for PCI-1716/L Shared by all enabled channels					
Convert clock source	Internal or external					
Data buffer size	8,192 samples Shared by all enabled channels					
Input range	±10 V, ±5 V, ±2.5 V, ±1.25 V, ±0.625 V, 0 ~ 10 V, 0 ~ 5 V, 0 ~ 2.5 V, 0 ~ 1.25 V					
Input impedance	100 MΩ typ.					
Max. input voltage	±11 V					
Input common-mode voltage range	±11 V					
Over-voltage protection	±15 V					
Linearity	INL		±1 LSB max.			
	DNL		±1 LSB max.			
DC performance	Idle channel noise		261 μV_{RMS}			
	Effective resolution		16.00 bits			
AC performance	SNR		82 dB			
	THD		-81 dB			
	THD + N		-78 dB			
	SFDR		84 dB			
	ENOB		12.73 bits			
PGA -3 dB Bandwidth	Range	±10 V	±5 V	±2.5 V	±1.25 V	±0.625 V
			0 ~ 10 V	0 ~ 5 V	0 ~ 2.5 V	0 ~ 1.25 V
	BW	4 MHz	4 MHz	2 MHz	1.5 MHz	0.65 MHz
PCI-1716/PCI-1716L Absolute Accuracy*	Range	±10 V	±5 V	±2.5 V	±1.25 V	±0.625 V
	Accuracy	±0.01%	±0.025%	±0.025%	±0.04%	±0.075%
	Range		0 ~ 10 V	0 ~ 5 V	0 ~ 2.5 V	0 ~ 1.25 V
	Accuracy		±0.025%	±0.025%	±0.04%	±0.075%
PCI-1716/PCI-1716L Absolute Accuracy**	Range	±10 V	±5 V	±2.5 V	±1.25 V	±0.625 V
	Accuracy	±0.05%	±0.125%	±0.125%	±0.2%	±0.375%
	Range		0 ~ 10 V	0 ~ 5 V	0 ~ 2.5 V	0 ~ 1.25 V
	Accuracy		±0.125%	±0.125%	±0.2%	±0.375%
PCI-1716H Absolute Accuracy*	Range	±10 V	±5 V	±2.5 V	±1.25 V	±0.625 V
	Accuracy	±0.01%	±0.025%	±0.025%	±0.04%	±0.075%
	Range		0 ~ 10 V	0 ~ 5 V	0 ~ 2.5 V	0 ~ 1.25 V
PCI-1716H Absolute Accuracy**	Accuracy		±0.025%	±0.025%	±0.04%	±0.075%
	Range	±10 V	±5 V	±2.5 V	±1.25 V	±0.625 V
	Accuracy	±0.05%	±0.125%	±0.125%	±0.2%	±0.375%
	Range		0 ~ 10 V	0 ~ 5 V	0 ~ 2.5 V	0 ~ 1.25 V

*Operating temperature within ±5°C of last auto calibration temperature

**Over full operating temperature range

A.3 Analog Output

(Not Available for PCI-1716L)

Channels	2 single-ended	
Resolution	16 bits	
Update rate	1 MS/s max. per channel	
Update clock source	Internal or external	
Data buffer size	8,192 samples Shared by all enabled channels	
Output range (internal reference)	±10 V, ±5 V, 0 ~ 10 V, 0 ~ 5 V	
Output range (external reference)	$\pm V_{REF}$, 0 ~ V_{REF}	
Power-on state	0 V @ ±10 V output range	
Driving capability	±20 mA max.	
Output impedance	0.1 Ω max.	
Linearity	INL	±1 LSB max.
	DNL	±1 LSB max.
Power-on glitch	30 mV for 10 ms	
Slew rate	20 V/μs	
Settling time	5 μs (to 4 LSBs of FSR)	
DC performance	Output noise	100 μVRMS
	Effective resolution	16 bits
	Ch-ch DC crosstalk	-140 dB
Absolute accuracy*	Range	All Ranges
	Accuracy	±0.01% of full-scale range max.
Absolute accuracy**	Range	All Ranges
	Accuracy	±0.05% of full-scale range max.

*Operating temperature within ±5°C of last auto calibration temperature

**Over full operating temperature range

A.4 Digital Input

Channels	16 (2 ports)	
Sample rate	1 MS/s max.	
Sample clock source	Internal or external	
Data buffer size	4,096 samples	
Input type	5 V TTL	
Input logic level	Logic high	2.0 V min.
	Logic low	0.8 V max.
	Working voltage	-0.25 V ~ 5.25 V
Input protection voltage	-0.5 V ~ 6.5 V	
Pull-up resistor	10 kΩ	
Response time	25 ns max.	
Debounce filter	25 ns ~ 105 ms	
Edge detection	Rising/falling/both edges	
Pattern match detection	By port detection	
State latch	Latch port state when interrupt occurs	

A.5 Digital Output

Channels	16 (2 ports)	
Update rate	1 MS/s max.	
Update clock source	Internal or external	
Data buffer size	4,096 samples	
Output type	5 V TTL	
Output logic level	Logic high	4.0 V min. @ 2 mA
	Logic low	0.4 V max. @ 2 mA
Load current	One channel	8 mA max.
	Per port summed	20 mA max.
Response time	25 ns max.	

A.6 Counter

Channels	1	
Resolution	32 bits	
Input type	5 V TTL	
Input logic level	Logic high	2.0 V min.
	Logic low	0.8 V max.
	Working voltage	-0.25 V ~ 5.25 V
Input protection voltage	-0.5 V ~ 6.5 V	
Pull-up resistor	10 kΩ	
Response time	25 ns max.	
Debounce filter	25 ns ~ 105 ms	
Output type	5 V TTL	
Output logic level	Logic high	4.0 V min. @ 2 mA
	Logic low	0.4 V max. @ 2 mA
Load current	8 mA max.	
Event counting	Input frequency	10 MHz max.
	Clock polarity	Rising/falling
	Gate function	Enabled/disabled
	Gate polarity	High/low active
Frequency measurement	Input frequency	0.1 Hz ~ 10 MHz
	Accuracy	F_{IN}/40 MHz or 50 ppm, whichever is larger
One shot	Internal clock frequency	10 MHz, 1 MHz, 100 kHz, 10 kHz
	Internal clock accuracy	50 ppm
	External clock frequency	10 MHz max.
	Delay count	1 ~ 4,294,967,295
	Gate polarity	Rising/falling
Timer/pulse	Timebase clock frequency	40 MHz
	Timebase clock accuracy	50 ppm
	Output frequency	0.1 Hz ~ 10 MHz
	Gate function	Enabled/disabled
	Gate polarity	High/low active

A.7 External Clock Input

Input type	5 V TTL	
Input logic level	Logic high	2.0 V min.
	Logic low	0.8 V max.
	Working voltage	-0.25 V ~ 5.25 V
Polarity	Rising edge	
Input protection voltage	-0.5 V ~ 6.5 V	
Pull-up resistor	10 kΩ	
Minimum width	100 ns	

A.8 External Clock Gate Input

Input type	5 V TTL	
Input logic level	Logic high	2.0 V min.
	Logic low	0.8 V max.
	Working voltage	-0.25 V ~ 5.25 V
Polarity	Low level pause	
Input protection voltage	-0.5 V ~ 6.5 V	
Pull-up resistor	10 kΩ	

A.9 External Clock Output

Output type	5 V TTL	
Output logic level	Logic high	4.0 V min. @ 2 mA
	Logic low	0.4 V max. @ 2 mA
Load current	8	mA max.

A.10 General

Power consumption	+5 V: 500 mA typ., 800 mA max. +12 V: 150 mA typ., 400 mA max.
Power supply output	+5 V (±5%): 200 mA max. +12 V (±5%): 100 mA max.
Dimension	175 x 100 x 18 mm3 (6.9 x 3.9 x 0.7 in.3)
Weight	108 g
I/O connector	68-pin SCSI
Form factor	PCI Universal
Operating temperature	0°C to 60°C (32°F to 140°F)
Storage temperature	-20°C to 70°C (-4°F to 158°F)
Operating humidity	10% to 90% RH, non-condensing
Storage humidity	5% to 95% RH, non-condensing

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