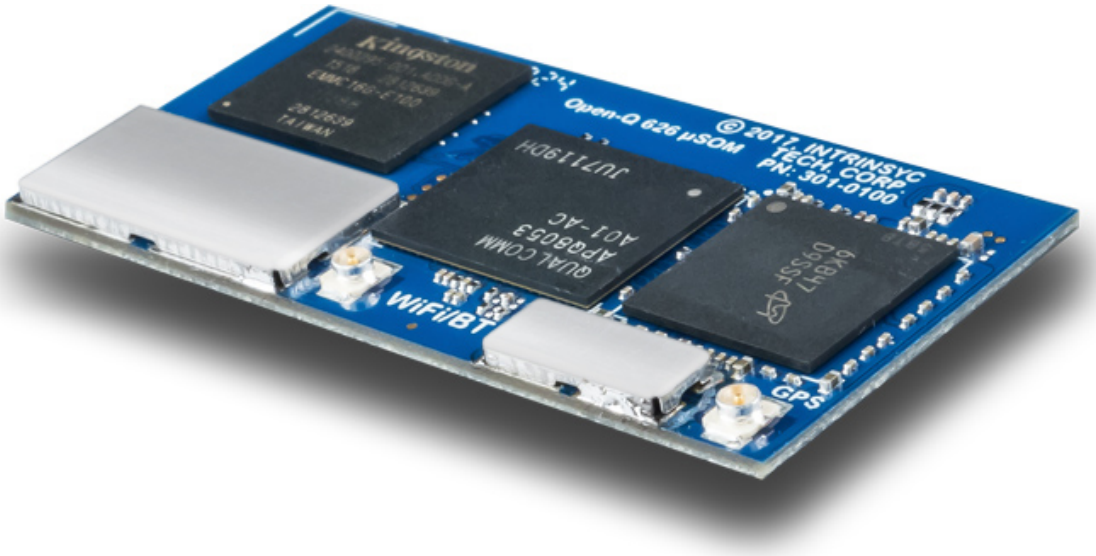

Open-Q 626 µSOM HW Device Specification

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1. INTRODUCTION

This document applies to the Open-Q 626 µSOM. Technical specifications for other SOMs in the Intrinsyc product line are covered under separate documents.

1.1 Purpose

The purpose of this document is to provide the technical specifications of the Intrinsyc Open-Q 626 µSOM.

1.2 Scope

This document covers the following information on the Open-Q 626 µSOM:

- Electrical and mechanical specifications
- SOM pin-out
- Device handling and packaging
- Ordering information.

1.3 Intended Audience

This document is intended for users who wish to understand the technical specifications of the Intrinsyc Open-Q 626 µSOM.

1.4 Acronyms and Abbreviations

Acronym / Abbreviation	Definition
ANT	ANTenna
BAT, BATT	BATTery
BAM	Bus Access Manager
BLSP	BAM-based Low-Speed Peripheral
BOM	Bill Of Materials
BT	Blue Tooth
CLK	Clock
CPU	Central Processing Unit
CS	Chip Select
CSI	Camera Serial Interface
DSI	Display Serial Interface
EMI	Electro-Magnetic Interference
EN	ENable
ERM	Eccentric Rotating Mass
ESD	Electro-Static Discharge
GND	GrouND
GPIO	General Purpose I/O
GPS	Global Positioning System
HDMI	High Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
INT	INTerrupt
JTAG	Joint Test Action Group

Acronym / Abbreviation	Definition
LDO	Low Drop-Out
LRM	Linear Resonant Actuator
LTE	Long-Term Evolution
LPI	Low Power Island
MDP	Mobile Display Port
MI2S	Mobile Inter-IC Sound
MIC	MICrophone
MIPI	Mobile Industry Processor Interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
PCB	Printed Circuit Board
PCIE	Peripheral Component Interconnect Express
PWM	Pulse-Width Modulation
QUP	Qualcomm Universal Peripheral
RF	Radio Frequency
RX	Receive
SCL	Serial CLock
SDA	Serial DAta
SDC	Secure Digital Interface
SOM	System On Module
SPI	Serial Peripheral Interface
SSC	Snapdragon Sensor Core
TX	Transmit
UART	Universal Asynchronous Receiver/Transmiter
UIM	User Interface Module
USB	Universal Serial Bus
WLAN	Wireless Local Area Network

1.5 Signal Name Suffix

Suffix	Definition
_N	Indicates that the signal is ACTIVE LOW
_P/N	Identifies the two signals comprising a differential pair

2. DOCUMENTS

This section lists any parent and supplementary documents for the Open-Q 626 µSOM Device Specification. Unless stated otherwise, applicable documents supersede this document and reference documents provide background and supplementary information.

2.1 Applicable Documents

REFERENCE	AUTHOR	TITLE
A-1	Intrinsyc	Intrinsyc Purchase and Software License Agreement for the Open-Q 626 µSOM

2.2 Reference Documents

Available at http://tech.intrinsyc.com (dev kit registration required).

REFERENCE	TITLE
R-1	Open-Q 626 µSOM Development Kit – User Guide
R-2	Open-Q 626 µSOM – Carrier Board Design Guide
R-3	Open-Q 626 µSOM Schematics (SOM and Carrier)
R-4	Open-Q 626 µSOM Modular Certification OEM Integrator Instructions

3. SUMMARY OF FEATURES

The Open-Q 626 µSOM contains the core of the Snapdragon 626 architecture. Measuring in at 50mm x 25mm, the SOM is where all the processing occurs. It connects to a carrier board via three 100 pin Hirose DF40 connectors which allows essential power rails and signals to be exposed for supporting peripherals and interfaces on the platform.

3.1 SOM Block Diagram

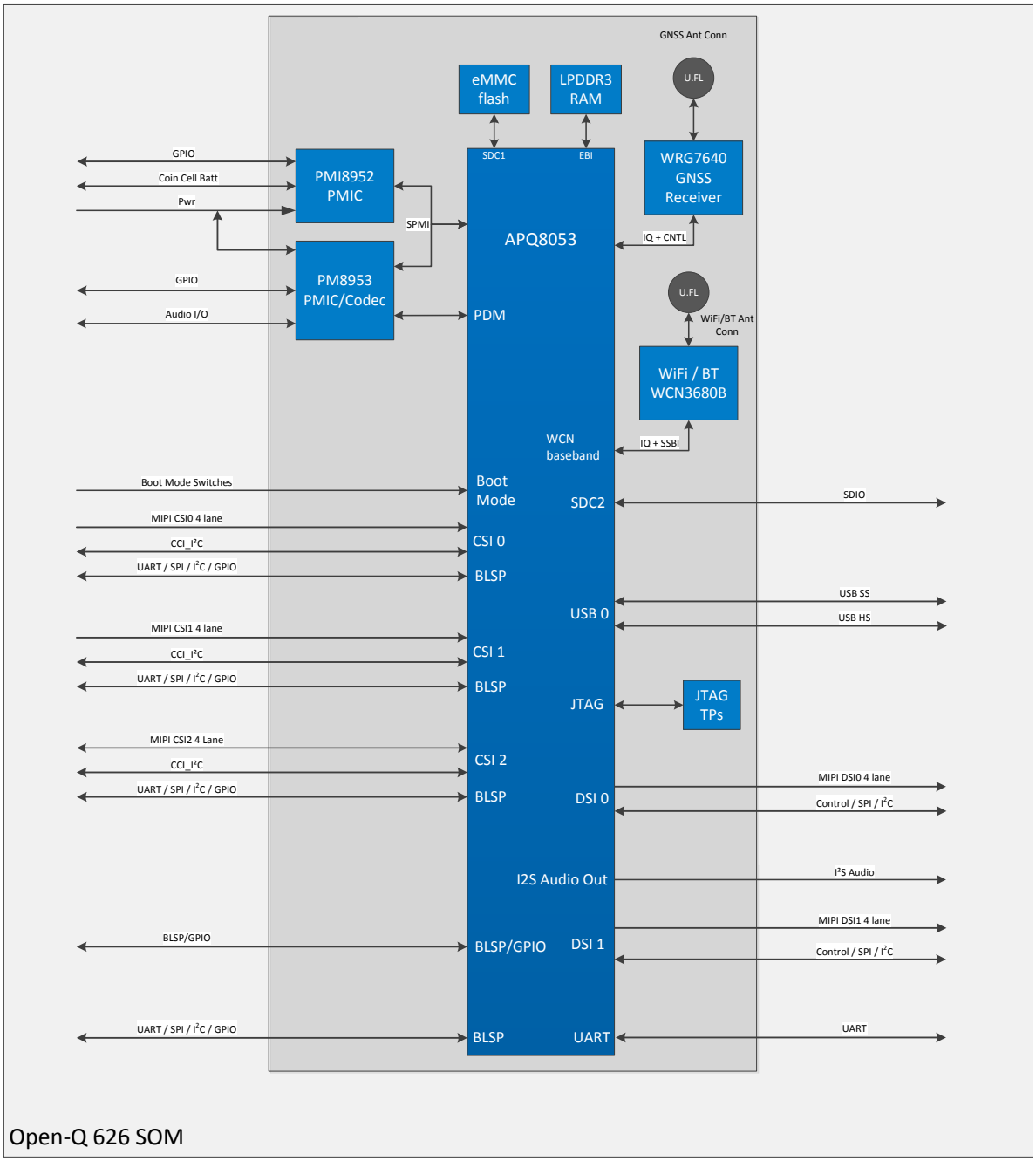

Figure 1 – Open-Q 626 µSOM Block Diagram

3.2 SOM Technical Specifications

See the table below for the Open-Q 626 µSOM technical specifications.

Table 1 – Open-Q 626 µSOM Technical Specifications

Subsystem / Connectors	Feature Set	Description	Specification
Chipset	APQ8053Pro	Qualcomm® Snapdragon™ 626 Processor	Octa-core, 64-bit ARM Cortex-A53 up to 2.2GHz. Adreno 506 GPU Hexagon 546 DSP
	PMIC (PM8953 & PMI8952)	Qualcomm® PMIC, companion power management chips for APQ8053Pro processor	NA
Memory	2GB LPDDR3	DDR3 Low Power Memory	Up to 1866MHz LPDDR3 BGA chip. Supports via 4x16bit channels
	16 GB eMMC	Primary Storage for platform. Mainly used for storing SW applications and user data etc.	eMMC v5.0 on board.
RF Connectivity	Wi-Fi 2.4 GHz/ 5GHz	Qualcomm WCN3680B Wi-Fi + BT Combo Chip	802.11a/b/g/n/ac 2.4/5.0 GHz 1X1
	BT 2.4 GHz	Qualcomm WCN3680B Wi-Fi + BT Combo Chip	Supports BT 4.2 + BR/EDR + BLE.
	GPS via WGR7640	GPS Frontend	GPS, GLONASS, COMPASS
RF Interfaces (see section below)	WLAN / BT	Antenna connector on SOM for Wi-Fi / Bluetooth.	1 x U.FL, 50 ohm coaxial connector
	GPS	Antenna connector on SOM for GPS.	1 x U.FL, 50 ohm coaxial connector
Multimedia	MIPI CSI	Three 4-lane MIPI CSI Camera interfaces	MIPI Alliance Specification v1.0
	MIPI DSI	Two 4-lane MIPI DSI Display interfaces	MIPI Alliance Specification v1.01. MIPI D-PHY Specification v0.65, v0.81, v0.90, v1.01
Audio Interfaces	Audio Outputs	Stereo Headphone output, Mono Speaker output, Mono Earpiece output	Connected from integrated audio codec in SOM PM8953 PMIC.
	Audio Inputs	3x Analog Mic inputs, 1x Stereo Digital Mic input	Connected from integrated audio codec in SOM PM8953 PMIC and Snapdragon 626 CPU.
	MI2S	2x Audio ports are routed out and configurable for MI2S or GPIO	
Digital Interfaces	USB	One USB 3.0 Type-C port	USB3.0 / USB2.0
	SDIO	One 4-bit Secure Digital interface	SD v3.0, dual voltage interface
	GPIO / I2C / SPI / UART	Configurable IO	Configurable IO exposed as GPIO or BLSP ports, giving GPIO, I2C, SPI, and UART connections options.
Connectors	3x 100-pin board to board connectors	3x Hirose 100-pin DF40C header connectors	300 pins total for connection to carrier board

4. I/O DEFINITIONS

4.1 Location of Major Components

The figures below identify the major components and connectors found on the Open-Q 626 µSOM top and bottom sides.

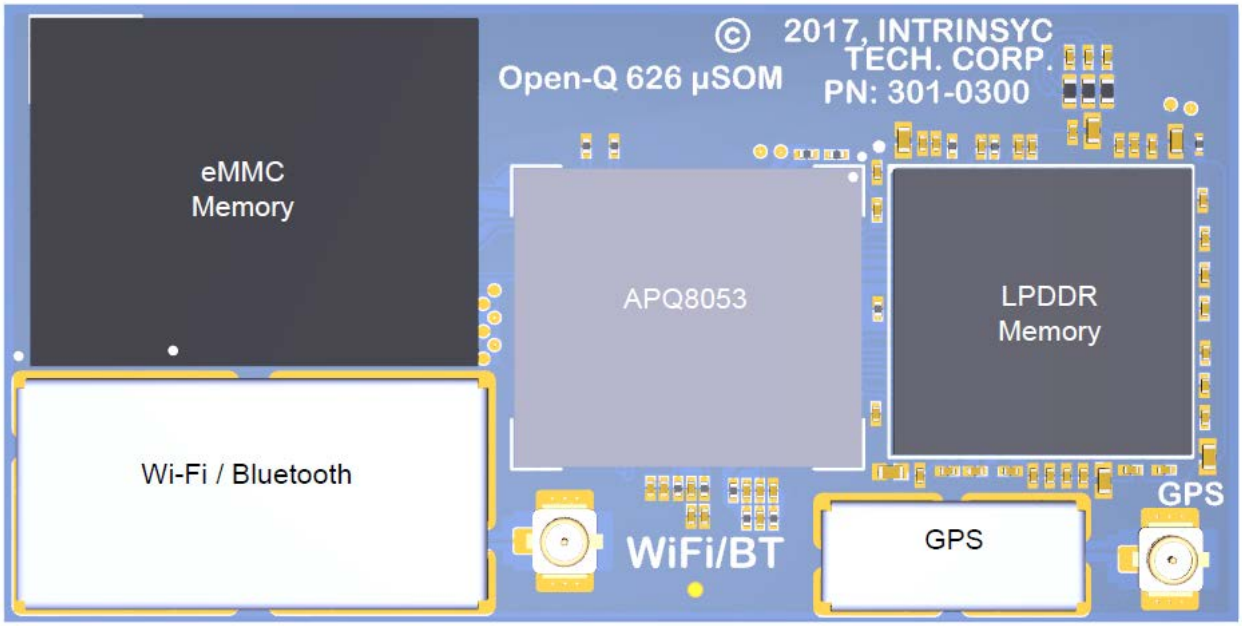

Figure 2 – Open-Q 626 µSOM Top View

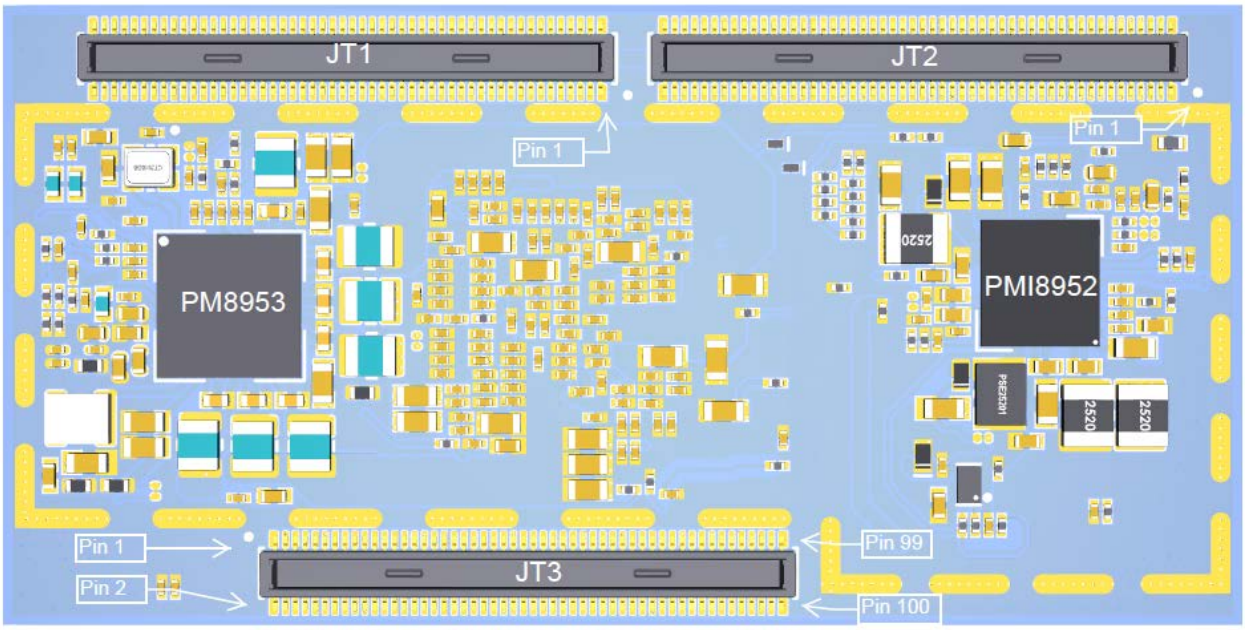

Figure 3 – Open-Q 626 µSOM Bottom View

The SOM mating connectors JT1, JT2, and JT3 are of type Hirose DF40C-100DP-0.4V(51) and are located on the bottom side of the SOM. The connector pin 1 locations are shown in the figure above (looking at bottom of SOM). Key dimensions are provided in later sections of this document. See section 6.3 for information on the available mating connectors.

4.2 B2B Connector Signal Assignments

The following tables list the pin-outs of the three Open-Q 626 µSOM board to board connectors. A more detailed description of the signal group functions can be found in document R-2 which provides background information for customers developing a custom Carrier Board for the Open-Q 626 µSOM.

Note: the SOM schematic (document R-3) is the controlling document. In the event of pin-out difference(s) between this document and the SOM schematic, the SOM schematic shall take precedence.

Table 2 – B2B Connector JT1 Pin-outs

Pin #	JT1 Signal Name	Description
1	GND	Ground reference for design.
2	GND	Ground reference for design.
3	CDC_HDS_MIC2_P	PM8953 Mic #2 input.
4	CDC_MIC3_P	PM8953 Mic #3 differential input.
5	CDC_MIC_BIAS1	PM8953 Mic Bias #1 voltage output.
6	CDC_MIC3_N	PM8953 Mic #3 differential input.
7	GND	Ground reference for design.
8	GND	Ground reference for design.
9	CDC_MIC_BIAS2	PM8953 Mic Bias #2 voltage output.
10	CDC_MIC1_N	PM8953 Mic #1 differential input.
11	GPIO_128_CAM_MCLK3	CPU GPIO128. Typically used as Camera MCLK3.
12	CDC_MIC1_P	PM8953 Mic #1 differential input.
13	GND	Ground reference for design.
14	GND	Ground reference for design.
15	GND	Ground reference for design.
16	MIPI_CSI0_CLK_P	MIPI CSI clock differential pair
17	GPIO_29_CCI_I2C_SDA0	CPU GPIO29. Pulled up to VREG_L6_1P8 via 2.2K resistor on dev kit carrier.
18	MIPI_CSI0_CLK_N	MIPI CSI clock differential pair
19	GND	Ground reference for design.
20	GND	Ground reference for design.
21	GPIO_31_CCI_I2C_SDA1	CPU GPIO31. Pulled up to VREG_L6_1P8 via 2.2K resistor on dev kit carrier.
22	MIPI_CSI0_LANE0_P	MIPI CSI data lane differential pair
23	GPIO_27_CAM_MCLK1	CPU GPIO27. Typically used as Camera MCLK1.
24	MIPI_CSI0_LANE0_N	MIPI CSI data lane differential pair

Pin #	JT1 Signal Name	Description
25	GPIO_28_CAM_MCLK2	CPU GPIO28. Typically used as Camera MCLK2.
26	GND	Ground reference for design.
27	GPIO_30_CCI_I2C_SCL0	CPU GPIO30. Pulled up to VREG_L6_1P8 via 2.2K resistor on dev kit carrier.
28	MIPI_CSI0_LANE1_P	MIPI CSI data lane differential pair
29	GPIO_32_CCI_I2C_SCL1	CPU GPIO32. Pulled up to VREG_L6_1P8 via 2.2K resistor on dev kit carrier.
30	MIPI_CSI0_LANE1_N	MIPI CSI data lane differential pair
31	GND	Ground reference for design.
32	GND	Ground reference for design.
33	MIPI_CSI1_LANE0_P	MIPI CSI data lane differential pair
34	MIPI_CSI0_LANE2_P	MIPI CSI data lane differential pair
35	MIPI_CSI1_LANE0_N	MIPI CSI data lane differential pair
36	MIPI_CSI0_LANE2_N	MIPI CSI data lane differential pair
37	GND	Ground reference for design.
38	GND	Ground reference for design.
39	MIPI_CSI1_CLK_P	MIPI CSI clock differential pair
40	MIPI_CSI0_LANE3_P	MIPI CSI data lane differential pair
41	MIPI_CSI1_CLK_N	MIPI CSI clock differential pair
42	MIPI_CSI0_LANE3_N	MIPI CSI data lane differential pair
43	GND	Ground reference for design.
44	GND	Ground reference for design.
45	MIPI_CSI1_LANE1_N	MIPI CSI data lane differential pair
46	MIPI_CSI2_CLK_P	MIPI CSI clock differential pair
47	MIPI_CSI1_LANE1_P	MIPI CSI data lane differential pair
48	MIPI_CSI2_CLK_N	MIPI CSI clock differential pair
49	GND	Ground reference for design.
50	GND	Ground reference for design.
51	MIPI_CSI1_LANE2_P	MIPI CSI data lane differential pair
52	MIPI_CSI2_LANE0_P	MIPI CSI data lane differential pair
53	MIPI_CSI1_LANE2_N	MIPI CSI data lane differential pair
54	MIPI_CSI2_LANE0_N	MIPI CSI data lane differential pair
55	GND	Ground reference for design.
56	GND	Ground reference for design.
57	MIPI_CSI1_LANE3_P	MIPI CSI data lane differential pair
58	MIPI_CSI2_LANE1_P	MIPI CSI data lane differential pair
59	MIPI_CSI1_LANE3_N	MIPI CSI data lane differential pair
60	MIPI_CSI2_LANE1_N	MIPI CSI data lane differential pair
61	GND	Ground reference for design.
62	GND	Ground reference for design.
63	USB1_SS_TX_P	USB port super-speed TX differential pair

Pin #	JT1 Signal Name	Description
64	MIPI_CSI2_LANE2_P	MIPI CSI data lane differential pair
65	USB1_SS_TX_N	USB port super-speed TX differential pair
66	MIPI_CSI2_LANE2_N	MIPI CSI data lane differential pair
67	GND	Ground reference for design.
68	GND	Ground reference for design.
69	USB1_SS_RX_P	USB port super-speed RX differential pair
70	MIPI_CSI2_LANE3_P	MIPI CSI data lane differential pair
71	USB1_SS_RX_N	USB port super-speed RX differential pair
72	MIPI_CSI2_LANE3_N	MIPI CSI data lane differential pair
73	GND	Ground reference for design.
74	GND	Ground reference for design.
75	CDC_EAR_P	PM8953 Earpiece audio differential output (mono).
76	PM_MPP_4_WLED_PWM_CTRL	PM8953 MPP4. Can be configured for White LED PWM control.
77	CDC_EAR_N	PM8953 Earpiece audio differential output (mono).
78	GPIO_85_KEY_VOLP_N	CPU GPIO85
79	GND	Ground reference for design.
80	GND	Ground reference for design.
81	CDC_HPH_R	PM8953 Stereo Headphone audio output.
82	GPIO_86_KEY_SNAPSHOT	CPU GPIO86
83	CDC_HPH_L	PM8953 Stereo Headphone audio output.
84	GPIO_87_KEY_FOCUS	CPU GPIO87
85	GND	Ground reference for design.
86	GND	Ground reference for design.
87	CDC_SPKR_DRV_P	PM8953 Loud Speaker audio differential output (mono).
88	CDC_SPKR_DRV_P	See JT1 pin 87
89	CDC_SPKR_DRV_N	PM8953 Loud Speaker audio differential output (mono).
90	CDC_SPKR_DRV_N	See JT1 pin 89
91	GND	Ground reference for design.
92	GND	Ground reference for design.
93	PM_MPP_3	PM8953 MPP3
94	CDC_HPH_REF	PM8953 Headphone GND reference input.
95	VREG_L6_1P8	LDO linear regulator L6 Default voltage = 1.80V Max Current = 250mA (shared with SOM circuits)
96	CDC_HS_DET	PM8953 Headset detect input.
97	VREG_L4_1P8	LDO linear regulator L4 Default voltage = 1.80V Maximum Current = 300mA
98	GND	Ground reference for design.

Pin #	JT1 Signal Name	Description
99	GPIO_26_CAM_MCLK0	CPU GPIO26. Typically used as Camera MCLK0.
100	VREG_L17_2P85	LDO linear regulator L17 Default voltage = 2.85V Maximum Current = 300mA

Table 3 – B2B Connector JT2 Pin-outs

Pin #	JT2 Signal Name	Description
1	SOM_SYS_PWR	3.80-4.20VDC power input to SOM.
2	GND	Ground reference for design.
3	SOM_SYS_PWR	See JT2 pin 1
4	GND	Ground reference for design.
5	SOM_SYS_PWR	See JT2 pin 1
6	SOM_SYS_PWR	See JT2 pin 1
7	SOM_SYS_PWR	See JT2 pin 1
8	SOM_SYS_PWR	See JT2 pin 1
9	SOM_SYS_PWR	See JT2 pin 1
10	SOM_SYS_PWR	See JT2 pin 1
11	SOM_SYS_PWR	See JT2 pin 1
12	SOM_SYS_PWR	See JT2 pin 1
13	SOM_SYS_PWR	See JT2 pin 1
14	CHG_VBAT_SNS	Battery sense input to the PMI8952 PMIC.
15	SOM_SYS_PWR	See JT2 pin 1
16	CS_P	Positive Current Sense (+) Terminal Sense
17	SOM_SYS_PWR	See JT2 pin 1
18	CS_N	Negative Current Sense (-) Terminal Sense
19	SOM_SYS_PWR	See JT2 pin 1
20	BAT_ID	Battery identification input to the PMI8952 PMIC on the SOM
21	SOM_SYS_PWR	See JT2 pin 1
22	BATT_N	Battery (-) Terminal Sense
23	SOM_SYS_PWR	See JT2 pin 1
24	BATT_P	Battery (+) Terminal Sense
25	USB_VBUS	PMI8952 USB charger input source. Output during USB host operation.
26	HAP_OUT_P	Differential Haptics Drive Output.
27	USB_VBUS	See JT2 pin 25
28	HAP_OUT_N	Differential Haptics Drive Output.
29	USB_VBUS	See JT2 pin 25
30	VREG_L17_2P85	See JT1 pin 100
31	USB_VBUS	See JT2 pin 25

Pin #	JT2 Signal Name	Description
32	KYPD_PWR_N	Power on input. Internally pulled up to +1.8V on SOM. Active low.
33	USB_VBUS	See JT2 pin 25
34	GPIO_132_CAM3_STANDBY_N	CPU GPIO132. Typically used as camera standby output.
35	PM_GPIO_8_VCONN_EN	PM8953 GPIO8. Typically used to control external VBUS power switch to support USB Type C functionality.
36	GPIO_4_BLSP2_UART_TX	CPU GPIO4
37	PM_GPIO_7_VBUS_MON	PM8953 GPIO7. Typically used as the USB VBUS sense to support USB Type C functionality.
38	GPIO_5_BLSP2_UART_RX	CPU GPIO5
39	GPIO_127	CPU GPIO127
40	GPIO_42_ACCEL_INT	CPU GPIO42
41	GPIO_44_MAG_DRDY_INT	CPU GPIO44
42	VREG_L2_1P1	LDO linear regulator L2 Default voltage = 1.10V Maximum Current = 1200mA
43	GPIO_130_CAM2_STANDBY_N	CPU GPIO130. Typically used as camera standby output.
44	VREG_L2_1P1	See JT2 pin 42
45	BAT_THERM	Battery thermistor input to the PMI8952 PMIC on the SOM
46	VREG_L2_1P1	See JT2 pin 42
47	GPIO_139_USB_SS_SWITCH_SEL	CPU GPIO139. Typically used for controlling the USB super-speed switch IC.
48	VREG_L2_1P1	See JT2 pin 42
49	HAP_CNTRL_ANLG	Haptic PWM control input.
50	GPIO_61_LCD0_RESET_N	CPU GPIO61. Typically used for LCD display reset input.
51	GPIO_65_TS_INT_N	CPU GPIO65. Typically used for touchscreen interrupt input.
52	GPIO_141	CPU GPIO141
53	USB_ID	USB port ID signal
54	GPIO_24_MDP_VSYNC_P	CPU GPIO24
55	PM_VCONN	PM8953 USB power input pin for USB Type C cable detection
56	GPIO_25_MDP_VSYNC_N	CPU GPIO25
57	GPIO_133_SD_CARD_DET_N	Secure Digital (SD) card detect signal. This GPIO is referenced to VREG_L5_1P8
58	GPIO_8_BLSP3_UART_TX	CPU GPIO8
59	CDC_LINEOUT_P	PM8953 Line-Out audio differential output (mono).
60	GPIO_11_BLSP3_I2C_SCL	CPU GPIO11. Pulled up to VREG_L5_1P8 via 2.2K resistor on dev kit carrier.
61	CDC_LINEOUT_N	PM8953 Line-Out audio differential output (mono).

Pin #	JT2 Signal Name	Description
62	GPIO_10_BLSP3_I2C_SDA	CPU GPIO10. Pulled up to VREG_L5_1P8 via 2.2K resistor on dev kit carrier.
63	RESIN_N	Reset input/Volume down. Internally pulled up to +1.8V on SOM. Active low
64	GPIO_9_BLSP3_UART_RX	CPU GPIO9
65	GPIO_13_CAP_INT_N	CPU GPIO13
66	GPIO_46_PRESSURE_INT	CPU GPIO46
67	GPIO_100_BACKLIGHT_EN	CPU GPIO100. Typically used for backlight enable.
68	GPIO_45_GYRO_INT	CPU GPIO45
69	GND	Ground reference for design.
70	GND	Ground reference for design.
71	MIPI_DSI0_LANE2_P	MIPI DSI data lane differential pair
72	MIPI_DSI0_LANE0_P	MIPI DSI data lane differential pair
73	MIPI_DSI0_LANE2_N	MIPI DSI data lane differential pair
74	MIPI_DSI0_LANE0_N	MIPI DSI data lane differential pair
75	GND	Ground reference for design.
76	GND	Ground reference for design.
77	MIPI_DSI0_LANE1_N	MIPI DSI data lane differential pair
78	MIPI_DSI1_LANE1_N	MIPI DSI data lane differential pair
79	MIPI_DSI0_LANE1_P	MIPI DSI data lane differential pair
80	MIPI_DSI1_LANE1_P	MIPI DSI data lane differential pair
81	GND	Ground reference for design.
82	GND	Ground reference for design.
83	MIPI_DSI0_CLK_N	MIPI DSI clock differential pair
84	MIPI_DSI1_LANE0_P	MIPI DSI data lane differential pair
85	MIPI_DSI0_CLK_P	MIPI DSI clock differential pair
86	MIPI_DSI1_LANE0_N	MIPI DSI data lane differential pair
87	GND	Ground reference for design.
88	GND	Ground reference for design.
89	MIPI_DSI1_CLK_P	MIPI DSI clock differential pair
90	MIPI_DSI1_LANE3_P	MIPI DSI data lane differential pair
91	MIPI_DSI1_CLK_N	MIPI DSI clock differential pair
92	MIPI_DSI1_LANE3_N	MIPI DSI data lane differential pair
93	GND	Ground reference for design.
94	GND	Ground reference for design.
95	MIPI_DSI0_LANE3_P	MIPI DSI data lane differential pair
96	MIPI_DSI1_LANE2_P	MIPI DSI data lane differential pair
97	MIPI_DSI0_LANE3_N	MIPI DSI data lane differential pair
98	MIPI_DSI1_LANE2_N	MIPI DSI data lane differential pair
99	GND	Ground reference for design.
100	GND	Ground reference for design.

Table 4 – B2B Connector JT3 Pin-outs

Pin #	JT3 Signal Name	Description
1	USBC_CC1	USB Type C Configuration Channel signals
2	VREG_L10_3P0	LDO linear regulator L10 Default voltage = 3.00V Maximum Current = 150mA
3	USBC_CC2	USB Type C Configuration Channel signals
4	VREG_L10_3P0	See JT3 pin 2
5	SDC2_CLK	SDC2 Secure Digital clock signal
6	NC	No Connection
7	SDC2_DATA3	SDC2 Secure Digital data bit 3
8	GND	Ground reference for design.
9	SDC2_DATA2	SDC2 Secure Digital data bit 2
10	GPIO_89_DMIC0_CLK	CPU GPIO89. Alternate function is digital MIC clock.
11	SDC2_CMD	SDC2 Secure Digital CMD signal
12	GPIO_90_DMIC0_DATA	CPU GPIO90. Alternate function is digital MIC data input.
13	SDC2_DATA1	SDC2 Secure Digital data bit 1
14	GND	Ground reference for design.
15	SDC2_DATA0	SDC2 Secure Digital data bit 0
16	USB2_HS_P	USB port high-speed differential pair
17	VREG_L17_2P85	See JT1 pin 100
18	USB2_HS_N	USB port high-speed differential pair
19	VREG_L11_SDC	LDO linear regulator L11 Default voltage = 2.95V Maximum Current = 600mA
20	GND	Ground reference for design.
21	VREG_L11_SDC	See JT3 pin 19
22	PM_VCOIN	Optional +3V coin cell backup battery connection to the PM8953 PMIC. This provides backup power for the real time clock only.
23	NC	No Connection
24	GPIO_98	CPU GPIO98
25	GPIO_12_CAM_IRQ	CPU GPIO12. Typically used as camera interrupt input.
26	GPIO_36_CCI_TIMER3	CPU GPIO36. Typically used for flash strobe timing.
27	GPIO_131_CAM3_RST_N	CPU GPIO131. Typically used as camera reset output.
28	GPIO_39_CAM1_STANDBY_N	CPU GPIO39. Typically used as camera standby output.
29	GPIO_64_TS0_RESET_N	CPU GPIO64. Typically used for touchscreen reset output.

Pin #	JT3 Signal Name	Description
30	VREG_L13_3P075	LDO linear regulator L13 Default voltage = 3.125 Max Current = 50mA (shared with SOM circuits)
31	GPIO_33_CCI_TIMER0	CPU GPIO33. Typically used for flash strobe timing.
32	GPIO_35_CCI_TIMER2	CPU GPIO35. Typically used for flash strobe timing.
33	GPIO_34_CCI_TIMER1	CPU GPIO34. Typically used for flash strobe timing.
34	GPIO_18_BLSP5_I2C_SDA	CPU GPIO18. Pulled up to VREG_L5_1P8 via 1K resistor on dev kit carrier.
35	GPIO_2_BLSP1_SPI_CS_N	CPU GPIO2
36	VREG_L6_1P8	See JT1 pin 95
37	GPIO_0_BLSP1_SPI_MOSI	CPU GPIO0
38	GPIO_19_BLSP5_I2C_SCL	CPU GPIO19. Pulled up to VREG_L5_1P8 via 1K resistor on dev kit carrier.
39	GPIO_1_BLSP1_SPI_MISO	CPU GPIO1
40	PMI_CHG_EN	PMI8952 battery charger enable input
41	GPIO_3_BLSP1_SPI_CLK	CPU GPIO3
42	GPIO_40_CAM1_RST_N	CPU GPIO40. Typically used as camera reset output.
43	GPIO_106_BOOT_CONFIG0	Boot configuration 0 / Watchdog Disable
44	NC	No Connection
45	GND	Ground reference for design.
46	GPIO_138_MI2S_2_D1	MI2S Interface #2, serial data channel 1 CPU GPIO138
47	GPIO_63_CODEC_INT1_N	CPU GPIO63
48	GPIO_135_MI2S_2_SCK	MI2S Interface #2, bit clock CPU GPIO135
49	PM_GPIO_1_DIV_CLK2	PM8953 GPIO1
50	GPIO_136_MI2S_2_WS	MI2S Interface #2, word select CPU GPIO136
51	VREG_L22_2P85	LDO linear regulator L22 Default voltage = 2.80V Maximum Current = 150mA
52	GPIO_137_MI2S_2_D0	MI2S Interface #2, serial data channel 0 CPU GPIO137
53	GND	Ground reference for design.
54	GND	Ground reference for design.
55	NC	No Connection
56	BB_CLK2	Baseband clock #2 output PM8953 BB_CLK2
57	CBL_PWR_N	PM8953 CBL_PWR_N input
58	GND	Ground reference for design.
59	GND	Ground reference for design.
60	GPIO_96	CPU GPIO96

Pin #	JT3 Signal Name	Description
61	APQ_RESOUT_N	CPU reset output
62	GPIO_23_SPI6_CLK	CPU GPIO23
63	GPIO_66_SEC_MI2S_MCLK_B	MI2S #1 or #2 master clock CPU GPIO66
64	GPIO_22_SPI6_CS_N	CPU GPIO22
65	GPIO_43_ALSP_INT_N	CPU GPIO43
66	GPIO_20_SPI6_MOSI	CPU GPIO20
67	PMI_GPIO_1	PMI8952 GPIO1
68	GPIO_21_SPI6_MISO	CPU GPIO21
69	GPIO_140_HRM_INT	CPU GPIO140
70	GPIO_48_SPI6_CS1_MAG_N	CPU GPIO48
71	VREG_L5_1P8	LDO linear regulator L5 Default voltage = 1.80V Max Current = 100mA (shared with SOM circuits)
72	GPIO_17_BLSP5_UART_RX	CPU GPIO17
73	VREG_L5_1P8	See JT3 pin 71
74	GPIO_7_BLSP2_I2C_SCL	CPU GPIO7. Pulled up to VREG_L5_1P8 via 2.2K resistor on dev kit carrier.
75	NC	No Connection
76	GPIO_16_BLSP5_UART_TX	CPU GPIO16
77	CHG_LED_RED_LED_DRV	Charging LED sink PMI8952 CHG_LED
78	GPIO_6_BLSP2_I2C_SDA	CPU GPIO6. Pulled up to VREG_L5_1P8 via 2.2K resistor on dev kit carrier.
79	PMI_MPP_2_GREEN_LED_DRV	PMI8952 MPP_2
80	GPIO_95_MI2S_1_D3	MI2S Interface #1, serial data channel 3 CPU GPIO95
81	PMI_MPP_4_BLUE_LED_DRV	PMI8952 MPP_4
82	GPIO_93_MI2S_1_D0	MI2S Interface #1, serial data channel 0 CPU GPIO93
83	VOUT_WLED	PMI8952 white LED SMPS output
84	GPIO_88_MI2S_1_D1	MI2S Interface #1, serial data channel 1 CPU GPIO88
85	PMI8952_WLED_SINK1	PMI8952 white LED low-side current sink input
86	GPIO_92_MI2S_1_WS	MI2S Interface #1, word select CPU GPIO92
87	PMI8952_WLED_SINK2	PMI8952 white LED low-side current sink input
88	GPIO_91_MI2S_1_SCK	MI2S Interface #1, bit clock CPU GPIO91
89	PMI8952_WLED_SINK3	PMI8952 white LED low-side current sink input
90	GPIO_94_MI2S_1_D2	MI2S Interface #1, serial data channel 2 CPU GPIO94
91	VREG_DISP_5V_P	PMI8952 SMPS output, display positive bias. Default voltage = 5V5

Pin #	JT3 Signal Name	Description
92	GPIO_129_CAM2_RST_N	CPU GPIO129. Typically used as camera reset output.
93	WLED_CABC	PMI8952 PWM input for dynamic dimming
94	GPIO_113_BOOT_CONFIG1	Boot configuration 1. Configures external boot device
95	VREG_DISN_5V_N	PMI8952 SMPS output, display negative bias. Default voltage = -5V5
96	GPIO_109_BOOT_CONFIG3	Boot configuration 3. Configures external boot device
97	PMI_USB_SNS	PMI8952 USB VBUS input voltage sense
98	GPIO_107_BOOT_CONFIG2	Boot configuration 2. Configures external boot device
99	GPIO_62_CODEC_INT2_N	CPU GPIO62
100	FORCED_USB_BOOT (APQ_GPIO_37)	Forced USB boot

4.3 RF Antenna Connections

The Open-Q 626 µSOM includes two U.FL coaxial receptacles (see table below) for connecting to Wi-Fi / Bluetooth and GPS RF antennas.

Table 5 – RF Signals via U.FL Coaxial Receptacles

Connector	Connector Type	Manufacturer + Part Number	Signal
J2600	U.FL Coaxial Receptacle	Hirose U.FL-R-SMT-1 (10)	GPS Receiver
J2200	U.FL Coaxial Receptacle	Hirose U.FL-R-SMT-1 (10)	Dual Band Wi-Fi + Bluetooth

The SOM implements Wi-Fi / Bluetooth connectivity via the Qualcomm WCN3680B chipset. This provides 802.11a/b/g/n/ac 2.4/5.0 GHz dual-band Wi-Fi, and Bluetooth 4.2, operating at 2.4GHz. The regulatory certifications that are included with the SOM are listed in document R-4 and described further in section 9.

The SOM implements GPS connectivity via the Qualcomm WGR7640 chipset. The GPS U.FL antenna connection is DC biased with a 2.7V voltage rail allowing the connection to power a remote LNA located either on the carrier board or as part of an active antenna assembly. See document R-2 for more details on how to connect this port on a custom carrier board design.

5. ELECTRICAL SPECIFICATIONS

The input power to the SOM is provided by a power supply (battery or wall adapter) and also a USB source, for battery charging purposes. All input power sources enter the PMI8952 power management IC on the SOM, which then distributes power (along with the PM8953 PMIC) to other circuits on the SOM and connected carrier board via LDO and switching power supply outputs.

5.1 Absolute Maximum Ratings

The table below shows the absolute maximum ratings in which the SOM input power sources can be exposed to without experiencing functional failure.

Table 6 – Absolute Maximum Input Power Ratings

Parameter	Min	Max	Units
Battery or DC power input (SOM_SYS_PWR)	-0.3	6	V
USB VBUS battery charger input voltage source (USB_VBUS)	-0.3	16	V

5.2 Operating Conditions

The table below shows the recommended operating conditions for the SOM to meet all performance specifications (provided the absolute maximum ratings have never been exceeded).

Table 7 – Operating Input Power Ratings

Parameter	Min	Typ	Max	Units
Battery or DC power input (SOM_SYS_PWR)	3.45[1]	3.8	4.2	V
USB VBUS battery charger input voltage source (USB_VBUS)	3.7	5	10	V
PM_VCOIN Input	2.0	3.0	3.25	V

5.3 Operating Temperature

The SOM operating temperature ratings listed below are based only on the component case temperature ratings of individual components populated on the SOM. Users should consider the specific environmental conditions in which the final product is used in.

Table 8 – Operating temperature range (Tc)

Parameter	Min	Typ	Max	Units
Overall SOM (case temperature)[2]	-25	+25	+85	°C

[1] The SOM may be configured to operate at lower input voltage levels but changes to bootloader or proprietary code are needed and this will require support from Intrinsyc. Intrinsyc's solutions and software engineering services can provide advice and support for specialty low voltage requirements. Please contact Intrinsyc sales at: https://www.intrinsyc.com/sales-inquiry

[2] For the temperature range outside of -20C to +60C, WiFi performance will be degraded.

5.4 Power Consumption

Power consumption measurements have been performed on the SOM running under common operational modes. All tests were executed at room temperature and with the default thermal solution that ships with the SOM development kit (heat sink on top of CPU) unless noted otherwise. In some test cases, ADB was used to monitor the SOM to ensure that the CPU was not throttling during the test. If ADB is not used, power consumption may be lower.

The table below contains the SOM power consumption numbers under common operational modes.

Table 9 – Power Consumption Ratings

Operational Modes	Description	Average	Peak
Boot	Power consumption during boot process	n/a	3.8W
Suspend (Wi-Fi Off)	SOM placed in standby (Wi-Fi Off, Display Off)	66mW	66mW
Idle (Wi-Fi Off)	SOM is idle (Wi-Fi Off, Display On)	218mW	935mW
Idle (Wi-Fi on)	SOM is idle (Wi-Fi On, Display On)	249mW	1.2W
Video Record (1080P)	SOM recording 1080P video	1.8W	2.9W
Video Record (4K UHD)	SOM recording 4K UHD video	2.4W	3.8W
Video Playback (1080P)	SOM playing back 1080P video	766mW	1.6W
Video Playback (4K UHD)	SOM playing back 4K UHD video	1.0W	2.5W
Audio Playback	SOM playing back MP3 (Display Off)	179mW	1.1W
Wi-Fi Download	SOM downloading data over Wi-Fi (Display Off)	978mW	2.3W
Wi-Fi Upload	SOM uploading data over Wi-Fi (Display Off)	995mW	2.3W
Full Load (All Cores)	Running all cores	2.5W	3.2W
Full Load (Single Core)	Running only cpu0	734mW	1.2W
UFS Write	Writing data to UFS (Display Off)	614mW	1.7W
UFS Read	Reading data from UFS (Display Off)	628mW	2.1W
Bluetooth	SOM playing music over Bluetooth (Display Off)	328mW	850mW

NOTES:

- The full load (All Core) test used a fan pointed at the heatsink to prevent thermal throttling of the CPU.

5.5 ESD Ratings

The SOM is not designed with additional ESD protection other than what is included in the integrated circuits. It is recommended to take proper precautions in a static free environment when handling the SOM.

6. MECHANICAL SPECIFICATIONS

The sections below present some mechanical details of the Open-Q 626 µSOM. For access to the 3D design files, please see http://tech.intrinsyc.com/ (dev kit registration required).

6.1 SOM Mechanical Outline

The outer dimensions of the SOM are 50.0 x 25.0mm, as shown below. The key inner-dimensions for the SOM relate to connector positioning; these dimensions are called out later in this document.

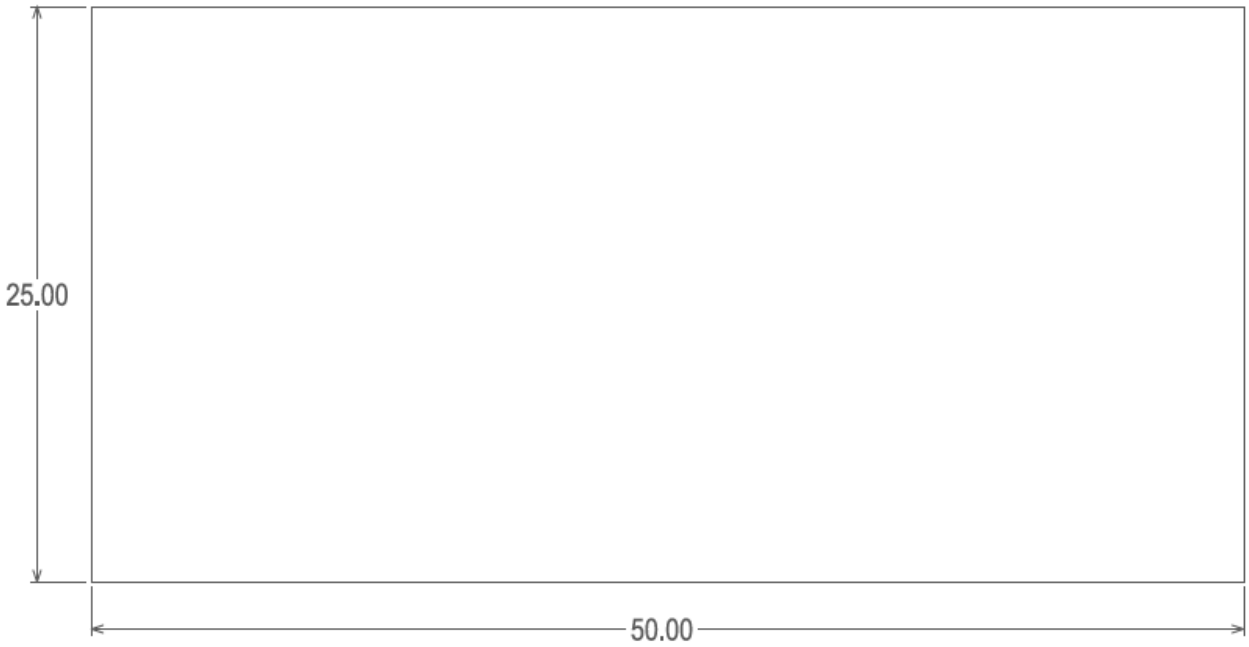

Figure 4 - SOM Mechanical Outline

6.2 Top and Bottom Height Restrictions

The tallest component on the top-side of the SOM is 1.33mm. This height does not include the mating RF antenna cable connectors.

The tallest component on the bottom-side of the SOM is 1.29mm.

NOTE: When designing the Carrier Board PCB, components should not be placed in the area immediately underneath the SOM.

6.3 Landing Pattern

Dimensions presented are in millimeters (mm). The footprint information in this section can be used as a guide when designing a landing area for the SOM.

Dimensions show the relative position of each connector on the SOM; referenced to the center of the connector body. NOTE: This information is given for reference. It is highly recommended that the Open-Q 626 µSOM Carrier Board design source files and document R-2 be used to ensure proper dimensioning on any custom carrier board design.

*The perspective of this figure is looking through the top side of the SOM.

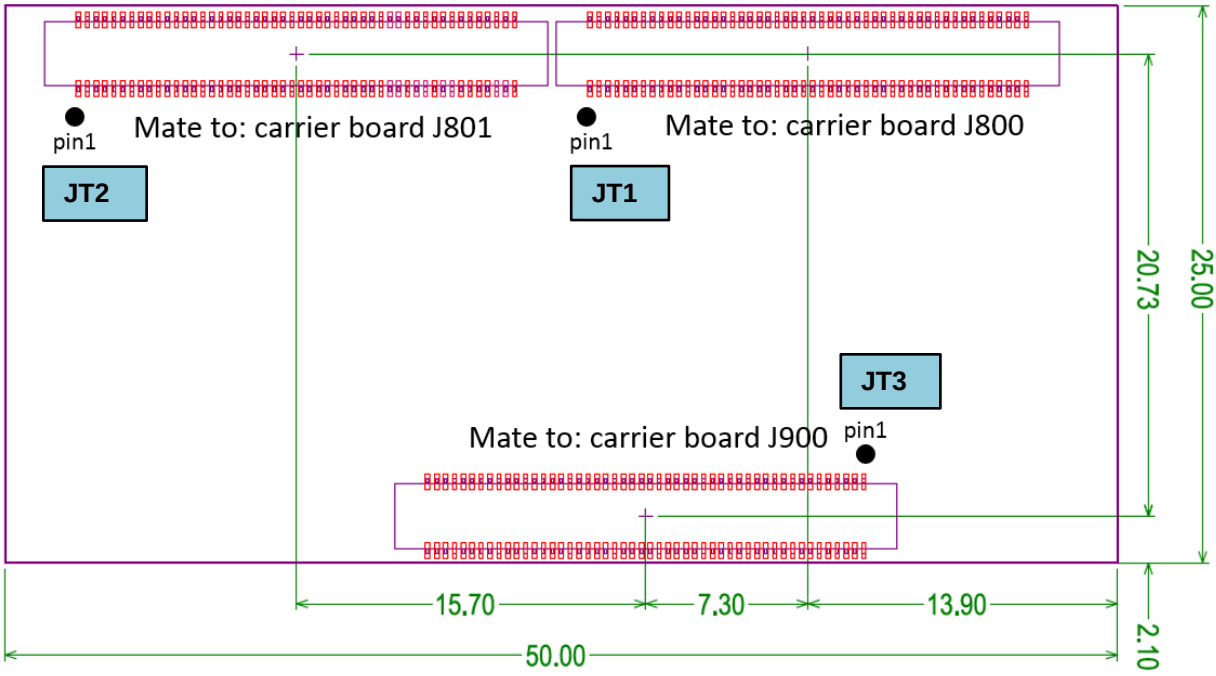

Figure 5 - SOM Land-Pattern Dimensions (mm)

The mating connector, Hirose DF40X-X-100DS-0.4V, is available in different heights, to achieve stack heights of 1.5mm or 3.0mm.

6.4 Thermal Characteristics

The APQ8053 has built in thermal protections which will reduce processor frequency as the die temperature approaches set operating limits. These limits protect the processor from damage that could be caused by elevated die temperature. Additional product-level thermal management will remove heat from the SOM and its components, allowing the processor to run at higher frequencies for longer time periods before approaching the built in die temperature limits. This enables the average processor speed to remain higher through processor-intensive applications. Effectively removing heat from the Open-Q 626 µSOM is required to optimize system performance and efficiency and to ensure that the APQ8053 processor can perform as desired.

For more information on thermal mitigation, see SOM Carrier Board Design Guide (Reference document R-2).

6.5 Weight

While still preliminary, the SOM is expected to weigh approximately 8 grams.

7. PRODUCT MARKING, ORDERING, AND SHIPPING INFO

7.1 Product Marking

The SOM part number and product marking can be identified on the white label on the top of the module. The figure and table below show a label example which includes the SOM name and QR code.

Figure 6 – Open-Q 626 µSOM Label (top of PCB)

Table 10 –Open-Q 626 µSOM Label Marking

Line	Marking	Description/ Notes
1	Open-Q 626 µSOM	Intrinsyc Technologies product name
2	QR code *	Embeds serial number and Wi-Fi MAC address. The serial number format is VVV-WWXX-YYYYYY-ZZZZZ - VVV = Product number - WW = PCB revision number - XX = BOM revision number - YYYYYY = Date of manufacture (mm/dd/yy) - ZZZZZ = Unique serial number for PCB The MAC address format is 0123456789AB - 12 hexadecimal digit MAC address
* QR code reader mobile app (e.g. Neo Reader) can be used to read embedded serial number and the MAC address.		

7.2 Product Ordering Information

When available, the Open-Q 626 µSOM can be ordered for evaluation and prototype use from the Intrinsyc online store at http://shop.intrinsyc.com. For volume production orders or for custom requirements please contact Intrinsyc sales at https://www.intrinsyc.com/sales-inquiry.

Orderable Part Numbers	
Open-Q 626 µSOM	QC-DB-M00004
Open-Q 626 µSOM Development Kit	QC-DB-M00003

7.3 Packaging and Shipping Information

The Open-Q 626 µSOM is packaged individually in small anti-static bags and bubble-wrap bags for protection during shipping – see Figure 8 below. They are then put into different sized boxes depending upon the quantity of the order. Small quantities are shipped in standard courier boxes with bubble-wrap protection and large quantity orders are packaged in a carton with dividers, as shown in Figure 9, below.

Figure 7 - Individual SOM Packaging

Figure 8 - Packaging for Large Quantity Shipments

8. HANDLING PRECAUTIONS

8.1 ESD Precautions

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

The Open-Q 626 µSOM is designed as a component meant to be integrated into a final product and therefore has no additional ESD protection built-in. It should be handled only in a static-safe environment to prevent damage.

8.2 SOM – Carrier Board Mating Cautions

Caution must be taken when connecting or disconnecting the SOM to a carrier board to prevent damage. Ensure that the SOM is inserted and removed straight up and down to prevent any sideways force on the connectors which could damage them.

Also note that the DF40C-100DX board to board connectors are rated for a maximum of 30 mating / un-mating cycles. Therefore the number of insertions and removals must be limited to ensure reliability of the connectors.

8.3 Storage

The SOM must be stored in an antistatic bag.

9. CERTIFICATION

9.1 Radio Certification

The Intrinsyc Open-Q 626 µSOM has been certified with FCC and Industry Canada as a modular radio transmitter for WLAN and Bluetooth. The FCC and Industry Canada ID numbers are:

- FCC ID: 2AFDI-ITCOQ626S
- IC: 9049A-ITCOQ626S

These certifications apply so long as the antenna structures and transmit powers used are equivalent to those used for the original certification. Changes to firmware, drivers, or board configuration files may have an impact to transmit power. For this reason, it is recommended to refer to the SOM certification documents (see document R-4) for information regarding the test configurations used for certification. Deviating from the documented configuration may trigger the need for re-certification.

9.2 ROHS/REACH Compliance

The Intrinsyc Open-Q 626 µSOM complies with the ROHS/REACH standard. The certificate of compliance is available at http://tech.intrinsyc.com (dev kit registration required).

10. COMPANY CONTACT

For more information, support or sales, please contact us.

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