OM-O2S / OM-O2SP

Onion Omega2S IoT compute modules

Data Sheet (Version 1.4)

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1. Overview

The Onion Omega2S is a Wi-Fi enabled, Linux compute module, designed specifically for IoT applications. It provides a drop-in, low-power solution for building IoT devices.

The module measures 34x20x2.8 mm and features a MIPS 24KEc processor running at 580 MHz, built-in DDR2 DRAM, flash storage, and a 2.4 GHz 802.11b/g/n Wi-Fi radio. It supports a wide variety of I/O protocols, with 42 pins available to the developer. The module is self-contained and only requires a power supply and an external WiFi antenna to operate.

By virtue of the Linux operating system, developers can create their own applications using a programming language of their choice, and make use of existing network stacks and a rich set of software packages to implement their desired software functionality.

Key highlights:

- Drop-in Wi-Fi enabled Linux compute module for IoT applications
- Dual mode 2.4 GHz 802.11 b/g/n Wi-Fi - simultaneously host a WiFi access point and connect to existing WiFi networks
- CPU, memory, and flash storage are built-in - Only requires external antenna
- Runs OpenWRT Linux operating system out of the box
- Features USB, SD/eMMC storage support, ethernet, 3x UARTs, I2C, SPI, GPIOs interfaces
- FCC and CE certified

Highlights on the software and operating system:

- The operating system is based on the OpenWRT Linux distribution
    - Support for modern programming languages: Python (2.7 and 3.6), NodeJS (8.10), GoLang, C, C++, and others
- The default device operating system image includes:
    - Onion's enhanced WiFi driver
    - A package manager (opkg)
    - A lightweight web server (uhttpd) and an extendable Remote Procedure Call daemon (RPCD and ubus)
    - Utilities to control the GPIOs (gpioctl, fast-gpio) and pin multiplexing (omega2-ctrl)
    - The sysfs interface for programmatic control of the hardware interfaces
    - OnionOS, a web-based, graphical user interface for the Omega2 family

The build system for creating the operating system image and software packages is open source, so developers can create their own customized operating system images tailored to their needs. It can be found on GitHub: https://github.com/OnionIoT/source.

Additionally, the source code for many software packages created by Onion can be found on GitHub: https://github.com/OnionIoT

This includes the Omega2 bootloader source code.

Extensive documentation can be found online on the Onion Docs site that describes technical details, software usage, and more.

1.1 Key Features

CPU	
Chipset	MT7688AN
Architecture	MIPS24KEc
Clock Speed	580MHz

Memory	
Flash	16MB (OM-O2S) or 32MB (OM-O2SP)
DDR2 DRAM	64MB (OM-O2S) or 128MB (OM-O2SP)

WIFI	
WiFi Protocol	IEEE 802.11 b/g/n
Base Band	2.4GHz
Data Rate	150 Mbit/s
Channel Bandwidth	20/40 MHz
Operation Mode	AP, STA, AP&STA
Encryption Mode	WEP64/128, AES, WPA, WPA2, WAP

Interfaces	
Ethernet	1 (10M/100M)
USB 2.0 Host	1
SDXC/eMMC	1
SPI	1
I2C	1
I2S	1
UART	3
PWM	4
GPIO	Up to 30

Power Supply Requirement	
DC Input	3.3V
No-load Running Current	200±40mA

Peak Current Requirement	800mA

Operation Conditions	
Ambient Temperature	-10°C ~ 55 °C
Storage Temperature	-20°C ~ 80° C
Operating Humidity	10%-95%RH (Non-Condensing)
Storage Humidity	5%-95%RH (Non-Condensing)

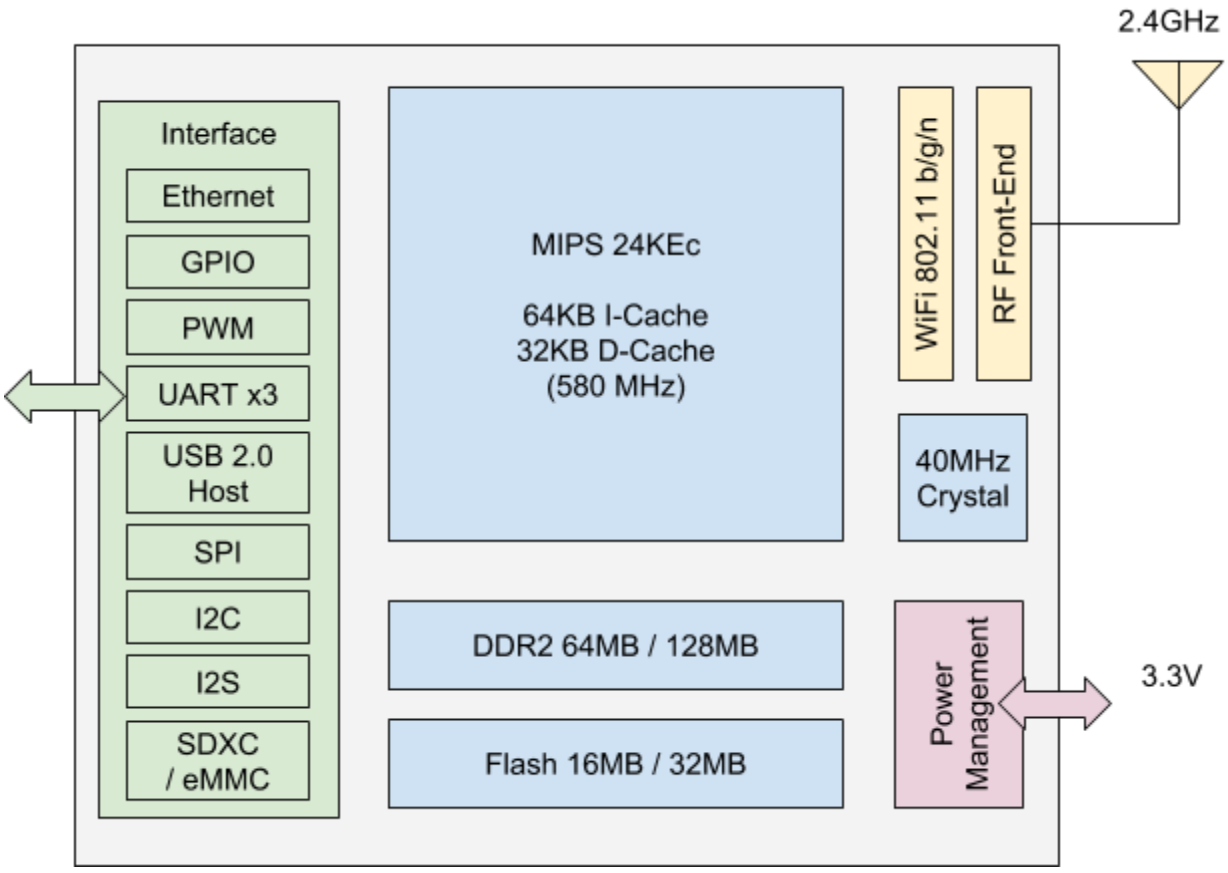
Dimensions	
Size	34*20*2.8mm

Additional specifications and operating details for the microprocessor in the Omega2S can be found in the Mediatek MT7688 Datasheet

1.2 Variants

Model	Name	RAM	Flash	Packaging
OM-O2S	Omega2S	64 MB	16 MB	SMT
OM-O2SP	Omega2S+	128 MB	32 MB	SMT

1.3 Block Diagram



2. Features

2.1 CPU

The processor is based on the MIPS architecture, it is a MIPS 24KEc, little-endian, 32-bit RISC core that operates at 580 MHz with a 64 KB Instruction Cache and 32 KB Data Cache.

2.2 Memory

Features on-board 16-bit DDR2 DRAM memory operating at 400 MHz

- Omega2S features 64 MB memory
- Omega2S+ features 128 MB memory

2.3 Flash

Features on-board SPI flash storage that contains the bootloader, Linux OS, and WiFi calibration data.

- Omega2S features 24-bit addressed 16 MB flash storage
- Omega2S+ features 32-bit addressed 32 MB flash storage

2.4 WiFi

The Omega supports 2.4 GHz IEEE 802.11 b/g/n WiFi with a maximum 150 Mbps PHY data rate. The embedded RF front-end is 1T1R, meaning that it is used for both transmitting and receiving by virtue of time-multiplexing.

The Omega's WiFi interface can simultaneously host its own WiFi Access Point while connecting to another WiFi network.

2.4.1 Antenna Interfaces

The Omega2S supports on-board antennas as well as external antennas. On-board antennas, such as ceramic chip antennas or PCB trace antennas, need to be connected to pin 24. External antennas can be connected directly to the u.FL connector on the module.

2.5 Interfaces

Describing the interfaces available on the Omega2S modules.

2.5.1 USB

There is one (1) USB 2.0 host controller available on dedicated pins.

Note 1: *A 5V power source needs to be supplied to the USB client device to properly operate.*
Note 2: *Special care needs to be taken to ensure the high-speed USB data lines are impedance*

matched when routing custom hardware with the Omega2S.
Note 3: *Use of an ESD protection device is recommended.*

2.5.2 SPI

One (1) SPI interface is available. The interface supports half-duplex transmissions and can operate in host-mode only. The maximum SPI clock frequency is 40 MHz.

The SPI interface features two Chip Select signals. The processor communicates with the on-board flash storage using the SPI protocol. The flash storage occupies SPI Chip Select 0, external devices can be connected to SPI Chip Select 1.

Note: *External devices connected to the SPI bus can affect the boot sequence under certain conditions. See section* ***3.3.2 - SPI Pins*** *for details.*

2.5.3 I2C

There is one (1) I2C controller available. The interface can operate in host-mode only. Standard (100kbps) and fast mode (400kbps) are supported. The I2C logic level is 3.3V.

2.5.4 I2S

The Omega2S has one (1) I2S interface available.

The I2S interface consists of two separate cores, a transmitter and receiver. Both can operate in either master or slave mode.

2.5.4.1 Features

- I2S transmitter / receiver, configurable as master or slave
- 16-bit data, sampling rates of 8 kHz, 16 kHz, 22.05 kHz, 44.1 kHz, and 48 kHz
- Stereo audio data transfer
- 32-byte FIFO for transmission
- GDMA access
- 12 Mhz bit clock from external source (when in slave mode)

2.5.5 SDIO/eMMC

There is a single SDIO interface. Only one of eMMC, SD/Micro-SD, or other SDIO device can be used. The SDIO interface supports the SDXC specification for SD cards, with a maximum capacity of 2 TB and a maximum transfer speed of 300 MB/s, and the eMMC5.1 interface for eMMC storage.

2.5.6 Ethernet

The Omega2 has a single 10/100M Ethernet integrated PHY.

It is recommended that typical ethernet magnetics be used, however for very short runs (<5m) a simpler approach using capacitive decoupling is possible. See the Omega2S reference schematic for details.

2.5.7 UART

There are three (3) 2-pin Serial UARTs available. The UART logic level is 3.3V.

Note: *All three UARTs are UART Lite controllers that do not feature hardware flow control.*

2.5.7.1 Features

- All standard baud rates up to 345,600 b/s
- 5-8 data bits
- 1-2 stop bits (1 or 2 stop bits are supported with 5 data bits)
- Even, odd, stick or no parity
- 16-byte receive buffer
- 16-byte transmit buffer
- Loopback control for link fault isolation

2.5.8 PWM

There are four (4) PWM channels available. The maximum PWM signal frequency is 40 MHz.

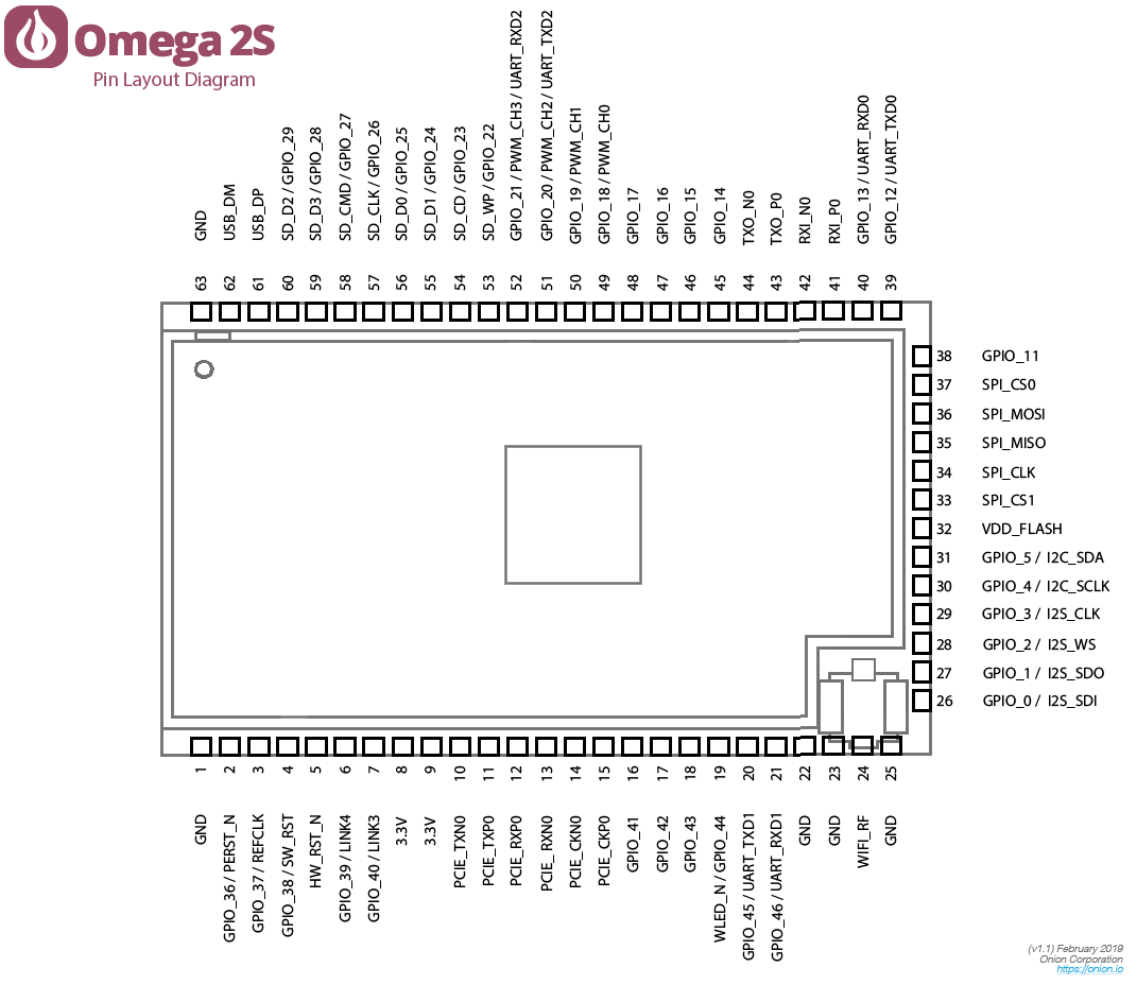
2.5.9 GPIO

Most pins on the module can be configured to operate as GPIO pins. The GPIO logic level is 3.3V and the pins can source or sink a maximum 8mA of current.

See the pin assignment section for details on GPIO capable pins.

3. Pin Definition

3.1 Pin Assignment



No	Name	I/O	Description
1	GND	I	Ground
2	GPIO_36 / PERST_N	I/O	General Purpose I/O / PCIe Device Reset - Active Low
3	GPIO_37 / REFCLK	I/O	General Purpose I/O / Reference Clock Output
4	GPIO_38 / SW_RST	I/O	General Purpose I/O / Default User Button - Programmed to trigger a reboot in Onion Firmware - Active High
5	HW_RST_N		Hardware Power On Reset - Active Low Performs hard reset (power-cycle) of the CPU
6	GPIO_39 / LINK4	I/O	General Purpose I/O
7	GPIO_40 / LINK3	I/O	General Purpose I/O
8	3.3V	I	3.3V Power Supply
9	3.3V	I	3.3V Power Supply
10	PCIE_TXN0		PCIe0 differential transmit TX -
11	PCIE_TXP0		PCIe0 differential transmit TX +
12	PCIE_RXP0		PCIe0 differential receive RX +
13	PCIE_RXN0		PCIe0 differential receive RX -
14	PCIE_CKN0	O	PCIe0 External reference clock output -
15	PCIE_CKP0	O	PCIe0 External reference clock output +
16	GPIO_41	I/O	General Purpose I/O
17	GPIO_42	I/O	General Purpose I/O
18	GPIO_43	I/O	General Purpose I/O
19	WLED_N / GPIO_44	O	WLAN Activity LED
20	GPIO_45 / UART_TXD1	I/O	General Purpose I/O / UART1 Lite TXD
21	GPIO_46 / UART_RXD1	I/O	General Purpose I/O / UART1 Lite RXD
22	GND	I	Ground pin
23	GND	I	Ground pin
24	WIFI_RF	O	RF output

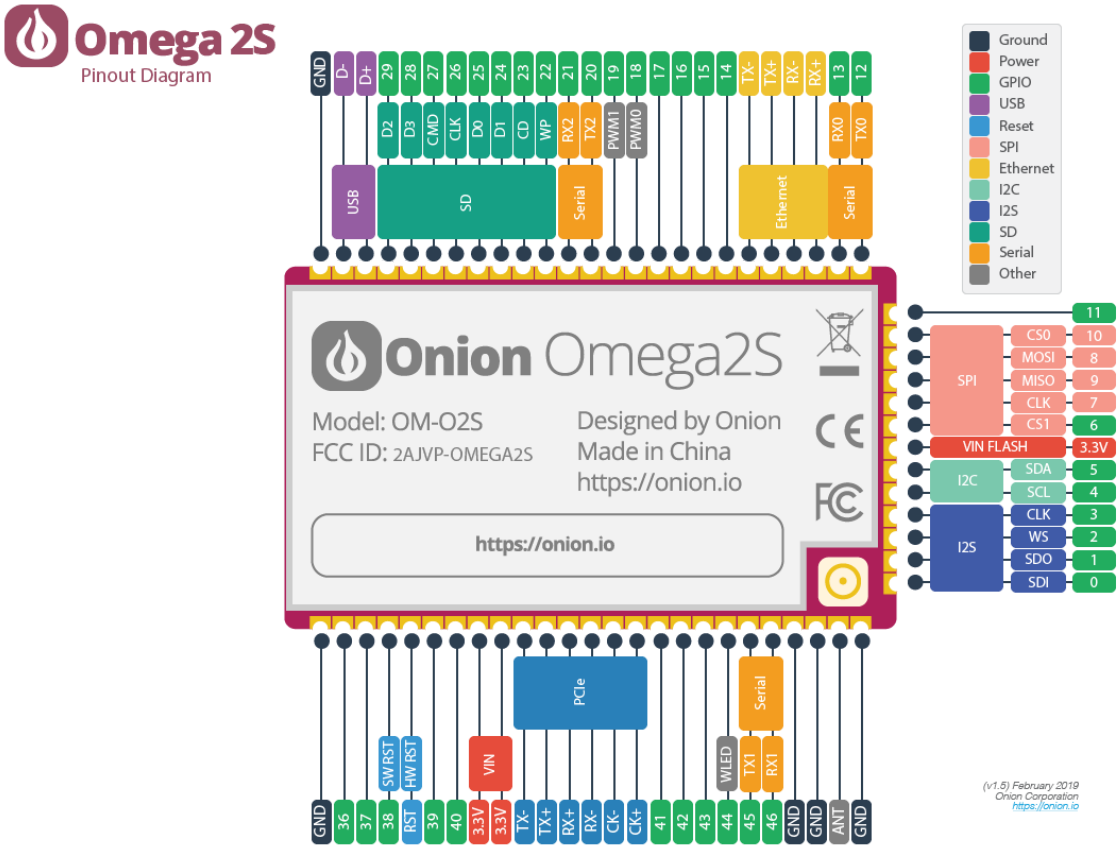
25	GND	I	Ground pin
26	GPIO_0 / I2S_SDI	I/O	General Purpose I/O / I2S Data Input
27	GPIO_1 / I2S_SDO	I/O	General Purpose I/O / I2S Data Output
28	GPIO_2 / I2S_WS	I/O	General Purpose I/O / I2S Word Select (also known as LRCLK - left/right clock)
29	GPIO_3 / I2S_CLK	I/O	General Purpose I/O / I2S Clock
30	GPIO_4 / I2C_SCLK	I/O	General Purpose I/O / I2C Clock
31	GPIO_5 / I2C_SDA	I/O	General Purpose I/O / I2C Data
32	VDD_FLASH	I	3.3V FLASH Power Supply
33	SPI_CS1	O	SPI Chip Select 1
34	SPI_CLK	O	SPI Clock
35	SPI_MISO	I	SPI Master Input/Slave Output
36	SPI_MOSI	O	SPI Master Output/Slave Input
37	SPI_CS0	O	SPI Chip Select 0
38	GPIO_11	I/O	General Purpose I/O
39	GPIO_12 / UART_TXD0	I/O	General Purpose I/O / Serial UART0 Lite TXD
40	GPIO_13 / UART_RXD0	I/O	General Purpose I/O / Serial UART0 Lite RXD
41	RXI_P0	I	10/100 PHY Port #0 RXP
42	RXI_N0	I	10/100 PHY Port #0 RXN
43	TXO_P0	O	10/100 PHY Port #0 TXP
44	TXO_N0	O	10/100 PHY Port #0 TXN
45	GPIO_14	I/O	General Purpose I/O / 10/100 PHY Port #1 TXP

46	GPIO_15	I/O	General Purpose I/O / 10/100 PHY Port #1 TXN
47	GPIO_16	I/O	General Purpose I/O / 10/100 PHY Port #1 RXP
48	GPIO_17	I/O	General Purpose I/O / 10/100 PHY Port #1 RXN
49	GPIO_18 / PWM_CH0	I/O	General Purpose I/O / PWM Channel 0 / 10/100 PHY Port #2 RXP
50	GPIO_19 / PWM_CH1	I/O	General Purpose I/O / PWM Channel 1 / 10/100 PHY Port #2 RXN
51	GPIO_20 / PWM_CH2 / UART_TXD2	I/O	General Purpose I/O / PWM Channel 2 / UART2 Lite TXD / 10/100 PHY Port #2 TXP
52	GPIO_21 / PWM_CH3 / UART_RXD2	I/O	General Purpose I/O / PWM Channel 3 / UART2 Lite RXD / 10/100 PHY Port #2 TXN
53	SD_WP / GPIO_22		SD Write-Protect, 1：yes, 0：no / 10/100 PHY Port #3 TXP
54	SD_CD / GPIO_23		SD Card Detect, 1：No card；0：Has a card / 10/100 PHY Port #3 TXN
55	SD_D1 / GPIO_24		SDIO Data 1 / 10/100 PHY Port #3 RXP
56	SD_D0 / GPIO_25		SDIO Data 0 / 10/100 PHY Port #3 RXN
57	SD_CLK / GPIO_26		SDIO Clock / 10/100 PHY Port #4 RXP
58	SD_CMD / GPIO_27		SDIO Command / 10/100 PHY Port #4 RXN
59	SD_D3 / GPIO_28		SDIO Data 3 / 10/100 PHY Port #4 TXP
60	SD_D2 / GPIO_29		SDIO Data 2 / 10/100 PHY Port #4 TXN
61	USB_DP	I/O	USB Port0 Differential Data +
62	USB_DM	I/O	USB Port0 Differential Data -
63	GND	I	Ground pin

Note：

The pins marked **Red** can affect system boot. They must be floating and **cannot** be Pulled Up or Pulled Down to ensure the system boots properly.

3.2 Pin Multiplexing Diagram



3.3 Special Pins

Information on pins with unique properties

3.3.1 - System Boot Pins

There are six (6) GPIOs that must be left floating at boot time. They cannot be pulled up or pulled down, or else the Omega cannot boot. Once the Omega has booted, these pins can be used normally.

No	Name	I/O	Description
2	GPIO_36 / PERST_N	I/O	General Purpose I/O / PCIe Device Reset - Active Low
20	GPIO_45 / UART_TXD1	I/O	General Purpose I/O / UART1 Lite TXD
27	GPIO_1 / I2S_SDO	I/O	General Purpose I/O / I2S Data Output
33	SPI_CS1	O	SPI Chip Select 1
34	SPI_CLK	O	SPI Clock
39	GPIO_12 / UART_TXD0	I/O	General Purpose I/O / Serial UART0 Lite TXD

3.3.2 - SPI Pins

The Omega's processor communicates with the on-board flash storage using the SPI protocol. It's physically connected as Chip Select 0 on the Omega's SPI bus. Since there are two SPI Chip Select signals it's possible to connect an additional SPI device to the Omega using Chip Select 1.

As such, the SPI communication pins - CLK, MOSI, and MISO - GPIOs 7, 8, and 9 **cannot be used as regular GPIOs**. Connecting non-SPI circuitry to these pins may prevent your Omega from booting or cause other damage to your unit.

No	Name	I/O	Description
33	SPI_CS1	O	SPI Chip Select 1
34	SPI_CLK	O	SPI Clock *Cannot be used as a regular GPIO*
35	SPI_MISO	I	SPI Master Input/Slave Output *Cannot be used as a regular GPIO*
36	SPI_MOSI	O	SPI Master Output/Slave Input *Cannot be used as a regular GPIO*

37	SPI_CS0	O	SPI Chip Select 0 Cannot be used as a regular GPIO

3.3.3 - Reset Pins

There are two reset pins:

No	Name	I/O	Description
4	GPIO_38 / SW_RST	I/O	General Purpose I/O / Default User Button - Programmed to trigger a reboot in Onion Firmware - Active High
5	HW_RST_N		Hardware Power On Reset - Active Low Performs hard reset (power-cycle) of the CPU

The **SW_RST** pin acts as the soft-reset on the Omega2S. This is actually GPIO38 which is configured in the Onion Omega2S firmware to be the programmable user button input. By default, the input is configured to be **active-high** and will **trigger a reboot of the Operating System**.

The **HW_RST_N** pin acts as the hard-reset on the Omega2S. This input is **active-low**, and, when triggered, will perform a **hard reset (ie a power-cycle) of the CPU**.
On the Omega2S+, note that a specific circuit is required to enable the hard-reset. See VDD_Flash section below.

3.3.4 - Power Supply Pins

The following pins must be supplied with 3.3V:

No	Name	I/O	Description
8	3.3V	I	3.3V Power Supply
9	3.3V	I	3.3V Power Supply
32	VDD_FLASH	I	3.3V FLASH Power Supply

Note: No power supply filtering capacitors are required when using the Omega module.

3.3.4.1 - VDD_Flash Pin

The VDD_FLASH pin is the 3.3V power supply for the built-in flash storage of the Omega2S. This pin **must** be supplied with 3.3V in order for the Omega to boot and function properly.

When using the Omega2S, the VDD_Flash pin should be pulled up to 3.3V.

When using the Omega2S+, there are some considerations that must be taken into account when it comes to the VDD_Flash pin.
In order for the HW_RST_N signal to properly power-cycle the CPU, the VDD_Flash pin must also be pulled down to Ground when the HW_RST_N is triggered. This is due to a limitation in the 32MB Flash Chip used in the Omega2S+.

If there is no need to support hard-reset in your Omega2S+ design, VDD_Flash should be simply pulled up to 3.3V.

See the Omega2S reference design schematic for details - can be found in Section 7.

4. Electrical Specifications

4.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power supply voltage	Vcc		3.63	V
Input pin voltage	Vin	GND - 0.3 V	Vcc + 0.3 V	V
DC current through any digital I/O pin (except supplies)	Ipin		8	mA
Storage Temperature	Tstg	-20	80	˚C

4.2 Operating Conditions

Operation beyond the specified operating conditions can affect device reliability.

Parameter	Symbol	Min	Typical	Max	Units
Power supply voltage	Vcc	2.97	3.3	3.63	V
Input pin voltage range	Vin	-0.3		3.3	V
Digital pin low level input voltage	Vil	-0.3		0.8	V
Digital pin high level input voltage	Vih	2		3.6	V
Digital pin low level output voltage	Vol			0.4	V
Digital pin high level output voltage	Voh	2.4		3.3	V
Operating Temperature	Topr	-10		55	˚C

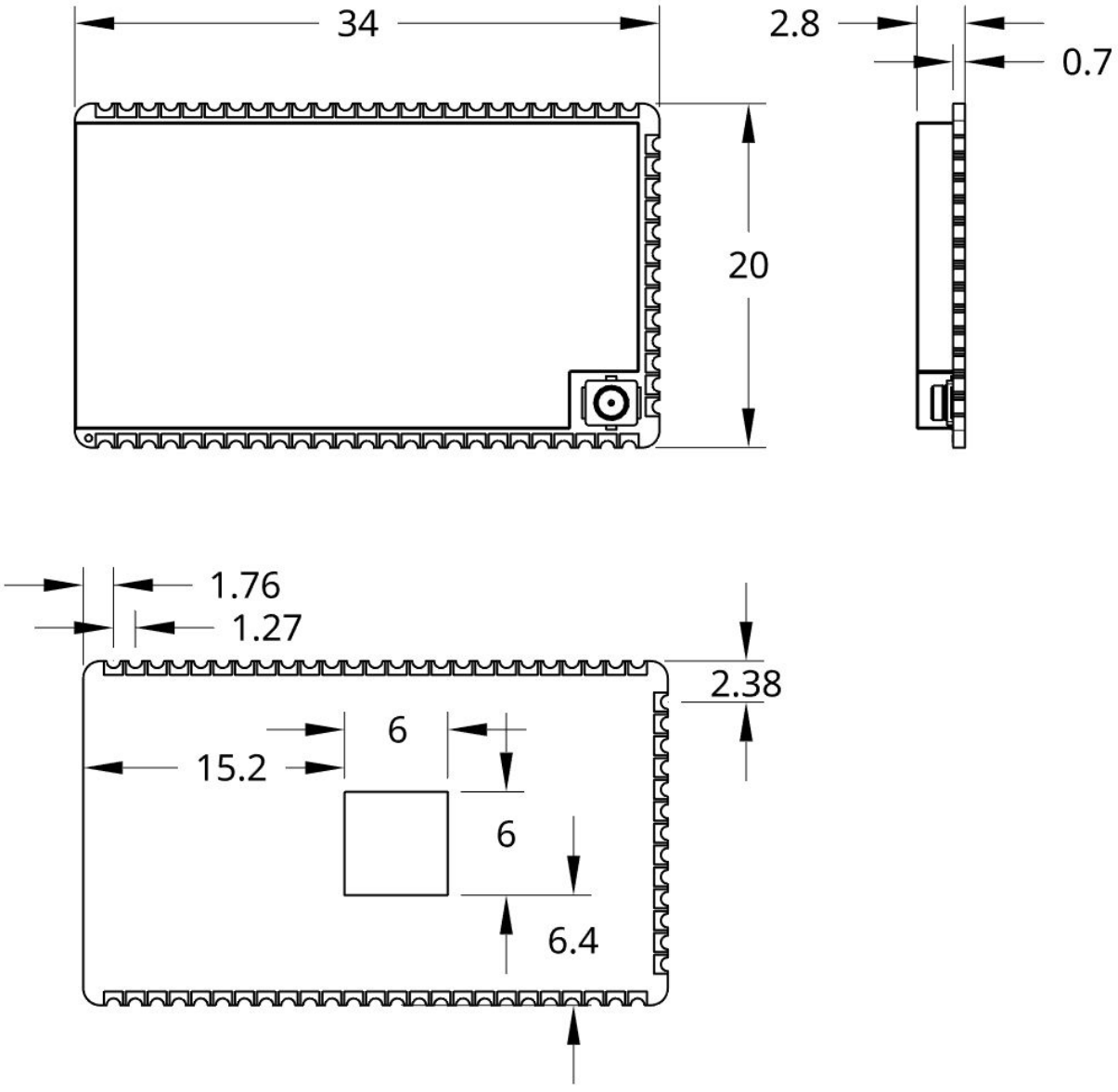
4.3 Power Consumption

State	Peak Current	Typical Current	Units
Booting	180	170	mA
Idle & Connected to WiFi network	190	170	mA
Idle & WiFi radio turned off	130	130	mA
Actively downloading files through WiFi	310	260	mA
Actively downloading files through WiFi, CPU at full load	400	310	mA

Note: All current measurements correspond to Vcc of 3.3V.
Note: These numbers are not based on exhaustive testing and should be used as reference values

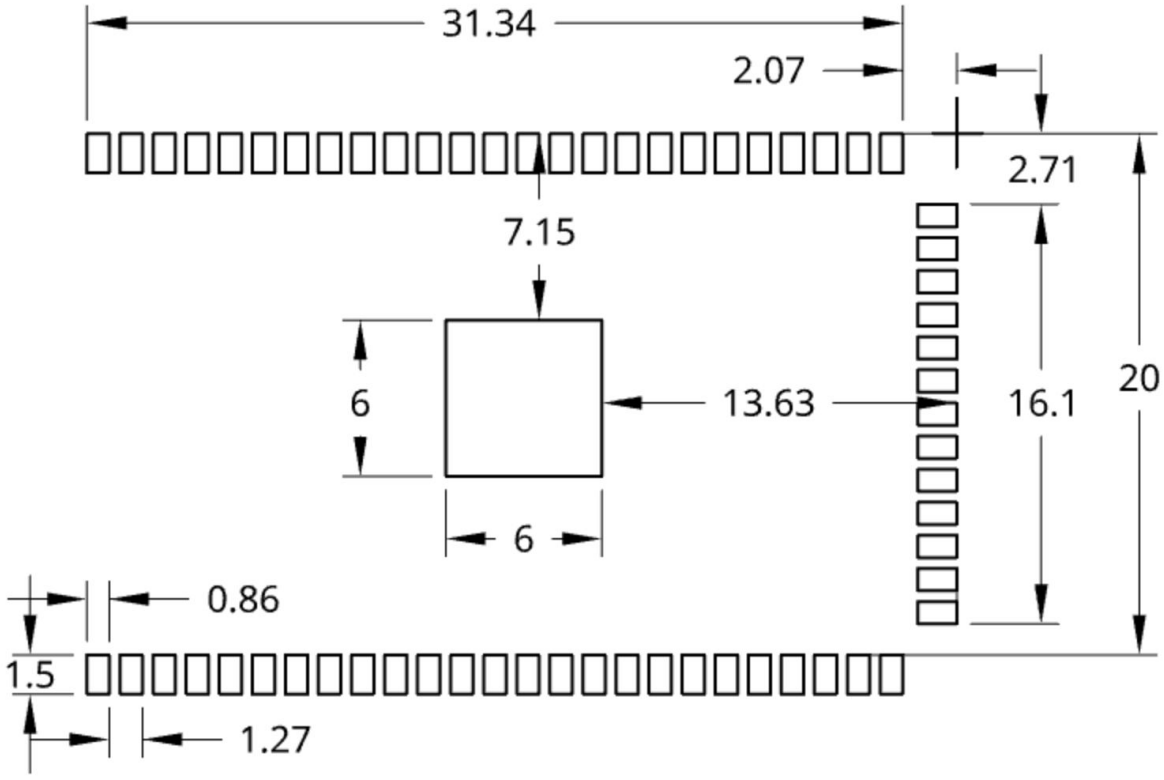
5. Mechanical Specifications

5.1 Mechanical Drawing



* All measurements in millimeters

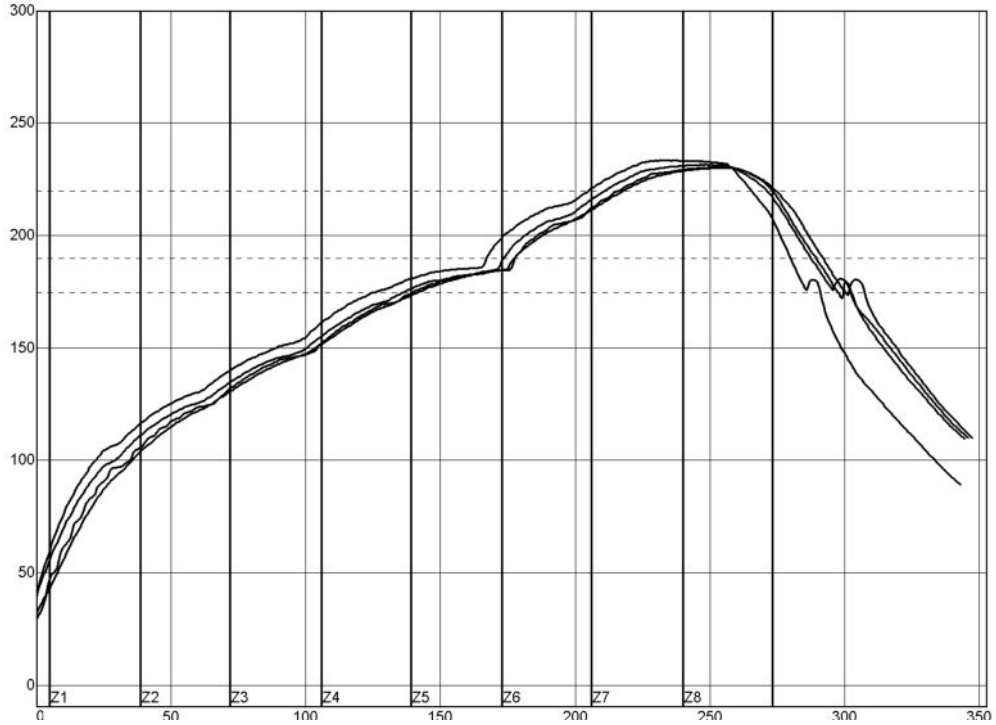
5.2 Recommended PCB Footprint



* All measurements in millimeters

6. Reflow Soldering

Reflow Profile for SIP on board Assembly



Preheat	Dwell	Peak
150˚C ~ 200˚C 90+5/-10 Sec	Over 220˚C 70+5/-10 Sec	240 +5/-10˚C

Ramp Up/Down Rate	
Up：3 +0/-2˚C /Sec	Down：2 +0/-1˚C /Sec

7. Additional Resources

7.1 Omega2S Reference Design Schematics

An Omega2S reference design and its schematic are available online.

7.1 Omega2 Online Documentation

Extensive documentation for the Omega2 family is hosted online. This documentation also applies to the Omega2S.

It can be found here: http://docs.onion.io/

8. Datasheet Revision History

Revision	Date	Description
1.4	March 7, 2019	Overview now highlights key aspects of the operating system and software. Updated SPI interface max speed.
1.3	February 20, 2019	Addition of feature details, updated pin layout diagram and pin numbering, improved mechanical drawing, added recommended PCB footprint
1.2	June 25, 2018	Added pin layout diagram, updated pinout diagram, added sections with information on special GPIOs
1.1	January 31, 2018	Updated pinout diagram, mechanical drawing, and pin definition table