OSD62x-PM Datasheet

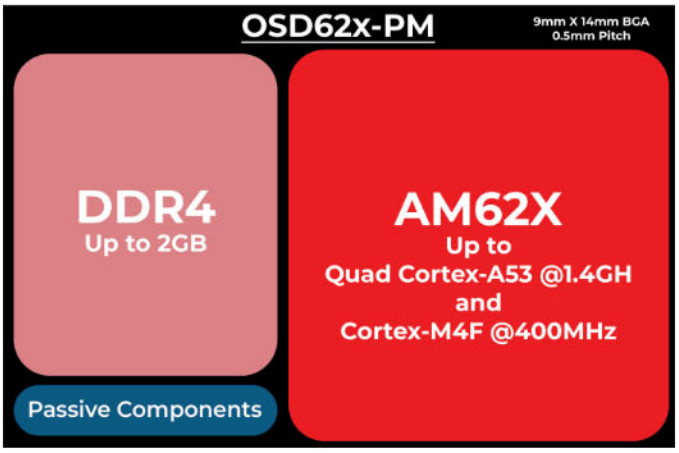
Rev. 1.0 6/1/2025

Introduction

The OSD62x-PM (Processor Module) System-in-Package (SiP) device is based on Texas Instruments AM62x Processor. This device integrates up to a quad-core 64-bit Arm® Cortex®-A53 at up to 1.4GHz and a single core Arm® Cortex®-M4F at up to 400MHz along with up to 2GB of DDR4 memory and associated passives into a single 9mm x 14mm BGA package.

Benefits

- Size optimized footprint with integrated DDR
- Compatible with AM62x development tools and software
- Significantly reduces design time
- Decreases layout complexity
- Optimized BGA ball layout allows lower cost PCB
- Simplifies component sourcing
- Increased reliability



Features

- Integrated into a 9mm X 14mm BGA Package:
  - Texas Instruments AM62
  - DDR4
  - Passives

- AM62 Features:
  - Up to 4x Arm® Cortex®-A53 @1.4GHz
  - Arm® Cortex®-M4F @400MHz
  - Display subsystem
    - Supports 2x 1920×1080 @ 60fps
    - OLDI/LVDS (4 lanes – 2x)
    - 24-bit RGB parallel interface
  - 3D Graphics Processing Unit
    - Supports up to 2048×1080 @60fps
    - OpenGL ES 3.1, Vulkan 1.2

- Access to All AM62 Peripherals Including:
  - MIPI CSI 1.3 Compliant + MIPI-DPHY 1.2
  - 10/100/1000 Ethernet Switch
    - Support for Time Sensitive Networking (TSN)
  - 2x USB2.0 Ports
  - 9x UART, 5x SPI, 6x I2C, 3x McASP
  - 3x ePWM, 3x eQEP, 3x eCAP
  - 3x CAN-FD
  - 1x eMMC, 2x SDIO, 1x GPMC

Package

- Size: 9mm x 14mm
- BGA pitch: 0.5mm

Temperature Range

- Industrial: -40° to 85°C

Table of Contents

1 Revision History

Revision Number	Revision Date	Changes	Author
1.0	6/1/2025	Production Release	Erik Welsh

NOTICE: These devices are susceptible to moisture and are classified as **MSL 4**. Ensure you are following the guidelines in the Storage Requirements section in this document.

2 Product Number Information

Figure 2-1 shows an example of an orderable product number for the OSD62x family. This section explains the different sections of the product number. It also lists the valid entries and their meaning for each designator.

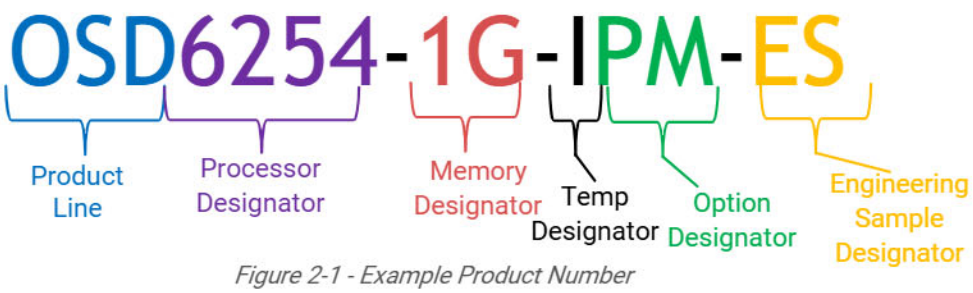


Figure 2-1 - Example Product Number

Product Designator – Three letters that designate the family of the device. Table 2-1 shows the family designator.

Table 2-1 - Family Designator

Family Designator	Product Line
OSD	OSD Product Line

Processor Designator – A set of letters and numbers that designate the specific processor in the device. Table 2-2 shows the valid values for the Processor Designator.

Table 2-2 - Processor Designators

Processor Designator	Processor
6254	Texas Instruments AM6254

Memory Designator – A set of letters and numbers that designate the DDR4 memory size in the device. Table 2-3 shows the valid values for the Memory Designator.

Table 2-3 - Memory Designator

Memory Designator	DDR Memory Size
1G	1GB DDR4 x16

Temp Designator – A letter or number that designates the operating case temperature range of the device. Table 2-4 shows the valid values for the Temp Designator.

Table 2-4 - Temp Designator

Temp Designator	Temperature Range
I	Industrial: -40 to 85°C

Option Designator – A set of letters or numbers that designates the set of features in the device. Table 2-5 shows the valid values for the Option Designator unique for the OSD62x devices.

Table 2-5 - Option Designator

Option Designator	Device Options
PM	Processor Module – AM62x + DDR4 + Passives

Engineering Sample Designator – A marker that designates if the product is an Engineering Sample or a Production device. Table 2-6 shows the valid values for the Engineering Sample Designator unique for the OSD62x devices.

Table 2-6 - Option Designator

Option Designator	Engineering Sample Designator
-ES	Part is an Engineering Sample and is covered by the Engineering Sample Disclaimer
[blank]	Production Device

3 Reference Documents

3.1 Data Sheets

Table 3-1 lists links to documents for the key devices used in the OSD62x-PM. Please refer to them for specifics on each device. The remainder of this document will describe how the devices are used in the OSD62x-PM system. It will also highlight any differences between the functionality and performance stated in the device specific datasheet and what should be expected from its operation in the OSD62x-PM.

Table 3-1 - Integrated Component Reference Documents

Component	Type	Document	Link
AM62x	**Processor**	Data Sheet	https://www.ti.com/lit/gpn/am625
		TRM	https://www.ti.com/lit/pdf/spruiv7

3.2 Other References

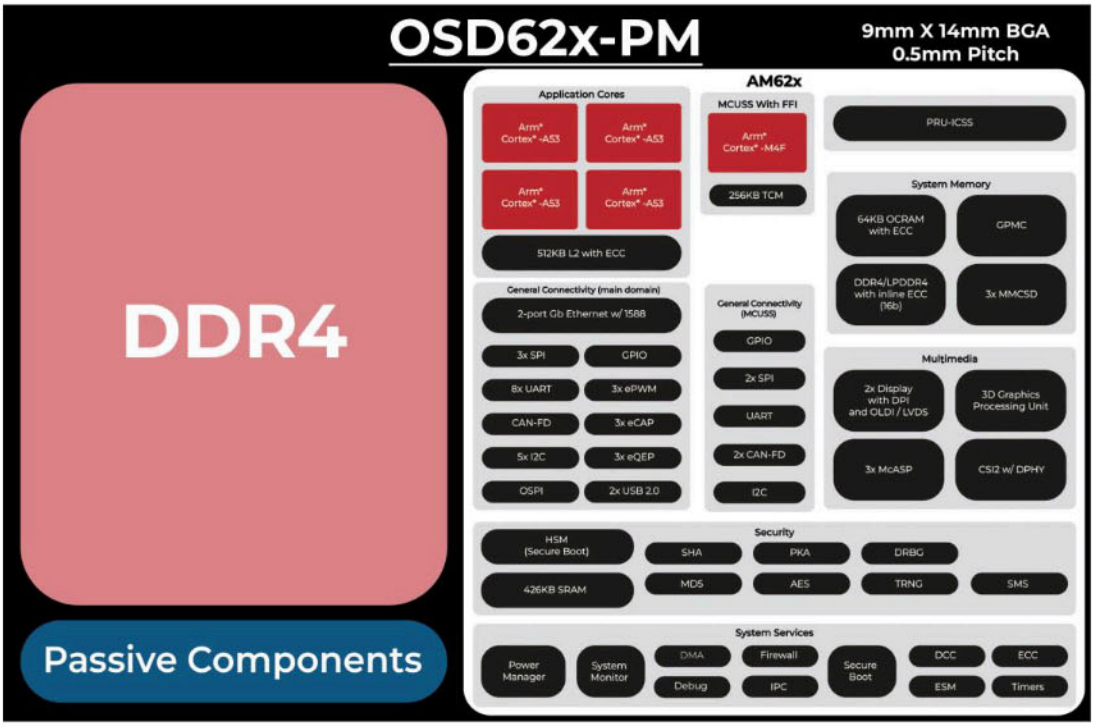
This section contains links to other reference documents helpful when using the OSD62x-PM device. Some are referenced in this document.

- OSD62x-PM Layout Guide:
  https://octavosystems.com/app_notes/osd62x-pm-layout-guide/
- OSD62x-PM Power Application Note:
  https://octavosystems.com/app_notes/osd62x-pm-power-application-note/
- OSD62x-PM Pin Mapping to AM62x:
  https://octavosystems.com/app_notes/osd62x-pm-pin-mapping-to-am62x/
- OSD62x-PM Thermal Guide:
  https://octavosystems.com/app_notes/osd62x-pm-thermal-guide/
- OSD62x-PM DDR Parameter Include File:
  https://github.com/octavosystems/osd62-pm-ddr
- OSD62x-PM Schematic Check List:
  https://octavosystems.com/app_notes/osd62x-pm-schematic-check-list/
- OSD62x-PM Footprint and symbol:
  https://octavosystems.com/octavo_products/osd62x-pm/#Symbols
- Handling & Process Recommendations:
  https://www.ti.com/lit/an/snoa550h/snoa550h.pdf

4 Block Diagram

The OSD62x-PM devices consist of 2 main components. The processor is the AM62x from Texas Instruments featuring up to a Quad-core Arm® Cortex®-A53 running up to 1.4GHz with a Single-core Arm® Cortex® M4F up to 400MHz. The system memory includes up to 16Gb (2GB) of DDR4 x16. Finally, there are required passives for the processor-DDR interface as well as passives to aid power requirements. Figure 4-1 shows a block diagram of the OSD62x-PM and breaks out the key functions of the AM62x.

Figure 4-1 – OSD62x-PM Detailed Block Diagram



4.1 Passives

Besides the 2 major components, the OSD62x-PM also integrates capacitors and resistors (Passives). The following sections detail the relevant integrated passives beyond what is required for the processor – DDR interface. Section 4.1.1 details the relevant integrated resistors, Section 4.1.2.1 details the integrated capacitors, and Section 4.1.2.2 details the recommended external capacitors you may need for proper operation of the OSD62x-PM.

4.1.1 Integrated Resistors

Table 4-1 lists the relevant pull-up/down resistor locations and values integrated into the OSD62x-PM beyond those required for the processor – DDR interface.

Table 4-1 – OSD62x-PM Integrated Resistors

From	To	Device	Description	Value (Ohms)
CSI0_RXRCALIB	GND	AM62x	CSI0 Calibration Resistor	499, ±1%
USB0_RCALIB	GND	AM62x	USB0 Calibration Resistor	499, ±1%
USB1_RCALIB	GND	AM62x	USB1 Calibration Resistor	499, ±1%

4.1.2 Capacitors

The OSD62x-PM includes some of the capacitors TI recommends for AM62x SoC. External capacitors will be needed to ensure proper operation. This section will cover the list of capacitors integrated into the OSD62x-PM and those recommended to be included externally.

4.1.2.1 Integrated Capacitors

Table 4-2 lists relevant integrated capacitors in the OSD62x-PM beyond those required by the processor – DDR interface.

Table 4-2 – OSD62x-PM Integrated Capacitors

AM62x Voltage Rail Pin Name	Device	OSD62x-PM Voltage Rail Pin Name	Total Internal Capacitance (µF)
CAP_VDDS0	AM62x	N/A(1)	1
CAP_VDDS1	AM62x	N/A(1)	1
CAP_VDDS2	AM62x	N/A(1)	1
CAP_VDDS3	AM62x	N/A(1)	1
CAP_VDDS4	AM62x	N/A(1)	1
CAP_VDDS5	AM62x	N/A(1)	1
CAP_VDDS6	AM62x	N/A(1)	1
CAP_VDDS_CANUART	AM62x	N/A(1)	1
CAP_VDDS_MCU	AM62x	N/A(1)	1
VDD_CORE	AM62x	VDD_CORE	6(2)
VDDA_CORE_CSIRX0	AM62x	VDDA_CORE_CSIRX0	0.01
VDDA_CORE_USB	AM62x	VDDA_CORE_USB	0.01
VDD_CANUART	AM62x	VDD_CANUART	0.01
VDDR_CORE	AM62x	VDDR_CORE	6(2)
VDDS_DDR	AM62x/DDR	VDDS_DDR	16(2)
VDDA_1P8_OLDI0	AM62x	VDDA_1P8_OLDI0	0.01
VDDA_1P8_CSIRX0	AM62x	VDDA_1P8_CSIRX0	0.01
VDDA_1P8_USB	AM62x	VDDA_1P8_USB	0.01
VDDA_MCU	AM62x	VDDA_MCU	0.01
VDDA_PLL0	AM62x	VDDA_PLL0	0.01
VDDA_PLL1	AM62x	VDDA_PLL1	0.01
VDDA_PLL2	AM62x	VDDA_PLL2	0.01
VDDS_OSC0	AM62x	VDDS_OSC0	0.01

1. Signal internal to the SiP.
2. Approximate Value.

4.1.2.2 External Capacitor Recommendations

The system designer will need to add the necessary capacitors to their design to ensure proper operation of the OSD62x-PM.

Table 4-3 is a list of recommended capacitors that a designer should include in a PCB design.

It is recommended that the external capacitors be placed as near to the appropriate power balls of the OSD62x-PM SiP as possible. The recommendations are based on Design Guidelines from Texas Instruments.

Note: Capacitors may be placed on either side of the PBC. See the Layout Guide for capacitor placement recommendations.

Table 4-3 – OSD62x-PM Recommended Capacitors

OSD62x-PM Voltage Rail	Device	Total Capacitance (µF)	Capacitor size (µF)				
			10	4.7	1	0.1	0.01
VDD_CORE(1)	AM62x	11	1			6	
VDDA_CORE_CSIRX0(1)	AM62x	4.8		1		1	
VDDA_CORE_USB(1)	AM62x	4.8		1		1	
VDD_CANUART(1)	AM62x	4.8		1		1	
VDDR_CORE	AM62x	0.4				3	
VDDS_DDR	AM62x/DDR	0.2				3	
DDR_VPP	DDR	0.1				1	
VDDA_1P8_OLDI0(2)	AM62x	1.1			1	1	
VDDA_1P8_CSIRX0(2)	AM62x	4.8		1		1	
VDDA_1P8_USB(2)	AM62x	4.8		1		1	
VDDA_MCU(2)	AM62x	4.8			1	1	
VDDA_PLL0(2)	AM62x	4.8			1	1	
VDDA_PLL1(2)	AM62x	4.8			1	1	
VDDA_PLL2 (2)	AM62x	4.8			1	1	
VPP(3)	AM62x	2.1			2	1	
VDDA_3P3_USB	AM62x	0.1				1	

1. If all core power rails are connected together, then only the capacitors for VDD_CORE are required.
2. If all 1.8V power rails are connected together, then only the capacitors for VDDA_1P8_OLDI0 and VDDA_1P8_CSIRX0 + 1x 1uF are required.
3. Only required for eFUSE programming. VPP supply should be disabled during normal operation.

** Please ensure that your design has enough 0.1µF capacitors to not cause EMI / EMC issues. From a design perspective, it is better to have more capacitor locations and not populate them, than to not have enough capacitor locations.

5 Ball Map

The signal names in the OSD62x-PM Ball Map for the AM62x have been named so they can be cross-referenced to the corresponding pin in the AM62x support documents.

Refer to Table 5-6 and Table 5-7 for more detailed signal name mapping between OSD62x-PM pin names and AM62x pin names.

The arrangement of the signals has been optimized for easy escape from the BGA. Table 5-1 through Table 5-5 show the ball map for the OSD62x-PM. Each is shown in a top view looking through the package. See Layout Guide in the Reference Documents section for more details.

Table 5-1 – OSD62x-PM Ball Map Top View

	1	2	3	4	5	6
A		VSS	MCU_ UART0_RTSN	MCU_ SPI0_CLK	MCU_ SPI0_D1	MCU_ SPI0_CS1
B	VSS	MCU_ UART0_RXD	MCU_ UART0_TXD	MCU_ UART0_CTSN	MCU_ SPI0_D0	MCU_ SPI0_CS0
C	WKUP_ UART0_TXD	WKUP_ UART0_RXD	VSS	VSS	MCU_RESETZ	MCU_ RESETSTATZ
D	WKUP_ UART0_CTSN	WKUP_ UART0_RTSN	VSS	VSS	PMIC_LPM_ EN0	MCU_PORZ
E	MCU_ MCAN0_RX	MCU_ MCAN0_TX	VSS	VSS	VSS	VSS
F	MCU_ MCAN1_RX	MCU_ MCAN1_TX	NC	RSVD1	RSVD0	RSVD2
G	MCU_OSC0_ XI	MCU_OSC0_ XO	NC	NC	NC	NC
H	WKUP_ LFOSC0_XI	WKUP_ LFOSC0_XO	NC	NC	NC	NC
J	MMC0_CLK	NC	NC	NC	NC	NC
K	MMC0_CMD	MMC0_ DAT0	NC	NC	NC	VSS
L	MMC0_ DAT1	MMC0_ DAT2	NC	NC	VSS	VSS
M	MMC0_ DAT3	MMC0_ DAT4	NC	VSS	VSS	VSS
N	MMC0_ DAT5	MMC0_ DAT6	VSS	VSS	VSS	VSS
P	MMC0_ DAT7	OLDI0_A0N	VSS	VSS	VSS	NC
R	OLDI0_A0P	OLDI0_A1N	VSS	VSS	NC	NC
T	OLDI0_A1P	OLDI0_A2N	VSS	NC	NC	NC
U	VSS	OLDI0_A2P	OLDI0_A3N	OLDI0_A4N	OLDI0_A5N	OLDI0_A6N
V		VSS	OLDI0_A3P	OLDI0_A4P	OLDI0_A5P	OLDI0_A6P

Table 5-2 – OSD62x-PM Ball Map Top View

	7	8	9	10	11	12
A	MCU_I2C0_SCL	WKUP_I2C0_SCL	UART0_CTSN	UART0_RXD	MCAN0_RX	I2C0_SCL
B	MCU_I2C0_SDA	WKUP_I2C0_SDA	UART0_RTSN	UART0_TXD	MCAN0_TX	I2C0_SDA
C	WKUP_CLKOUT0	EMU1	TRSTN	TMS	SPI0_CLK	SPI0_D1
D	MCU_ERRORN	EMU0	TCK	TDI	TDO	SPI0_D0
E	VSS	VSS	VSS	VSS	VSS	VSS
F	RSVD8	RSVD4	RSVD5	DDR_RSVD0	VDDSHV_CANUART	VDDSHV_MCU
G	NC	NC	NC	VDDSHV_CANUART	VDDSHV_MCU	VDD_CANUART
H	NC	NC	NC	NC	NC	VDD_CORE
J	NC	NC	NC	NC	NC	VDD_CORE
K	VSS	VSS	VSS	VDDS_DDR	VDDS_DDR	VDD_CORE
L	VSS	VSS	VDDS_DDR	VDDS_DDR	VDDS_DDR	NC
M	VSS	VDDS_DDR	VDDS_DDR	VDDS_DDR	NC	VDDA_CORE_USB
N	VDDA_3P3_USB	VDDS_DDR	VDDS_DDR	DDR_VPP	VDDSHV4	VDDA_TEMP
P	NC	NC	NC	VDDSHV4	VDDA_1P8_OLDI0	VDDA_1P8_USB
R	NC	NC	NC	NC	NC	NC
T	NC	NC	NC	NC	NC	NC
U	OLDI0_A7N	OLDI0_CLK0N	OLDI0_CLK1N	USB1_DM	USB1_VBUS	USB0_DM
V	OLDI0_A7P	OLDI0_CLK0P	OLDI0_CLK1P	USB1_DP	USB0_VBUS	USB0_DP

Table 5-3 – OSD62x-PM Ball Map Top View

	13	14	15	16	17	18
A	I2C1_SCL	VSS	VMON_VSYS	MCASP0_ AXR3	MCASP0_ AXR1	MCASP0_ ACLKX
B	I2C1_SDA	VSS	VMON_3P3_ SOC	MCASP0_ AXR2	MCASP0_ AXR0	MCASP0_ AFSX
C	SPI0_CS1	VSS	VMON_1P8_ SOC	VPP	EXTINTN	RESETSTATZ
D	SPI0_CS0	VSS	VDDS_OSC0	EXT_ REFCLK1	RESET_ REQZ	PORZ_OUT
E	VSS	NC	NC	VSS	VSS	VSS
F	VDDA_MCU	VDDA_PLL2	NC	NC	NC	NC
G	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	NC	NC
H	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDDR_CORE	VDDR_CORE
J	VDD_CORE	VSS	VSS	VDD_CORE	VDDR_CORE	VDDR_CORE
K	VDD_CORE	VSS	VSS	VDD_CORE	VDDR_CORE	VDDR_CORE
L	VDD_CORE	VDD_CORE	VDD_CORE	NC	VDDR_CORE	VDDR_CORE
M	VDDA_CORE_ CSIRX0	NC	NC	NC	NC	RSVD6
N	VDDA_PLL0	VDDA_PLL1	NC	NC	RSVD3	RSVD7
P	VDDA_1P8_ CSIRX0	NC	NC	VSS	VSS	VSS
R	NC	NC	NC	NC	NC	NC
T	NC	NC	NC	NC	NC	NC
U	CSI0_RXN3	CSI0_RXN2	CSI0_RXP1	CSI0_RXP0	CSI0_ RXCLKP	NC
V	CSI0_RXP3	CSI0_RXP2	CSI0_RXN1	CSI0_RXN0	CSI0_ RXCLKN	NC

Table 5-4 – OSD62x-PM Ball Map Top View

	19	20	21	22	23	24
A	MCASP0_ AFSR	MMC1_ DAT2	MMC1_ CMD	MMC1_ DAT0	MMC1_ SDCD	OSPI0_ CLK
B	MCASP0_ ACLKR	MMC1_ DAT3	MMC1_ CLK	MMC1_ DAT1	MMC1_ SDWP	OSPI0_ D0
C	USB0_ DRVVBUS	MMC2_ SDWP	MMC2_ DAT3	MMC2_ DAT1	MMC2_ CMD	OSPI0_ CSN3
D	USB1_ DRVVBUS	MMC2_ SDCD	MMC2_ DAT2	MMC2_ DAT0	MMC2_ CLK	OSPI0_ CSN2
E	VSS	VSS	VSS	VSS	VSS	VSS
F	VSS	VSS	VSS	VSS	VSS	VSS
G	VSS	VSS	VDDSHV5	VDDSHV5	VSS	VSS
H	VSS	VSS	VDDSHV6	VDDSHV6	NC	VSS
J	VSS	VSS	VDDSHV0	VDDSHV0	NC	VSS
K	VSS	VSS	VDDSHV1	VDDSHV1	NC	VSS
L	VSS	VSS	VDDSHV3	VDDSHV3	NC	VSS
M	NC	VSS	VDDSHV2	VDDSHV2	VSS	VSS
N	NC	VSS	VSS	VSS	VSS	VSS
P	VSS	VSS	VSS	VSS	VSS	VSS
R	RGMII2_ TXC	RGMII2_ TD3	RGMII2_ TD1	RGMII2_ RXC	RGMII2_ RD3	RGMII2_ RD1
T	VSS	RGMII2_ TX_CTL	RGMII2_ TD2	RGMII2_ TD0	RGMII2_ RX_CTL	RGMII2_ RD2
U	VSS	RGMII1_ RXC	RGMII1_ RD2	RGMII1_ RD0	RGMII1_ TXC	RGMII1_ TD2
V	VSS	RGMII1_ RX_CTL	RGMII1_ RD3	RGMII1_ RD1	RGMII1_ TX_CTL	RGMII1_ TD3

Table 5-5 – OSD62x-PM Ball Map Top View

	25	26	27	28
A	OSPI0_ D1	OSPI0_ D3	VSS	
B	OSPI0_ D2	OSPI0_ D4	OSPI0_ D5	VSS
C	OSPI0_ CSN1	OSPI0_ LBCLKO	OSPI0_ D6	OSPI0_ D7
D	OSPI0_ CSN0	OSPI0_ DQS	GPMC0_ AD7	GPMC0_ AD6
E	GPMC0_ CSN3	GPMC0_ CSN2	GPMC0_ AD5	GPMC0_ AD4
F	GPMC0_ CSN1	GPMC0_ CSN0	GPMC0_ AD3	GPMC0_ AD2
G	GPMC0_ DIR	GPMC0_ WPN	GPMC0_ AD1	GPMC0_ AD0
H	GPMC0_ ADVN_ALE	GPMC0_ OEN_REN	GPMC0_ AD15	GPMC0_ AD14
J	GPMC0_ WEN	GPMC0_ BE0N_CLE	GPMC0_ AD13	GPMC0_ AD12
K	GPMC0_ BE1N	GPMC0_ CLK	GPMC0_ AD10	GPMC0_ AD11
L	GPMC0_ WAIT0	GPMC0_ WAIT1	GPMC0_ AD8	GPMC0_ AD9
M	VOUT0_ DATA3	VOUT0_ DATA4	VOUT0_ DATA14	VOUT0_ DATA15
N	VOUT0_ DATA1	VOUT0_ DATA2	VOUT0_ DATA12	VOUT0_ DATA13
P	VOUT0_ HSYNC	VOUT0_ DATA0	VOUT0_ DATA10	VOUT0_ DATA11
R	VOUT0_ DE	VOUT0_ VSYNC	VOUT0_ DATA8	VOUT0_ DATA9
T	RGMII2_ RD0	VOUT0_ PCLK	VOUT0_ DATA6	VOUT0_ DATA7
U	RGMII1_ TD0	MDIO0_ MDIO	VOUT0_ DATA5	VSS
V	RGMII1_ TD1	MDIO0_ MDC	VSS	

5.1 Ball Description

Table 5-6 and Table 5-7 list the unique signals and pin numbers of the OSD62x-PM. Where applicable they also provide the signal name and ball number of the equivalent signal of the AM62x AMC package. Additionally, all the processor signals have the same function as the equivalent pin in the AM62x except where noted.

Table 5-6 – OSD62x-PM Ball Descriptions for Power and Grounds

OSD62x-PM		AM62x (AMC)		Comments
Pin Name	**Pin Number**	**Pin Name**	**Pin Number**	
VDD_CORE	G13, G14, G15, G16, H12, H13, H14, H15, H16, J12, J13, J16, K12, K13, K16, L13, L14, L15	VDD_CORE / VDDA_DDR_PLL0	H12, H14, J11, J13, J9, K10, K14, L11, L13, M12, M14, M8, N11, N13, N9, P8, L9	Core Supply
VDDA_CORE_CSIRX0	M13	VDDA_CORE_CSIRX0	P12	CSIRX0 core supply
VDDA_CORE_USB	M12	VDDA_CORE_USB	P11	USB0 and USB1 core supply
VDD_CANUART	G12	VDD_CANUART	H8	CANUART core supply
VDDR_CORE	H17, H18, J17, J18, K17, K18, L17, L18	VDDR_CORE	H11, M10, M13	RAM supply
VDDS_DDR	K10, K11, L9, L10, L11, M8, M9, M10, N8, N9	VDDS_DDR / VDDS_DDR_C	C1, J8, K7, K9, L8, U1, L7	DDR supply
DDR_VPP	N10	-	-	DRAM VPP voltage supply
VDDA_1P8_OLDI0	P11	VDDA_1P8_OLDI0	P9, R9	OLDI0 1.8 V analog supply
VDDA_1P8_CSIRX0	P13	VDDA_1P8_CSIRX0	R12	CSIRX0 1.8 V analog supply
VDDA_1P8_USB	P12	VDDA_1P8_USB	R11	USB0 and USB1 1.8 V analog supply
VDDA_PLL0	N13	VDDA_PLL0	N10	MAIN PLL, DDR PLL, DSS PLL0, and DSS PLL1 analog supply
VDDA_PLL1	N14	VDDA_PLL1	P14	PER0 PLL and PER1 PLL analog supply
VDDA_PLL2	F14	VDDA_PLL2	K12	ARM0 PLL and SMS PLL analog supply
VDDA_MCU	F13	VDDA_MCU	H10	RCOSC, POR, POK, and MCU PLL analog supply
VDDA_TEMP	N12	VDDA_TEMP0 / VDDA_TEMP1	M7, F16	TEMP analog supply
VDDS_OSC0	D15	VDDS_OSC0	J7	MCU_OSC0 supply
VDDA_3P3_USB	N7	VDDA_3P3_USB	R10	USB0 and USB1 3.3 V analog supply
VPP	C16	VPP	F7	eFuse ROM programming supply
VDDSHV_CANUART	F11, G10	VDDSHV_CANUART	G7, H7	IO supply for CANUART
VDDSHV_MCU	F12, G11	VDDSHV_MCU	F10, G10	IO supply for MCU
VDDSHV0	J21, J22	VDDSHV0	F12, G13	IO supply for IO group 0
VDDSHV1	K21, K22	VDDSHV1	K15, K16	IO supply for IO group 1
VDDSHV2	M21, M22	VDDSHV2	R14, R15	IO supply for IO group 2
VDDSHV3	L21, L22	VDDSHV3	N15, N16	IO supply for IO group 3
VDDSHV4	N11, P10	VDDSHV4	N7, P7	IO supply for IO group 4
VDDSHV5	G21, G22	VDDSHV5	F14, G14	IO supply for IO group 5
VDDSHV6	H21, H22	VDDSHV6	H15, H16	IO supply for IO group 6
VMON_VSYS	A15	VMON_VSYS	F6	Voltage monitor input
VMON_1P8_SOC	C15	VMON_1P8_SOC	H9	Voltage monitor input for 1.8V SoC power supply
VMON_3P3_SOC	B15	VMON_3P3_SOC	K11	Voltage monitor input for 3.3V SoC power supply
VSS	A2, A14, A27, B1, B14, B28, C3, C4, C14, D3, D4, D14, E3, E4, E5, E6, E7,	VSS	A1, A21, A4, AA1, AA12, AA15, AA21, AA9, D11, D19, D4,	Ground

OSD62x-PM		AM62x (AMC)		Comments
Pin Name	Pin Number	Pin Name	Pin Number	
	E8, E9, E10, E11, E12, E13, E16, E17, E18, E19, E20, E21, E22, E23, E24, F19, F20, F21, F22, F23, F24, G19, G20, G23, G24, H19, H20, H24, J14, J15, J19, J20, J24, K6, K7, K8, K9, K14, K15, K19, K20, K24, L5, L6, L7, L8, L19, L20, L24, M4, M5, M6, M7, M20, M23, M24, N3, N4, N5, N6, N20, N21, N22, N23, N24, P3, P4, P5, P16, P17, P18, P19, P20, P21, P22, P23, P24, R3, R4, T3, T19, U1, U19, U28, V2, V19, V27		E2, F11, F13, F15, F4, F9, G16, G6, G9, H1, H13, H6, J10, J12, J14, J16, J6, K13, K3, K6, K8, L1, L10, L12, L14, L16, L6, M11, M16, M18, M6, M9, N12, N14, N6, P1, P10, P13, P15, P16, P3, P6, R16, R5, R7, R8, T10, T12, T15, T3, T6, T7, T9, U10, U13, U5, U8, V11, V14, V19, W10, W13, W7, Y11, Y14, Y3, Y4, Y6	

Table 5-7 – OSD62x-PM Ball Descriptions for IO Signals

OSD62x-PM		AM62x (AMC)		Comments
Pin Name	Pin No.	Pin Name	Pin No.	
CSI0_RXCLKN	V17	CSI0_RXCLKN	AA14	
CSI0_RXCLKP	U17	CSI0_RXCLKP	AA13	
CSI0_RXN0	V16	CSI0_RXN0	Y13	
CSI0_RXN1	V15	CSI0_RXN1	V13	
CSI0_RXN2	U14	CSI0_RXN2	U12	
CSI0_RXN3	U13	CSI0_RXN3	W12	
CSI0_RXP0	U16	CSI0_RXP0	Y12	
CSI0_RXP1	U15	CSI0_RXP1	V12	
CSI0_RXP2	V14	CSI0_RXP2	U11	
CSI0_RXP3	V13	CSI0_RXP3	W11	
EMU0	D8	EMU0	D9	
EMU1	C8	EMU1	B10	
EXTINTN	C17	EXTINTN	B16	
EXT_REFCLK1	D16	EXT_REFCLK1	C14	
GPMC0_ ADVN_ALE	H25	GPMC0_ ADVN_ALE	K20	
GPMC0_CLK	K26	GPMC0_CLK	M19	
GPMC0_DIR	G25	GPMC0_DIR	J19	
GPMC0_OEN_REN	H26	GPMC0_OEN_REN	K21	
GPMC0_WEN	J25	GPMC0_WEN	J17	
GPMC0_WPN	G26	GPMC0_WPN	J20	
GPMC0_AD0	G28	GPMC0_AD0	K19	
GPMC0_AD1	G27	GPMC0_AD1	L19	
GPMC0_AD2	F28	GPMC0_AD2	L20	
GPMC0_AD3	F27	GPMC0_AD3	L21	
GPMC0_AD4	E28	GPMC0_AD4	M21	
GPMC0_AD5	E27	GPMC0_AD5	L17	
GPMC0_AD6	D28	GPMC0_AD6	L18	
GPMC0_AD7	D27	GPMC0_AD7	M20	
GPMC0_AD8	L27	GPMC0_AD8	N20	
GPMC0_AD9	L28	GPMC0_AD9	N21	
GPMC0_AD10	K27	GPMC0_AD10	M17	
GPMC0_AD11	K28	GPMC0_AD11	N18	
GPMC0_AD12	J28	GPMC0_AD12	N17	
GPMC0_AD13	J27	GPMC0_AD13	N19	
GPMC0_AD14	H28	GPMC0_AD14	P19	
GPMC0_AD15	H27	GPMC0_AD15	P20	
GPMC0_BE0N_CLE	J26	GPMC0_BE0N_CLE	K17	
GPMC0_BE1N	K25	GPMC0_BE1N	K18	
GPMC0_CSN0	F26	GPMC0_CSN0	J18	
GPMC0_CSN1	F25	GPMC0_CSN1	H17	
GPMC0_CSN2	E26	GPMC0_CSN2	H18	
GPMC0_CSN3	E25	GPMC0_CSN3	H19	
GPMC0_WAIT0	L25	GPMC0_WAIT0	P21	
GPMC0_WAIT1	L26	GPMC0_WAIT1	P17	
I2C0_SCL	A12	I2C0_SCL	E12	
I2C0_SDA	B12	I2C0_SDA	D14	
I2C1_SCL	A13	I2C1_SCL	A17	
I2C1_SDA	B13	I2C1_SDA	A16	
MCAN0_RX	A11	MCAN0_RX	A15	
MCAN0_TX	B11	MCAN0_TX	B13	
MCASP0_ACLKR	B19	MCASP0_ACLKR	D16	
MCASP0_ACLKX	A18	MCASP0_ACLKX	C17	
MCASP0_AFSR	A19	MCASP0_AFSR	D15	
MCASP0_AFSX	B18	MCASP0_AFSX	C16	

OSD62x-PM		AM62x (AMC)		Comments
Pin Name	Pin No.	Pin Name	Pin No.	
MCASP0_AXR0	B17	MCASP0_AXR0	D18	
MCASP0_AXR1	A17	MCASP0_AXR1	A18	
MCASP0_AXR2	B16	MCASP0_AXR2	B17	
MCASP0_AXR3	A16	MCASP0_AXR3	B18	
MCU_ERRORN	D7	MCU_ERRORN	B1	
MCU_I2C0_SCL	A7	MCU_I2C0_SCL	B9	
MCU_I2C0_SDA	B7	MCU_I2C0_SDA	A10	
MCU_MCAN0_RX	E1	MCU_MCAN0_RX	C4	
MCU_MCAN0_TX	E2	MCU_MCAN0_TX	C5	
MCU_MCAN1_RX	F1	MCU_MCAN1_RX	D6	
MCU_MCAN1_TX	F2	MCU_MCAN1_TX	D5	
MCU_OSC0_XI	G1	MCU_OSC0_XI	A5	
MCU_OSC0_XO	G2	MCU_OSC0_XO	A6	
MCU_PORZ	D6	MCU_PORZ	B2	
MCU_RESETSTATZ	C6	MCU_RESETSTATZ	A12	
MCU_RESETZ	C5	MCU_RESETZ	C9	
MCU_SPI0_CLK	A4	MCU_SPI0_CLK	B7	
MCU_SPI0_CS0	B6	MCU_SPI0_CS0	E7	
MCU_SPI0_CS1	A6	MCU_SPI0_CS1	C8	
MCU_SPI0_D0	B5	MCU_SPI0_D0	E8	
MCU_SPI0_D1	A5	MCU_SPI0_D1	D8	
MCU_UART0_CTSN	B4	MCU_UART0_CTSN	B8	
MCU_UART0_RTSN	A3	MCU_UART0_RTSN	D7	
MCU_UART0_RXD	B2	MCU_UART0_RXD	A8	
MCU_UART0_TXD	B3	MCU_UART0_TXD	B6	
MDIO0_MDC	V26	MDIO0_MDC	V17	
MDIO0_MDIO	U26	MDIO0_MDIO	U16	
MMC0_CLK	J1	MMC0_CLK	Y1	
MMC0_CMD	K1	MMC0_CMD	V3	
MMC1_CLK	B21	MMC1_CLK	A20	
MMC1_CMD	A21	MMC1_CMD	C18	
MMC1_SDCD	A23	MMC1_SDCD	C15	
MMC1_SDWP	B23	MMC1_SDWP	B15	
MMC2_CLK	D23	MMC2_CLK	E21	
MMC2_CMD	C23	MMC2_CMD	C21	
MMC2_SDCD	D20	MMC2_SDCD	D20	
MMC2_SDWP	C20	MMC2_SDWP	C20	
MMC0_DAT0	K2	MMC0_DAT0	V2	
MMC0_DAT1	L1	MMC0_DAT1	V1	
MMC0_DAT2	L2	MMC0_DAT2	W2	
MMC0_DAT3	M1	MMC0_DAT3	W1	
MMC0_DAT4	M2	MMC0_DAT4	Y2	
MMC0_DAT5	N1	MMC0_DAT5	W3	
MMC0_DAT6	N2	MMC0_DAT6	W4	
MMC0_DAT7	P1	MMC0_DAT7	V4	
MMC1_DAT0	A22	MMC1_DAT0	A19	
MMC1_DAT1	B22	MMC1_DAT1	B19	
MMC1_DAT2	A20	MMC1_DAT2	B20	
MMC1_DAT3	B20	MMC1_DAT3	C19	
MMC2_DAT0	D22	MMC2_DAT0	B21	
MMC2_DAT1	C22	MMC2_DAT1	D21	
MMC2_DAT2	D21	MMC2_DAT2	E19	
MMC2_DAT3	C21	MMC2_DAT3	E20	
OLDI0_A0N	P2	OLDI0_A0N	AA2	
OLDI0_A0P	R1	OLDI0_A0P	AA3	
OLDI0_A1N	R2	OLDI0_A1N	V5	
OLDI0_A1P	T1	OLDI0_A1P	V6	

OSD62x-PM		AM62x (AMC)		Comments
Pin Name	Pin No.	Pin Name	Pin No.	
OLDI0_A2N	T2	OLDI0_A2N	U7	
OLDI0_A2P	U2	OLDI0_A2P	U6	
OLDI0_A3N	U3	OLDI0_A3N	W6	
OLDI0_A3P	V3	OLDI0_A3P	W5	
OLDI0_A4N	U4	OLDI0_A4N	AA4	
OLDI0_A4P	V4	OLDI0_A4P	Y5	
OLDI0_A5N	U5	OLDI0_A5N	AA6	
OLDI0_A5P	V5	OLDI0_A5P	AA5	
OLDI0_A6N	U6	OLDI0_A6N	AA10	
OLDI0_A6P	V6	OLDI0_A6P	Y9	
OLDI0_A7N	U7	OLDI0_A7N	AA8	
OLDI0_A7P	V7	OLDI0_A7P	Y8	
OLDI0_CLK0N	U8	OLDI0_CLK0N	V7	
OLDI0_CLK0P	V8	OLDI0_CLK0P	V8	
OLDI0_CLK1N	U9	OLDI0_CLK1N	Y7	
OLDI0_CLK1P	V9	OLDI0_CLK1P	AA7	
OSPI0_CLK	A24	OSPI0_CLK	G19	
OSPI0_DQS	D26	OSPI0_DQS	H20	
OSPI0_LBCLKO	C26	OSPI0_LBCLKO	G18	
OSPI0_CSN0	D25	OSPI0_CSN0	F19	
OSPI0_CSN1	C25	OSPI0_CSN1	F17	
OSPI0_CSN2	D24	OSPI0_CSN2	E17	
OSPI0_CSN3	C24	OSPI0_CSN3	E18	
OSPI0_D0	B24	OSPI0_D0	F18	
OSPI0_D1	A25	OSPI0_D1	G17	
OSPI0_D2	B25	OSPI0_D2	F21	
OSPI0_D3	A26	OSPI0_D3	F20	
OSPI0_D4	B26	OSPI0_D4	G21	
OSPI0_D5	B27	OSPI0_D5	H21	
OSPI0_D6	C27	OSPI0_D6	G20	
OSPI0_D7	C28	OSPI0_D7	J21	
PMIC_LPM_EN0	D5	PMIC_LPM_EN0	C7	
PORZ_OUT	D18	PORZ_OUT	E13	
RESETSTATZ	C18	RESETSTATZ	E14	
RESET_REQZ	D17	RESET_REQZ	E15	
RGMII1_RXC	U20	RGMII1_RXC	AA16	
RGMII1_RX_CTL	V20	RGMII1_RX_CTL	W14	
RGMII1_TXC	U23	RGMII1_TXC	W16	
RGMII1_TX_CTL	V23	RGMII1_TX_CTL	V15	
RGMII2_RXC	R22	RGMII2_RXC	V18	
RGMII2_RX_CTL	T23	RGMII2_RX_CTL	W19	
RGMII2_TXC	R19	RGMII2_TXC	Y18	
RGMII2_TX_CTL	T20	RGMII2_TX_CTL	Y21	
RGMII1_RD0	U22	RGMII1_RD0	W15	
RGMII1_RD1	V22	RGMII1_RD1	Y16	
RGMII1_RD2	U21	RGMII1_RD2	AA17	
RGMII1_RD3	V21	RGMII1_RD3	Y15	
RGMII1_TD0	U25	RGMII1_TD0	U14	
RGMII1_TD1	V25	RGMII1_TD1	AA19	
RGMII1_TD2	U24	RGMII1_TD2	Y17	
RGMII1_TD3	V24	RGMII1_TD3	AA18	
RGMII2_RD0	T25	RGMII2_RD0	W18	
RGMII2_RD1	R24	RGMII2_RD1	Y20	
RGMII2_RD2	T24	RGMII2_RD2	Y19	
RGMII2_RD3	R23	RGMII2_RD3	W20	
RGMII2_TD0	T22	RGMII2_TD0	AA20	
RGMII2_TD1	R21	RGMII2_TD1	U15	

OSD62x-PM		AM62x (AMC)		Comments
Pin Name	Pin No.	Pin Name	Pin No.	
RGMII2_TD2	T21	RGMII2_TD2	W17	
RGMII2_TD3	R20	RGMII2_TD3	V16	
AM62X_RSVD0	F5	RSVD0	B3	Reserved Pin
AM62X_RSVD1	F4	RSVD1	C3	Reserved Pin
AM62X_RSVD2	F6	RSVD2	E6	Reserved Pin
AM62X_RSVD3	N17	RSVD3	F8	Reserved Pin
AM62X_RSVD4	F8	RSVD4	R6	Reserved Pin
AM62X_RSVD5	F9	RSVD5	T13	Reserved Pin
AM62X_RSVD6	M18	RSVD6	T14	Reserved Pin
AM62X_RSVD7	N18	RSVD7	M4	Reserved Pin
AM62X_RSVD8	F7	RSVD8	M5	Reserved Pin
DDR_RSVD0	F10	-	-	Reserved Pin
SPI0_CLK	C11	SPI0_CLK	D12	
SPI0_CS0	D13	SPI0_CS0	C11	
SPI0_CS1	C13	SPI0_CS1	D13	
SPI0_D0	D12	SPI0_D0	C12	
SPI0_D1	C12	SPI0_D1	A14	
TCK	D9	TCK	C10	
TDI	D10	TDI	D10	
TDO	D11	TDO	E10	
TMS	C10	TMS	B11	
TRSTN	C9	TRSTN	A11	
UART0_CTSN	A9	UART0_CTSN	B14	
UART0_RTSN	B9	UART0_RTSN	C13	
UART0_RXD	A10	UART0_RXD	A13	
UART0_TXD	B10	UART0_TXD	E11	
USB0_DM	U12	USB0_DM	AA11	
USB0_DP	V12	USB0_DP	Y10	
USB0_DRVVBUS	C19	USB0_DRVVBUS	D17	
USB0_VBUS	V11	USB0_VBUS	V10	
USB1_DM	U10	USB1_DM	W8	
USB1_DP	V10	USB1_DP	W9	
USB1_DRVVBUS	D19	USB1_DRVVBUS	E16	
USB1_VBUS	U11	USB1_VBUS	U9	
VOUT0_DE	R25	VOUT0_DE	T17	
VOUT0_HSYNC	P25	VOUT0_HSYNC	W21	
VOUT0_PCLK	T26	VOUT0_PCLK	U17	
VOUT0_VSYNC	R26	VOUT0_VSYNC	T16	
VOUT0_DATA0	P26	VOUT0_DATA0	R21	
VOUT0_DATA1	N25	VOUT0_DATA1	P18	
VOUT0_DATA2	N26	VOUT0_DATA2	R18	
VOUT0_DATA3	M25	VOUT0_DATA3	R19	
VOUT0_DATA4	M26	VOUT0_DATA4	R20	
VOUT0_DATA5	U27	VOUT0_DATA5	T20	
VOUT0_DATA6	T27	VOUT0_DATA6	T21	
VOUT0_DATA7	T28	VOUT0_DATA7	T19	
VOUT0_DATA8	R27	VOUT0_DATA8	U21	
VOUT0_DATA9	R28	VOUT0_DATA9	R17	
VOUT0_DATA10	P27	VOUT0_DATA10	T18	
VOUT0_DATA11	P28	VOUT0_DATA11	U20	
VOUT0_DATA12	N27	VOUT0_DATA12	U19	
VOUT0_DATA13	N28	VOUT0_DATA13	V21	
VOUT0_DATA14	M27	VOUT0_DATA14	U18	
VOUT0_DATA15	M28	VOUT0_DATA15	V20	
WKUP_CLKOUT0	C7	WKUP_CLKOUT0	B12	
WKUP_I2C0_SCL	A8	WKUP_I2C0_SCL	E9	
WKUP_I2C0_SDA	B8	WKUP_I2C0_SDA	A9	

OSD62x-PM		AM62x (AMC)		Comments
Pin Name	Pin No.	Pin Name	Pin No.	
WKUP_LFOSC0_XI	H1	WKUP_LFOSC0_XI	A2	
WKUP_LFOSC0_XO	H2	WKUP_LFOSC0_XO	A3	
WKUP_UART0_CTSN	D1	WKUP_UART0_CTSN	A7	
WKUP_UART0_RTSN	D2	WKUP_UART0_RTSN	B4	
WKUP_UART0_RXD	C2	WKUP_UART0_RXD	B5	
WKUP_UART0_TXD	C1	WKUP_UART0_TXD	C6	
NC	E14, E15, F3, F15, F16, F17, F18, G3, G4, G5, G6, G7, G8, G9, G17, G18, H3, H4, H5, H6, H7, H8, H9, H10, H11, H23, J2, J3, J4 J5, J6, J7, J8, J9, J10, J11, J23, K3, K4, K5, K23, L3, L4, L12, L16, L23, M3, M11, M14, M15, M16, M17, M19, N15, N16, N19, P6, P7, P8, P9, P14, P15, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18, U18, V18			Reserved Pins

5.2 Reserved Balls

The OSD62x-PM ball map contains balls which are marked with “RSVD”. These balls must remain unconnected on the system PCB.

5.3 No Connect Balls

The OSD62x-PM ball map contains balls which are marked “NC”. These balls must remain unconnected on the system PCB since they may be used for other purposes in future versions of OSD62x-PM.

6 OSD62x-PM Components

The OSD62x-PM integrates the Texas Instruments AM62x System on Chip (SoC). Figure 6-1 shows a block diagram for the OSD62x-PM. Refer to the documents listed in Section 3 for specification details on the SoC. Along with the AM62x are the DDR4 Memory, and the associated resistors and capacitors, integrated into a single design-in-ready package. The following subsections contain specific device information needed for the integrated components to design your system with the OSD62x-PM.

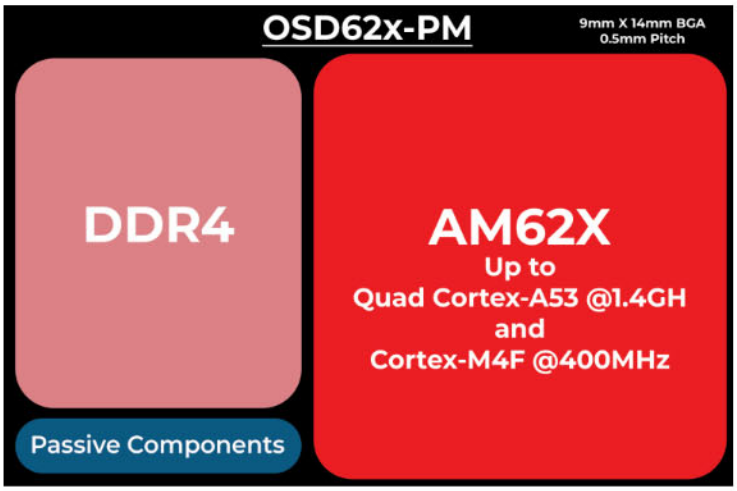


Figure 6-1 – OSD62x-PM Internal Components

6.1 AM62x Processor

The heart of the OSD62x-PM is the Texas Instruments Sitara® AM62x SoC. It features up to Quad Arm® Cortex®-A53 processors, a single-core Arm® Cortex®-M4F processor, as well as other accelerators and peripherals. Refer to Figure 4-1 and the references listed in Section 3 for more details. For detailed SoC variants, refer to the Device Comparison Table in the AM62x Datasheet. The AM62x SoC in the OSD62x-PM is configured to perform identically to an AM62x standalone device. Please refer to the Datasheet listed in the Reference Documents section for details on the AM62x processor.

6.2 DDR4 Memory

The OSD62x-PM integrates DDR4 memory in a x16 configuration and handles all the connections and passive components needed between the AM62x and the DDR4.

The integrated DDR supports the full 1600MT/s (800MHz) speed of the AM62x device across the entire temperature range.

DDR parameters required to exercise the DDR have already been calculated and are provided in the DDR Parameter Include File that can be found in the Other References section of this document.

7 Electrical & Thermal Characteristics

Absolute Maximum Ratings and Recommended Operating Conditions for the OSD62x-PM are the same as the AM62x, unless otherwise noted. Please refer to the Specifications Section (Section 7) in the AM62x Datasheet for more information. Ratings specific to OSD62x-PM and SoC ratings (for reference) are provided below.

Table 7-1 – OSD62x-PM Absolute Maximum Ratings(1) (2)

Description	Item	Value	Unit
DDR VPP Supply	DDR_VPP	-0.4V to 3.0V(3)	V
Tc (OSD62x-PM Case Temperature)	Industrial (I)	-40 to 85	C

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to network ground terminal.
3. DDR VPP must be equal to or greater than VDDS_DDR at all times when powered.

Table 7-2 - OSD62x-PM SoC Absolute Maximum Ratings[1,2]

Voltage Rail		Voltage		Unit
		Min	Max	
VDD_CORE **VDDR_CORE** **VDD_CANUART** **VDDA_CORE_CSIRX0** **VDDA_CORE_USB**		-0.3	1.05	V
VDDS_DDR		-0.3	1.5	V
VDDS_OSC0 **VDDA_MCU** **VDDA_PLL0** **VDDA_PLL1** **VDDA_PLL2** **VDDA_1P8_CSIRX0** **VDDA_1P8_OLDI0** **VDDA_1P8_USB** **VDDA_TEMP** **VPP**		-0.3	1.98	V
VDDSHV_MCU **VDDSHV_CANUART** **VDDSHV0** **VDDSHV1** **VDDSHV2** **VDDSHV3** **VDDSHV4** **VDDSHV5** **VDDSHV6** **VDDA_3P3_USB**		-0.3	3.63	V
MCU_PORz **VMON_3P3_SOC**		-0.3	3.63	V
MCU_I2C0_SCL **MCU_I2C0_SDA**	3.3V Operation	-0.3	3.63[3]	V
WKUP_I2C0_SCL **WKUP_I2C0_SDA** **EXTINTn**	1.8V Operation		1.98[3]	
VMON_1P8_SOC **VMON_VSYS**[4]		-0.3	1.98	V
USB0_VBUS[5,6] **USB1_VBUS**[5,6]		-0.3	3.6	V
All other IO pins[5]		-0.3	IO Supply + 0.3	V

1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed in the Recommended Operating Conditions tables. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
2) All voltage values are with respect to VSS, unless otherwise noted.
3) The absolute maximum ratings for these pins depends on their IO supply operating voltage. Therefore, this value is also defined by the maximum VIH value found in the I2C Open-Drain, and Fail-Safe (I2C OD FS) Electrical Characteristics section of the AM62 datasheet, where the electrical characteristics table has separate parameter values for 1.8-V mode and 3.3-V mode.
4) The VMON_VSYS pin provides a way to monitor the system power supply. For more information, see the System Power Supply Monitor Design Guidelines in the AM62 datasheet.
5) This parameter applies to all IO pins which are not part of note 3 and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be –0.3 to +0.3 volts. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.
6) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see section "USB Design Guidelines" in AM62 Datasheet

Table 7-3 - Recommended Operating Conditions (1) – Input Voltage Rails

Voltage Rail		Voltage				Current Limit	
	I/O	Min	Nom	Max	Unit	Max	Unit
DDR_VPP	N/A	2.375	2.5	2.750	V	60	mA
VDDS_DDR (1.2V only)	N/A	1.14	1.2	1.26	V	600	mA

(1) Over operating case temperature range, unless otherwise noted.

Table 7-4 - OSD62x-PM SoC Recommended Operating Conditions

Voltage Rail		Voltage			
	Mode	Min[1]	Nom	Max[1]	Unit
VDD_CORE[2] VDDA_CORE_CSIRX0[2] VDDA_CORE_USB[2] VDD_CANUART[3]	0.85V operation	0.715	0.75	0.79	V
	0.75V operation	0.81	0.85	0.895	V
VDDR_CORE		0.81	0.85	0.895	V
VDDS_OSC0 VDDA_MCU VDDA_PLL0 VDDA_PLL1 VDDA_PLL2 VDDA_1P8_CSIRX0 VDDA_1P8_OLDI0 VDDA_1P8_USB VDDA_TEMP		1.71	1.8	1.89	V
VPP[4,8]	During OTP programming[9]	1.71	1.8	1.89	V
	Normal operation		0		V
VMON_1P8_SOC		1.71	1.8	1.89	V
VDDA_3P3_USB VMON_3P3_SOC		3.135	3.3	3.465	V
VMON_VSYS		0	see[5]	1	V
USB0_VBUS USB1_VBUS		0	see[6]	3.465	V
VDDSHV_CANUART[7] VDDSHV_MCU VDDSHV0 VDDSHV1	1.8V operation	1.71	1.8	1.89	V
VDDSHV2 VDDSHV3 VDDSHV4 VDDSHV5 VDDSHV6	3.3V operation	3.135	3.3	3.465	V

1) The voltage at the device ball must never drop below the MIN voltage or rise above the MAX voltage for any amount of time during normal device operation.
2) A_CORE_CSIRX0, and VDDA_CORE_USB shall be sourced from the same power source. Care should be taken to ensure that voltage differential between VDD_CORE and VDDA_CORE_USB is within +/- 1%.
3) VDD_CANUART shall be connected to an always on power source when using Partial IO low power mode. VDD_CANUART shall be connected to the same power source as VDD_CORE, VDDA_CORE_CSIRX0, and VDDA_CORE_USB when not using Partial IO low power mode.
4) Refer to the Recommended Operating Conditions for OTP eFuse Programming table in the AM62 datasheet for more information on VPP supply voltages based on eFuse usage.
5) The VMON_VSYS pin provides a way to monitor the system power supply. For more information, see the System Power Supply Monitor Design Guidelines in the AM62 datasheet.
6) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see the USB Design Guidelines in the AM62 datasheet.
7) VDDSHV_CANUART shall be connected to an always on power sources when using Partial IO low power mode. VDDSHV_CANUART shall be connected to any valid IO power source when not using Partial IO low power mode.
8) If there is no hardware support for OTP eFuse ROM programming, this signal can be left unconnected.
9) Make sure the slew rate for this voltage input for OTP eFuse ROM programming is < 6E + 4 V/s.

7.1 Power Sequencing

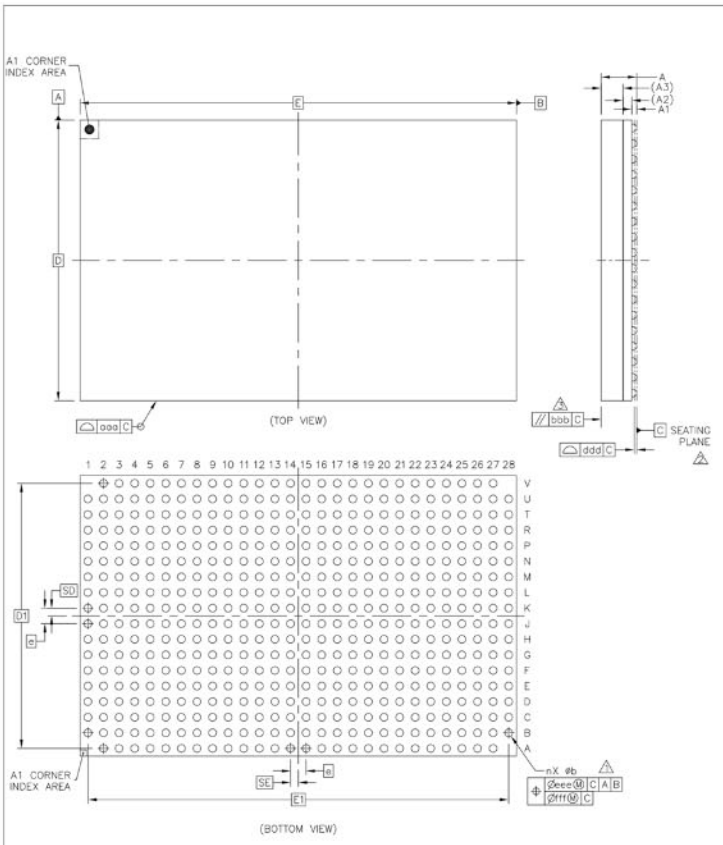
OSD62x-PM power rails have sequencing requirements. Please refer to AM62x datasheet and OSD62x-PM Power application note for additional information on power sequencing.

8 Packaging Information

The OSD62x-PM is packaged in a 9 mm X 14 mm BGA Package. It has 14 x 28 Ball Grid Array in the center of the package consisting of 500 pins with 0.5 mm pitch. This section provides the specifics on this package.

8.1 Mechanical Dimensions

The mechanical drawings for the OSD62x-PM are provided below. All measurements are in millimeters. Refer to the OSD62x-PM Layout Guide for more details. A footprint and schematic symbol are available from Octavo Systems.



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.3
STAND OFF	A1	0.11	---	0.21
SUBSTRATE THICKNESS	A2		0.28	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		9	BSC
	E		14	BSC
BALL DIAMETER			0.25	
BALL OPENING			0.25	
BALL WIDTH	b	0.2	---	0.3
BALL PITCH	e		0.5	BSC
BALL COUNT	n		500	
EDGE BALL CENTER TO CENTER	D1		8.5	BSC
	E1		13.5	BSC
BODY CENTER TO CONTACT BALL	SD		0.25	BSC
	SE		0.25	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

8.1.1 Landing Pad Sizing

For the nominal ball diameter of 0.30mm, specification IPC-7351A states that for NSMD pads, the nominal land diameter is 0.25mm with a land variation of 0.25mm to 0.20mm. Footprints provided by Octavo Systems generally use the minimum land pad size to enable lower cost routing (see Layout Guide in the Reference Documents section for more information). However, some applications may require a larger land pad size to enable a more robust structural connection to the circuit board or other manufacturing constraints. Check the requirements of the application and manufacturer to determine the appropriate land pad size.

8.2 Thermal Considerations

The power dissipation and thermal characteristics of the OSD62x-PM SiP are highly dependent on the type of application. Please see the Thermal Guide in the Reference Documents section for further information.

8.3 Reflow Instructions

The reflow profile for this package should be in accordance with the Lead-free process for BGA. A peak reflow temperature is recommended to be 245°C.

Texas Instruments provides a good overview of Handling & Process Recommendations in AN-2029 for this type of device. A link to the document can be found in the Reference Documents section of this document.

8.4 Storage Requirements

The OSD62x-PM Family of devices are sensitive to moisture and need to be handled in specific ways to make sure they function properly during and after the manufacturing process. The OSD62x-PM Family of devices are rated with a **Moisture Sensitivity Level (MSL) of 4**. This means that they are stored in a sealed Dry Pack with desiccant bag and a Humidity Indicator Card (HIC). **If the HIC reads > 10% when read at 23 ± 5 C or the HIC is not present; the devices must be baked in per the directions in 8.4.3 before use.**

8.4.1 Floor Life

Once the sealed Dry Pack is opened the device can be stored **for up to 72 hours in a room ≤ 30°C and ≤60% Relative Humidity (RH). If any of these conditions are not met the devices must be baked as outlined in section 8.4.3 before use.**

8.4.2 Shelf Life

Octavo System devices are shipped in Moisture Barrier Bags (MBB) that have been partially vacuumed sealed with a desiccant bag. This combination supports a shelf life of the devices in

an unopened factory bag for **24 Months from the seal date.** If this is exceeded, then the devices must be **baked per the directions in section** 8.4.3 **before use**.

8.4.3 Baking

The devices need to be baked if they have been exposed to environments outside of those outlined in sections 8.4.1 and 8.4.2, or if there is concern about the moisture content of the devices. The devices must be baked for **34hrs at 125°C with a RH of <5%.**