

1 Introduction

The [OSD32MP15x](#), the STM32MP1 System in Package, was designed to minimize the number of Printed Circuit Board (PCB) layers and make the layout process easy. This OSD32MP15x Layout Guide document will cover important aspects of PCB layout design specific to the OSD32MP15x and help designers quickly begin the PCB layout process. First, this document will discuss the layout of the OSD32MP15x BGA. Then this OSD32MP15x Layout Guide will discuss a few common layout scenarios using relevant examples with recommendations on pours for Power, Ground and other supporting circuitry.

This OSD32MP15x Layout Guide document assumes that the reader is already familiar with layout design process and the OSD32MP15x ([OSD32MP15x Data Sheet](#)). The document should not be used as a comprehensive layout tutorial or a generic layout design guide.

Notice: The information provided within this document is for informational use only. Octavo Systems provides no guarantees or warranty to the information contained.



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2 OSD32MP15x Layout Specifications

The [OSD32MP15x Family of System-In-Package \(SiP\) products](#) are building blocks designed to allow easy and cost-effective implementation of systems based on STMicroelectronic STM32MP1 dual core Cortex-A7 line of processors. The OSD32MP15x, a STM32MP1 system in package, integrates the STM32MP157C processor along with the STPMU1 PMIC, up to 1 Gigabyte (GB) of DDR3 Memory, a 4 Kilobyte (KB) EEPROM for non-volatile configuration storage and resistors, capacitors, and inductors into a single 18mm x 18mm design-in-ready package.

This section will introduce important specifications, ball mapping and footprint information of [the OSD32MP15x, a STM32MP1 system in package](#).

2.1 Background Information

To understand layout guidelines and methodology used for the recommendations made in this document in more detail, please refer to the following documents:

- [PCB Design Guidelines for Reduced EMI](#)
- [OSD32MP15x datasheet link](#)

2.2 Ball function map

The Ball function map shown in Figure 1 provides a visual representation of the arrangement of the pins of the OSD32MP15x. This can help with the placement and orientation of the OSD32MP15x in a design.

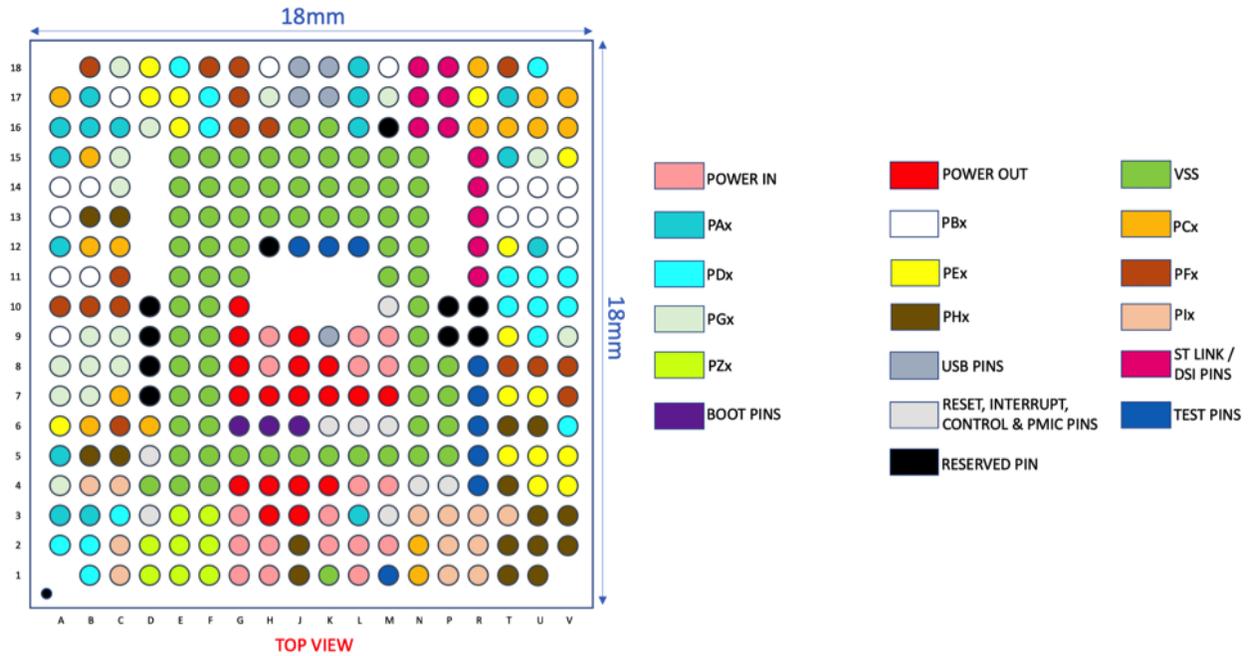


Figure 1 OSD32MP15x BGA Color Map

2.3 Footprint Configuration

The OSD32MP15x footprint parameters are shown in Figure 2 and listed in Table 1.

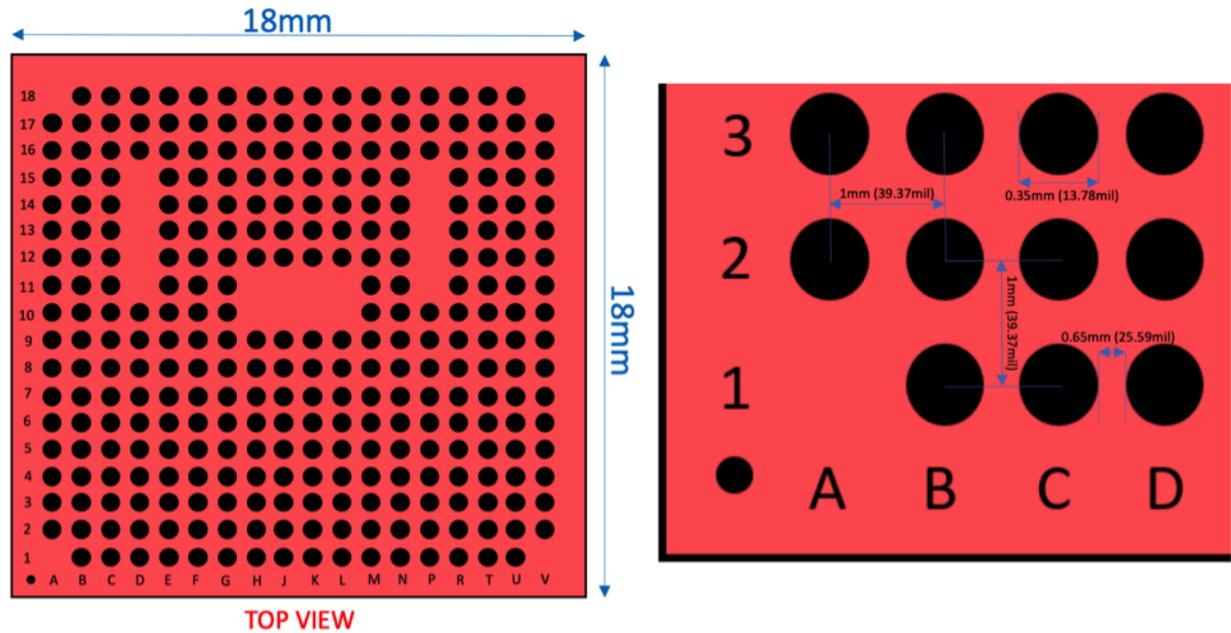


Figure 2 OSD32MP15x Footprint Dimensions

<u>Parameter</u>	<u>Value</u>
Package Dimension	18mm x 18mm x 1.85mm
Number of Balls	302
Ball Grid	18 rows x 18 columns
Ball Pitch	1mm (39.37mils)
Landing Pad Size	0.35mm (13.78 mils)

Table 1 - Important OSD32MP15x Layout Information

The landing pad size was determined from the IPC-7351A specification. To find more information about IPC-7351A specifications, refer **BGA Ball Pad Size** section of [BGA PCB Design document](#) from Texas Instruments (TI).

For more information on the footprint configuration, please see the **Mechanical Dimensions** section of the [OSD32MP15x datasheet](#).

3 Routing and Vias

When pricing a PCB, the size of the traces and vias directly affect the cost to manufacture the board. However, larger traces and vias, while cheaper, can make layout more difficult. Therefore, it is necessary to understand the optimum size of traces and vias for a given design. This section will provide background information on trace and via sizes and discuss layout tradeoffs when designing with the OSD32MP15x BGA.

3.1 Trace size background information

The number of traces that can pass between any two pads of a BGA footprint depends on the trace width and trace spacing. Trace width is the actual width of the trace. Trace spacing is the distance between the edges of any two adjacent traces or a trace and a pad. Trace width and trace spacing are shown pictorially in Figure 3.

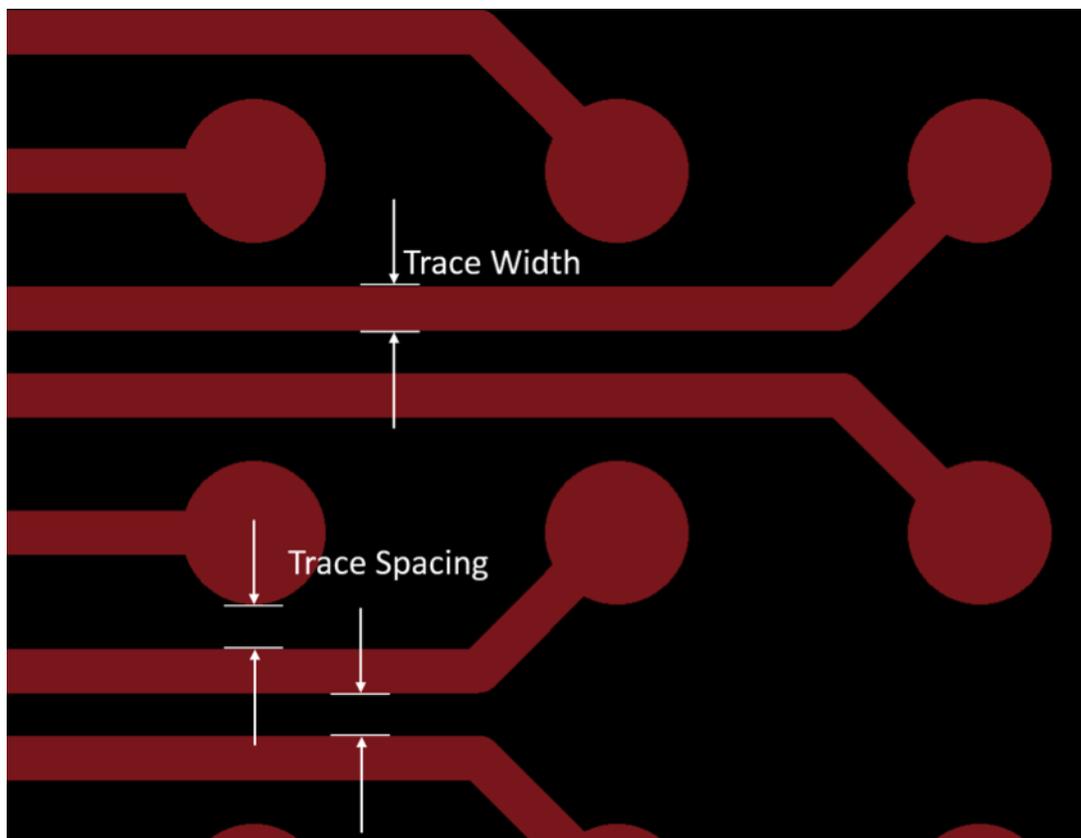


Figure 3 Trace width and Trace spacing

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In this document, a “x/y trace” indicates a PCB that uses design rules with trace width of x mils and trace spacing of y mils. For example, a 5/6 trace indicates a PCB with trace width of 5mils and trace spacing of 6mils.

The number of traces that can be routed between any two adjacent pads of the BGA can be calculated using the formula (formula assumes all the traces are equal width):

$$t_n t_w + (t_n + 1) t_s \leq B_P - B_D$$

where,

- t_n = number of traces
- t_w = trace width
- t_s = trace spacing
- B_P = BGA pitch
- B_D = BGA landing pad diameter

For example, to calculate the number of 5/5 traces that can be routed between adjacent pads of the OSD32MP15x BGA: $t_w = 5\text{mils}$, $t_s = 5\text{mils}$, $B_P = 39.37\text{mil}$ (1mm) and $B_D = 13.78\text{mil}$ (0.35mm)

Using all this in the above equation:

$$\begin{aligned} 5t_n + 5(t_n + 1) &\leq 25.59 \\ 10t_n &\leq 20.59 \\ t_n &\leq \mathbf{2.059 \text{ traces.}} \end{aligned}$$

This result indicates that two (2) full 5/5 traces can be routed between adjacent balls of the OSD32MP15x BGA. Similarly, the number of traces can be calculated for other routing rules, see Table 2. In the OSD32MP15x BGA, almost all signal pins are in the first three rows / columns of the BGA. This means to fully escape the BGA, only 2 traces are needed to be routed between each pair of pads. See Section 4.1 for more details on OSD32MP15x fanout.

Trace width(mils) / Trace spacing(mils)	Number of traces between two adjacent BGA pads
Larger than 5/5	1
5/5	2
3.65/3.65 or smaller	3 or more

Table 2 – Number of traces between OSD32MP15x BGA pads for common trace/space rules

3.1.1 Example: 5/5 traces routed between pads of the OSD32MP15x

On all sides, the first three rows of OSD32MP15x can be easily accessed using 5/5 traces as shown in Figure 4.

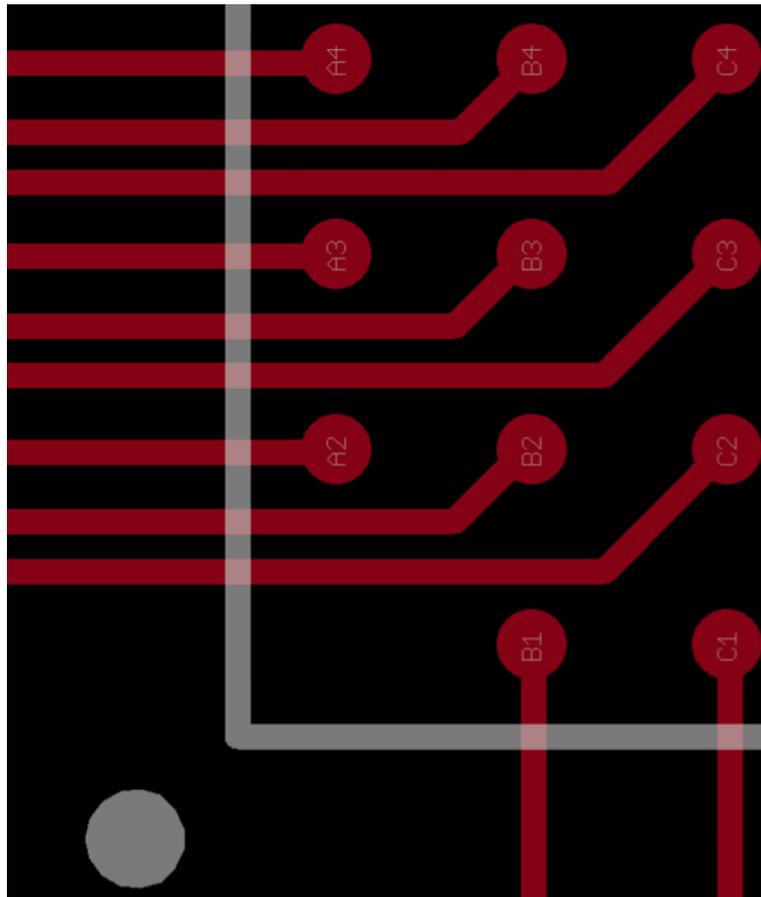


Figure 4 5/5 Traces routed between pads of OSD32MP15x

3.2 Via size background information

There are two important parameters for vias: drill diameter and annular ring thickness. Drill diameter is the diameter of the actual drilled hole in the PCB. The annular ring thickness is the thickness of the pad that surrounds the drilled hole. These dimensions are shown pictorially in Figure 5.

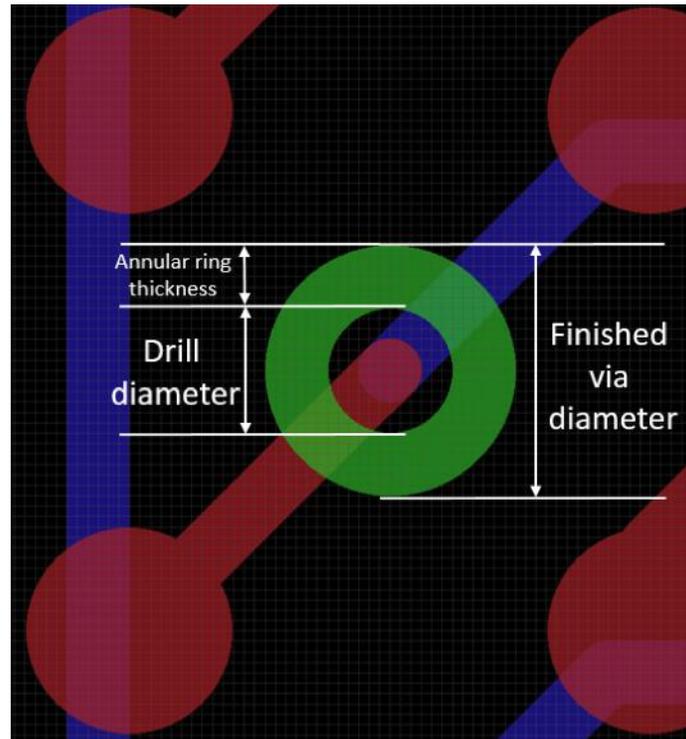


Figure 5 Drill, annular ring and via dimensions

To determine the diameter of the finished via, use the following formula:

$$\text{Finished via diameter} = \text{Drill diameter} + 2 \times (\text{Annular ring thickness})$$

Via spacing is the distance between the edges of any two adjacent vias as shown in Figure 6. When placing vias, make sure the spacing between the vias match the trace spacing design rules that were chosen.

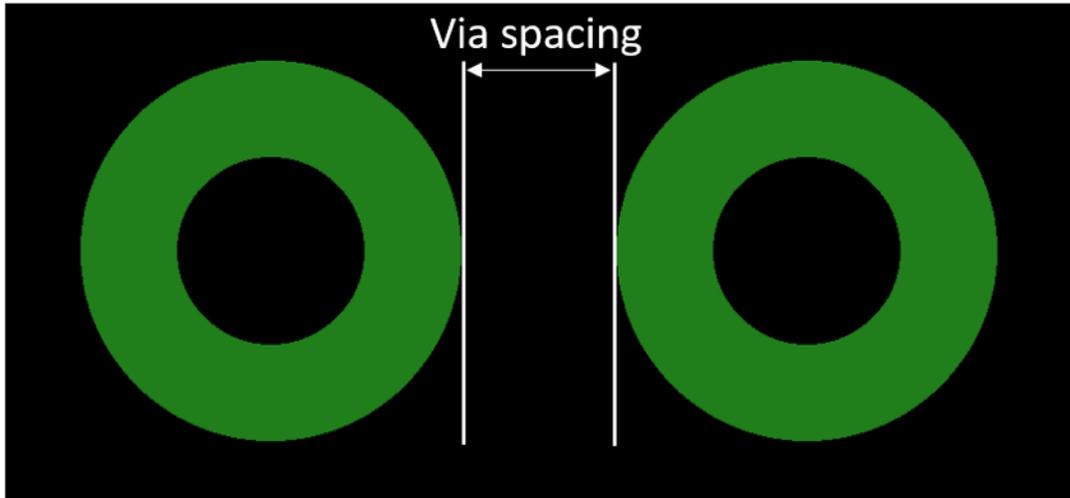


Figure 6 Via Spacing

In this document, a “x/y via” indicates a via with drill diameter of x mils and finished via diameter of y mils. For example, a 12/24 via indicates a via with drill diameter of 12mils and finished via diameter of 24mils.

3.2.1 Example: A 12/24 via between 4 pads of the OSD32MP15x

One 12/24 via can be easily placed between four adjacent balls of the BGA as shown in Figure 7. A 12/24 via falls under Standard Manufacturing capabilities of most PCB manufacturers. It is relatively cheaper than much smaller vias.

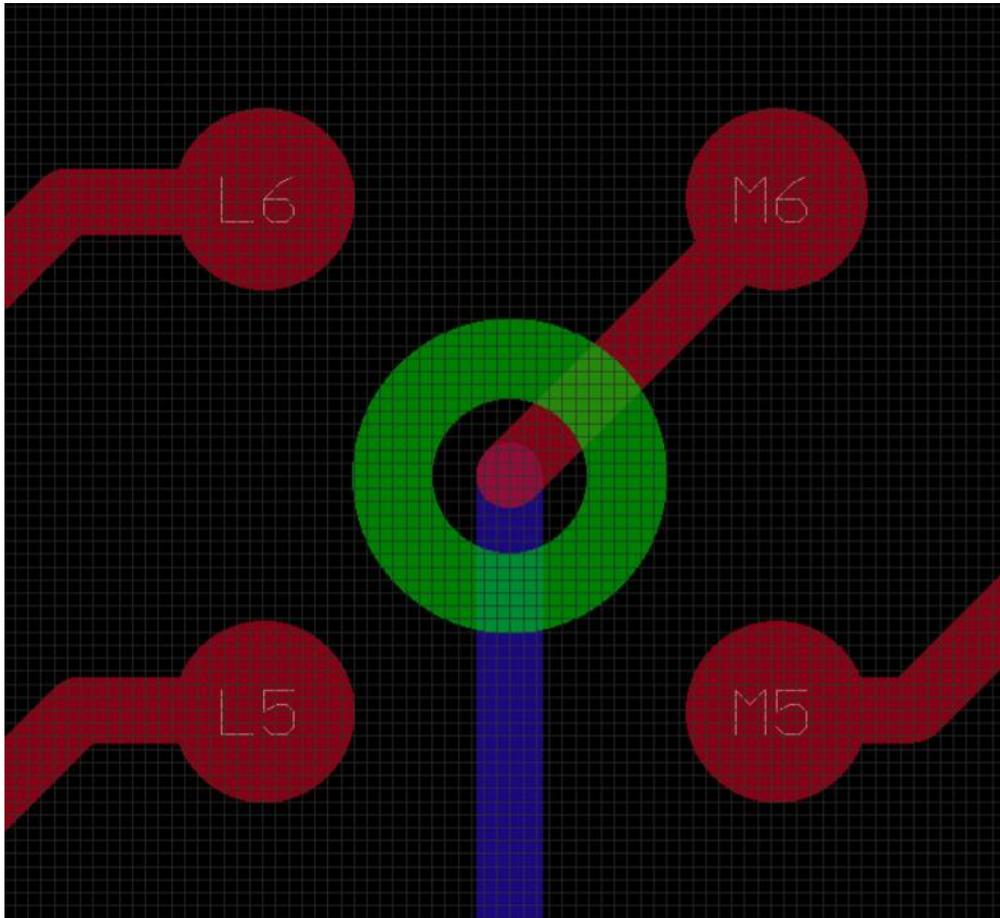


Figure 7 One 12/24mil via between four adjacent pads of OSD32MP15x

3.2.2 Example: A 10/18 via and 5/5 trace between 4 pads of the OSD32MP15x

Figure 8 shows one 10/18 via and one 5/5 trace between four adjacent pads of OSD32MP15x.

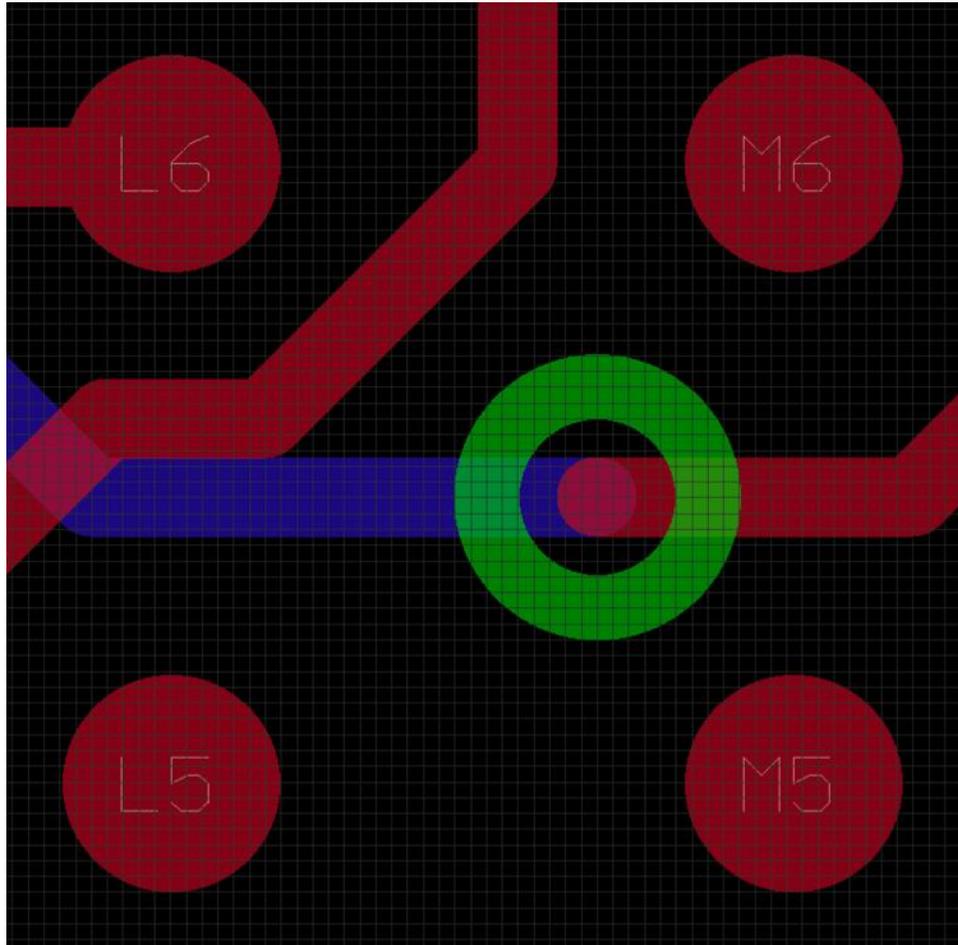


Figure 8 One 10/18 via and one 5/5 trace between four adjacent pads of OSD32MP15x

3.2.3 Example: Two 10/16 vias between 4 pads of the OSD32MP15x

In case of a tighter design, two 10/16 vias can be placed between four adjacent balls of the BGA as shown in Figure 9. A 10/16 via falls under Extended Manufacturing capabilities of most PCB manufacturers. This via size may be slightly more expensive than 12/24 via. However, based on your manufacturer's capabilities and your design requirements, you could choose to use a much smaller via than 10/16.

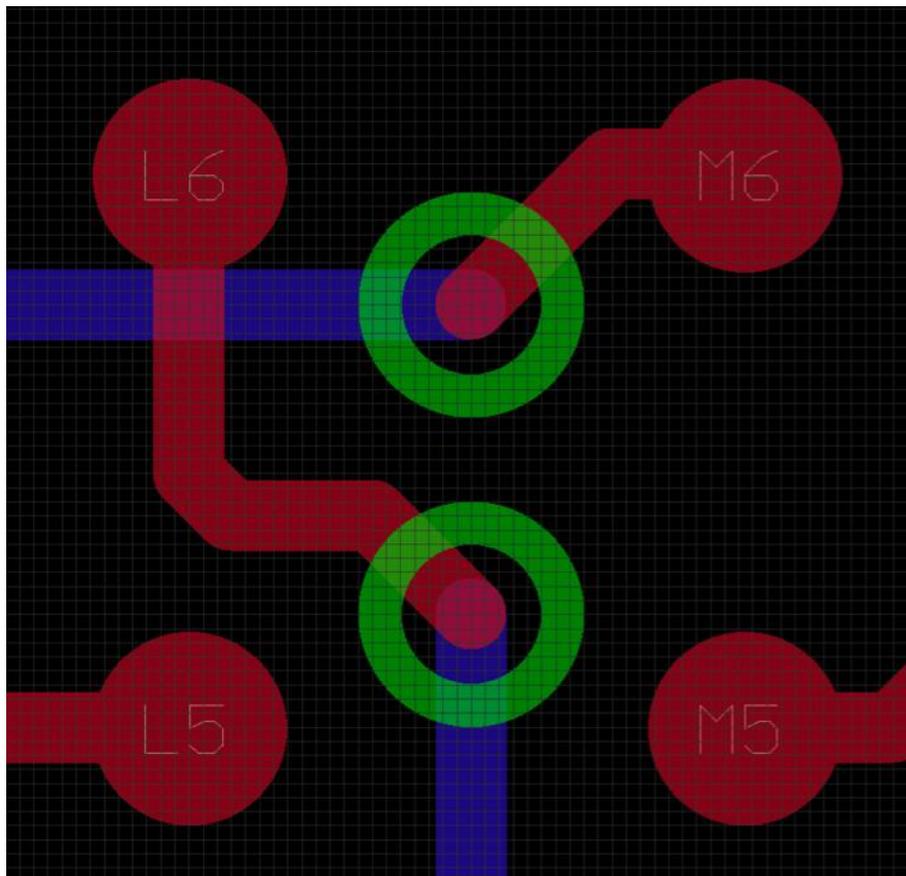


Figure 9 Two 10/16 vias between four adjacent pads of OSD32MP15x

4 OSD32MP15x Layout Examples

Once the design rules for traces and vias have been chosen for the PCB, the BGA can now be routed. The following sections provide examples of how to lay out the OSD32MP15x.

4.1 Signal Pin Fanout

Figure 10 shows the fanout of all pads of the OSD32MP15x using 5/5 traces.

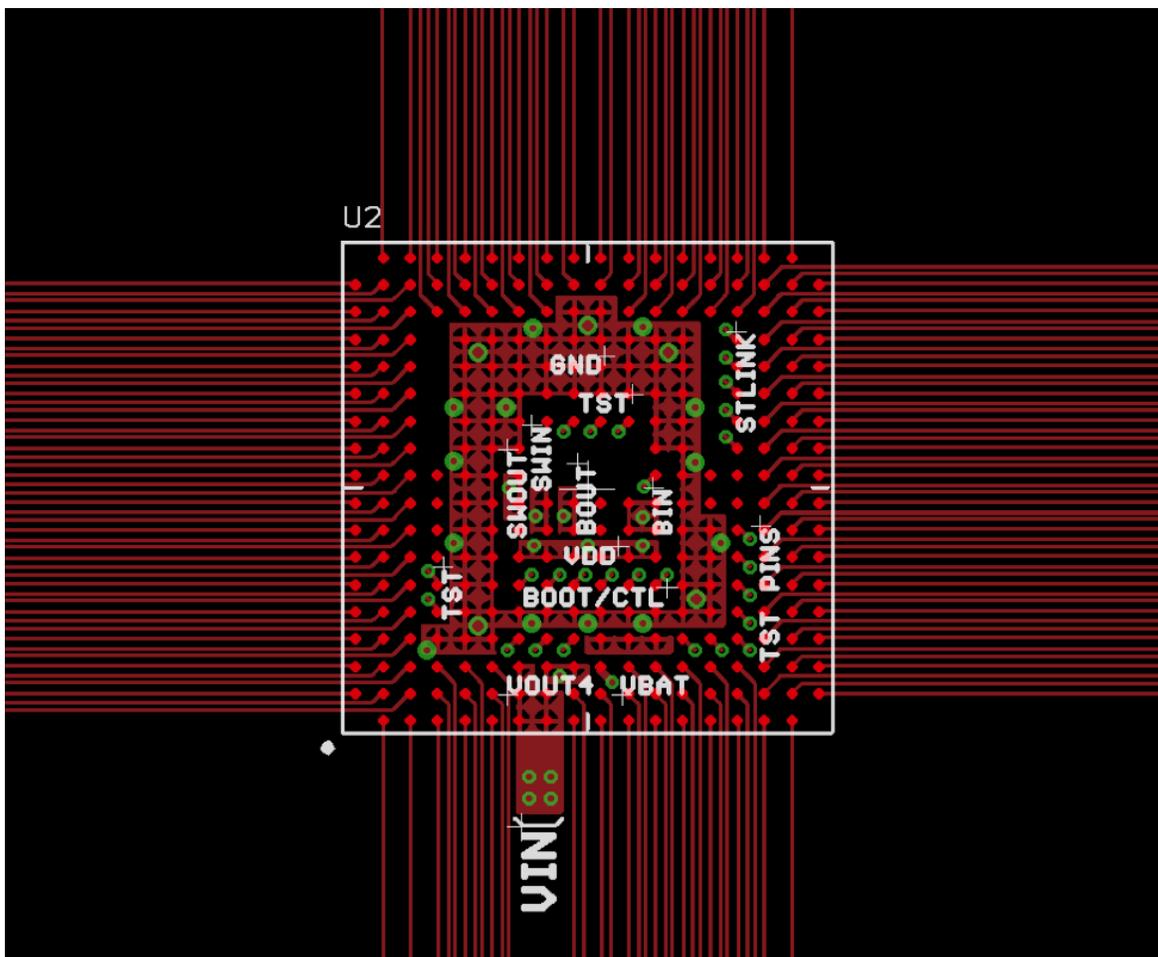


Figure 10 OSD32MP15x fanout of all signals

4.2 Power Inputs

Power to the two input power rails (5V_VIN and VBAT) of OSD32MP15x can be supplied through a copper pour and vias as shown in Figure 11 (Note: PMIC_LDO25IN is sourced by VIN in the below pictures representing typical use case).

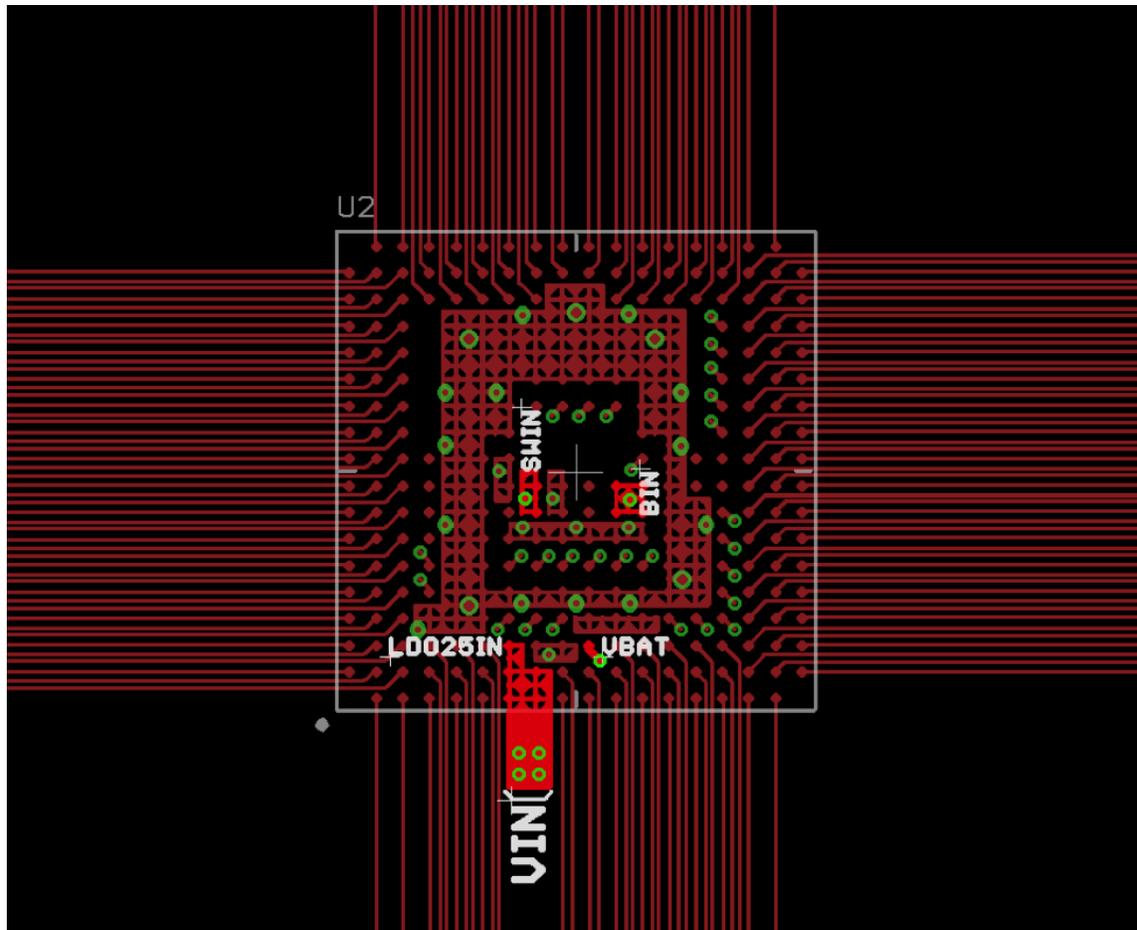


Figure 11 Power input copper pours and vias

4.3 Power Outputs

Power from the output power rails of the OSD32MP15x can be connected to the rest of the PCB using copper pours as shown in Figure 12.

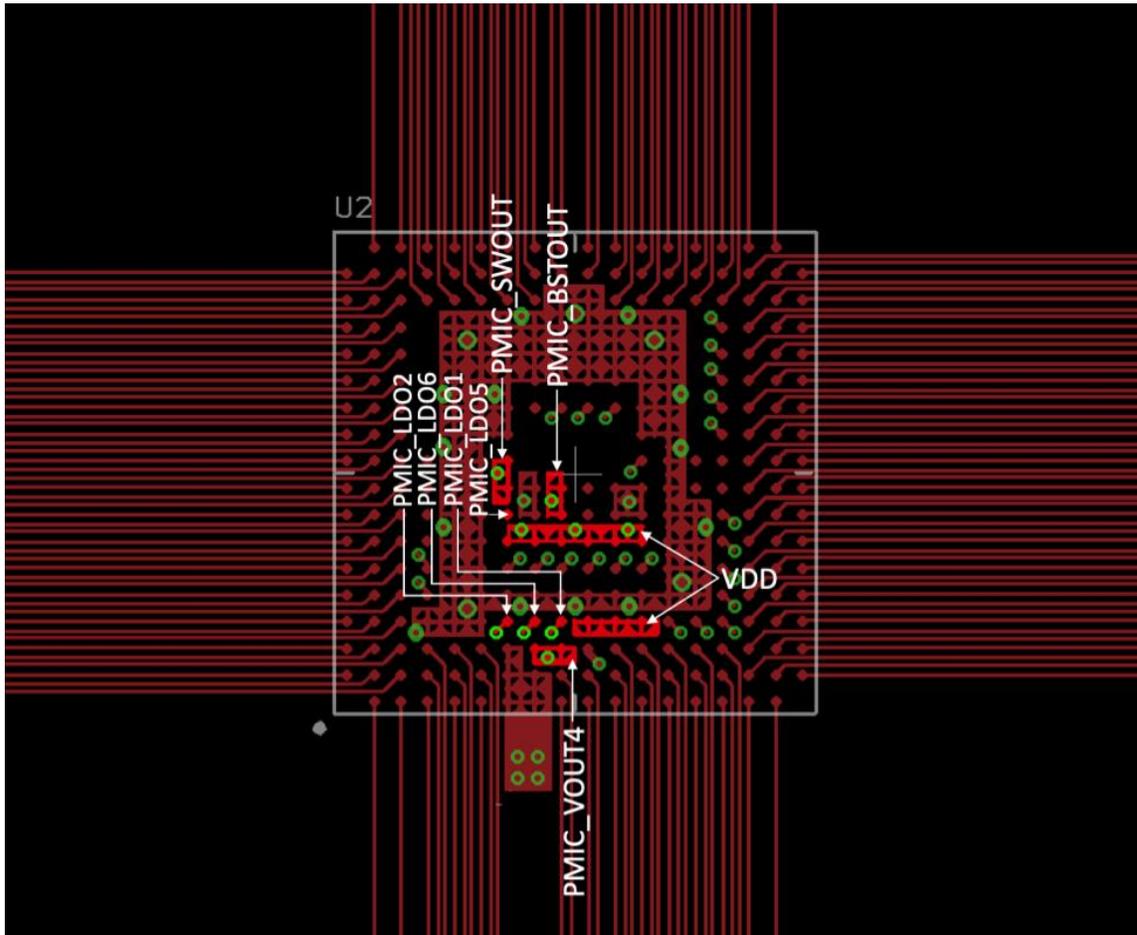


Figure 12 Output power copper pours

4.4 Ground connections

The ground pins of the OSD32MP15x can be connected to ground plane using copper pours as shown in Figure 13.

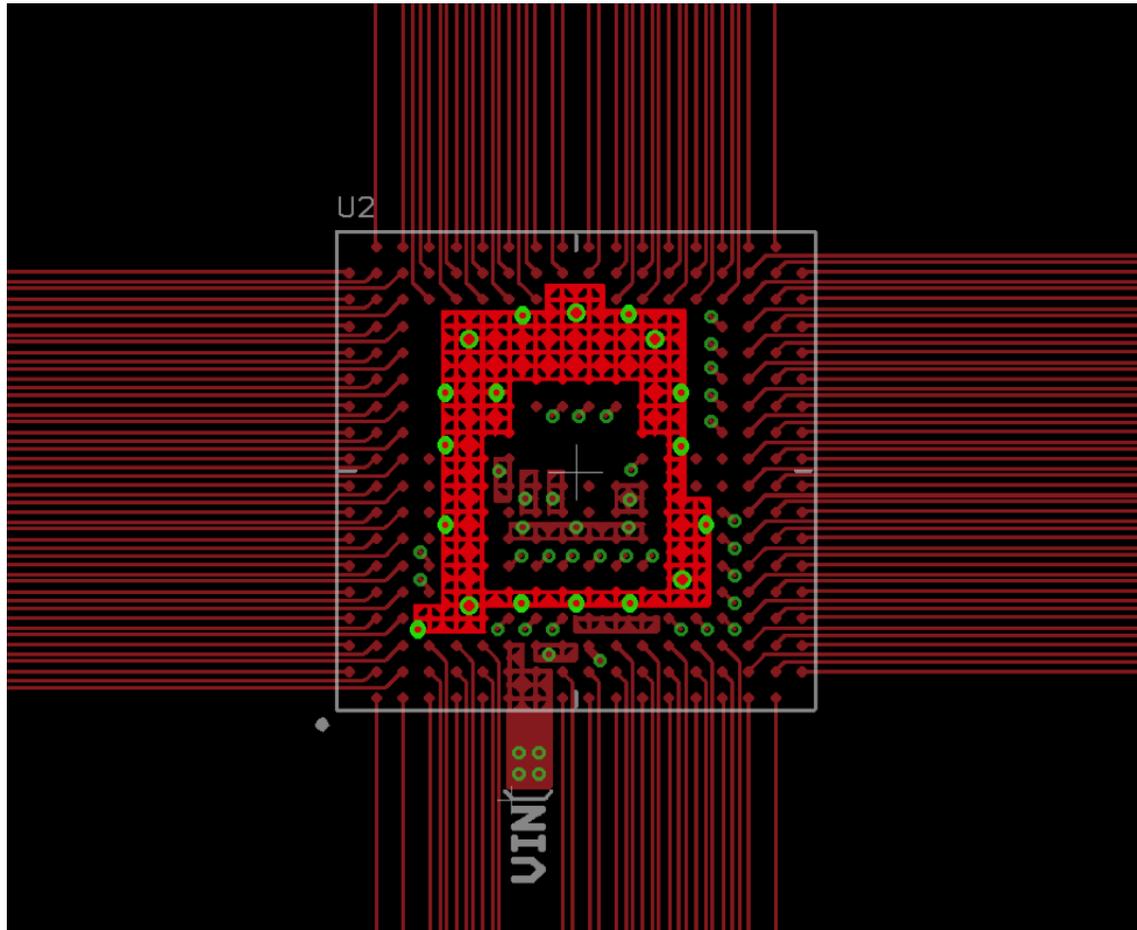


Figure 13 Ground pour Type 1

For space constrained design, the ground copper pours can also be configured as shown in Figure 14.

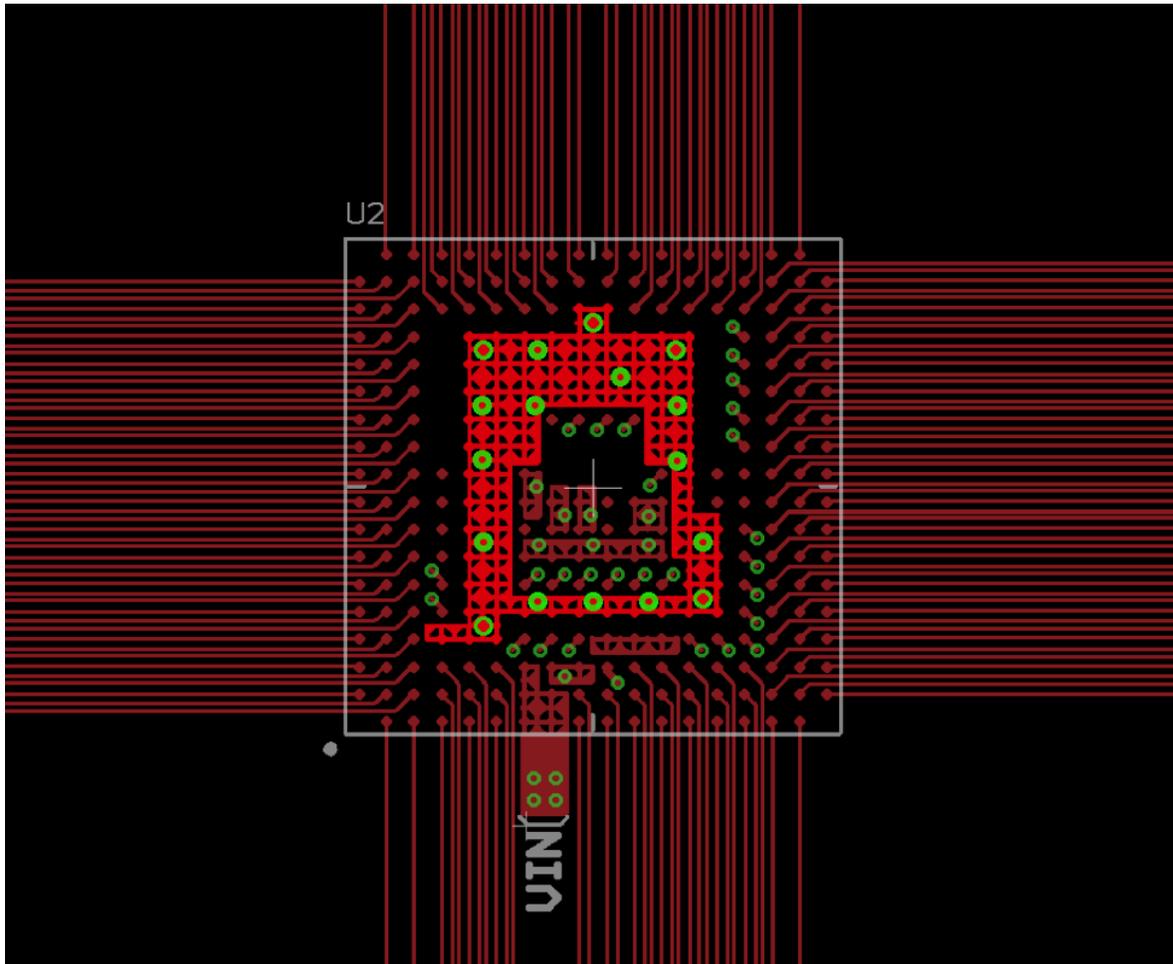


Figure 14 Ground pour Type 2

4.5 EEPROM

The write protect pin of the EEPROM (EEPROM_WP) of the OSD32MP15x needs to be driven low before information can be written into it. This can be done in many ways: The EEPROM_WP pin can be driven by another device on the PCB; It can be driven by one of the OSD32MP15x pins; It can be routed to a pad to be driven by an external device; It can be routed to a jumper; etc.

Figure 15 shows an example of the EEPROM_WP pin routed to a jumper using 100mil header. The other side of the jumper is connected to GND which allows the EEPROM_WP signal to be easily driven low. This can be a useful layout in prototype designs that are not space constrained.

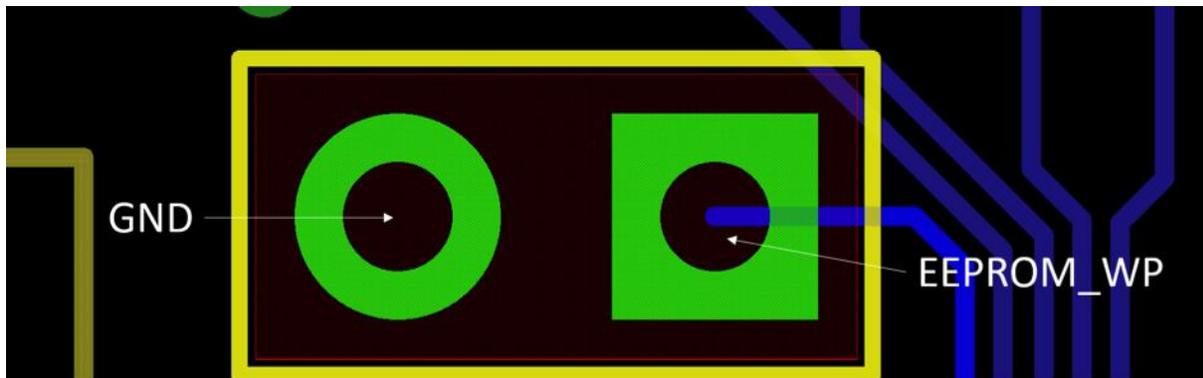


Figure 15 EEPROM_WP jumper

5 References

- [OSD32MP15x Data Sheet](#)
- [AM335x Layout Guidelines](#)

6 Revision History

Revision Number	Revision Date	Changes	Author
1.0	2/18/2019	Initial Revision	Eshtaartha Basu
2.0	3/18/2019	Updated all figures, intro remarks, fixed datasheet link	Eshtaartha Basu
