Introduction

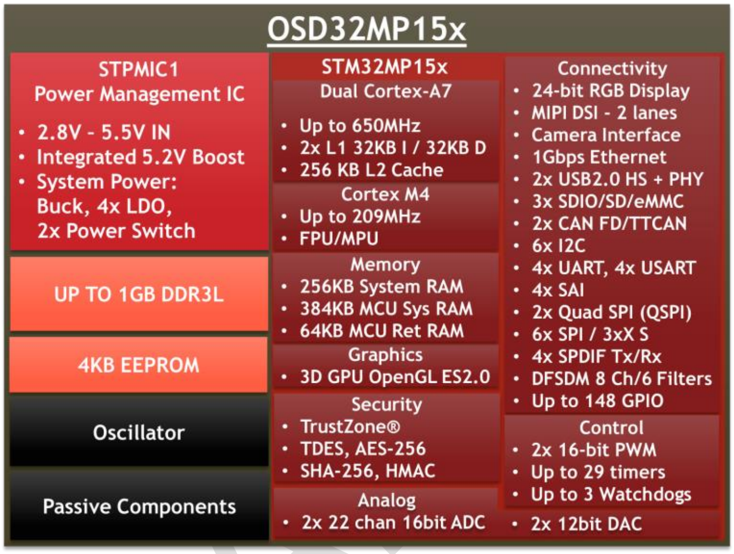
The OSD32MP15x System-in-Package (SiP) devices deliver all the power of a Microprocessor in a package that feels like a Microcontroller in the smallest possible footprint.

At their core, the OSD32MP15x devices have the versatile STMicroelectronics STM32MP15x featuring Dual Arm® Cortex® A7 Cores and an Arm® Cortex® M4. Along with the processor, the OSD32MP15x Family integrates up to 1GB of DDR3, STPMIC1 Power Management IC, EEPROM, MEMs Oscillators, and passive components into a single easy to use BGA package.

This integration enables the fastest designs with the STM32MP15x by removing the tedious tasks that don't add value to an end system.

Features

- ST STM32MP15x, DDR3, STPMIC1, 4KB EEPROM, Oscillators and passive components integrated into a single package
- STM32MP15x Features:
  - Arm® Cortex®-A7 up to 650MHz x2
  - Arm® Cortex®-M4 up to 209MHz
  - NEON™SIMD Coprocessor x2
  - TrustZone®
  - USB 2.0 HS + PHY x2
  - Ethernet 10/100/1000
  - CAN FD/TTCAN x2, UART x4, USART x4, SPI x6, I2C x6, I2S x3, QSPI x2
  - eMMC/SD/SDIO Ports x3
  - GPIO x148
  - 24-bit RGB Display, MIPI DSI
  - Camera Interface
  - 22 Channel 16-bit ADC x2, 12-bit DAC x2



OSD32MP15x Block Diagram

- Access to all Signals of the STM32MP1 TFBGA 361 Package
- Up to 1GB DDR3
- Low Power MEMS Oscillator x2
- Single Voltage Input: 2.8V-5.5V
- Integrated Boost: 5.2V
- System Power: Buck, LDOx4, Power Switch x2

Benefits

- Integrates over 100 components
- Compatible with STM32MP1 development tools and software
- Significantly reduces design time
- Up to 64% reduction in board space vs discrete implementation
- Decreases layout complexity
- Wide BGA ball pitch allows for low-cost assembly
- Simplifies component sourcing
- Increased reliability through reduced number of components

Package

- 18mm X 18mm BGA
- 302 Ball, 1mm Pitch
- Temp Range: 0 to 85°C, -40 to 85°C

Table of Contents

1 Revision History

Revision Number	Revision Date	Changes	Author
0.01	2/18/2019	Preliminary Release	Greg Sheridan, Erik Welsh, Eshtaartha Basu
0.02	3/14/2019	Updated Pin Mapping and Mechanical Drawing to reflect final design	Greg Sheridan
0.03	3/18/2019	Fixed Small Type on Pin F1 of Ball Map	Greg Sheridan
0.04	5/10/2019	Updated Mechanical Diagram to the final package/Updated Block Diagrams to better represent peripherals	Greg Sheridan
0.05	7/24/2019	Updated pin map for LSE oscillator	Erik Welsh

WARNING!

This Datasheet is in a preliminary form. The information in it is subject to change significantly before the production version is released. Any design done using this datasheet must be confirmed with the information in the production release of the datasheet. Octavo Systems will not be responsible for any issues caused by using the information in this datasheet.

2 Block Diagram

The OSD32MP15x devices consist of 6 main components serving 5 distinct functions. The main processor is the STM32MP15x from STMicroelectonics featuring dual core Arm® Cortex®-A7 running up to 650MHz and an Arm® Cortex® M4 at 209MHz. The power system consists of the STPMIC1A Power Management IC (PMIC). The system memory includes up to 1GB DDR3. A 4KB EEPROM provides nonvolatile memory for configuration. Finally, there are two low power, low jitter, highly stable MEMS CMOS Oscillators. One is used for the primary clock input and the other is used for the Real Time Clock (RTC) input. Figure 2.1 shows a detailed block diagram of the OSD32MP15x and breaks out the key functions of the STM32MP15x processor.

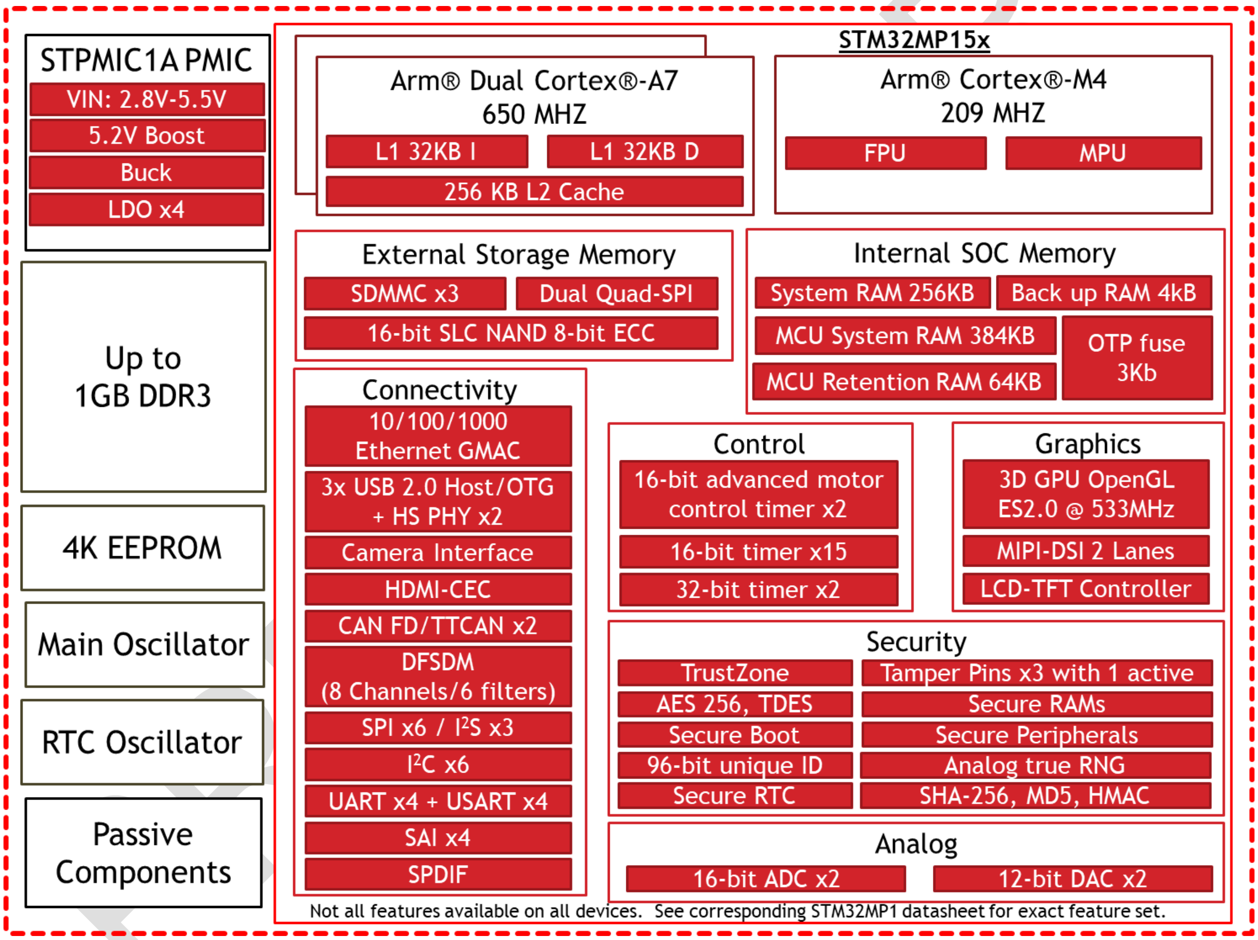


Figure 2.1 - OSD32MP15x Detailed Block Diagram

2.1 Passives

Besides the six major components, the OSD32MP15x also integrates capacitors, resistors, inductors, and ferrite beads (Passives). Table 2-1 and Table 2-2 lists the equivalent capacitance and resistance integrated into the OSD32MP15x. This includes the approximate bulk capacitance on input and output power rails as well as all pull-up resistor locations and values. The OSD32MP15x does not require any external decoupling / bypass capacitors in most applications.

Table 2-1 - OSD32MP15x Capacitors (Approximate Bulk Capacitance)

From	To	Device	Description	Type	Value
VIN	DGND	STPMIC1	VIN input capacitance	C	25uF
PMIC_BSTIN	DGND	STPMIC1	PMIC_BSTIN input capacitance	C	4.7uF
PMIC_LDO25IN	DGND	STPMIC1	VIN_BAT input capacitance	C	1uF
PMIC_VOUT4	DGND	STPMIC1	PMIC_VOUT4 output capacitance	C	22uF
PMIC_BSTOUT	DGND	STPMIC1	PMIC_BSTOUT output capacitance	C	10uF
PMIC_SWOUT	DGND	STPMIC1	PMIC_SWOUT output capacitance	C	4.7uF
PMIC_LDO1	DGND	STPMIC1	PMIC_LDO1 output capacitance	C	4.7uF
PMIC_LDO2	DGND	STPMIC1	PMIC_LDO2 output capacitance	C	4.7uF
PMIC_LDO5	DGND	STPMIC1	PMIC_LDO5 output capacitance	C	4.7uF
PMIC_LDO6	DGND	STPMIC1	PMIC_LDO6 output capacitance	C	4.7uF

Table 2-2 - OSD32MP15x Resistors (Pull-ups / Pull-downs)

From	To	Device	Description	Type	Value
PDR_ON	VDD	STM32MP15x	PDR_ON input pull-up	R	10K Ohm
PDR_ON_CORE	VDD	STM32MP15x	PDR_ON_CORE input pull-up	R	10K Ohm
PZ4/PMIC_SCL	VDD	STM32MP15x	I2C4 SCL pull-up	R	1.5K Ohm
PZ5/PMIC_SDA	VDD	STM32MP15x	I2C4 SDA pull-up	R	1.5K Ohm
EEPROM_WP	VDD	EEPROM	EEPROM WP pull-up	R	10K Ohm
HSE_OSC_OE	VDD	Oscillator	Enable pull-up	R	10K Ohm

3 Product Number Information

Figure 3.1 shows an example of an orderable product number for the OSD32MP15x family. This section explains the different sections of the product number. It will also list the valid entries and their meaning for each designator.

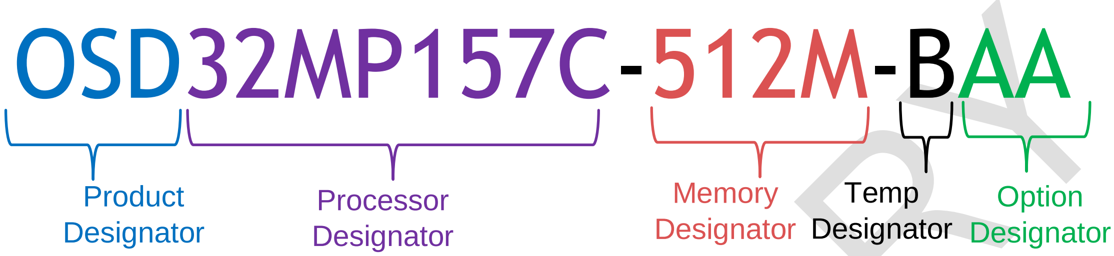


Figure 3.1. Example Product Number

Product Designator – Three letters that designate the family of device.

Table 3-1 - Family Designator

Family Designator	Product Line
OSD	OSD Product Line.

Processor Designator – A set of letters and numbers that designate the specific processor in the device. Table 3-2 shows the valid values for the Processor Designator.

Table 3-2 - Processor Designators

Processor Designator	Processor
32MP157C	ST Microelectronics STM32MP157C

Memory Designator – A set of letters and numbers that designate the DDR3 memory size in the device. Table 3-3 shows the valid values for the Memory Designator.

Table 3-3 - Memory Designator

Memory Designator	DDR Memory Size
1G	1GB DDR3
512M	512 MB DDR3

Temp Designator – A letter or number that designates the operating case temperature range of the device. Table 3-4 shows the valid values for the Temp Designator.

Table 3-4 - Temp Designator

Temp Designator	Temperature Range
B	Commercial: 0 to 85°C
I	Industrial: -40 to 85°C

Option Designator – A set of two letters or numbers that designates the set of features in the device. Table 3-5 shows the valid values for the Option Designator unique for the OSD32MP15x devices.

Table 3-5 - Option Designator

Option Designator	Device Options
AA	24MHz Main Oscillator, 32KHz RTC Oscillator, 4KB EEPROM

4 Reference Documents

4.1 Data Sheets

Below are links to the data sheets for the key devices used in the OSD32MP15x. Please refer to them for specifics on that device. The remainder of this document will describe how the devices are used in the OSD32MP15x system. It will also highlight any differences between the performance stated in the device specific datasheet and what should be expected from its operation in the OSD32MP15x.

- Processor

Processor Version	**Datasheet**
STM32MP157C	https://www.st.com/resource/en/datasheet/stm32mp157c.pdf

- PMIC STPMIC1 https://www.st.com/resource/en/data_brief/stpmic1.pdf
- EEPROM 24LC32A http://www.microchip.com/wwwproducts/en/24LC32A

4.2 Other References

This section contains links to other reference documents that could be helpful when using the OSD32MP15x device. Some are referenced in this document.

- TI AN-2029 – Handling & Process recommendations
  http://www.ti.com/lit/snoa550
- OSD32MP15x Layout Guide
  https://octavosystems.com/app_notes/osd32mp15x-layout-guide/
- OSD32MP15x CubeMX Configuration Guide
  TBD
- OSD32MP15x DDR Programming Guide
  TBD
- DDR configuration on STM32MP1 Series MPU
  https://www.st.com/resource/en/application_note/dm00505673.pdf

5 Ball Map

The pins on the OSD32MP15x belong to 4 distinct categories, STM32MP15x signals, STPMIC1A signals, control signals for internal components and Power Domains. The signal names for the STM32MP15x and the STPMIC1 have been named so they can be easily cross-referenced to the corresponding pin in the ST Datasheet.

All STM32MP1 signals on the OSD32MP15x Ball Map match the signal names of the default function after reset of the STM32MP15x datasheet.

All the STPMIC1 signals have the prefix PMIC_ then the STPMIC1 signal name from the ST Datasheet.

Some of the control signals for the processor and PMIC and connected internally but can still be accessed outside of the OSD32MP15. These signals have both the processor pin name and the PMIC pin name. For example: PZ5/PMIC_SDA.

The arrangement of the signals has been optimized for easy escape of the BGA. Table 5-1 through Table 5-5 show the ball map for the OSD32MP15x.

Table 5-1 - OSD32MP15x Ball Map Top View (Columns A-D)

	A	B	C	D
18		PF11	PG10	PE8
17	PC0	PA6	PB5	PE7
16	PA5	PA4	PA1	PG8
15	PA2	PC1	PG5	
14	PB13	PB12	PG11	
13	PB10	PH2	PH3	
12	PA7	PC4	PC5	
11	PB0	PB1	PF12	
10	PF13	PF14	PF15	RSVD
9	PB11	PG4	PG3	RSVD
8	PG2	PG1	PG0	RSVD
7	PG14	PG13	PC2	RSVD
6	PE2	PC3	PF3	PC13/PMIC_WAKEUP
5	PA3	PH6	PH7	PWR_ON/PMIC_PWRCTRL
4	PG12	PI10	PI11	VSS
3	PA13	PA14	PD14	PMIC_PONKEYN
2	PD15	PD8	PI9	PZ7
1		PD9	PI8	PZ6

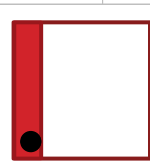


Table 5-2 - OSD32MP15x Ball Map Top View (Columns E-H)

	E	F	G	H
18	PD11	PF6	PF9	PB6
17	PE10	PD13	PF8	PG7
16	PE9	PD12	PF7	PF10
15	VSS	VSS	VSS	VSS
14	VSS	VSS	VSS	VSS
13	VSS	VSS	VSS	VSS
12	VSS	VSS	VSS	RSVD
11	VSS	VSS	VSS	
10	VSS	VSS	PMIC_SWOUT	
9	VSS	VSS	PMIC_SWOUT	PMIC_SWIN
8	VSS	VSS	PMIC_LDO5	PMIC_SWIN
7	VSS	VSS	VDD	VDD
6	VSS	VSS	BOOT2	BOOT1
5	VSS	VSS	VSS	VSS
4	VSS	VSS	PMIC_LDO2	PMIC_LDO6
3	PZ5/PMIC_SDA	PZ2	PMIC_LDO25IN	PMIC_VOUT4
2	PZ4/PMIC_SCL	PZ1	VIN	VIN
1	PZ3	PZ0	VIN	VIN

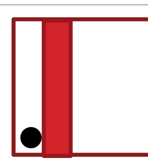


Table 5-3 - OSD32MP15x Ball Map Top View (Columns J-M)

	J	**K**	**L**	**M**
18	USB_DP2	USB_DM1	PA12	PB2
17	USB_DM2	USB_DP1	PA11	PG9
16	VSS	VSS	PA10	RSVD
15	VSS	VSS	VSS	VSS
14	VSS	VSS	VSS	VSS
13	VSS	VSS	VSS	VSS
12	VTT_DDR	VDD_DDR	VREF_DDR	VSS
11				VSS
10				BYPASS_REG1V8
9	PMIC_BSTOUT	OTG_VBUS	PMIC_BSTIN	PMIC_BSTIN
8	PMIC_BSTOUT	PMIC_VBUSOTG	PMIC_BSTIN	PMIC_BSTIN
7	VDD	VDD	VDD	VDD
6	BOOT0	PWR_LP	PDR_ON_CORE	PDR_ON
5	VSS	VSS	VSS	VSS
4	PMIC_LDO1	VDD	VDD	VDD
3	PMIC_VOUT4	VBAT	PA0/PMIC_INTN	NRST
2	HSE_OSC_TP	VREF-	ANA1	VREF+
1	HSE_OSC_OE	VSSA	ANA0	VDDA

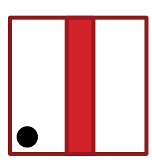


Table 5-4 - OSD32MP15x Ball Map Top View (Columns N-T)

	N	P	R	T
18	DSI_D1N	DSI_D0N	PC6	PF2
17	DSI_D1P	DSI_D0P	PE4	PA8
16	DSI_CKP	DSI_CKN	PC7	PC8
15	VSS		JTCK-SWCLK	PA15
14	VSS		JTMS-SWDIO	PB14
13	VSS		JTDI	PB8
12	VSS		JTDO-TRACESWO	PE3
11	VSS		NJTRST	PD3
10	VSS	RSVD	RSVD	PD6
9	VSS	RSVD	RSVD	PE6
8	VSS	VSS	VDDA1V1_REG	PF5
7	VSS	VSS	VDDA1V8_REG	PE1
6	VSS	VSS	VDD1V2_DSI_REG	PH5
5	VSS	VSS	VDD3V3_USB	PE13
4	NRST_CORE	EEPROM_WP	VDD_CORE	PH8
3	PI7	PI6	PI3	PI0
2	LSE_OSC_TP	PI5	PI2	PH15
1	RSVD	PI4	PI1	PH14

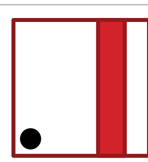
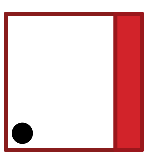


Table 5-5 - OSD32MP15x Ball Map Top View (Columns U-Y)

	U	V
18	PD2	
17	PC11	PC12
16	PC9	PC10
15	PG6	PE5
14	PB4	PB3
13	PB9	PB15
12	PA9	PB7
11	PD1	PD0
10	PD5	PD4
9	PD7	PG15
8	PF0	PF1
7	PE0	PF4
6	PH4	PD10
5	PE12	PE11
4	PE15	PE14
3	PH10	PH9
2	PH12	PH11
1	PH13	



5.1 Ball Description

Table 5-6 lists all the unique signals of the OSD32MP15x and provides the pin number of the OSD32MP15x as well as a mapping to the equivalent pin on the STM32MP1 TFBGA361 package. All the processor signals have the same function as the equivalent pin in the STM32MP1 except where noted.

The OSD32MP15x also provides access to the VREF- signal of the STM32MP15x which is not accessible in the TFBGA361 package.

The functions of each of the pins can be configured through the CubeMX software. For more detail on the pin functions please refer to the datasheet of the integrated device in section 4.1.

Table 5-6 - OSD32MP15x Ball Descriptions

Pin Name	Pin Number		Notes
	OSD32MP15x	STM32MP15x TFBGA361 Package	
ANA0	L1	U3	
ANA1	L2	U4	
BOOT0	J6	N1	Must be connected to VDD or VSS. Can use adjacent VDD or VSS ball.
BOOT1	H6	N4	Must be connected to VDD or VSS. Can use adjacent VDD or VSS ball.
BOOT2	G6	M2	Must be connected to VDD or VSS. Can use adjacent VDD or VSS ball.
BYPASS_REG1V8	M10	AB13	
DSI_CKN	P16	A16	
DSI_CKP	N16	B16	
DSI_D0N	P18	B15	
DSI_D0P	P17	C15	
DSI_D1N	N18	A17	
DSI_D1P	N17	B17	
EEPROM_WP	P4	N/A	Write Protect Pin for EEPROM. It is internally Pulled Up. Referrer to the Passives Section for more information
HSE_OSC_OE	J1	N/A	Enable Pin for the integrated HSE. It is internally Pulled Up. Refer to the Passives Section for more information
HSE_OSC_TP	J2	P1	Output of HSE That is connected to input for HSE PH0-OSC_IN
JTCK-SWCLK	R15	B20	
JTDI	R13	A20	
JTDO-TRACESWO	R12	A19	
JTMS-SWDIO	R14	C20	
NJTRST	R11	B19	
NRST	M3	M3	
NRST_CORE	N4	M4	
OTG_VBUS	K9	AC19	
PA0/PMIC_INTN	L3	AB3	This pin is connected internally to PMIC INTN
PA1	C16	AA4	
PA10	L16	Y17	
PA11	L17	AA18	
PA12	L18	AB19	
PA13	A3	N2	
PA14	B3	T2	
PA15	T15	C19	
PA2	A15	AC3	
PA3	A5	U2	

PA4	B16	V4	
PA5	A16	V3	
PA6	B17	AC8	
PA7	A12	AB8	
PA8	T17	A13	
PA9	U12	A8	
PB0	A11	AB6	
PB1	B11	AA7	
PB10	A13	Y3	
PB11	A9	AB1	
PB12	B14	AC5	
PB13	A14	AA10	
PB14	T14	C13	
PB15	V13	B12	
PB2	M18	Y16	
PB3	V14	A11	
PB4	U14	B13	
PB5	C17	Y8	
PB6	H18	Y14	
PB7	V12	D11	
PB8	T13	AB10	
PB9	U13	B10	
PC0	A17	AB5	
PC1	B15	AA6	
PC10	V16	D15	
PC11	U17	D16	
PC12	V17	D13	
PC13/PMIC_WAKEUP	D6	K2	This pin is connected internally to PMIC WAKEUP
LSE_OSC_TP	N2	L2	If the LSE is integrated, it is the Output of the LSE. If the LSE is not integrated it is the LSE Input to the processor
RSVD	N1	L1	Always the OSC32 output of the processor
PC2	C7	Y2	
PC3	B6	W2	
PC4	B12	AC7	
PC5	C12	AB7	
PC6	R18	B14	
PC7	R16	B11	
PC8	T16	D18	
PC9	U16	D17	
PD0	V11	B8	
PD1	U11	B9	
PD10	V6	B5	
PD11	E18	AC10	
PD12	F16	Y18	
PD13	F17	AA19	
PD14	C3	L3	
PD15	A2	J2	
PD2	U18	D12	
PD3	T11	D14	
PD4	V10	B6	
PD5	U10	A7	
PD6	T10	D2	
PD7	U9	D10	
PD8	B2	K3	
PD9	B1	K1	
PDR_ON	M6	R3	
PDR_ON_CORE	L6	T3	
PE0	U7	D6	
PE1	T7	C8	
PE10	E17	Y15	
PE11	V5	A4	
PE12	U5	B4	

PE13	T5	A3	
PE14	V4	C6	
PE15	U4	D3	
PE2	A6	Y1	
PE3	T12	C9	
PE4	R17	D19	
PE5	V15	C11	
PE6	T9	C10	
PE7	D17	AA11	
PE8	D18	AC13	
PE9	E16	AA9	
PF0	U8	D8	
PF1	V8	A5	
PF10	H16	Y12	
PF11	B18	Y10	
PF12	C11	Y9	
PF13	A10	Y5	
PF14	B10	AC4	
PF15	C10	Y4	
PF2	T18	A14	
PF3	C6	U1	
PF4	V7	D9	
PF5	T8	D7	
PF6	F18	AA13	
PF7	G16	AB12	
PF8	G17	AC11	
PF9	G18	AA14	
PG0	C8	AC2	
PG1	B8	W1	
PG10	C18	AB11	
PG11	C14	Y7	
PG12	A4	K4	
PG13	B7	AA2	
PG14	A7	AA1	
PG15	V9	B7	
PG2	A8	V2	
PG3	C9	T4	
PG4	B9	AB2	
PG5	C15	Y6	
PG6	U15	A10	
PG7	H17	AC14	
PG8	D16	AB9	
PG9	M17	Y13	
PH10	U3	C2	
PH11	V2	C4	
PH12	U2	B2	
PH13	U1	D1	
PH14	T1	C3	
PH15	T2	B1	
PH2	B13	AB4	
PH3	C13	AA3	
PH4	U6	B3	
PH5	T6	A2	
PH6	B5	Y11	
PH7	C5	W4	
PH8	T4	D5	
PH9	V3	C5	
PI0	T3	C1	
PI1	R1	E3	
PI10	B4	T1	
PI11	C4	P4	
PI2	R2	E2	
PI3	R3	E1	

PI4	P1	E4	
PI5	P2	F3	
PI6	P3	F4	
PI7	N3	F2	
PI8	C1	L4	
PI9	C2	H4	
PMIC_BSTIN	L8, L9, M8, M9	N/A	Input to PMIC Boost
PMIC_BSTOUT	J8, J9	N/A	Output of PMIC Boost
PMIC_LDO1	J4	N/A	Output of PMIC LDO1
PMIC_LDO2	G4	N/A	Output of PMIC LDO2
PMIC_LDO25IN	G3	N/A	Input to PMIC LDO2 and LDO5
PMIC_LDO5	G8	N/A	Output of PMIC LDO5
PMIC_LDO6	H4	N/A	Output of PMIC LDO6
PMIC_PONKEYN	D3	N/A	PMIC PONKEYn
PMIC_SWIN	H8, H9	N/A	Input of PMIC PWR_SW
PMIC_SWOUT	G10, G9	N/A	Output of PMIC PWR_SW
PMIC_VBUSOTG	K8	N/A	Output of PMIC PWR_USB_SW
PMIC_VOUT4	H3, J3	N/A	Output of PMIC Buck4
PWR_LP	K6	N3	
PWR_ON/PMIC_PWRCTRL	D5	R2	This pin is connected internally to the PMIC PWRCTRL Pin
PZ0	F1	G3	
PZ1	F2	G1	
PZ2	F3	J4	
PZ3	E1	G4	
PZ4/PMIC_SCL	E2	G2	This Pin must be configured as an I2C Bus. It is connected internally to PMIC SCL
PZ5/PMIC_SDA	E3	H2	This Pin must be configured as an I2C Bus. It is connected internally to PMIC SDA
PZ6	D1	H1	
PZ7	D2	J3	
RSVD	D10, D7, D8, D9, H12, M16, P10, P9, R10, R9	N/A	Reserved for Future Use
USB_DM1	K18	AB17	
USB_DM2	J17	AB16	
USB_DP1	K17	AC17	
USB_DP2	J18	AC16	
VBAT	K3	1F1	
VDD_CORE	R4	N/A	Test Point for VDD_CORE Voltage
VDD_DDR	K12	N/A	Test Point for VDD_DDR Voltage
VDD	G7, H7, J7, K4, K7, L4, L7, M4, M7	1F3, 1G4, 1J2, 1H3, 1H5, 1J4, 1J6	VDD Pins should be connected together. See Layout Guide for recommendation
VDD1V2_DSI_REG	R6	C18	Test Point for VDD1V2_DSI_REG
VDD3V3_USB	R5	N/A	Test Point for VDD3V3_USB
VDDA	M1	1H1	
VDDA1V1_REG	R8	AB15	Test Point for VDDA1V1_REG
VDDA1V8_REG	R7	AB14	Test Point for VDDA1V8_REG
VIN	G1, G2, H1, H2	N/A	Input Power Rail
VREF_DDR	L12	N/A	Test Point for VREF_DDR Voltage
VREF-	K2	N/A	VREF- For the STM32MP1
VREF+	M2	R4	
VSS	D4, E10, E11, E12, E13, E14, E15, E4, E5, E6, E7, E8, E9, F10, F11, F12, F13, F14,	A1, A23, C7, C12, C21, D4, F21, H3, K21, P3, P21, V21, W3, AA5, AA8, AA12, AA21, AC1, AC23, 1A3, 1A5, 1A7, 1B2, 1B4, 1B6,	

	F15, F4, F5, F6, F7, F8, F9, G11, G12, G13, G14, G15, G5, H13, H14, H15, H5, J13, J14, J15, J16, J5, K13, K14, K15, K16, K5, L13, L14, L15, L5, M11, M12, M13, M14, M15, M5, N10, N11, N12, N13, N14, N15, N5, N6, N7, N8, N9, P5, P6, P7, P8	1B8, 1C1, 1C3, 1C5, 1C7, 1C9, 1D2, 1D4, 1D6, 1D8, 1E1, 1E3, 1E5, 1E7, 1E9, 1F2, 1F4, 1F6, 1F8, 1G3, 1G5, 1G7, 1G9, 1H4, 1H6, 1H8, 1J3, 1J5, 1J7	
VSSA	K1	1H2	
VTT_DDR	J12	N/A	Test Point for VTT_DDR

5.2 Reserved Balls

The OSD32MP15x ball map contains balls which are marked Reserved. These balls must remain unconnected on the system PCB since they may be used for other purposes in future versions of the OSD32MP15x.

5.3 Test Point Signals

There is a subset of signals that are available on the OSD32MP15x ball map but ***should not be*** used externally to the device. These signals are used internally to the OSD32MP15x and using them could significantly affect the performance of the device. They are provided for test purposes only. The list of signals that should not be used can be found in Table 5-7.

Table 5-7 – Test Point Signals

Test Point Only Signals
VDD
VDD_CORE
VDD_DDR
VDD1V2_DSI_REG
VDD3V3_USB
VDDA1V1_REG
VDDA1V8_REG
VREF_DDR
VTT_DDR

6 OSD32MP15x Components

The OSD32MP15x integrates the ST Microelectronics STM32MP15x Dual Arm® Cortex®-A7 and Arm® Cortex®-M4 processor along with the ST STPMIC1 PMIC, up to 1 GB of DDR3 Memory, a 4KB EEPROM for non-volatile storage, two MEMS Oscillators for the primary clock input and the RTC input, and the resistors, capacitors, and inductors into a single design-in-ready package. The following section contains any specific device information needed for the integrated components to design your system with the OSD32MP15x. Specifics on the Power Management System will be covered in Section 7.

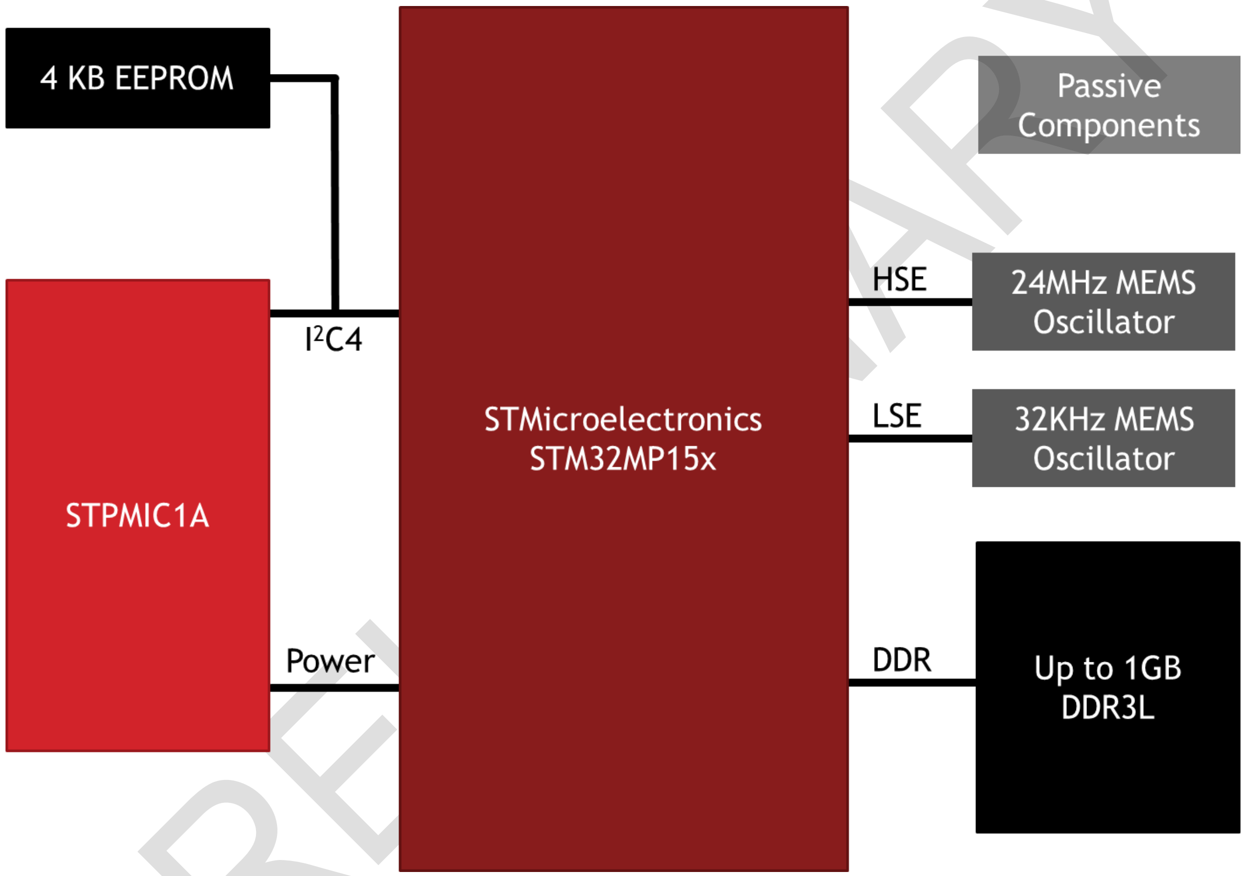


Figure 6.1 - OSD32MP15x Internal Connections Block Diagram

6.1 STM32MP15x Processor

The heart of the OSD32MP15x is the ST Microelectronics Dual Arm® Cortex®-A7 + Arm® Cortex® M4 STM32MP15x processor. The processor in the OSD32MP15x is configured to perform identically to a standalone device. Please refer to the data sheet in the Reference Documents section for details on using the STM32MP15x processor.

6.1.1 I/O Voltages

All the I/O Voltages of the OSD32MP15x are fixed to 3.3V just like the STM32MP15x. Please refer to the STM32MP15x datasheet in the Reference Documents section for more information.

6.2 DDR3 Memory

The OSD32MP15x integrates a DDR3 memory into the device and handles all the connections needed between the STM32MP15x and the DDR3. You will still have to set the proper registers to configure the STM32MP15x DDRCTRL and DDRPHYC to work correctly with the memory included in the OSD32MP15x. Typically, this would require you to run through the procedure outlined in the ***DDR configuration on STM32MP1 Series MPUs*** in the Reference Documents section of this document.

This procedure has been run for the OSD32MP15x of each of the memory variations available and a list of the recommended values for the registers is provided in OSD32MP15x DDR programming guide located in the Reference Documents section of this document. This guide will provide the correct set of values based on the DDR configuration in the OSD32MP15x.

6.3 MEMS Oscillators

The OSD32MP15x integrates a main 24MHz oscillator and a 32KHz Oscillator. One is used as the High-speed External (HSE) clock source and the other as the Low-speed External (LSE) clock source.

The configuration of the oscillators is described in Table 3-5.

This section outlines the key parameters for each of the oscillators that could be integrated.

6.3.1 HSE MEMS Oscillator

The OSD32MP15x integrates a 24MHz oscillator used as the HSE clock source. The key parameters for the oscillator are outlined in Table 6-1.

Table 6-1 – HSE MEMS Oscillator Parameters

Parameter	Min	Typ	Max	Units	Notes
Active Supply Current		790		µA	
Standby Supply Current		0.7	1.3	µA	
Initial Stability			±15	ppm	@25C
Frequency Stability			±100	ppm	All temp ranges
Aging			±3	ppm	First year @ 25C
Period Jitter, RMS			25	ps_{RMS}	
Cycle-to-Cycle Jitter			2.5	ns	
Frequency		24		MHz	

The pin HSE_OSC_TP is the output of the MEMS Oscillator. This is the same signal that is being fed into the processor.

To disable the HSE Oscillator the HSE_OSC_OE pin must be pulled low. This pin has a weak internal pull up resistor integrated into the OSD32MP15x so a strong pull down is required to pull it low. See Table 2-2 for more information on the internal pull up.

6.3.2 LSE MEMS Oscillator

The OSD32MP15x integrates a 32KHz oscillator used as the LSE clock source. The key parameters for the oscillator are outlined in Table 6-2.

Table 6-2 – LSE MEMS Oscillator Parameters

Parameter	Min	Typ	Max	Units	Notes
Active Supply Current		1		µA	
Initial Stability			±10	ppm	@25C
Frequency Stability			±100	ppm	All temp ranges
Aging			±1	ppm	First year @ 25C
Period Jitter, RMS			35	ps_{RMS}	
Frequency		32.768		KHz	

When the LSE is integrated, the LSE_OSC_TP pin becomes a test point for the output of the integrated oscillator. It is the signal that is being fed to the processor.

RSVD pin N1 is the OSC32_OUT from the processor.

6.4 EEPROM

The OSD32MP15x contains a 4KB EEPROM for non-volatile storage of configuration information. The EEPROM is connected to I2C4at the 7-bit I2C address 0x50 (0b1010000). Please refer to the data sheet in the Reference Documents section for details on using the EEPROM.

6.4.1 EEPROM Contents

EEPROM address space 0x000 to 0xEFF is empty and can be used for board specific information or other configuration data. The final 256 bytes of the EEPROM (0xF00 to 0xFFF) are reserved for device specific information. The reserved space contents of the EEPROM can be found in Table 6-3

Table 6-3 - EEPROM Contents Programmed by Octavo Systems

Name	Description	Size (bytes)	Start address	End address	Contents
RSVD	Reserved for Future Use	256	0xF00	0xFFF	All 0xFF

6.4.2 EEPROM Write Protection

By default, the EEPROM is write protected (i.e., the EEPROM_WP pin is pulled high as seen in Table 2-1). To program values into the EEPROM, it is required to drive the EEPROM_WP pin to a logic low. See the OSD32MP15x Layout Guide in the Reference Documents section for layout / manufacturing recommendations for the EEPROM_WP pin.

7 Power Management

The power management portion of the OSD32MP15x consists of the STPMIC1A (PMIC). The PMIC provides the necessary power rails to the STM32MP15x, DDR3, and all the other internal components to the OSD32MP15x. It also provides power supply outputs that may be used to power circuitry external to the OSD32MP15x. This section describes how to power the OSD32MP15x in a system and the outputs that can be used.

7.1 Power Input

The OSD32MP15x is powered by VIN on the STPMIC1A. This input supports a voltage range from 2.8V to 5.5V that is suitable for applications that are powered by 5V DC wall adaptors, 1-cell 3.6 V Li-Ion/Li-PO Battery or from a USB port.

7.2 System Output Power

The OSD32MP15x produces the following output power supplies that can be used for general system power. Each of the output voltages can be programed by the STM32MP15x processor via the I2C bus. Please refer to the datasheet for the STPMIC1 and the STMP32MP15x in the Reference Documents section.

In order to support the full range of output voltages supported by the regulators listed below the input voltage must be at a sufficient voltage to properly support the desired output voltage. Please refer to the STPMIC datasheet in the Reference Documents section to ensure that the desired output voltage is supported by the supplied input voltage.

7.2.1 PMIC_VOUT4

PMIC_VOUT4 is produced by Buck4 of the STPMIC1A. The input of Buck4 is tied to VIN internal to the OSD32MP15x. By default, it is configured to operate at 3.3V. It can be programmed to have a voltage output from 0.6V to 3.9V

7.2.2 PMIC_LDO1

PMIC_LDO1 is produced by LDO1 of the STPMIC1A. The input of LDO1 is tied to PMIC_VOUT4 (Buck4 Output) internal to the OSD32MP15x. By default, LDO1 is configured to operate at 1.8V. It can be programmed to have a voltage output from 1.7V to 3.3V.

Note that PMIC_LDO1 and PMIC_LDO6 are powered by PMIC_VOUT4. The total load on these LDOs plus any external load on PMIC_VOUT4 must not exceed the capabilities of the Buck4 regulator outlined in Section 0.

7.2.3 PMIC_LDO2

PMIC_LDO2 is produced by LDO2 of the STPMIC1A. The input of LDO is brought out to PMIC_LDO25IN allowing flexibility in determining the input voltage. In order to use this LDO PMIC_LDO25IN must be connected to a sufficient voltage source.

By default, LDO2 is configured to operate at 1.8V. it can be programmed to have a voltage output from 1.7V to 3.3V.

Note that PMIC_LDO2 and PMIC_LDO5 are powered by the same input voltage source. A sufficient input voltage source must be provided in order to use both LDOs.

7.2.4 PMIC_LDO5

PMIC_LDO5 is produced by LDO5 of the STPMIC1A. The input of LDO is brought out to PMIC_LDO25IN allowing flexibility in determining the input voltage. In order to use this LDO PMIC_LDO25IN must be connected to a sufficient voltage source.

By default, LDO5 is configured to operate at 2.9V. it can be programmed to have a voltage output from 1.7V to 3.3V

Note that PMIC_LDO2 and PMIC_LDO5 are powered by the same input voltage source. A sufficient input voltage source must be provided in order to use both LDOs.

7.2.5 PMIC_LDO6

PMIC_LDO6 is produced by LDO6 of the STPMIC1A. The input of LDO6 is tied to PMIC_VOUT4 (Buck4 Output) internal to the OSD32MP15x. By default, LDO6 is configured to operate at 1.0V. It can be programmed to have a voltage output from 0.9V to 3.3V.

Note that PMIC_LDO1 and PMIC_LDO6 are powered by PMIC_VOUT4. The total load on these LDOs plus any external load on PMIC_VOUT4 must not exceed the capabilities of the Buck4 regulator outlined in Section 0.

7.2.6 PMIC_BSTOUT

PMIC_BSTOUT is the output of the integrated Boost converter in the STPMIC1A. The input to the Boost converter is brought out through PMIC_BSTIN to give flexibility to the input of the boost converter. The OSD32MP15x also integrates an input inductor and capacitor so only a voltage input needs to be provided to use the boost.

The Boost converter has a fixed voltage of 5.2V and is designed to power USB devices. It also supports the BYPASS mode as described in the STPMIC datasheet.

7.2.7 PMIC_VBUSOTG

PMIC_VBUSOTG is the output of the PWR_USB_SW in the STPMIC1A. It is designed to power USB OTG port or USB Type-C. The input of the switch is connected to the PMIC_BSTOUT internal to the STPMIC1A. The output voltage of the PWR_USB_SW is about equal to the PMIC_BSTOUT.

7.2.8 PMIC_SWOUT

PMIC_SWOUT is the output of the PWR_SW internal to the STPMIC1A. The input of the switch is brought out to PMIC_SWIN to allow flexibility in the input voltage. The output voltage of PMIC_SWOUT will be about equal to the input voltage provided on PMIC_SWIN.

7.3 Internal Power

The OSD32MP15x has power rails generated by the STPMIC1A that are used internally to the OSD32MP15x. While some of the output voltages of the regulators can be adjusted, they should not be. Adjusting the voltages on these rails will cause the OSD32MP15x device not to function.

These rails are made available through the associated pin. They are made available only for monitoring and test points. They must not be used to power external circuitry. Doing so will prevent the OSD32MP15x from functioning properly.

7.3.1 VDD_CORE

VDD_CORE is generated by Buck1 in the STPMIC1A. It provides the core power to the STM32MP15x integrated into the OSD32MP15x. Its voltage is 1.2V.

7.3.2 VDD_DDR

VDD_DDR is generated by Buck2 in the STPMIC1A. It provides the power to the DDR memory integrated into the OSD32MP15x. Its voltage is 1.1V.

7.3.3 VDD

VDD is generated by Buck3 in the STPMIC1A. It provides the power to the VDD Power domain of the STM32MP15x integrated into the OSD32MP15x. Its voltage is 3.3V.

7.3.4 VTT_DDR

VTT_DDR is generated by LDO3 in the STPMIC1A. It provides power to the DDR VTT. Its voltage is 1.8V.

7.3.5 VDD3V3_USB

VDD3V3_USB is generated by LDO4 in the STPMI1A. It provides power for the VDD_USB power domain of the STM32MP15x. It has a fixed voltage of 3.3V.

7.3.6 VREF_DDR

VREF_DDR is generated by DDR_VREF in the STPMI1A. It provides power for the reference voltage for the integrated DDR. It has a fixed voltage of 0.55V.

7.3.7 VDD1V2_DSI_REG

VDD1V2_DSI_REG is generated by the $V_{DDA1V2\_DSI\_REG}$ regulator in the STM32MP1. It is connected internal of the STM32MP15 to the DSI PLL. Its voltage is 1.2V.

7.3.8 VDDA1V1_REG

VDDA1V1_REG is generated by the V_{DDA1V1_REG} regulator in the STM32MP1. It is connected internal of the STM32MP15 to the USB PHY. Its voltage is 1.1V.

7.3.9 VDDA1V8_REG

VDDA1V8_REG is generated by the V_{DDA1V8_REG} regulator in the STM32MP1. It is connected internal of the STM32MP15 to the USB PHY and USB PLL. Its voltage is 1.8V.

7.4 Total Current Consideration

The total current consumption of all power rails must not exceed the recommended input currents described in Table 8-2. This includes power consumption within the SiP from the STM32MP15x, the DDR3, MEMS Oscillators, and other internal components as well as all external loads on the output power rails from Section 7.2.

8 Electrical & Thermal Characteristics

Table 8.1 lists electrical and thermal characteristic parameters of OSD32MP15x.

Table 8-1. OSD32MP15x Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted) (1) (2)

			Value	Unit
Supply voltage range (with respect to VSS)		VIN	TBD	V
Input/Output voltage range (with respect to VSS)		All pins unless specified separately	-0.3 to 3.6	V
Terminal current		VIN	TBD	mA
T_C	**Operating case temperature**	Commercial (B)	0 to 85	°C
		Industrial (I)	-40 to 85	°C
T_{stg}	**Storage temperature**		-40 to 125	°C
ESD rating		(HBM) Human body model	±2000	V
		(CDM) Charged device model	±500	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

Table 8-2. Recommended Operating Conditions over operating free-air temperature range (unless otherwise noted)

	Min	Nom	Max	Unit
Supply voltage, VIN	2.8		5.5	V
Input current from VIN			TBD	A
Output voltage range for PMIC_VOUT4	0.6	3.3	3.9	V
Output voltage range for PMIC_LDO1	1.7	1.8	3.3	V
Output voltage range for PMIC_LDO2	1.7	1.8	3.3	V
Output voltage range for PMIC_LDO5	1.7	2.9	3.9	V
Output voltage range for PMIC_LDO6	0.9	1.0	3.3	V
Output voltage range for PMIC_BSTOUT		5.2		V
Output voltage range for PMIC_VBUSOTG	~PMIC_BSTOUT			V
Output voltage range for PMIC_SWOUT	~PMIC_SWIN			V
Output voltage range for VDD_CORE[1]		1.2		V
Output voltage range for VDD_DDR[1]		1.1		V
Output voltage range for VDD[1]		3.3		V
Output voltage range for VTT_DDR[1]		1.8		V
Output voltage range for VDD3V3_USB[1]		3.3		V
Output voltage range for VREF_DDR[1]		0.55		V
Output voltage range for VDD1V2_DSI_REG[1]		1.2		V
Output voltage range for VDDA1V1_REG[1]		1.1		V
Output voltage range for VDDA1V8_REG[1]		1.8		V
Output current for PMIC_VOUT4[2]	0		TBD	mA
Output current for PMIC_LDO1[2]	0		TBD	mA
Output current for PMIC_LDO2[2]	0		TBD	mA
Output current for PMIC_LDO5[2]	0		TBD	mA
Output current for PMIC_LDO6[2]	0		TBD	mA
Output current for PMIC_BSTOUT[2]	0		TBD	mA
Output current for PMIC_VBUSOTG[2]	0		TBD	mA
Output current for PMIC_SWOUT[2]	0		TBD	mA

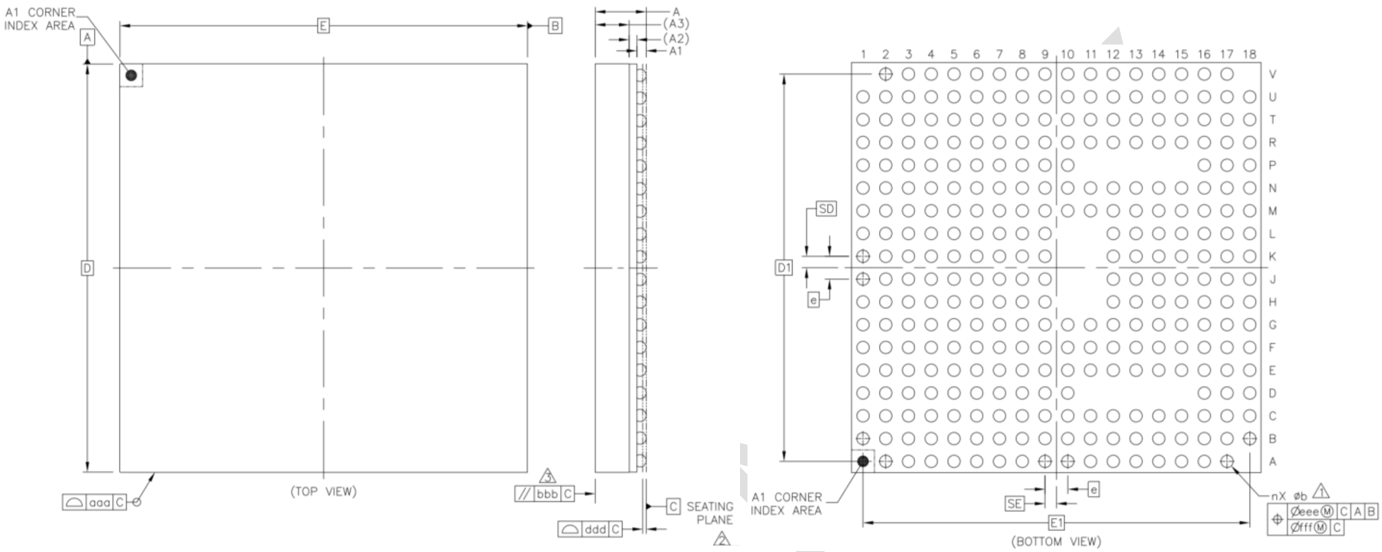
(1) *These voltage rails are for reference only and should not be used to power anything on the PCB.*
(2) Please note that the total input current on VIN must not exceed the recommended maximum value even if individual currents drawn from these power supply outputs are less than or equal to the maximum recommended operating output currents. See section 7.4 for more details.

9 Packaging Information

The OSD32MP15x is packaged in a 302 ball, Ball Grid Array (BGA). The package size is 18 X 18 millimeters with a ball pitch of 1 millimeter. This section will give you the specifics on the package.

9.1 Mechanical Dimensions

The mechanical drawings of the OSD32MP15x show pin A1 in the lower left-hand corner when looking at the balls from the bottom of the device.



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	2.4
STAND OFF	A1	0.36	---	0.46
SUBSTRATE THICKNESS	A2		0.34	REF
MOLD THICKNESS	A3		1.5	REF
BODY SIZE	D		18	BSC
	E		18	BSC
BALL DIAMETER			0.5	
BALL OPENING			0.4	
BALL WIDTH	b	0.44	---	0.64
BALL PITCH	e		1	BSC
BALL COUNT	n		302	
EDGE BALL CENTER TO CENTER	D1		17	BSC
	E1		17	BSC
BODY CENTER TO CONTACT BALL	SD		0.5	BSC
	SE		0.5	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.15	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

9.2 Reflow Instructions

The reflow profile for this package should be in accordance with the Lead-free process for BGA. A peak reflow temperature is recommended to be 245°C.

Texas Instruments provides a good overview of Handling & Process Recommendations in AN-2029 for this type of device. A link to the document can be found in the Reference Documents section of this document.

9.3 Storage Requirements

The OSD335x Family of devices are sensitive to moisture and need to be handled in specific ways to make sure they function properly during and after the manufacturing process. The OSD335x Family of devices are rated with a Moisture Sensitivity Level (MSL) of 4. This means that they are typically stored in a sealed Dry Pack.

Once the sealed Dry Pack is opened the OSD335x needs to be used within 72 hours to avoid further processing. If the OSD335x has been exposed for more than 72 hours, then it is required that you bake the device for 34 hours at 125°C before using.

Alternatively, the devices could be stored in a dry cabinet with humidity <10% to avoid the baking requirement.

For more information, please refer to the Texas Instruments AN-2029 which can be found in the Reference Documents section of this document.