**NXP Semiconductors**
Application Note

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# Hardware Development Guide for the MIMXRT1020 Processor

## 1 Introduction

This document guides the hardware engineers to design and test their MIMXRT1020 processor-based designs. The document provides information about board layout recommendations and design checklists to ensure first-pass success and avoid any board bring-up problems.

This guide is released with the relevant device-specific hardware documentation such as data sheets, reference manuals, and application notes available on nxp.com.

## 2 Background

The MIMXRT1020 processors are the latest additions to the growing family of real-time processing products from NXP, offering high-performance processing optimized for lowest power consumption and best real-time response. The MIMXRT1020 processors feature advanced implementation of the Arm® Cortex®-M7 core, which operates at speeds of up to 500/400 MHz.

### Contents

The MIMXRT1020 processors are specifically useful for applications such as:

- Industrial Human Machine Interfaces (HMI)
- Motor control
- Home appliances
- IoT

# 3 Power supply

See Table 1 and Table 2 for the power domains and power supply decoupling recommendations.

**Table 1. Power domains**

| Power rail | MIN (V) | TYP (V) | MAX (V) | Description |
|---|---|---|---|---|
| VDD_SOC_IN | 0.925 | — | 1.3[1] | Power for the core supply |
| VDD_HIGH_IN | 3 | 3.3 | 3.6 | VDD_HIGH_IN supply voltage |
| DCDC_IN | 3 | 3.3 | 3.6 | Power for the DCDC |
| VDD_SNVS_IN | 2.4 | 3.0 | 3.6 | Power for the SNVS and RTC |
| USB_OTG1_VBUS | 4.4 | 5.0 | 5.5 | Power for the USB VBUS |
| VDDA_ADC_3P3 | 3 | 3.3 | 3.6 | Power for the 12-bit ADC |
| NVCC_SD0 | 3 | 3.3 | 3.6 | Power for the GPIO in the SDIO1 bank (3.3 V mode) |
| | 1.65 | 1.8 | 1.95 | Power for the GPIO in the SDIO1 bank (1.8 V mode) |
| NVCC_GPIO | 3 | 3.3 | 3.6 | IO power for the GPIO |

1. Max is 1.26 V for the industrial part numbers

**Table 2. Power supply decoupling recommendations**

| Power rail | Decoupling and bulk capacitors(min qty) | Description |
|---|---|---|
| VDD_SOC_IN | 7 × 0.22 μF[2] + 1 × 4.7 μF[1] | Place at least one 4.7 μF capacitor and seven 0.22 μF capacitors next to PIN 5,31, 39, and so on. |
| VDD_HIGH_IN | 1 × 0.22 μF[2] + 1 × 4.7 μF[1] | Place at least one 4.7 μF capacitor and one 0.22 μF capacitors next to PIN 69. |
| VDD_HIGH_CAP | 1 × 0.22 μF[2] + 1 × 4.7 μF[1] | VDDHIGH_CAP is restricted to the MX6RT. |
| DCDC_IN | 1 × 0.22 μF[2] + 1 × 4.7 μF[1] | Place at least one 4.7 μF capacitor and one 0.22 μF |
| VDD_SNVS_IN | 1 × 0.22 μF[2] | — |
| VDD_SNVS_CAP | 1 × 0.22 μF[2] + 1 × 4.7 μF[1] | Select a small capacitor with low ESR. Do not connect any loads to VDD_SNVS_CAP. |

| | | |
|---|---|---|
| USB_OTG1_VBUS | 1 × 1 μF[1] | 10-V rated. |
| VDDA_ADC_3P3 | 1 × 0.22 μF[2] + 1 × 1 μF[1] | Place the buck and bypass capacitors next to PIN 73. |
| NVCC_SD0 | 1 × 0.1 μF + 1 × 4.7 μF[1] | Place the buck and bypass capacitors next to PIN 44. |
| NVCC_GPIO | 4 × 0.1 μF + 7 × 4.7 μF[1] | Place at least four 4.7 μF capacitor and seven 0.1 μF capacitors next to PIN 11, 20, 29, and so on. |

1. For the 4.7-μF capacitors, use the 0402 package.
2. For the 0.22-μF capacitors, use the 0402 package.
3. For the 22-μF capacitors, the 0603 package is preferred; 0805 and 1206 packages are acceptable.

**Table 3. Power sequence and recommendations**

| Item | Recommendation | Description |
|---|---|---|
| Power sequence | Comply with the power-up/power-down sequence guidelines (as described in the data sheet) to guarantee a reliable operation of the device. | Any deviation from these sequences may result in these situations:<br>• Excessive current during the power-up phase<br>• Prevention of the device from booting<br>• Irreversible damage to the processor (worst-case scenario) |
| SNVS domain signals | Do not overload the coin cell backup power rail VDD_SNVS_IN.<br>Note that these I/Os are associated with VDD_SNVS_IN (most inputs have on-chip pull resistors and do not require external resistors):<br>• PMIC_STBY_REQ—configurable output<br>• PMIC_ON_REQ—push-pull output<br>• TEST_MODE—on-chip pulldown<br>• WAKEUP—the GPIO that wakes the SoC up in the SNVS mode | Concerning i.MX RT1020:<br>• When VDD_SNVS_IN = VDD_HIGH_IN in the SNVS domain, the current is drawn from both equally.<br>• When VDD_HIGH_IN > VDD_SNVS_IN, VDD_HIGH_IN supplies all the SNVS domain current and the current flows into VDD_SNVS_IN to charge the coin cell battery.<br>• When VDD_SNVS_IN > VDD_HIGH_IN. |
| Power ripple | Maximum ripple voltage limitation. | The common limitation for the ripple noise shall be less than 5 % Vp-p of the supply voltage average value. The related power rails affected are VDD_xxx_IN and VDD_xxx_CAP. |

| | | |
|---|---|---|
| VDD_SNVS_IN and VDD_HIGH_IN | If VDD_SNVS_IN is directly supplied by a coin cell battery, a Schottky diode is required between VDD_HIGH_IN and VDD_SNVS_IN. The cathode is connected to VDD_SNVS_IN. Alternately, VDD_HIGH_IN and VDD_SNVS_IN can be tied together if the real-time clock function is not needed during the system power-down. | When no power is supplied to VDD_VSNVS_IN, the diode limits the voltage difference between the two on-chip SNVS power domains to approximately 0.3 V. The processor allows the current to flow between the two SNVS power domains, proportionally to the voltage difference. |

- Power Up Sequence Requirement
  - VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_HIGH_IN supply
  - If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on
  - When internal DCDC is enabled, external delay circuit is required to delay the “DCDC_PSWITCH” signal at least 1 ms after DCDC_IN is stable
  - POR_B must be held low during the entire power up sequence
- Power Down Sequence Requirement
  - VDD_SNVS_IN supply must be turned off after any other power supply or be connected (shorted) with VDD_HIGH_IN supply
  - If a coin cell is used to power VDD_SNVS_IN, then ensure that it is removed after any other supply is switched off

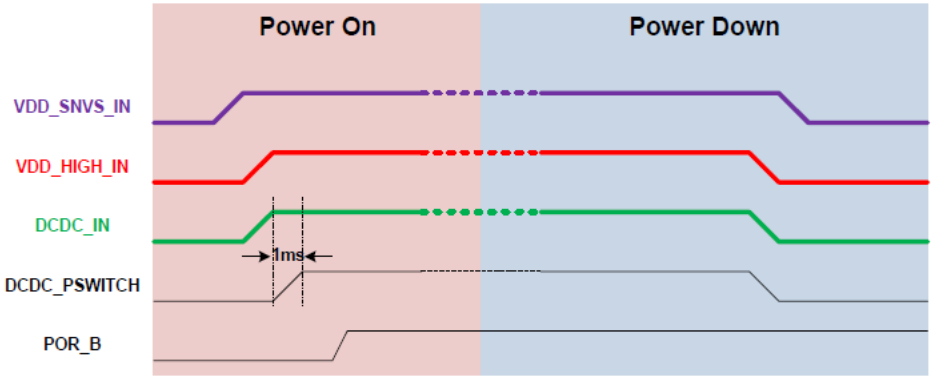


**Figure 1. Power up and power down sequence**

For RT1020-EVK, see Figure 2

  - First, it powers up SNVS.
  - PMIC_REQ_ON is then switched on to enable the external DC/DC to power up other power domains.
  - DCDC_PSWITCH is delayed more than 1ms to switch the internal DCDC on.
  - DCDC_OUT output powers the VDD_SOC_IN.

- The ON/OFF button is used to switch PMIC_REQ_ON on/off to control power modes.
- The RESET button and the WDOG output are used to reset the system power.

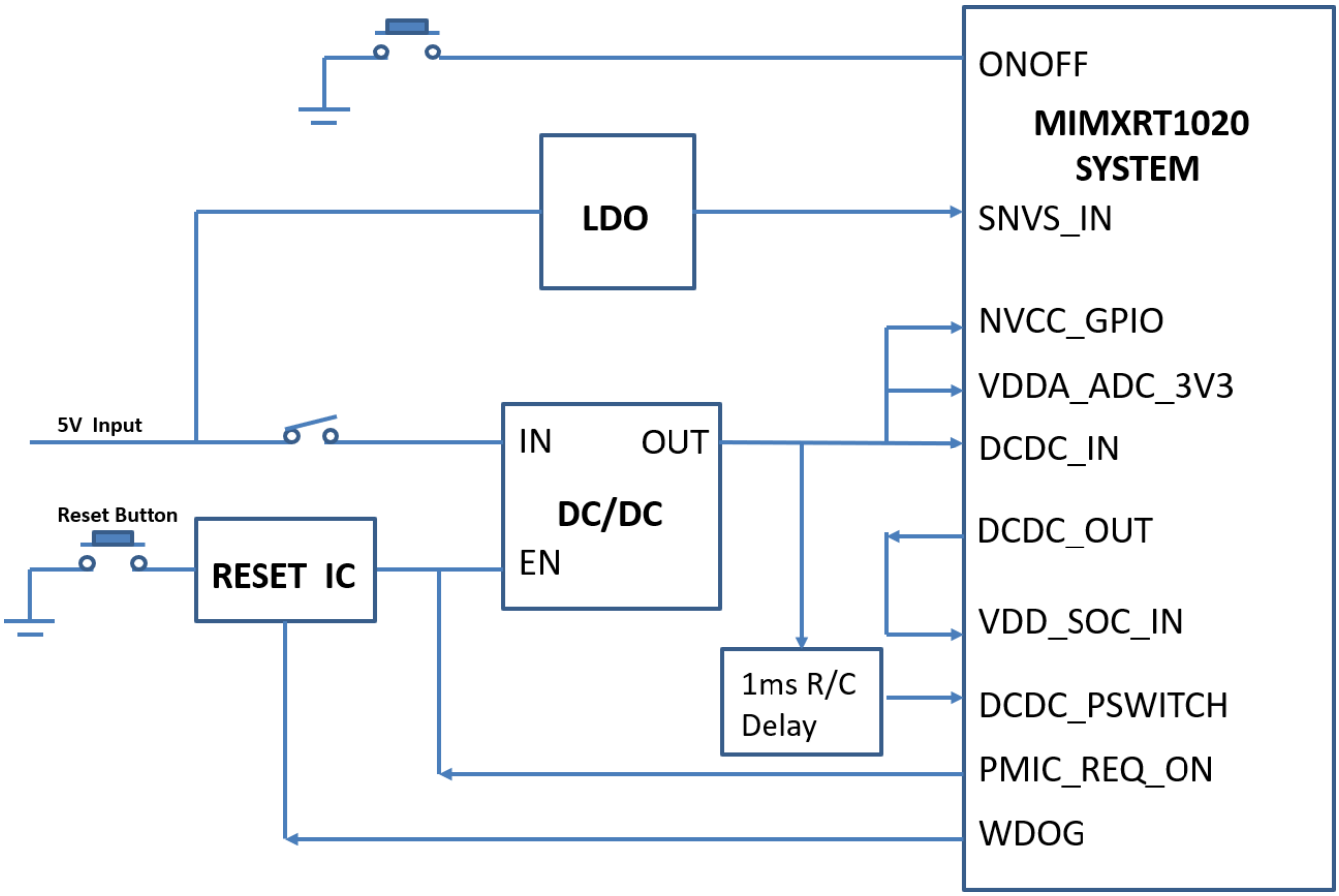


**Figure 2. Power control diagram**

- About on chip DC/DC module

The internal DC/DC switching frequency is about 1.5 MHz. The DC/DC requires external inductor and capacitors, the illustration is as below Figure **3**, please pay attention to below items:

- The recommended value for the external inductor is about 4.7~10 uH , saturation current >1A, ESR < 0.2 Ohm.
- The external buck capacitor total is about 33uF, this includes all the capacitors used on DCDC_OUT and VDD_SOC_IN.
- DCDC_PSWITCH should delay 1ms with respect to DCDC_IN to guarantee that DCDC_IN is stable before the DC/DC starts up.
- If you want to bypass internal DC/DC, you still need to power DCDC_IN. DCDC_PSWITCH should be grounded to disable the DC/DC, and DCDC_LP should be left floating.
- Try to keep the DC/DC current loop as small as possible to avoid EMI issues.

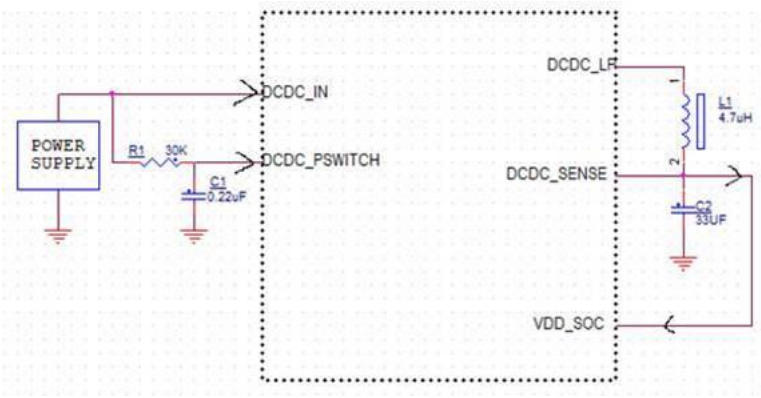


**Figure 3. DC/DC function diagram**

# 4 Clocks

See Table 4 for the clock configuration. The 32.768 kHz and 24 MHz oscillators are used for the EVK Design and it can't be replaced with crystal with other frequency.

**Table 4. Clocks' configurations**

| Signal name | Recommended connections | Description |
|---|---|---|
| 1.RTC_XTALI/RTC_XTALO | For the precision 32.768-kHz oscillator, connect a crystal between RTC_XTALI and RTC_XTALO. Choose a crystal with a maximum ESR (Equivalent Series Resistance) of 100 k and follow the manufacturer's recommendation for the loading capacitance. Do not use an external biasing resistor because the bias circuit is on the chip. | To hit the exact oscillation frequency, the board capacitors must be reduced to account for the board and chip parasitic. The integrated oscillation amplifier is self-biasing, but relatively weak. Care must be taken to limit the parasitic leakage from RTC_XTALI and RTC_XTALO to either the power or the ground (>100 M). This de-bias the amplifier and reduces the start-up margin. |
| | For the external kHz source (if feeding an external clock into the device), RTC_XTALI can be driven DC-coupled with RTC_XTALO floating or driven by a complimentary signal. | If you want to feed an external low-frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven by a complementary signal. The logic level of this forcing clock must not exceed the VDD_SNVS_CAP level and the frequency shall be <100 kHz under the typical conditions. |
| | An on-chip loose-tolerance ring oscillator of approximately 40 kHz is available. If RTC_XTALI is tied to GND and RTC_XTALO is floating, the on-chip oscillator is engaged automatically. | When a high-accuracy real-time clock is not required, the system may use the on-chip 40-kHz oscillator. The tolerance is ±50 %. The ring oscillator starts faster than the external crystal and is used until the external crystal reaches a stable oscillation. The ring oscillator also starts automatically if no clock is detected at RTC_XTALI at any time. |
| 2. XTALI/XTALO | For the precision 24-MHz oscillator, connect a fundamental-mode crystal between XTALI and XTALO. A typical 80 ESR crystal rated for a maximum drive level of 250 μW is acceptable. Alternately, a typical 50 ESR crystal rated for a maximum drive level of 200 μW may be used. | The SDK software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24-MHz oscillator is available in the system. In this case, please refer to section of Bypass Configuration (24 MHz) from the reference manual. There are three configurations that can be utilized, but configuration 2 is recommended. The logic level of this forcing clock must not exceed the NVCC_PLL level. |

# 5 Debugging and programming

See Table 5 for the JTAG interface summary and recommendation. The RT1020 EVK also features an OpenSDA, which makes it easier to debug without an external debugger.

**NOTE**

For RT1020 silicon, debugger defaults to be in SWD mode instead of JTAG.

**Table 5. JTAG interface summary**

| JTAG signals | I/O type | On-chip termination | External termination |
|---|---|---|---|
| JTAG_TCK | Input | 100 kΩ pull-down | Not required; can use 10 kΩ pull-up |
| JTAG_TMS | Input | 47 kΩ pull-up | Not required; can use 10 kΩ pull-up |
| JTAG_TDI | Input | 47 kΩ pull-up | Not required; can use 10 kΩ pull-up |
| JTAG_TDO | 3-state output | no pull-up/pull-down | Do not use pull-up or pull-down |
| JTAG_TRSTB | Input | 47 kΩ pull-up | Not required; can use 10 kΩ pull-up |
| JTAG_MOD | Input | 100 kΩ pull-down | Use 4.7 kΩ pull-down or tie to GND |

**Table 6. JTAG recommendation**

| Signals | Recommendation | Description |
|---|---|---|
| 1. JTAG_TDO | Do not add external pull-up or pull-down resistors on JTAG_TDO. | JTAG_TDO is configured with an on-chip keeper circuit, such that the floating condition is actively eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental. See Table 5 for a summary of the JTAG interface. |
| 2. All JTAG Signals | Ensure that the on-chip pull-up/pull-down configuration is followed if external resistors are used with the JTAG signals (except for JTAG_TDO). For example, do not use an external pull-down on an input that has an on-chip pull-up. | External resistors can be used with all JTAG signals except for JTAG_TDO, but they are not required. See Table 5 for a summary of the JTAG interface. |

| | | |
|---|---|---|
| 3. JTAG_MOD | JTAG_MOD is called SJC_MOD in some documents. Both names refer to the same signal. JTAG_MOD shall be externally connected to GND for normal operation in a system. The termination to GND through an external pull-down resistor is allowed. Use a 4.7-kΩ resistor. | When JTAG_MOD is low, the JTAG interface is configured for a common software debug, adding all the system TAPs to the chain.<br>When JTAG_MOD is high, the JTAG interface is configured to a mode compliant with the IEEE 1149.1 |

**Table 7. OpenSDA recommendation**

| Signals | Recommendation | Description |
|---|---|---|
| SWD_DIO | Connect to the K20/LPC4322 signal through a buffer | The OpenSDA in the EVK board is implemented as a debugger, which eliminates the cost for the users. |
| SWD_CLK | Connect to the K20/LPC4322 signal through a buffer | |
| UART_TXD/UART_RXD | Connect to the K20/LPC4322 signal through a buffer | The UART signals connected to K20/LPC4322 realize a virtual COM port for the OpenSDA USB for debugging. |

The ROM's Serial Downloader mode provides a means to download a Program Image to the chip over USB or UART serial connection. In this mode, typically a host PC can communicate to the ROM bootloader using serial download protocol. NXP's ROM flashloader also uses these same serial connections. It is strongly recommended for all boards to make at least one of the serial downloader ports (USB1 or UART1) available to be able to make use of NXP's image and fuse programming enablement.

**Table 8. Serial downloader I/Os table**

| Signals | Recommendation | Description |
|---|---|---|
| UART1 | The Serial Downloader provides a means to download a program image to the chip over the USB and UART serial connections.<br>In this mode, ROM programs WDOG1 for a time-out specified by the fuse WDOG Time-out Select (See the Fusemap chapter for details) if the WDOG_ENABLE eFuse is 1 and continuously polls for the USB and UART connection.<br>. | The ROM code firstly polls the UART1 signals from TXD1/RXD1.<br>Add a 10-kΩ pull up resistor to the TXD1/RXD1 pins to avoid an invalid trigger of the UART port in the serial download mode. |
| USB1 | | If there is no polling activity from UART1 in the serial download mode, the ROM code acts as an HID device for PC downloading. |

# 6 Boot, reset, and miscellaneous

See Table 9 for the boot, reset, and miscellaneous configurations, such as ON/OFF, TEST_MODE, NC pins, and other.

**Table 9. Boot configuration**

| Item | Recommendation | Description |
|---|---|---|
| 1. BOOT_CFG[11:0] | The BT_CFG[] signals are required for a proper functionality and operation and shall not be left floating during development if BT_CFG[] fuses and BT_FUSE_SEL are not configured. | See the “System Boot” chapter in your chip reference manual for the correct boot configuration. Note that an incorrect setting may result in an improper boot sequence. |
| 2. BOOT_MODE[1:0] | For BOOT_MODE1 and BOOT_MODE0, use one of these options to achieve logic 0:<br>• Tie to GND through any-value external resistor<br>• Tie directly to GND. For logic 1, use one of these options:<br>  ○ Tie directly to the NVCC_GPIO_XX rail.<br>  ○ Tie to the NVCC_GPIO_XX rail through an external 10 k resistor.<br>A value of 4.7 k is preferred for high-noise environments.<br>If a switch control is desired, no external pull-down resistors are necessary. Simply connect the SPST switches directly to the NVCC_GPIO_XX rail. | BOOT_MODE1 and BOOT_MODE0 each have on-chip pull-down devices with a nominal value of 100 kΩ, a projected minimum of 60 kΩ, and a projected maximum of 140 kΩ.<br>When the on-chip fuses determine the boot configuration, both boot mode inputs can be disconnected. |
| 3. BOOT_CFG and BOOT_MODE signals multiplexed with SEMC signals | To reduce incorrect boot-up mode selections, do one of the following:<br>• Use the SEMC boot interface lines only as processes or outputs. Ensure that the SEMC boot interface lines are not loaded down (such that the level is interpreted as low during the powerup) when the intent is to be at a high level, or the other way around.<br>• If the SEMC boot signal must be configured as an input, isolate the SEMC signal from the target driving source with an analog switch and apply the logic value with a second analog switch. Alternately, the peripheral devices with 3-state outputs may be used. Ensure that the output is high-impedance. | Using the SEMC boot interface lines as inputs may result in a wrong boot because of the source overcoming the pull resistor value.<br>A peripheral device may require the SEMC signal to have an external or on-chip resistor to minimize signal floating. If the usage of the SEMC boot signal affects the peripheral device, then an analog switch, an open collector buffer, or an equivalent shall isolate the path. A pull-up or pull-down resistor at the peripheral device may be required to maintain the desired logic level. See the switch or device data sheet for the operating specifications. |

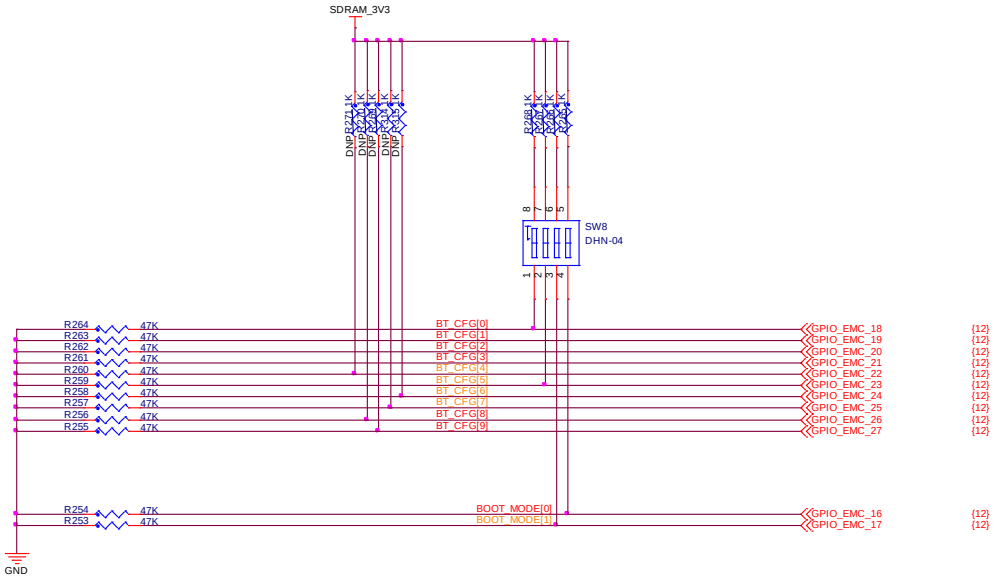


**Figure 4. Boot mode setting**

**Table 10. Reset and miscellaneous recommendations**

| Item | Recommendation | Description |
|---|---|---|
| 1. POR_B | If the external POR_B signal is used to control the processor POR, then POR_B must be immediately asserted at the powerup and remain asserted until the VDD_HIGH_CAP and VDD_SNVS_CAP supplies are stable. VDD_SOC_IN may be applied in either order with no restrictions. In the absence of an external reset feeding the SRC_POR_B input, the internal POR module takes control. | See the "System Boot" chapter in your chip reference manual for the correct boot configuration. Note that an incorrect setting may result from an improper boot sequence. POR_B signal has internal 100K pull up to SNVS domain, should pull up to VDD_SNVS_IN if need to add external pull up resistor, otherwise it will cause additional leakage during SNVS mode. It's recommended to add the external reset IC to the circuit to guarantee POR_B is properly processed during power up/down, please refer to the EVK design for details.<br>Note:<br>1. As the Low DCDC_IN detection threshold is 2.6 V, the reset IC's reset threshold must be higher than 2.6 V, then the whole chip is reset before the internal DCDC module reset to guarantee the chip safety during power down.<br>2. For power on reset, on any conditions ones need to make sure the voltage on DCDC_PSWITCH PIN is below 0.5 V before power up. |

| | | |
|---|---|---|
| 2. ON/OFF | For portable applications, the ON/OFF input may be connected to the ON/OFF SPST push-button. The on-chip de-bouncing is provided, and this input has an on-chip pullup. If not used, ON/OFF can be a no-connect. A 4.7-kΩ to 10-kΩ series resistor can be used when the current drain is critical. | A brief connection to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to GND generates an interrupt (intended to be a software-controllable power-down). Approximately five seconds (or more) to GND causes a forced OFF. Both boot mode inputs can be disconnected. |
| 3. TEST_MODE | The TEST_MODE input is internally connected to an on-chip pull-down device. You may either float this signal or tie it to GND. | This input is reserved for NXP manufacturing use. |
| 4. GPANAIO | GPANAIO must be a no-connect. | This output is reserved for NXP manufacturing use. |
| 5. NC pin | The NC contacts are no-connect and shall float. | Depending on the feature set, some versions of ICs may have the NC contacts connected inside the BGA. |

**Table 11. ROM Bootloader Peripheral PinMux**

| BT Device | IO Func | ALT | PAD |
|---|---|---|---|
| UART1 | lpuart1.TX | 2 | GPIO_AD_B0_06 |
| | lpuart1.RX | 2 | GPIO_AD_B0_07 |
| | lpuart1.CTS_B | 2 | GPIO_AD_B0_08 |
| | lpuart1.RTS_B | 2 | GPIO_AD_B0_09 |
| UART2 | lpuart2.CTS_B | 2 | GPIO_AD_B1_06 |
| | lpuart2.RTS_B | 2 | GPIO_AD_B1_07 |
| | lpuart2.TX | 2 | GPIO_AD_B1_08 |
| | lpuart2.RX | 2 | GPIO_AD_B1_09 |
| SPI-1 | lpspi1.SCK | 1 | GPIO_AD_B0_10 |
| | lpspi1.PCS0 | 1 | GPIO_AD_B0_11 |
| | lpspi1.SDO | 1 | GPIO_AD_B0_12 |
| | lpspi1.SDI | 1 | GPIO_AD_B0_13 |
| SPI-2 | lpspi2.SCK | 4 | GPIO_SD_B1_07 |
| | lpspi2.SDO | 4 | GPIO_SD_B1_08 |
| | lpspi2.SDI | 4 | GPIO_SD_B1_09 |
| | lpspi2.PCS0 | 4 | GPIO_SD_B1_06 |
| SPI-3 | lpspi3.SCK | 2 | GPIO_AD_B1_12 |
| | lpspi3.PCS0 | 2 | GPIO_AD_B1_13 |
| | lpspi3.SDO | 2 | GPIO_AD_B1_14 |
| | lpspi3.SDI | 2 | GPIO_AD_B1_15 |
| SPI-4 | lpspi4.SCK | 4 | GPIO_EMC_32 |
| | lpspi4.PCS0 | 4 | GPIO_EMC_33 |

| BT Device | IO Func | ALT | PAD |
|---|---|---|---|
| | lpspi4.SDO | 4 | GPIO_EMC_34 |
| | lpspi4.SDI | 4 | GPIO_EMC_35 |
| NAND | semc.DATA[0] | 0 | GPIO_EMC_00 |
| | semc.DATA[1] | 0 | GPIO_EMC_01 |
| | semc.DATA[2] | 0 | GPIO_EMC_02 |
| | semc.DATA[3] | 0 | GPIO_EMC_03 |
| | semc.DATA[4] | 0 | GPIO_EMC_04 |
| | semc.DATA[5] | 0 | GPIO_EMC_05 |
| | semc.DATA[6] | 0 | GPIO_EMC_06 |
| | semc.DATA[7] | 0 | GPIO_EMC_07 |
| | semc.DATA[8] | 0 | GPIO_EMC_32 |
| | semc.DATA[9] | 0 | GPIO_EMC_33 |
| | semc.DATA[10] | 0 | GPIO_EMC_34 |
| | semc.DATA[11] | 0 | GPIO_EMC_35 |
| | semc.DATA[12] | 0 | GPIO_EMC_36 |
| | semc.DATA[13] | 0 | GPIO_EMC_37 |
| | semc.DATA[14] | 0 | GPIO_EMC_38 |
| | semc.DATA[15] | 0 | GPIO_EMC_39 |
| | semc.ADDR[9] | 0 | GPIO_EMC_25 |
| | semc.ADDR[11] | 0 | GPIO_EMC_26 |
| | semc.ADDR[12] | 0 | GPIO_EMC_27 |
| | semc.BA1 | 0 | GPIO_EMC_14 |
| | semc.CSX[0] | 0 | GPIO_EMC_40 |
| NOR | semc.DATA[0] | 0 | GPIO_EMC_00 |
| | semc.DATA[1] | 0 | GPIO_EMC_01 |
| | semc.DATA[2] | 0 | GPIO_EMC_02 |
| | semc.DATA[3] | 0 | GPIO_EMC_03 |
| | semc.DATA[4] | 0 | GPIO_EMC_04 |
| | semc.DATA[5] | 0 | GPIO_EMC_05 |
| | semc.DATA[6] | 0 | GPIO_EMC_06 |
| | semc.DATA[7] | 0 | GPIO_EMC_07 |
| | semc.DATA[8] | 0 | GPIO_EMC_32 |
| | semc.DATA[9] | 0 | GPIO_EMC_33 |
| | semc.DATA[10] | 0 | GPIO_EMC_34 |
| | semc.DATA[11] | 0 | GPIO_EMC_35 |
| | semc.DATA[12] | 0 | GPIO_EMC_36 |
| | semc.DATA[13] | 0 | GPIO_EMC_37 |

| BT Device | IO Func | ALT | PAD |
|---|---|---|---|
| | semc.DATA[14] | 0 | GPIO_EMC_38 |
| | semc.DATA[15] | 0 | GPIO_EMC_39 |
| | semc.ADDR[0] | 0 | GPIO_EMC_16 |
| | semc.ADDR[1] | 0 | GPIO_EMC_17 |
| | semc.ADDR[2] | 0 | GPIO_EMC_18 |
| | semc.ADDR[3] | 0 | GPIO_EMC_19 |
| | semc.ADDR[4] | 0 | GPIO_EMC_20 |
| | semc.ADDR[5] | 0 | GPIO_EMC_21 |
| | semc.ADDR[6] | 0 | GPIO_EMC_22 |
| | semc.ADDR[7] | 0 | GPIO_EMC_23 |
| | semc.ADDR[11] | 0 | GPIO_EMC_26 |
| | semc.ADDR[12] | 0 | GPIO_EMC_27 |
| | semc.BA0 | 0 | GPIO_EMC_13 |
| | semc.BA1 | 0 | GPIO_EMC_14 |
| | semc.CSX[0] | 0 | GPIO_EMC_40 |
| SD1 | usdhc1.CD_B | 0 | GPIO_SD_B0_06 |
| | usdhc1.WP | 2 | GPIO_AD_B0_04 |
| | usdhc1.VSELECT | 0 | GPIO_AD_B1_07 |
| | usdhc1.RESET_B | 0 | GPIO_AD_B1_06 |
| | usdhc1.CMD | 0 | GPIO_SD_B0_02 |
| | usdhc1.CLK | 0 | GPIO_SD_B0_03 |
| | usdhc1.DATA0 | 0 | GPIO_SD_B0_04 |
| | usdhc1.DATA1 | 0 | GPIO_SD_B0_05 |
| | usdhc1.DATA2 | 0 | GPIO_SD_B0_00 |
| | usdhc1.DATA3 | 0 | GPIO_SD_B0_01 |
| SD2 | usdhc2.CD_B | 0 | GPIO_SD_B1_06 |
| | usdhc2.WP | 3 | GPIO_AD_B1_13 |
| | usdhc2.RESET_B | 0 | GPIO_SD_B1_07 |
| | usdhc2.CMD | 0 | GPIO_SD_B1_02 |
| | usdhc2.CLK | 0 | GPIO_SD_B1_03 |
| | usdhc2.DATA0 | 0 | GPIO_SD_B1_04 |
| | usdhc2.DATA1 | 0 | GPIO_SD_B1_05 |
| | usdhc2.DATA2 | 0 | GPIO_SD_B1_00 |
| | usdhc2.DATA3 | 0 | GPIO_SD_B1_01 |
| | usdhc2.DATA4 | 0 | GPIO_SD_B1_08 |
| | usdhc2.DATA5 | 0 | GPIO_SD_B1_09 |
| | usdhc2.DATA6 | 0 | GPIO_SD_B1_10 |

| BT Device | IO Func | ALT | PAD |
|---|---|---|---|
| | usdhc2.DATA7 | 0 | GPIO_SD_B1_11 |
| FlexSPI | flexspi.B_DATA[3] | 1 | GPIO_SD_B1_00 |
| | flexspi.B_DATA[2] | 1 | GPIO_SD_B1_03 |
| | flexspi.B_DATA[1] | 1 | GPIO_SD_B1_04 |
| | flexspi.B_DATA[0] | 1 | GPIO_SD_B1_02 |
| | flexspi.B_SCLK | 1 | GPIO_SD_B1_01 |
| | flexspi.B_DQS | 6 | GPIO_SD_B0_05 |
| | flexspi.B_SS0_B | 6 | GPIO_SD_B0_04 |
| | flexspi.B_SS1_B | 6 | GPIO_SD_B0_01 |
| | flexspi.A_DQS | 1 | GPIO_SD_B1_05 |
| | flexspi.A_SS0_B | 1 | GPIO_SD_B1_11 |
| | flexspi.A_SS1_B | 6 | GPIO_SD_B0_00 |
| | flexspi.A_SCLK | 1 | GPIO_SD_B1_07 |
| | flexspi.A_DATA[0] | 1 | GPIO_SD_B1_08 |
| | flexspi.A_DATA[1] | 1 | GPIO_SD_B1_10 |
| | flexspi.A_DATA[2] | 1 | GPIO_SD_B1_09 |
| | flexspi.A_DATA[3] | 1 | GPIO_SD_B1_06 |
| FlexSPI 2nd Option | flexspi.A_DATA[3] | 1 | GPIO_AD_B1_00 |
| | flexspi.A_SCLK | 1 | GPIO_AD_B1_01 |
| | flexspi.A_DATA[0] | 1 | GPIO_AD_B1_02 |
| | flexspi.A_DATA[2] | 1 | GPIO_AD_B1_03 |
| | flexspi.A_DATA[1] | 1 | GPIO_AD_B1_04 |
| | flexspi.A_SS0_B | 1 | GPIO_AD_B1_05 |
| SEMC | semc.DQS | 0 | GPIO_EMC_28 |
| | semc.RDY | 0 | GPIO_EMC_41 |
| FlexSPI RESET | gpio1.IO[29] | 5 | GPIO_AD_B1_13 |

# 7 Layout recommendations

## 7.1 Stackup

A high-speed design requires a good stackup to have the right impedance for the critical traces.

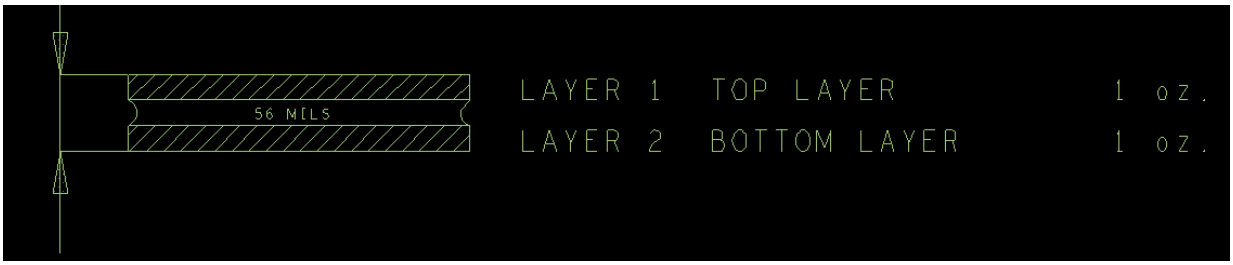


**Figure 5. RT1020-EVK stackup**

The constraints for the trace width depend on many factors, such as the board stackup and the associated dielectric and copper thickness, required impedance, and required current (for power traces). The stackup also determines the constraints for routing and spacing. Consider the following when designing the stackup and selecting the material for your board:

- The board stackup is critical for the high-speed signal quality.
- Preplan the impedance of the critical traces.
- The high-speed signals must have reference planes on adjacent layers to minimize crosstalk.
- The NXP reference design equals Isola FR4.
- The NXP validation boards equal Isola FR4.
- The recommended stackup is two layers, with the layer stack shown in Figure 5.

The left-hand image shows the detail provided by NXP inside the fabrication detail as a part of the Gerber files. The right-hand side shows the solution suggested by the PCB fabrication company for the requirements. Figure 4 shows the RT1020-EVK PCB stackup implementation:

| Layers | Single Ended | | Differential | | | Differential | | |
|---|---|---|---|---|---|---|---|---|
| | Trace Width (Mils) | Impedance (Ohms) | Trace Width (Mils) | Trace Spacing "Airgap" (Mils) | Impedance (Ohms) | Trace Width (Mils) | Trace Spacing "Airgap" (Mils) | Impedance (Ohms) |
| L1 | 5.00 | 50 | 4.2 | 6.00 | 100 | 4.70 | 5.00 | 90 |
| L2 | 5.00 | 50 | | | | 4.70 | 5.00 | 90 |

**Figure 6. RT1020-EVK stackup implementation**

## 7.2 Placement of bulk and decoupling capacitors

Place the small decoupling capacitors and the larger bulk capacitors on the bottom side of the CPU. The 0402 decoupling capacitors and the 0603 bulk capacitors must be placed as close as possible to the power balls. Placing the decoupling capacitors close to the power pins is critical to minimize inductance and ensure the high-speed transient current demand of the processor. The correct via size, trace width, and trace space are critical to preserve the adequate routing space. The recommended geometry is as follows:

- The via type is 18/8 mils, the trace width is 5 mils, and the trace space is 7 mils.
- Use the NXP design strategy for power and decoupling.

## 7.3 FlexSPI

FlexSPI is a flexible SPI (Serial Peripheral Interface) host controller which supports two SPI channels and up to 4 external devices. Each channel supports Single/Dual/Quad/ Octal mode data transfer (1/2/4/8 bidirectional data lines). FlexSPI is the most commonly used external memory.

Refer to section FlexSPI parameters from the datasheet, there are several sources for the internal sample clock for FlexSPI read data:
• Dummy read strobe generated by FlexSPI controller and looped back internally (FlexSPIn_MCR0[RXCLKSRC] = 0x0)

• Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad (FlexSPIn_MCR0[RXCLKSRC] = 0x1)

• Read strobe provided by memory device and input from DQS pad (FlexSPIn_MCR0[RXCLKSRC] = 0x3)

So for QSPI Flash without a DQS provided by the memory, only the option of FlexSPIn_MCR0[RXCLKSRC] = 0x1 can achieve 133 MHz SDR R/W speed, and FlexSPI_DQS pin should be left floating.

For Octal Flash where a DQS signal is provided by the memory,but as RT1020 mainly used 3.3 V supply and Octal Flash is supporting 1.8V only, so this option is not used.

## 7.4 SDRAM

The SDRAM interface (running at up to 133 MHz) is one of the critical interfaces for the chip routing. Ideally, route all signals at the same length as the EVK board. See the RT1020-EVK layout to route all signals at the same length (±50 mils).

The SDRAM routing must be separated into two groups: data and address/control. See the EVK layout to separate all SDRAM signals into two groups:

- All data lines and DM[x]
- All address lines and control lines

**NOTE**

i.MX RT1020, the SDRAMs that SEMC can support need at least 9 column address lines.

The RT1020-EVK is a two-layer board design and does not have reference plane to control impedance to accurate 50 ohms. Thus, it is recommended to put a serial resistor to all the signal lines in case there is a need to adjust impedance.

## 7.5 USB

Use these recommendations for the USB:

- Route the high-speed clocks and the DP and DM differential pair firstly.
- Route the DP and DM signals on the top (or bottom) layer of the board.
- The trace width and spacing of the DP and DM signals must meet the differential impedance requirement of 90 Ω.
- Route the traces over the continuous planes (power and ground):
  - They must not pass over any power/GND plane slots or anti-etch.
  - When placing the connectors, make sure that the ground plane clear-outs around each pin have ground continuity between all pins.
- Maintain the parallelism (skew-matched) between DP and DM, and match the overall differential length difference to less than 5 mils.
- Maintain the symmetric routing for each differential pair.
- Do not route the DP and DM traces under the oscillators or parallel to the clock traces (and/or data buses).
- Minimize the lengths of the high-speed signals that run parallel to the DP and DM pair.
- Keep the DP and DM traces as short as possible.
- Route the DP and DM signals with a minimum number of corners. Use 45-degree turns instead of 90-degree turns.
- Avoid layer changes (vias) on the DP and DM signals. Do not create stubs or branches.
- Provide the ground return vias within a 50-mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
- When the USB signals are not used, it is recommended that not to connect USB_OTG1_CHD_B, USB_OTG1_DN, USB_OTG1_DP, USB_OTG1_VBUS, USB_OTG2_DN, USB_OTG2_DP, USB_OTG2_VBUS pads.

## 7.6 High-speed signal routing recommendations

The following list provides recommendations for routing the traces for high-speed signals. Note that the propagation delay and the impedance control must match to have a correct communication with the devices.

- The high-speed signals (SDRAM, USB, SD card) must not cross gaps in the reference plane.
- Avoid creating slots, voids, and splits in the reference planes. Review the via voids to ensure that they do not create splits (space out vias).
- Provide the ground return vias within a 100-mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
- A solid GND plane must be directly under the crystal-associated components, and traces.
- The clocks or strobes that are on the same layer need at least 2.5× spacing from the adjacent traces (2.5× height from the reference plane) to reduce crosstalk.
- Provide the ground return vias within a 100-mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
- All synchronous modules must have the bus length matching and relative clock length control.
- For the SD module interfaces:
  - Match the data, clock, and CMD trace lengths (length delta depends on the bus rates).
  - Follow similar SDRAM rules for data, address, and control as for the SD module interfaces.

# 8 Two layer board design

## 8.1 MCU pinout

From design phase, RT1020 pinout was adjusted properly to meet two-layer board design especially for some high-speed signals. For example, signals like SDRAM, SDHC, ENET need to route at same length and don't across with each other, see Figure 7. RT1020-EVK SDRAM signals and Figure 7. RT1020-EVK USB signals for reference.

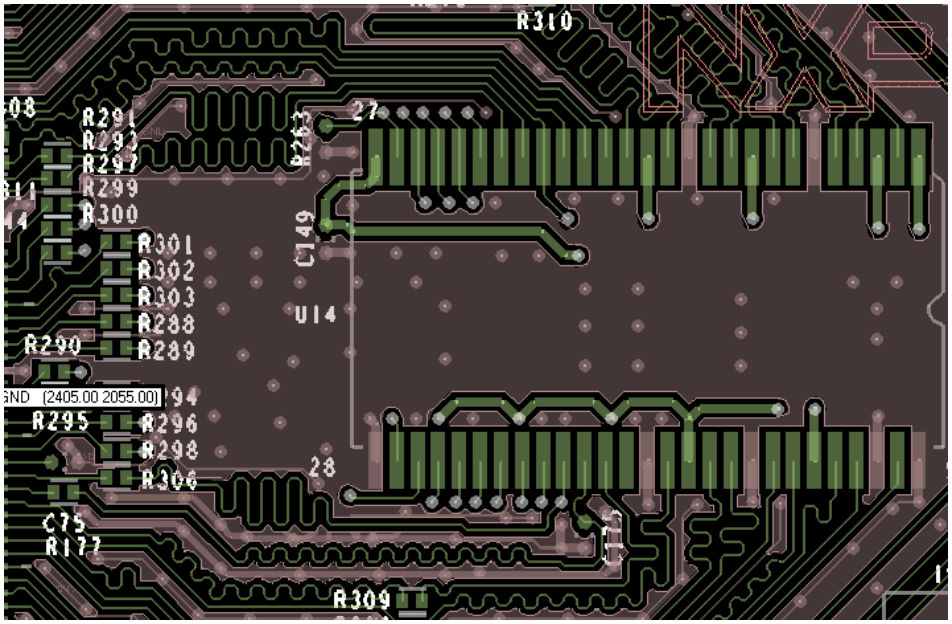


**Figure 7. RT1020-EVK SDRAM signals**

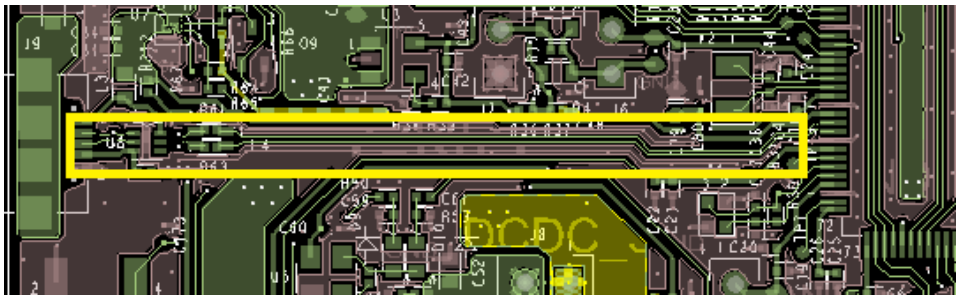

**Figure 8. RT1020-EVK USB signals**

## 8.2 Power supply

RT1020 power supply is designed with two-layer board, almost each power domain will have GND pad in parallel, please see Figure 7. RT1020-EVK MCU power pin for reference. With such power pin

design, it is easier for placing decoupling capacitor to the board.

At the same time, it needs to keep the bottom layer of MCU to have a somehow overall GND plane and make sure the board has a good current loop to the external power supply to improve the EMC performance, please see Figure 9. RT1020-EVK GND plane for reference.

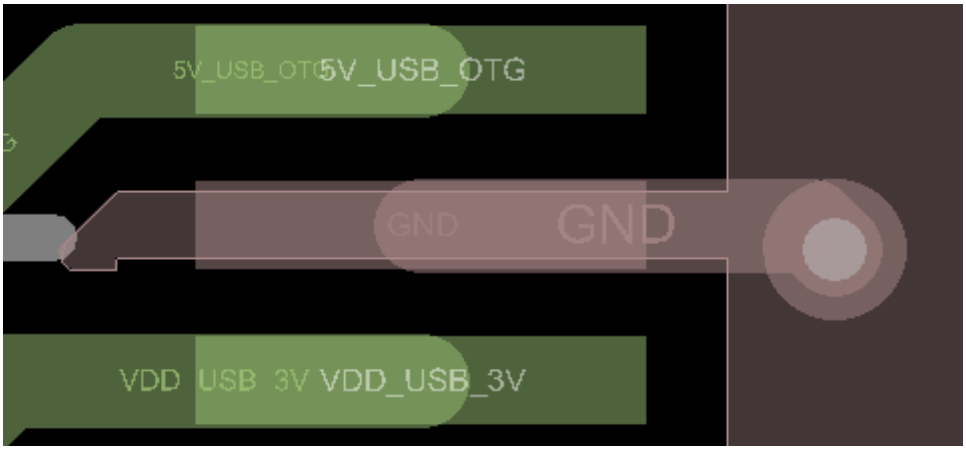


**Figure 9. RT1020-EVK MCU power**

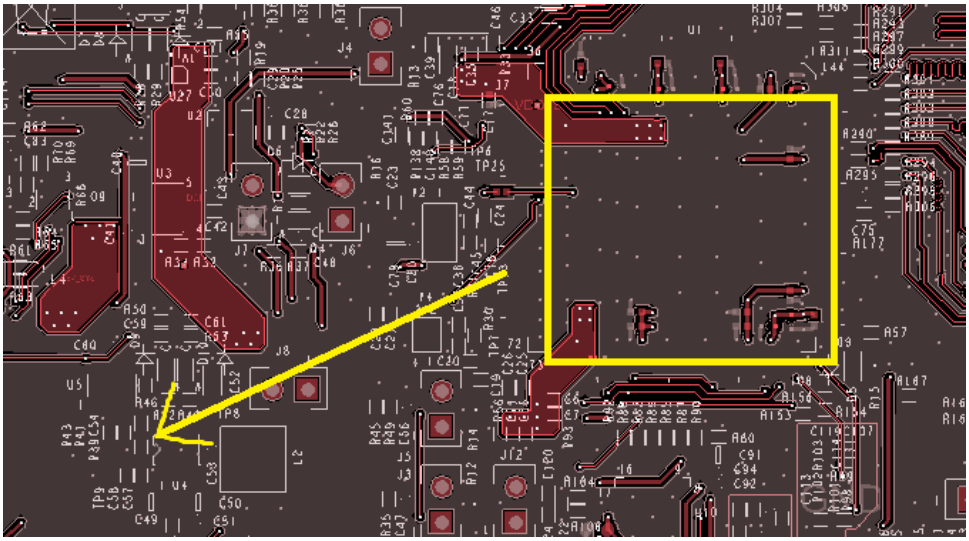

**Figure 10. RT1020-EVK GND plane**

## 8.3 Routing rule

There are some general high-speed layout guideline which mentioned above. For two-layer board design, it's better to have each high-speed signals with GND in parallel which will help impedance matching and improve the signal quality, see Figure 10. RT1020-EVK high speed signals for reference.

For two-layer board design, please make sure that at least one layer has a good GND plane (normally bottom layer), which means need to route most of the signals at the top layer, see Figure 11. RT1020-EVK bottom layer for reference.

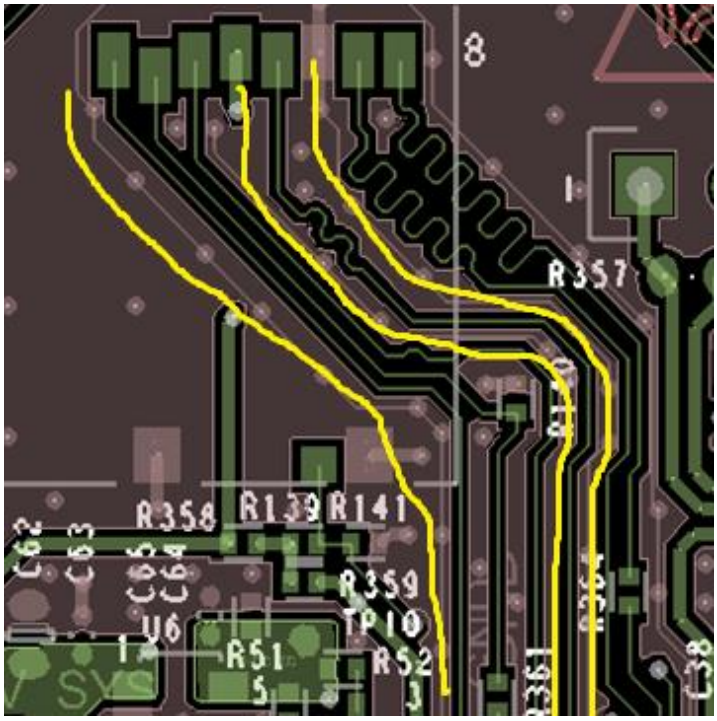


**Figure 11. RT1020-EVK high speed signals**

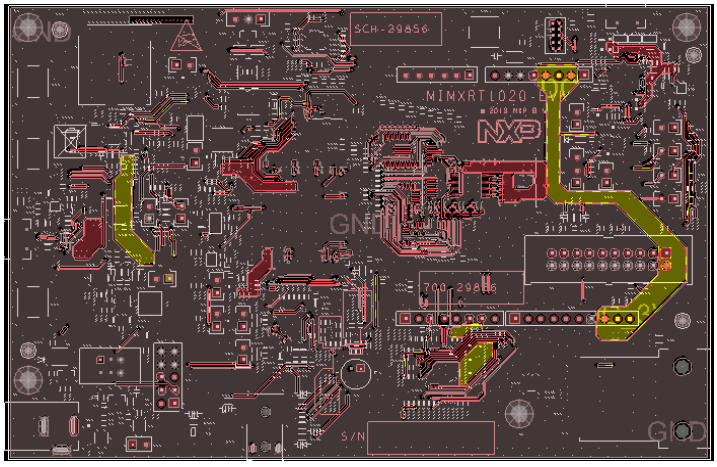

**Figure 12. RT1020-EVK bottom layer**

## 8.4 Special notes

Pay special attention to SDRAM drive signals, as there are more than thirty drive signals it must keep one GND line parallelly to each four signals.

To balance 133MHz R/W speed and board EMC performance, the SDRAM drive strength is lowered to DSR level 3 in the software.

For RT1020 SEMC module to support SDRAM, SEMC_DQS pin(GPIO_EMC_28) is kept floating to achieve high-speed access.

For RT1020 FlexSPI module to support QSPI flash, FlexSPI_DQS pin(GPIO_SD_B1_05) is kept floating to achieve high-speed access.

# 9 Revision history

Table 12 summarizes the changes done to this document since the initial release.

**Table 12. Revision history**

| Revision number | Date | Substantive changes |
|---|---|---|
| 0 | 5/2018 | Initial release |
| 1 | 1/2019 | Updated the special notes section. |
| 2 | 2/2019 | Updated on-chip termination values in Table 5. Debugging and programming |
| 3 | 08/2019 | Updated section 3,5,6, 7 and Table 4 |

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