AN12549

PN5190 antenna design guide

Rev. 1.1 — 23 April 2021 Application note
562211 COMPANY PUBLIC

Document information

Information	Content
Keywords	PN5190, NFC antenna design, NFC antenna tuning
Abstract	This document describes the NFC antenna design and tuning related to the PN5190. This includes the Dynamic Power Control 2.0 functionality. It gives some layout recommendations as well some guidelines, how to adjust (“calibrate”) the DPC.

Revision history

Revision history

Rev	Date	Description
1.1.	20210423	Section 3.4 "Layout recommendation for HVQFN" added
1.0	20210120	First official released version

1 Introduction

The antenna design for the PN5190 is not much different than the antenna design for most of the other NXP reader ICs in general. However, some PN5190 specific details need to be considered to get an optimum performance.

This document describes the generic NFC and RFID antenna design as simple as possible, focusing on the requirements for EMVCo POS design.

1.1 Dynamic Power Control 2.0

The Dynamic Power Control (DPC 2.0) feature of the PN5190 allows an improved antenna design with improved transfer function. It is required to configure (“calibrate”) the DPC properly to get the optimum performance.

The NFC Cockpit (PN5190 GUI) supports the process of the DPC calibration, which includes the adjustment of the basic settings, the step by step calibration itself and the PCD TX shaping. The steps to calibrate the DPC and optimize the PN5190 registers are described in Section 5.

Note: *A wrong antenna tuning or a bad DPC calibration might drive a too strong HF field and even might destroy the PN5190.*

1.2 Prerequisites

Then NFC antenna design requires a basic understanding of analog electronic design. The tuning procedure is quite simple and explained in detail, and therefore does not require any specific RF know-how.

The NFC antenna itself is a part of an RF transformer rather than an only typical RF antenna. Therefore some typical antenna definitions do not apply for NFC antennas:

The NFC antenna changes its impedance during normal operation and therefore a 50 Ω design does not make sense at all.

However, the NFC Reader is an RF device as such, where on one hand power level of up to 2 W are driven, and in the other hand the receiver circuit needs to detect data signals in the mV range. That requires a careful design, especially for the layout.

The environment is part of the antenna design. Especially metal design has a huge influence on the antenna behavior and so on the NFC performance. Without the environment design, no antenna design can be done. That means, the mechanical frame conditions need to be known and considered. The housing and mounting places has a huge influence on the overall performance.

Note: *The use of a Vector Network Analyzer (VNA) is required for a proper antenna tuning.*

2 NFC reader antenna design

For the NFC operation three different communication modes are specified in [4]:

1. In the **card emulation mode (CM)** the NFC device can be used in (existing) NFC reader infrastructure. In the CM the NFC device behaves in principle like a PICC, as defined in [2]. This mode is optional.
2. In the **card reader mode (RM)** the NFC device can be used with (existing) NFC cards. In the RM the NFC device behaves in principle like a PCD, as defined in [2]. This mode is mandatory.
3. In the **peer to peer mode (P2P)** the NFC device can communicate to other NFC devices, either being the initiator, starting the communication, or being the target, answering the communication.

For the communication between two NFC devices the two different P2P modes are available:

1. **Active P2P**: Both NFC devices, the initiator as well as the target, are required to generate their own magnetic field, when sending data. This mode is optional.
2. **Passive P2P**: The initiator always generates the magnetic field, while the target uses the load modulation principle to send its data. This mode is mandatory.

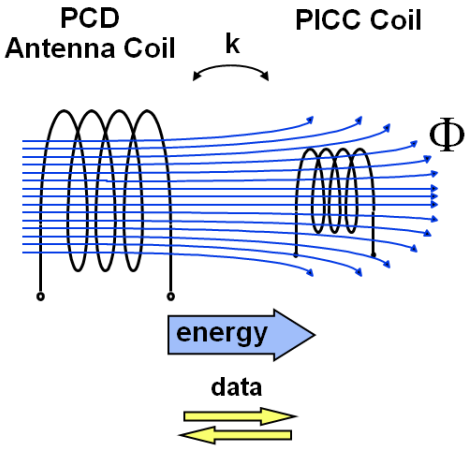
2.1 ISO/IEC 14443 specifics

The ISO/IEC 14443 (called “ISO” in the following, details see [2]) specifies the contactless interface as widely being used with contactless smartcards like e.g. MIFARE product-based cards.

The ISO/IEC 14443 defines the communication between a reader (“proximity coupling device” = PCD) and a contactless smart card (“proximity chip card” = PICC). In four parts, it describes the physical characteristics (i.e. the size of the PICC antennas), the analog parameters like e.g. modulation and coding schemes, the card activation sequences (“Anticollision”) and the digital protocol. The ISO/IEC 10373-6 (see [3]) describes as well the test setup as well as all the related tests for cards and the reader.

The ISO/IEC 14443 reader antenna consists of an antenna coil, which is matched to the reader IC. This antenna coil, as shown in Figure 1,

1. generates the magnetic field to provide the power to operate a card (PICC),
2. transmits the data from the reader (PCD) to the card (PICC), and receives the data from the card (PICC) to the reader (PCD).

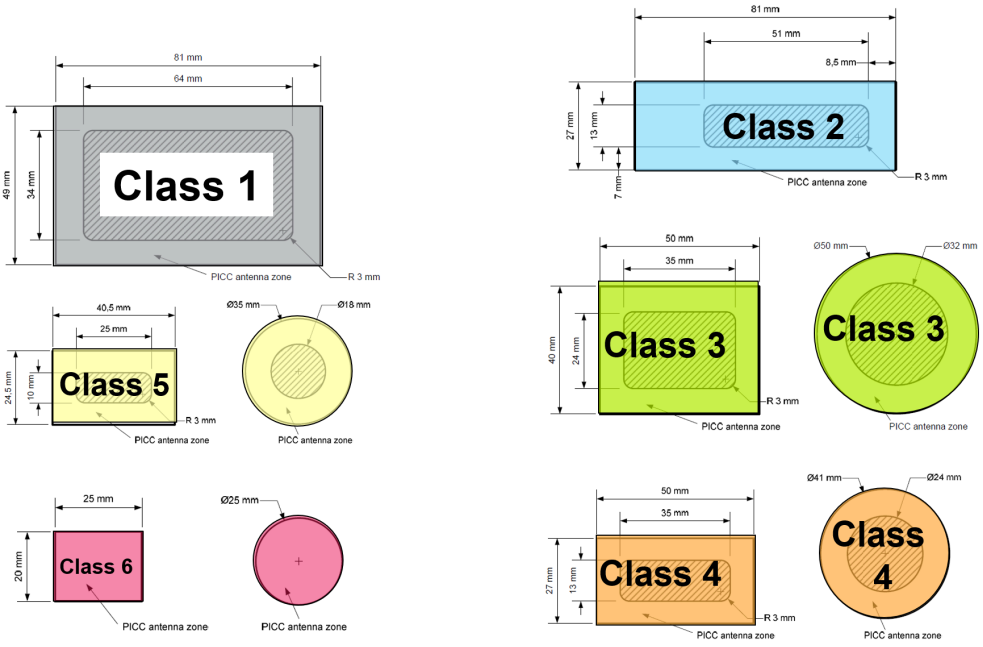


1. k = coupling coefficient
2. Φ = magnetic flux

Figure 1. Magnetic coupling between reader (PCD) and card (PICC)

According to the ISO/IEC 14443 the PICC antenna coils can be categorized into the classes 1 …6, as shown in Figure 2.

The PCD antenna is not defined as such, but the PCD must support the classes 1, 2, and 3. The support of the classes 4, 5, and 6 is optional.



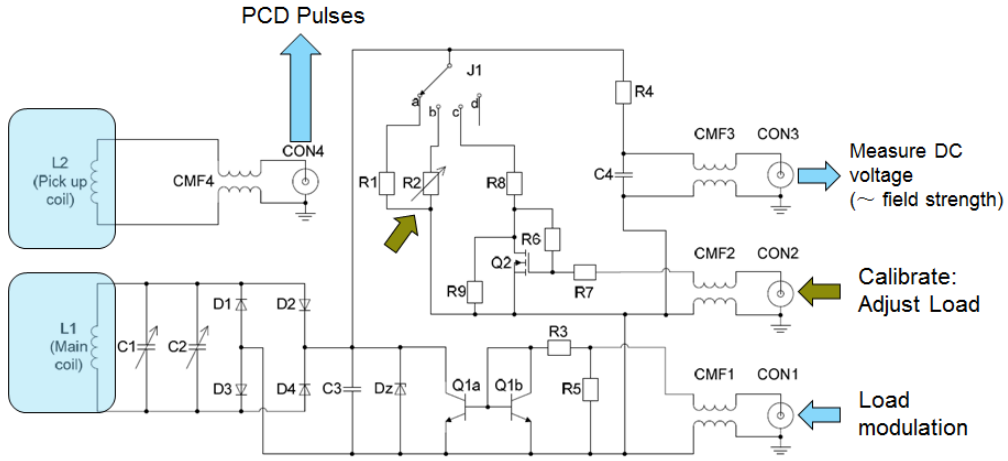
1. A PCD must always support the classes 1, 2, and 3. The Classes 4, 5 and 6 are optional.

Figure 2. PICC Classes according to the ISO/IEC 14443

The PCD antenna coil sizes are not specified. So for ISO/IEC 14443 compliant readers all different sizes of antenna coils from a few 10 mm^2 up to 20 cm diameter can be found in various shapes.

The ISO/IEC 14443 does not specify an operating volume. The reader manufacturer needs to guarantee that within the operating volume - that they themselves define - all related ISO/IEC 10373-6 tests can be passed.

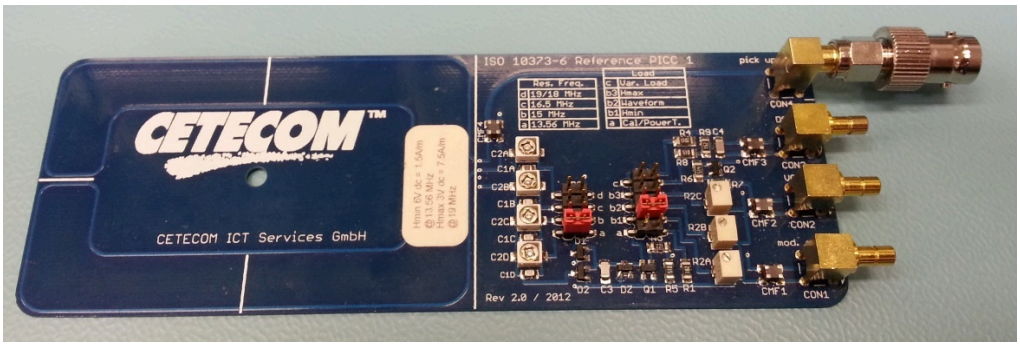
The compliance tests require calibrated ReferencePICCs, as defined in ISO/IEC10373-6. The schematic of such ReferencePICC is shown in Figure 3. For each PICC Class there is one Reference PICC, which needs to be calibrated according to the required measurement. Practically it makes sense to use one calibrated ReferencePICC for each measurement case.



1. Details see [3].

Figure 3. Schematics of the ISO/IEC 10373-6 ReferencePICC

Some ReferencePICCs, which are commercially available (e.g. Figure 4), are pre-calibrated and equipped with several jumper options to address the most relevant tests with a single ReferencePICC.



1. The jumper settings allow the use of different pre-calibration settings.

Figure 4. ISO/IEC 10373-6 Reference PICC Class 1

Still for each PICC Class a separated ReferencePICC is required.

The **most** relevant analog tests for PCDs are:

1. Field strength test (min and max)
2. Wave shape tests (for all bit rates)
3. Load modulation amplitude tests

Note: *This application note does not replace the detailed test description in the ISO/IEC 10373-6.*

There is no common certification process for ISO/IEC14443 compliance in place, even though many national bodies use the ISO/IEC 14443 to operate the electronic passports and electronic ID cards. For these programs, some nations have established a certification process to guarantee interoperability. An example is given in [5].

2.1.1 Field strength

For the field strength test it is preferred to have the PCD send a continuous carrier, i.e. it performs no modulation.

The field strength tests simply require the calibrated ReferencePICC and a DC voltage measurement device (volt meter or oscilloscope). The field strength is equivalent to the calibrated (and required) voltage level. The ISO/IEC 10373-6 defines minimum voltage levels, corresponding to the minimum required field strength, and maximum voltage levels, corresponding to the maximum allowed field strength. The measured voltage levels must stay in between these limits.

2.1.2 Wave shapes

The PCD needs to send the related pulse(s): It may send an ISO/IEC 14443 REQA and / or REQB with the required bit rate, as e.g. specified in [5]. Any other command fits the purpose, too.

The standard way of activating higher bitrates is not very useful for the wave shape test, since the ReferencePICC for ISO/IEC 14443-2 tests does not allow the protocol layer, which is normally required to switch to higher bit rates.

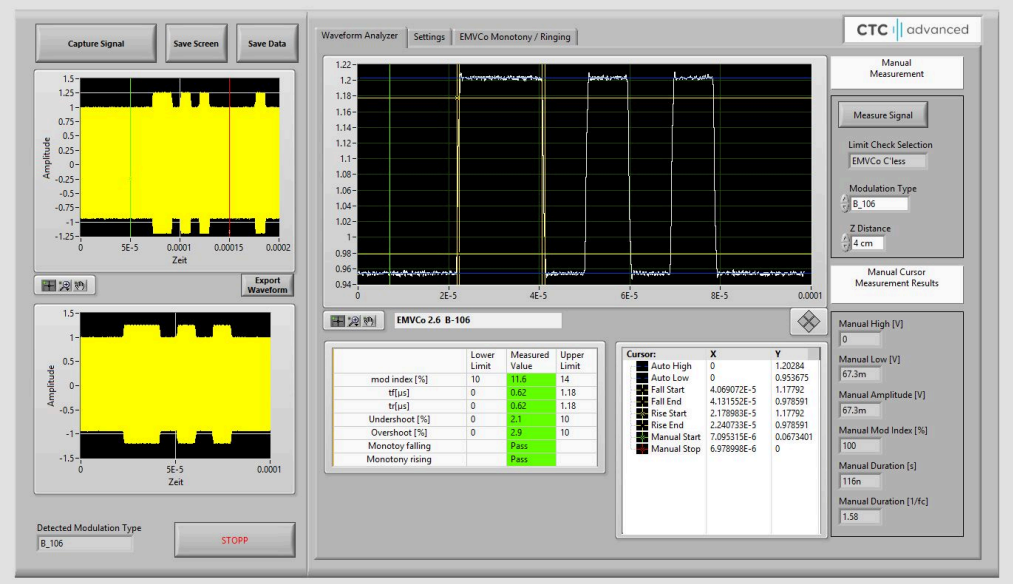
Note: *For the test of higher bit rates, it makes sense to implement some specific test commands, which send artificial commands, e.g. REQA and / or REQB, using the coding and modulation of the corresponding higher bit rates. This feature is provided via the NFC Cockpit, where the REQA or REQB polling can be done with any of the supported data rates. This allows to easily test the analog performance as such, ignoring the high-level features, which are required to activate the protocol layer.*

The wave shape tests require

1. A calibrated ReferencePICC, which is placed at the position of the calibrated field strength (corresponding to the DC voltage as measured in Section 2.1.1),
2. A digital oscilloscope with a measurement bandwidth of 500Msamples or higher, and
3. A tool that filters and transforms the oscilloscope data into the envelope signal according to the ISO/IEC 10373-6.

The tool normally returns the filtered and transformed envelop as well as the corresponding values of rise and fall times, residual carrier levels and over- and undershoots, which must be kept within the given limits.

An easy to use tool for such tests can be the CTC Advanced WaveChecker, as shown in Figure 5.



1. Example of EMVCo type B signal

Figure 5. CTC Advanced WaveChecker

2.1.3 Load modulation

The PCD needs to send a test command, which allows to check a response from the ReferencePICC. The response from ReferencePICC then needs to be properly received by the NFC Reader.

The load modulation tests require

1. A calibrated ReferencePICC, which is placed at the position of the calibrated field strength (corresponding to the DC voltage as measured in Section 2.1.1),
2. A signal generator with a pattern generator (Arbitrary Wave Generator, AWG), that provides the load modulation input signal as a response to the PCD test commands.

The response must be triggered by the PCD test command, i.e. the signal generator needs a delayed trigger input either from the field or from the PCD itself. The voltage level of the load modulation input signal for each test case must be (pre-) calibrated in the TestPCD set up.

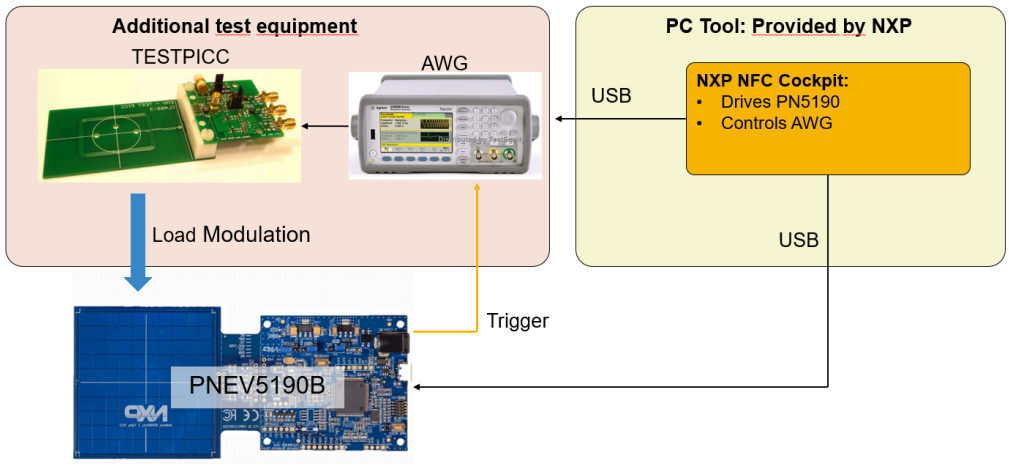
The PCD must be able to receive all the responses with the given minimum load modulation signal level. The Figure 6 shows a minimum required setup to test and optimize the load modulation performance of the PN5190 NFC Reader. The NFC Cockpit controls the PN5190 in the PNEV5190B (or in any customer design).

The AWG (Keysight 33511B with arbitrary license) can easily be controlled by:

1. The **NXP NFC Cockpit**: this feature is provided by the NXP NFC Cockpit, if the AWG support is selected during the installation of the NFC Cockpit. However, there is no direct information available about the required LMA level, since there is no calibration procedure available.
2. The **CTC Advanced WavePlayer** (see [15]): this PC tool is provided by CTC Advanced. It is available in combination with calibration data for ISO ReferencePICCs and EMVCo TestPICCs. This allows an accurate ISO and EMVCo Pretest.

The AWG needs to be triggered to send the “card response”. This trigger can be derived in different ways:

1. From a sniffer device, which traces the PCD commands, e.g. the FIME Smartspy Contactless (see [14]).
2. From a trigger output of an oscilloscope, which triggers itself by the sent waveshapes. Those waveshapes (RF trace) can be traced with a simple pickup coil.
3. From a PN5190 test signal, which indicates that the command has been sent (e.g. falling edge of TxActive).



1. The NFC Cockpit supports the Keysight 33511B series (see [13]), if the arbitrary function is enabled.

Figure 6. Minimum test setup for LMA tests

2.2 EMVCo specifics

EMVCo specifies a contactless interface for point of sales (POS) terminals (= PCD) and the corresponding contactless payment cards (= PICC) in [6]. This interface is very similar to the one defined ISO/IEC 14443, but it uses its own set of requirements and specification details. Especially the EMVCo test equipment and way of testing is quite different from the test specification as defined in ISO/IEC 10373-6.

On one hand EMVCo specifies and requires only the bit rate of 106 kbit/s for both type A and B, but no higher bit rates, which simplifies the design in principle.

On the other hand EMVCo specifies an operating volume as well as intensive analog and digital tests. For those tests the SW implementation of a certain test transaction is required (“EMVCo Loopback”).

The advantage of this way of testing is that the test parameters can be tested “from the outside”, i.e. it is not required to access the POS terminal itself to check whether or not the POS as properly received the card response.

The disadvantage of such a test is that a multiple set of parameters must be ok to pass the test. The test fails, if only a single parameter fails. This makes debugging extremely complex, and a parameter optimization is impossible.

Example: the LMA test fails, if e.g. the EMD handling is not implemented properly or if the wave shapes are not good enough.

2.2.1 EMVCo analog test with version 3.0

With the introduction of the version 3.0 of EMVCo Contactless specification, the test effort has increased a lot. For the reader tests three calibrated EMVCo TestPICCs are required. These EMVCo TestPICCs can be bought only from one of the accredited laboratories.

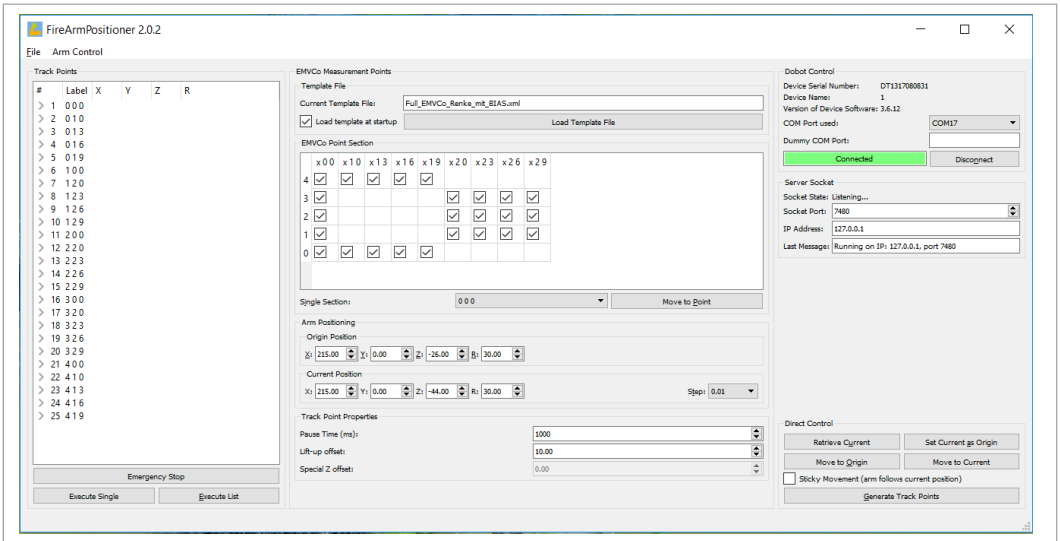
The relevant analog tests for PCDs in principle are:

1. PCD power test (field strength)
2. Modulation PCD-> PICC tests (wave shape tests)
3. Load modulation tests (PICC -> PCD tests)

Note: *This application note does not replace the detailed test description in the EMVCo specification.*

The EMVCo version 3.0 adds a number of tests. This does not change the design in principle, but increases the effort, especially the test effort. For the debugging and optimization of parameters it is recommended to use a robot to cover the operating volume.

NXP provides a simple PC tool (FireArmPositioner, see [16]), which allows the control of a low-cost robot to step through the defined positions of the EMVCo operating volume. It requires the Dobot Magician and a homemade fixture to fix the EMVCo TESTPICCs to robot arm.

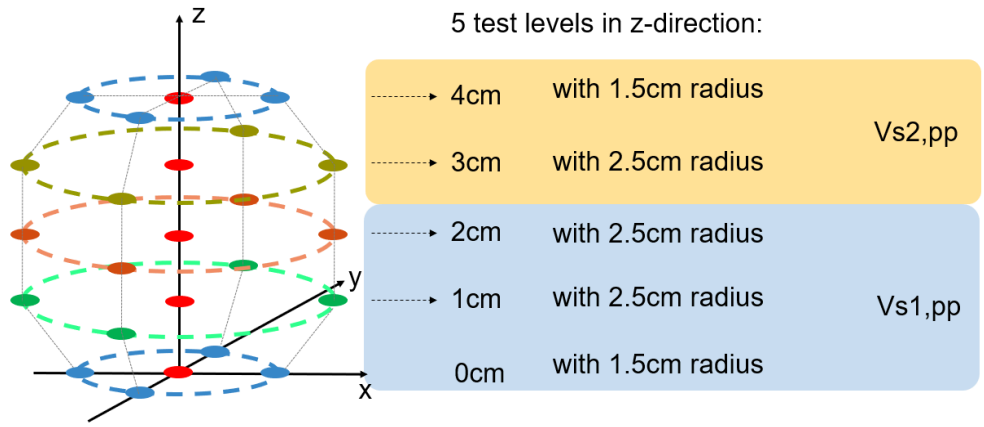


1. This tool controls the Dobot Magician (see [16])

Figure 7. NXP FireArmPositioner

2.2.2 EMVCo operating volume

One main difference for the tests between ISO/IEC and EMVCo is the definition of an operating volume, as shown in Figure 8. This volume is tested with the EMVCo TestPICCs.



1. 25 positions in total: position 000 is defined by the landing zone
2. Details see [6]

Figure 8. EMVCo POS operating volume requirement

Within this volume, the given parameters must be fulfilled.

It helps to use a robot to position the TestPICCs in any of the defined 25 positions.

2.2.3 EMVCo field strength (= “power transfer”)

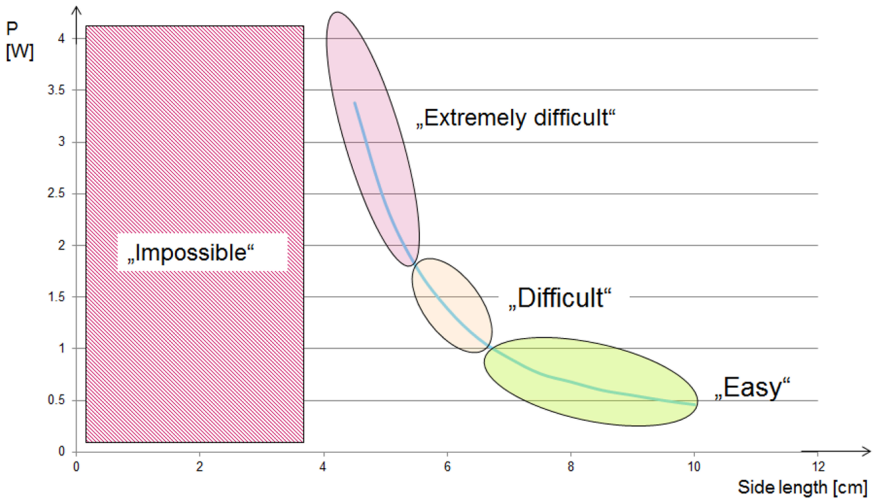
For the manual field strength test, it is preferred to have the PCD send a continuous carrier, i.e. it performs no modulation.

The voltage level which can be measured in all of the given positions with all three TestPICCs needs to be between the minimum and maximum limit, as given in [6].

Due to the operating volume, it can become challenging to meet the EMVCo requirements with small antennas.

The Figure 9 shows the required power versus antenna size. The curve is based on an antenna simulation, which uses a few simplifications, so it does not take the loading effect of the EMVCo TestPICCs into account. On the other hand the simulation was done under ideal environmental conditions, i.e. no metal environment influences the antenna. The simulation results can be taken as reference to estimate the design effort especially for small antennas compared to “normal” antenna sizes.

Note: *The PN5190 allows a more flexible antenna design, since it drives more power into the antenna than other NFC Reader ICs, while at the same time the DPC 2.0 controls the power transfer as well as the TxShaping at closer distances. However, even the PN5190 cannot overcome the physical limitations. Especially the Interoperability tests reveal the gaps of the compliance tests, when test cards with small half size antennas are tested. In such cases, and of the POS antenna is small, the coupling in some of the operating volume positions can be (close to) zero, and then no communication is possible.*



1. Simulation of a square antenna
2. These simulation results do neither take any specific environment nor loading effects into account.

Figure 9. EMVCo POS Reader Antenna size

2.2.4 EMVCo wave shapes

The PCD needs to send the related pulse(s): It may send an EMVCo WUPA and / or WUPB (or standard REQA / REQB).

The wave shape tests require

1. Three calibrated EMVCo TestPICCs, which are placed at each of the given position (see [6]),
2. A digital oscilloscope with a measurement bandwidth of 500Msamples or higher, and
3. A tool that filters and transforms the oscilloscope data into the envelope signal according to the EMVCo test requirement.

The tool normally returns the filtered and transformed envelop as well as the corresponding values of rise and fall times, residual carrier levels and over- and undershoots, which must be kept within the given limits. An easy solution is the CTC Advanced WaveChecker (see [12]).

Note: *In some positions, the signal level, as picked up by the defined Pick-Up coil, might be very low, sometimes in the range of 10 mV (= noise level). This can happen, even though the power transfer indicates enough field in the position of the TESTPICC, especially, if the field distribution becomes inhomogeneous in that position, so the Pick-Up coil cannot work properly. In such a case the geometry of the POS antenna or at least the position of the landing zone needs to be changed, since the EMVCo test does not allow a pickup with external sniffer coil.*

2.2.5 EMVCo LMA

The PCD needs to send a test command, which allows to check the reception of a response from the TestPICC. In the official tests, the EMVCo loop back command sequence is used for this.

Note: *Since the official tests do not allow a useful debugging or optimization, simple tests commands are a lot more useful than the full EMVCo test sequence. Such a simple test command can be easily debugged and typically allows an easier triggering. The NFC Cockpit allows such simple tests, including the use of an Arbitrary Wave Generator (AWG) to drive the card response. The principle is described in* Section 2.1.3*. For EMVCo only calibrated EMVCo TESTPICCs need to be used instead of the ISO ReferencePICCs.*

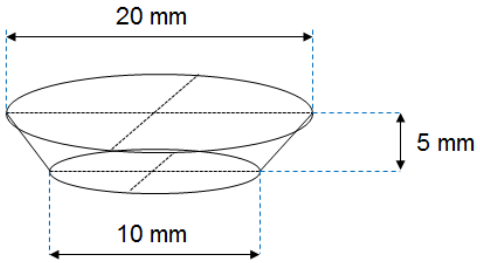
Note: *EMVCo tests "negative" and "positive" load modulation. The CTC Advanced WvePlayer tool allows to provide both signal forms according to the EMVCo specification, but the AWG support of the NFC Cockpit does not. Technically the PN5190 does not make any difference between "negative" and "positive" load modulation, so basically it is good enough to test either one. However, due to a bad saturation and heating effect of the TESTPICC the "negative" load modulation can only be applied for a very short period of time, which requires the test tool to switch the load before and after the response. This load switch causes EMD events, which need to be handled by the PCD, before these tests can be applied.*

2.3 NFC specifics

The standard NFC device needs to fulfill the reader mode (PCD), the passive target and the passive initiator. The passive target from an antenna point of view is very similar to the optional card mode (PICC).

2.3.1 NFC operating volume

The NFC Forum specifies an operating volume as shown in Figure 10. All specified parameters are tested at given test points within this volume. This is valid not only for reader mode tests, but all tests.



1. Details see NFC Analog Technical Specification, [4]

Figure 10. NFC operating volume

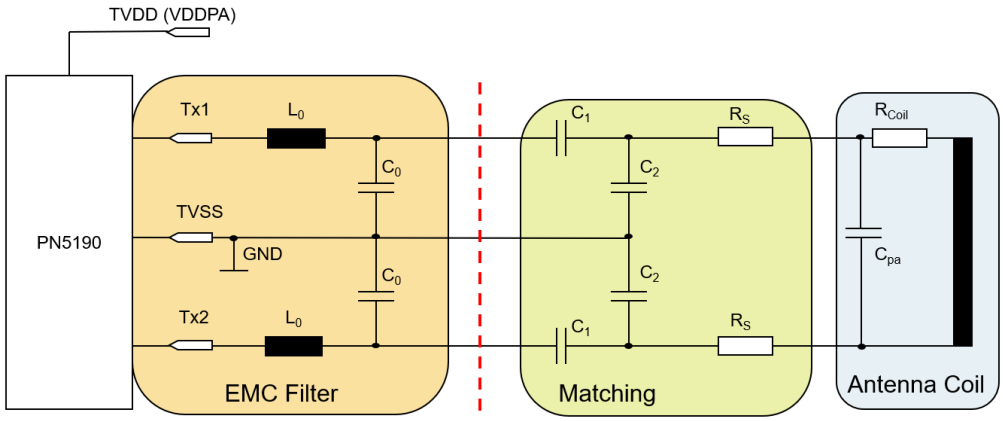
3 PN5190 antenna requirements

The PN5190 uses the NXP NFC standard antenna circuit, as well known with other NFC NXP reader ICs.

The PN5190 is optimized to support the NFC, ISO and EMVCo with a minimum of additional components. The PN5190 simply requires the antenna matching circuitry, some block capacitors and the crystal.

However, the calculation and tuning of the matching components as well as the setting adjustment need to be done carefully to provide the full performance as well as to meet CE and FCC regulations.

The design starts with the TX part, as shown in Figure 11.



1. The circuit is shown simplified.

Figure 11. TX part of the PN5190 antenna circuit

Note: *It makes sense to foresee two parallel footprints for each of the tuning capacitors. That allows to place two parallel capacitors instead of only a single one for better value adjustment.*

3.1 Start parameters

For the start of the antenna tuning procedure some start parameters needs to be defined. These values might be taken to start an antenna design, using the NXP NFC Antenna Tool, which can be downloaded from the NXP NFC Antenna Design Hub (refer to [11]).

3.1.1 Target impedance

The target impedance defines the current consumption and the field strength. The lower the target impedance, the higher the driver current ITVDD gets, and the more output power the PN5190 can drive.

The ITVDD limit of $ITVDD_{max}$ = 350 mA defines the minimum target impedance of

$$Z \approx 13 \ldots 14\Omega$$

An impedance of less than 20 Ω typically drives more than 200 mA. Normally the lowest possible target impedance is chosen to get the maximum possible output power, especially since the DPC 2.0 can control and limit the output power per setting.

However, the control range of the DPC 2.0 is limited from TVDD = 1.5 … 5.7V. It can be shown that in some cases in close distances with a small antenna, the maximum allowed power transfer (field strength) is exceeded even with the lowest TVDD settings. In those case the target impedance needs to be increased.

If no other input is known, the recommended target impedance is

$$Z \approx 15 \ \ldots \ 17\Omega$$

3.1.2 Q factor

The Q- factor in principle defines the bandwidth, which is available to transfer data. This definition includes the complete transfer channel, including the PICC or phone. The limits are normally specified via the wave shape requirements.

The final Q factor of the overall antenna setup depends on many frame conditions, such like environment or PICC loading, which are not fully known or even change during the operation or test. So it makes no sense to calculate and adjust the antenna based on a too precise value. The final Q must be tuned with the pulse shape measurements, if the antenna shall be fully optimized.

Reasonable values vary from 10 up to 30, and a typical starting value can be a number between 20 and 25.

Q = 22 might be taken, if no other input is known.

The higher the Q factor, the better the power transfer, but the lower the stability gets.

Note: *While ISO allows data rates of up 848 kbit/s, NFC allows the data rates of up to 424 kbit/s. EMVCo systems are limited to 106 kbit/s. So typically the Q of EMVCo reader systems can be higher than the Q of ISO or NFC reader systems.*

3.1.3 EMC filter cut-off frequency

The cut-off frequency of the EMC filter needs to be above the 13.56 MHz to pass enough energy, but clearly below 27.12 MHz to block the second harmonic.

The cut-off frequency defines the “symmetry” of the antenna. For “asymmetric” antenna tunings (like e.g. used for the CLRC663), the cut-off frequency is typically

$$f_{EMCasymmteric} \approx 16 \ldots 22MHz$$

For the PN5190 a “symmetric” antenna design is recommended, which requires a lower cut-off frequency:

$$f_{EMCPN5190} \approx 14.3 \ldots 14.6MHz$$

3.1.4 EMC filter inductor

The inductor L0 as part of the EMC filter is a key component in the overall antenna design. It defines the output power, the wave shapes and loading behavior as well as the radiation of unwanted harmonics.

Losses:

In general, the losses of L0 must be as low as possible.

Be aware that those losses are specified or measured under NFC operating conditions (at 13.56 MHz and the required power / current level)! Typically the specification of inductors use lower frequencies and lower power conditions.

Power rating:

Consider the NFC use case with high current. Under normal conditions, the L0 can heat up easily, especially if the L0 has higher losses.

Non-linearity:

Some of the high Q inductors use ferrite cores, which might go into saturation. This can easily cause a non-linear behavior, which limits the output power and / or disturbs the wave shapes.

Typically a lower inductance value provides lower losses, too. Since the PN5190 does not need to keep the correlation requirement (as known from PN5180), the inductance value can be quite low. Use L0 = 160 nH, if no other input is known.

Note: *It is recommended to foresee a footprint size of 0805 in such a way that both 0805 as well as 0603 components can be assembled. That gives the maximum flexibility for the final choice of L0.*

3.2 Comparison to PN5180 antenna design

In principle the antenna design for the PN5190 is the same as the one for the other NXP NFC reader ICs (like e.g. the PN5180). However, the PN5190 provides some new features, which need to be considered to get the best performance.

3.2.1 Power

The DPC 2.0 of the PN5190 directly measures the driver current, so no correlation requirement (as known from the PN5180 or PN7462) needs to be considered. That allows to use lower inductance values for L0, which decreases the losses.

The better EMC filter inductor in combination with the improved PN5190 TX driver design (lower losses + higher TVDD) and the increased driver current limit (from 250 mA to 350 mA) increases the output power quite a lot. So in many cases it makes sense to increase the antenna impedance to reduce the power as such.

At the same time, the control range has increased compared to PN5180: The PN5190 allows the full power control over the VDDPA from 5.7 V down to 1.5 V, if needed.

3.2.2 Wave shaping

The DPC 2.0 provides an easy to use TX shaping feature, which compensates ringing or damping effects under different loading conditions. This feature is similar to the know TX shaping feature of the PN5180, but a lot easier to adjust. The PN5190 TX shaping

allows the flexibility to create any shaping for the falling and the rising edge of the ASK modulation pulses, which might compensate any setup issues.

Some of the EMVCo tests can only be passed with the help of such a feature, if certain antenna forms are used.

3.2.3 Receiver performance

The PN5190 provides a complete new RX concept, compared to the known NFC reader ICs like e.g. the PN5180. With this concept the overall sensitivity, but even more important, the robustness against noise signals has been improved. The adjustment of RX settings has become less complex.

However, the external RX circuit stays as simple as it has been.

3.3 Layout recommendations for BGA

To provide a proper performance and still meet the regulations like CE, FCC or MIC, the basic analog design must be kept. The following section provides some hints, which parts of the design is most critical in terms of layout, and it gives proven recommendations.

Two main parts need to be considered: the RF and antenna circuit itself, and the power supply.

3.3.1 PN5190 BGA RF circuit recommendations

The following layout recommendations for the PN5190 can be given:

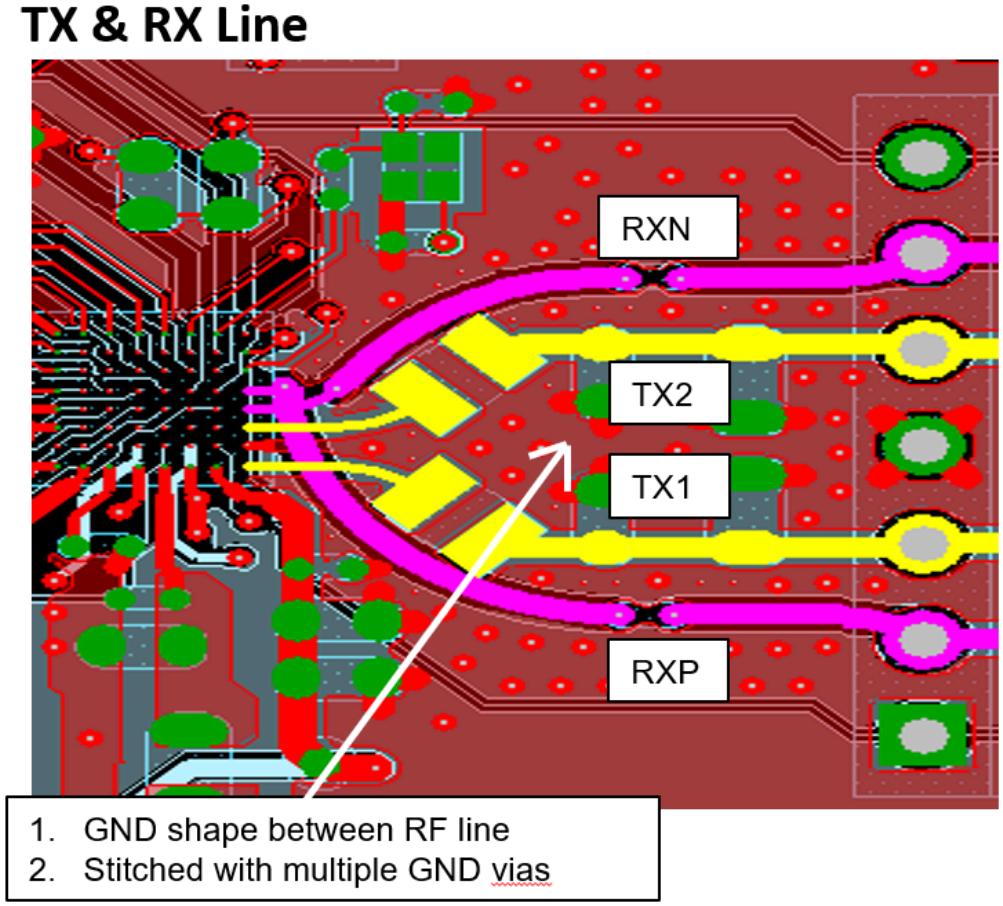
1. Place components as close to the IC as possible.
2. Place two closely placed inductors L0 either perpendicular to each other or in 45 degree angle.
3. Place the capacitor of RX line close to PN5190.
4. Place the inductor L0 very close to PN5190 to have shorter TX line.

For the routing, the following guide lines can be given:

1. Route TX line in Top Layer (due to huge current).
2. Route RX line in Top Layer (if possible) or route in Layer 3 (Internal signal Layer 1) depending on matching network & Antenna placement.
3. Do not use any via for TX Line.
4. Blind Via is used for the RX line.
5. Route with any angle routing. No 90 degree/45 degree or odd angle bends required.
6. RX & TX line must be routed with GND separation (avoid cross talking!).
7. Route TX line symmetrical to each other and route RX line symmetrical to each other.

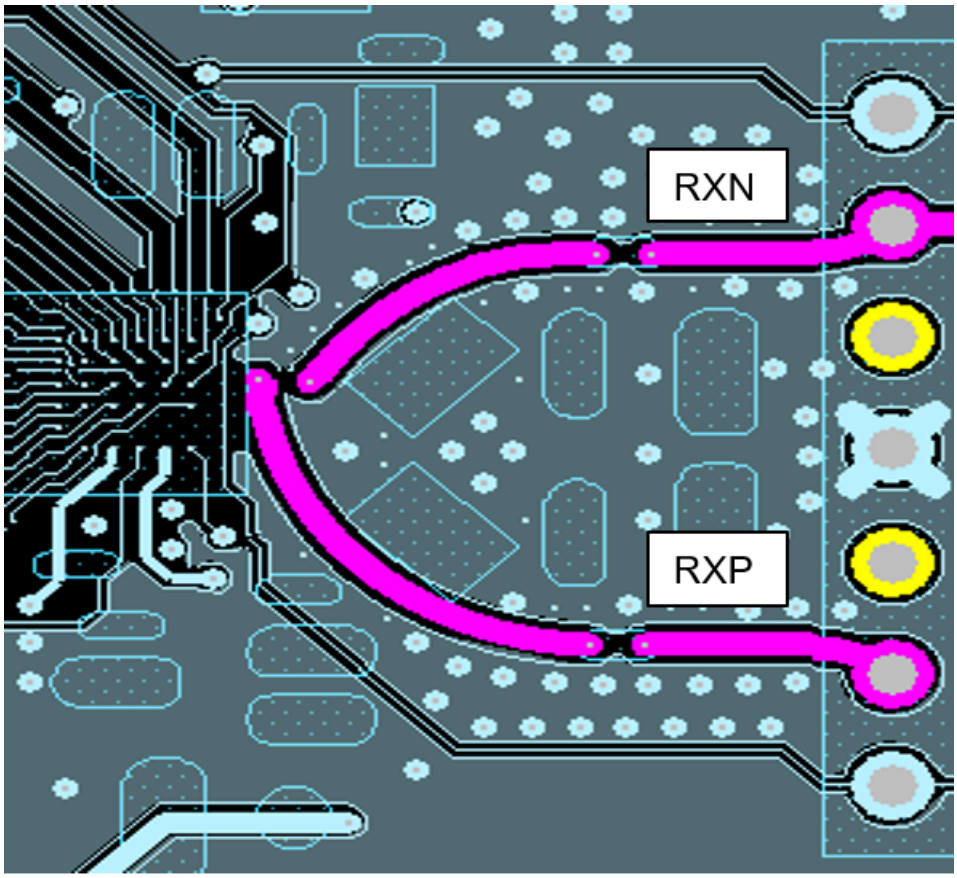
An important part of the layout is the GND layer (see Figure 13).

1. Provide solid GND plane on adjacent Layer (L2_GND).
2. Fill all layers with GND shape.
3. Stitch with multiple GND via around RF line.
4. No Test point allowed.
5. No silk label on RF traces.



1. Screenshot with multiple layers

Figure 12. PN5190 Layout Reference example



1. Part of the signal layer 1
2. Middle Layer = GND area and RX lines

Figure 13. PN5190 Layout Reference middle layer example

Consider a proper heat sink for the lossy components like EMC filter inductors and damping resistors, as well as for the PN5190 itself.

3.3.2 PN5190 BGA power supply circuit recommendation

Next to the RF and antenna design, the power supply is important for a proper functionality and performance. Especially for the DC/DC-Converter the layout needs to be carefully designed.

The PN5190 is optimized to support the EMVCo operating volume with 3.3 V input supply. Therefore the TX output can drive up to ITVDD = 350 mA. Based on a power supply voltage VDDPA = TVDD = 5.7 V that means a possible total power consumption for the total antenna circuit of up to $P_{tot} \approx 2$ W.

The following guidelines are optimized for the standard use case, using the DC-DC for the VUP supply.

In that combination, the overall mean input current consumption at a supply voltage of 3.3 V can easily be up to 800 mA or higher. The rush in current can be even much higher.

VBATPWR, VDDBOOST, BOOST_LX

1. Place components as close as possible
2. Route VBATPWR, BOOSTLX, VDDBOOST as short as possible

3. Provide Cu shape. If shape is not possible, then route with wide trace (150mils)
4. No vias allowed
5. BOOST_LX is noisy source, so sensitive signals should be far away from this net

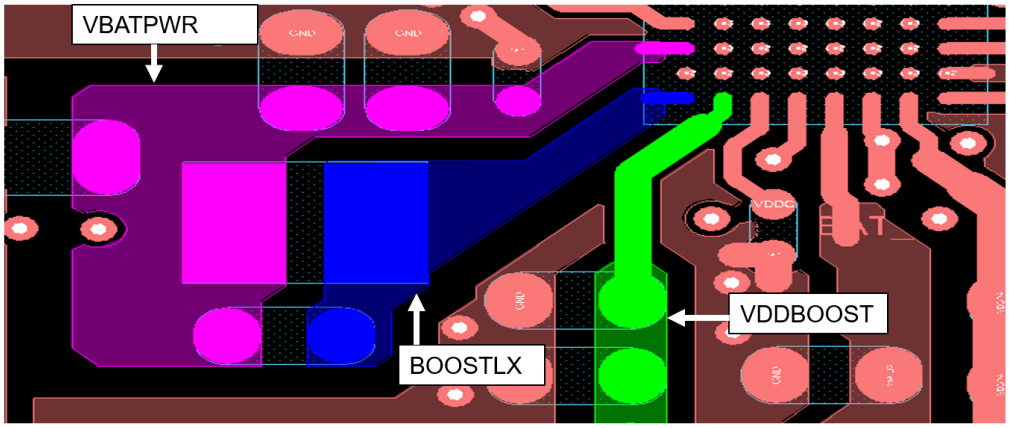


Figure 14. Layout example for VBATPWR, VDDBOOST, and BOOST_LX

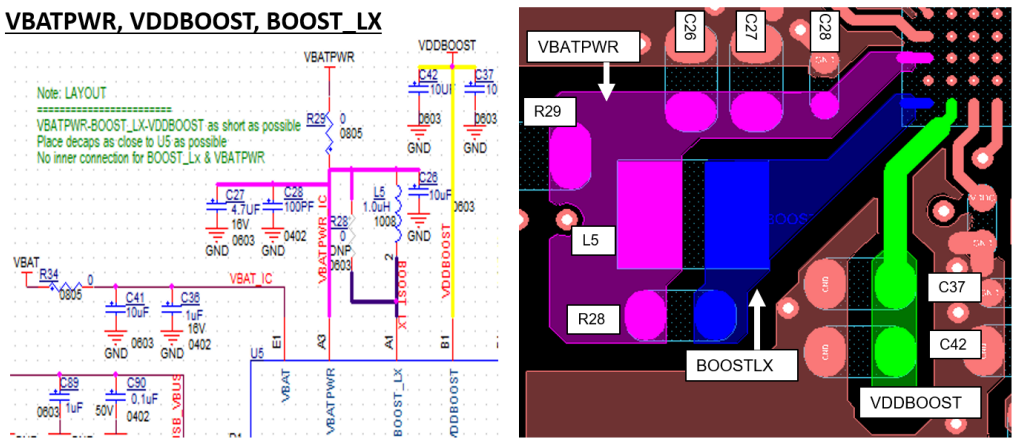


Figure 15. Layout example 2 for VBATPWR, VDDBOOST, and BOOST_LX

VDDNV:

- Place 0.22 µF capacitor as close as possible to VDDNV pad
- Route with 10 mil width & No via allowed

VDDC:

- Place 0.22 µF capacitor as close as possible to VDDC pad
- Route with 10 mil width & No via allowed

VDDPA:

- 100 pF + 4.7 µF should be as close as possible near to VDDPA pads
- Provide shape or thicker trace width (30 mil or more)
- Try to avoid via

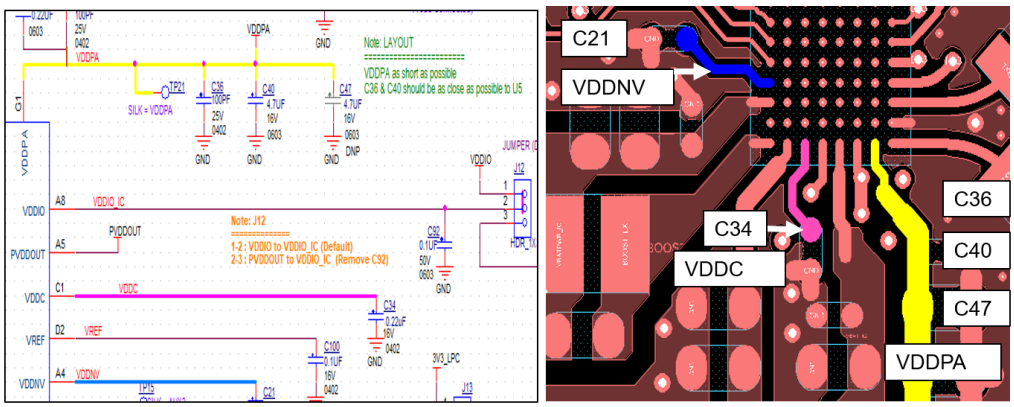
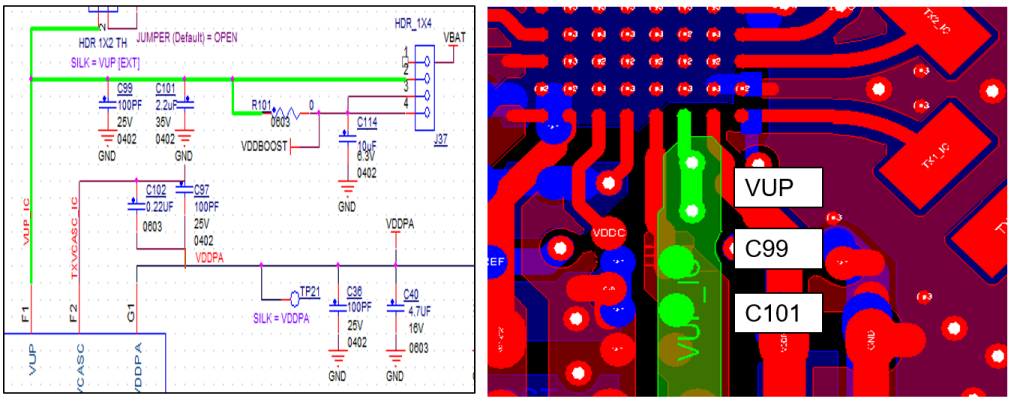


Figure 16. Layout example for VDDNV, VDDC, and VDDPA

VUP:

- Place component as close as possible to VUP pad
- Place low value capacitor close to the pin
- Try to place the components on the same side of the chip
- Provide Cu shape



1. As there is no space on top side, here the related capacitors are placed on the bottom side.

Figure 17. Layout example for VUP

VREF:

1. Place 0.1 µF cap as close as possible to VREF pad
2. Route with 20 mil trace width

VMID:

1. Place cap as close as possible to pin
2. Route with wide trace

TXVCM:

1. Place cap as close as possible to pin
2. Route with wide trace

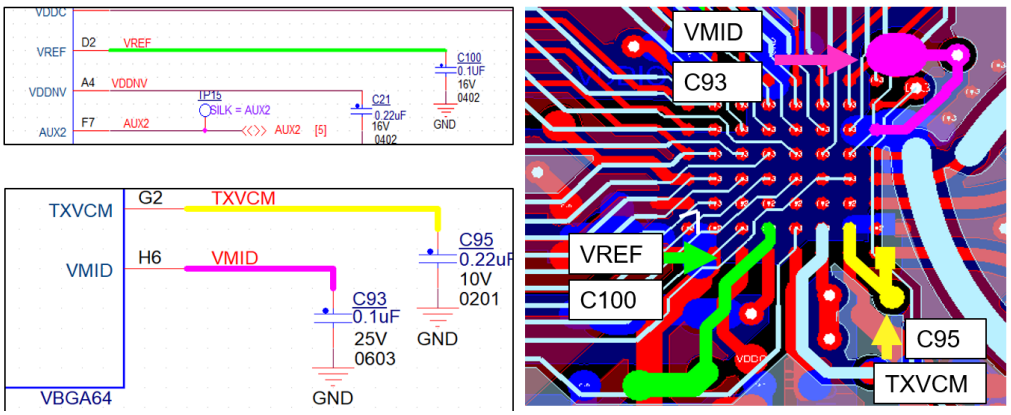


Figure 18. Layout example for VREF, VMID, and TXVCM

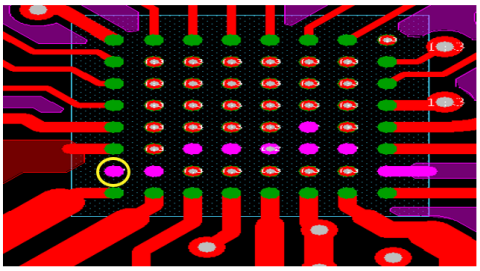
Table 1. Power supply design considerations

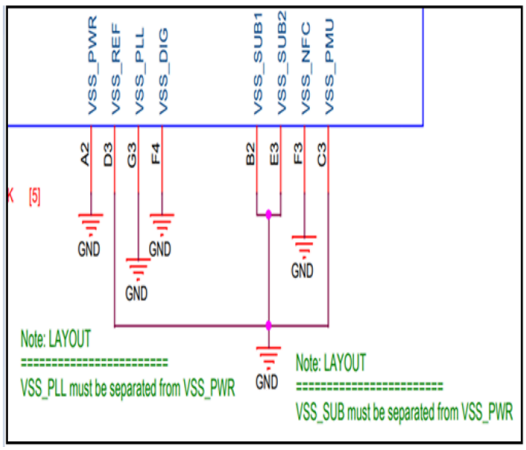
Keep the parasitic capacitance and inductance value lower or equal than this value.

Net name	Parasitic capacitance	Parasitic inductance (BGA pin to first node)	Max VCC	Max ICC	Routing details
VDDBOOST	5.5 pF	0.41 nH	6 V	750 mA	Cu Shape
BOOST_LX	3.5 pF	0.19 nH	6 V	1900 mA	Cu Shape / thicker track width
VBATPWR	7.7 pF	0.56 nH	5.5 V	800 mA	Cu Shape
VDDC	1.5 pF	0.88 nH	1.14 V	30 mA	10 mil width
VDDNV	1.0 pF	0.98 nH	2.2 V	150 mA	10 mil width
VDDPA	1.8 pF	0.26 nH	6 V	750 mA	Cu Shape
VUP	8.1 pF	0.68 nH	6 V	750 mA	Cu Shape
VREF			0.9 V	1 mA	Thicker track width
VMID			1.8 V	20 mA	Thicker track width
TXVCM			3 V	20 mA	Thicker track width

3.3.3 PN5190 BGA GND design recommendation

VSSPWR:





1. Drop a separate via for VSS_PWR to GND and do not share with any other pin

Figure 19. Layout example for the VSS_PWR

VSS_SUB:

- VSS SUB must be separated from VSS_PWR
- Drop a via to connect it to GND plane.
- If it is not possible to connect to GND plane directly, then route to the mentioned pin & drop a via as shown in the snapshot
  - Route to VSS-PMU and drop via or
  - Route to VSS-REF and drop via

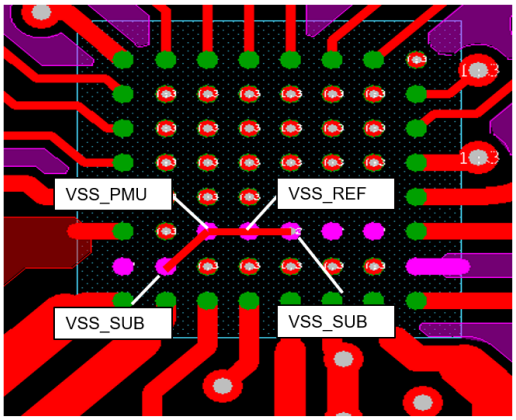


Figure 20. Layout example for VSS_SUB, VSS_PMU, and VSS_REF

VSS_PLL:

- It should directly connect to GND plane
- It should not share with any GND pin of the BGA

VSS_DIG:

- It should directly connect to GND plane
- It should not share with any GND pin of the BGA

VSS_NFC:

- It should directly connect to GND plane
- It should not share with any GND pin of the BGA

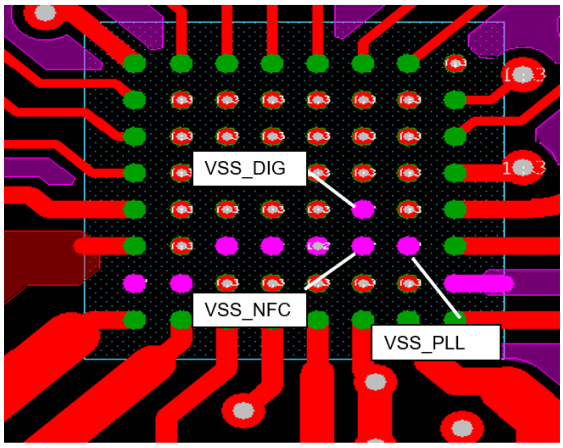


Figure 21. Layout example for the VSS_PLL, VSS_DIG, and VSS_NFC

Table 2. GND design considerations

VSS routing guidance

Net Name	Max ICC	Routing details	Comments
VSS_PWR	1900 mA	Connect directly to GND plane	
VSS_SUB	10 mA	Connect directly to GND plane	Can be shared with VSS_REF & VSS_PMU
VSS_REF	1 mA	Connect directly to GND plane	Can be shared with VSS_SUB & VSS_PMU
VSS_PMU	100 mA	Connect directly to GND plane	Can be shared with VSS_SUB & VSS_REF
VSS_PLL	20 mA	Connect directly to GND plane	
VSS_DIG	30 mA	Connect directly to GND plane	
VSS_NFC	35 mA	Connect directly to GND plane	
VSS_PA	400 mA	Connect directly to GND plane	

3.3.4 PN5190 BGA clock design recommendation

Clock:

- Place XTAL and the associated components as close as possible to the PN5190
- Keep traces as close as possible and keep the length equal
- Keep load capacitance close to the crystal
- Isolate the crystal away from all other signals
- Avoid vias.
- Provide proper GND isolation to avoid noise

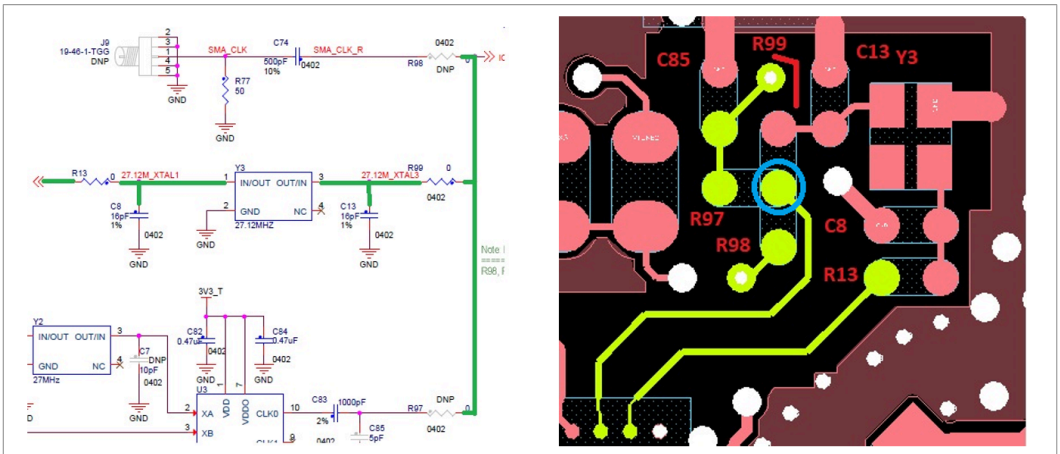


Figure 22. Layout example for the Clock

3.4 Layout recommendation for HVQFN

To provide a proper performance and still meet the regulations like CE, FCC or MIC, the basic analog design must be kept. The following section provides some hints, which parts of the design is most critical in terms of layout, and it gives proven recommendations for the HVQFN package version.

Two main parts need to be considered: the RF and antenna circuit itself, and the power supply.

3.4.1 PN5190 HVQFN RF circuit recommendations

The following layout recommendations for the PN5190 in HVQFN can be given:

1. Place components as close to the IC as possible.
2. Place two closely placed inductors L0 either perpendicular to each other or in 45 degree angle.
3. Place the capacitor of RX line close to PN5190.
4. Place the inductor L0 very close to PN5190 to have shorter TX line.

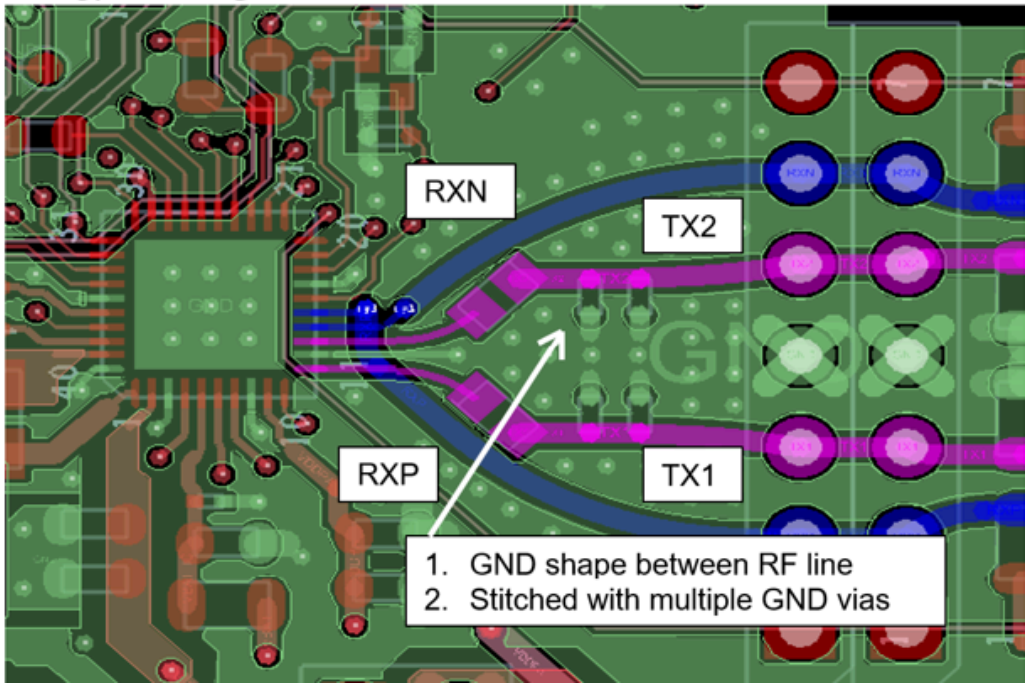
For the routing, the following guide lines can be given:

1. Route TX line in Top Layer (due to huge current).
2. Route RX line in Top Layer (if possible) or route in Layer 3 (Internal signal Layer 1) depending on matching network and antenna placement.
3. Do not use any via for TX Line.
4. Blind Via is used for the RX line.

5. Route with any angle routing. No 90 degree / 45 degree or odd angle bends required.
6. RX and TX line must be routed with GND separation (avoid cross talking!).
7. Route TX line symmetrical to each other and route RX line symmetrical to each other.

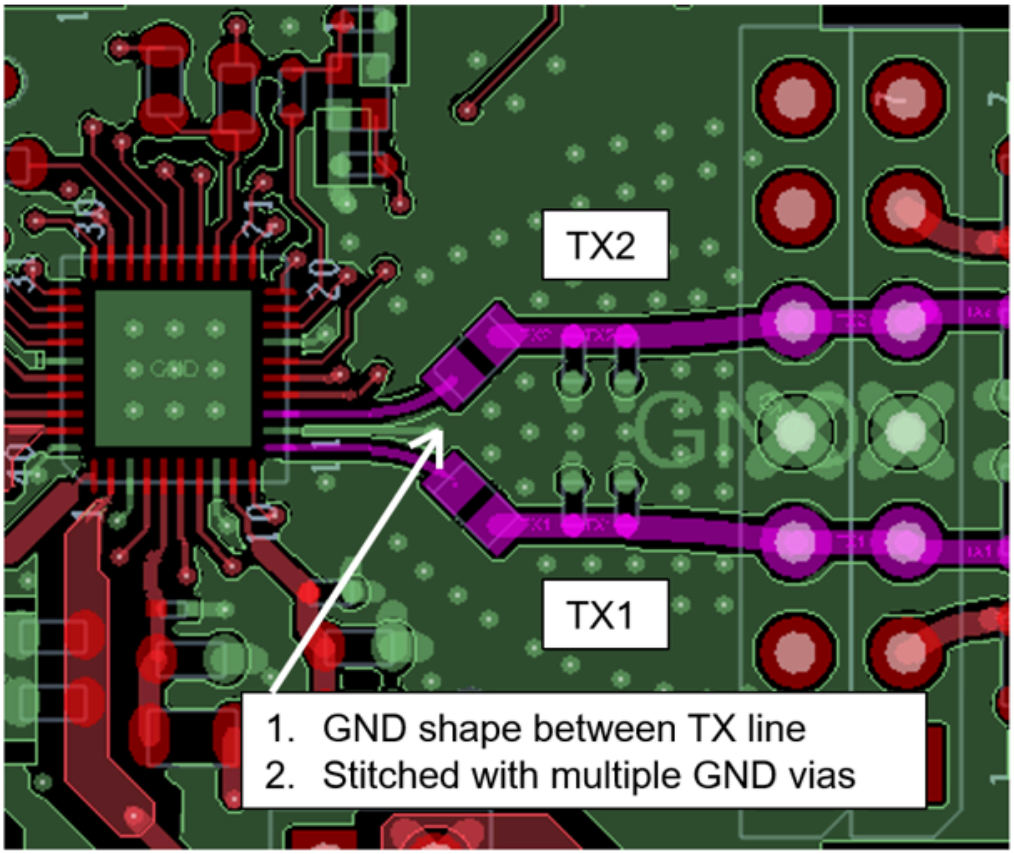
An important part of the layout is the GND layer (see Figure 12).

1. Provide solid GND plane on adjacent Layer (L2_GND).
2. Fill all layers with GND shape.
3. Stitch with multiple GND via around RF line.
4. No Test point allowed.
5. No silk label on RF traces.



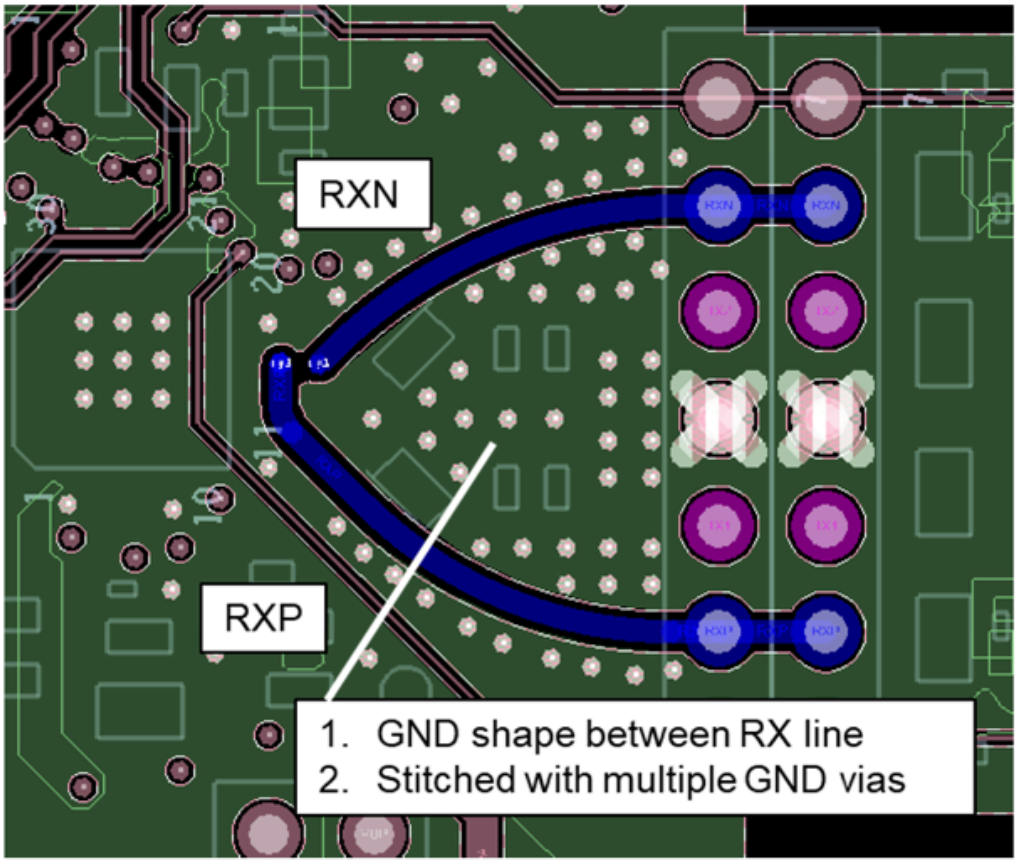
1. Screenshot with multiple layers

Figure 23. PN5190 HVQFN layout reference example



1. Screenshot with multiple layers

Figure 24. PN5190 HVQFN Tx layout reference example



1. Screenshot with multiple layers

Figure 25. PN5190 HVQFN Rx layout reference example

Consider a proper heat sink for the lossy components like EMC filter inductors and damping resistors, as well as for the PN5190 itself.

3.4.2 PN5190 HVQFN power supply circuit recommendation

Next to the RF and antenna design, the power supply is important for a proper functionality and performance. Especially for the DC/DC-Converter the layout needs to be carefully designed.

The PN5190 is optimized to support the EMVCo operating volume with 3.3 V input supply. Therefore the Tx output can drive up to ITVDD = 350 mA. Based on a power supply voltage VDDPA = TVDD = 5.7 V that means a possible total power consumption for the total antenna circuit of up to $P_{tot} \approx 2$ W.

The following guidelines are optimized for the standard use case, using the DC-DC for the VUP supply.

In that combination, the overall mean input current consumption at a supply voltage of 3.3 V can easily be up to 800 mA or higher. The rush in current can be even much higher.

VBATPWR, VDDBOOST, BOOST_LX

1. Place components as close as possible
2. Route VBATPWR, BOOSTLX, VDDBOOST as short as possible
3. Provide Cu shape. If shape is not possible, then route with wide trace (150mils)

4. No vias allowed
5. BOOST_LX is noisy source, so sensitive signals should be far away from this net.

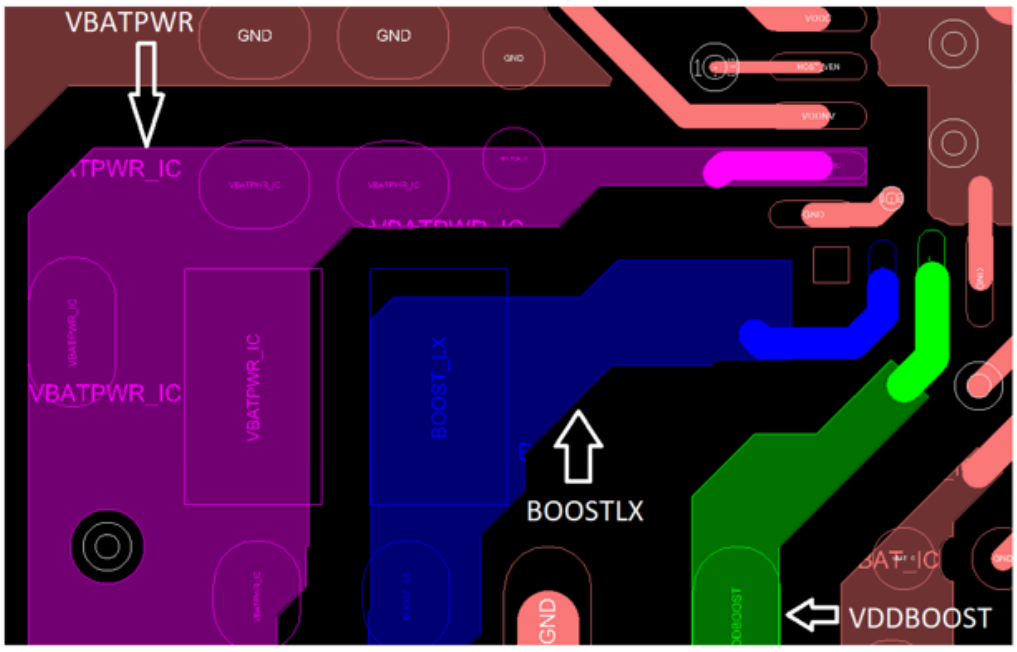


Figure 26. PN5190 HVQFN layout example for VBATPWR, VDDBOOST, and BOOST_LX

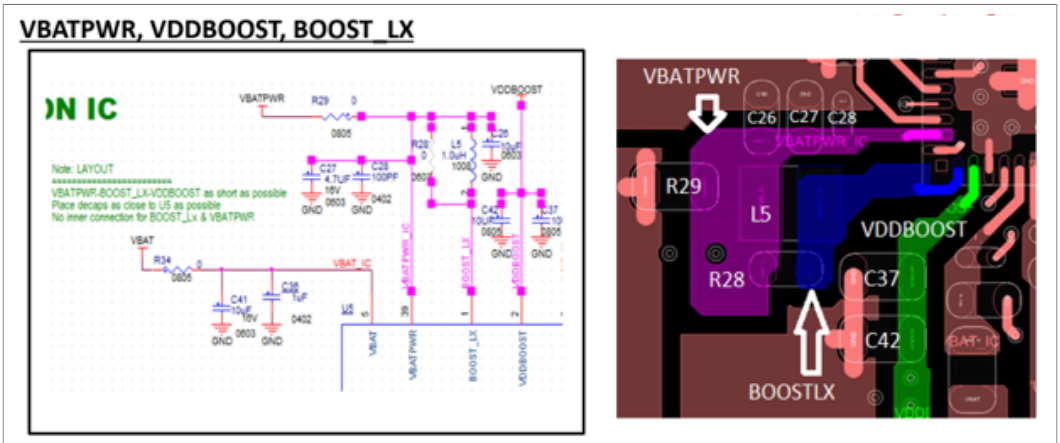


Figure 27. PN5190 HVQFN layout example 2 for VBATWPR, VDDBOOST, and BOOST_LX

VDDNV:

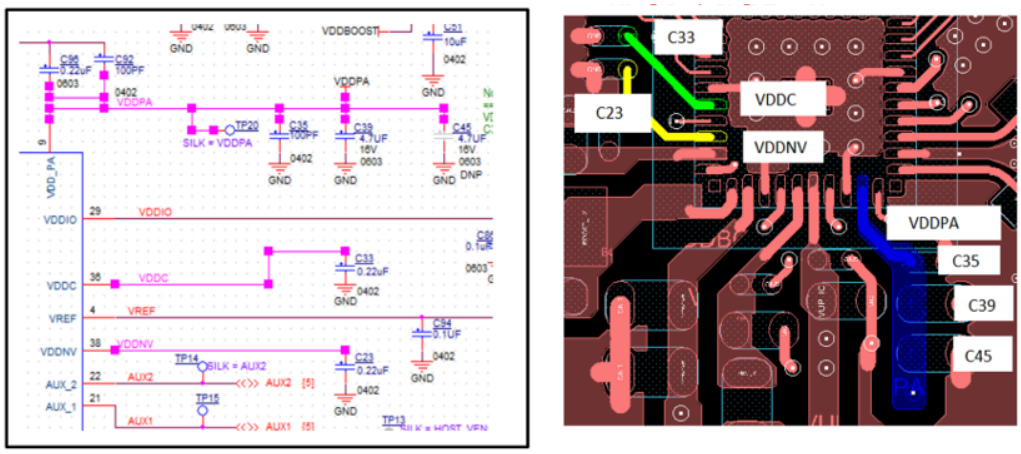
- Place 0.22 µF capacitor as close as possible to VDDNV pad
- Route with 10 mil width and No via allowed

VDDC:

- Place 0.22 µF capacitor as close as possible to VDDC pad
- Route with 10 mil width and No via allowed

VDDPA:

- 100 pF + 4.7 µF should be as close as possible near to VDDPA pads
- Provide shape or thicker trace width (30 mil or more)
- Try to avoid via

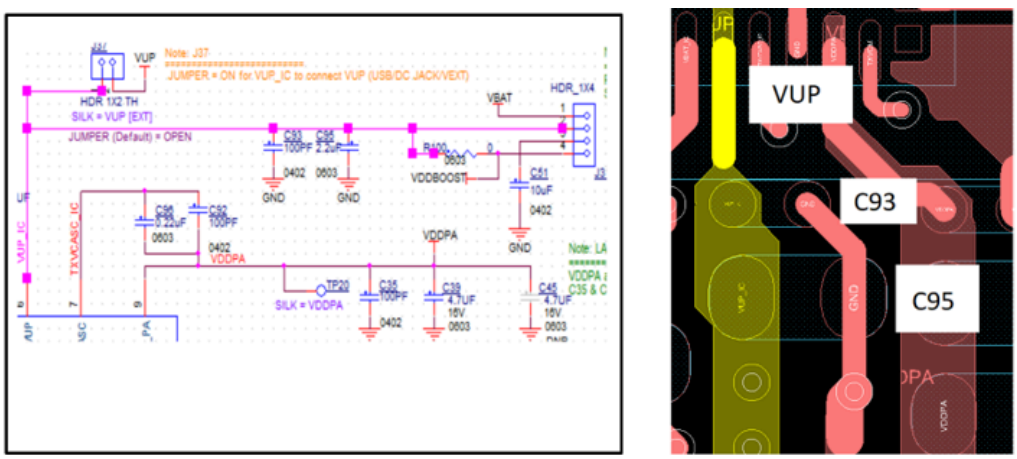


1. Screenshot with multiple layers

Figure 28. PN5190 HVQFN layout example for VDDNV, VDDC, and VDDPA

VUP:

- Place component as close as possible to VUP pad
- Place low value capacitor close to the pin
- Try to place the components on the same side of the chip
- Provide Cu shape



1. Screenshot with multiple layers

Figure 29. PN5190 HVQFN layout example for VUP

VREF:

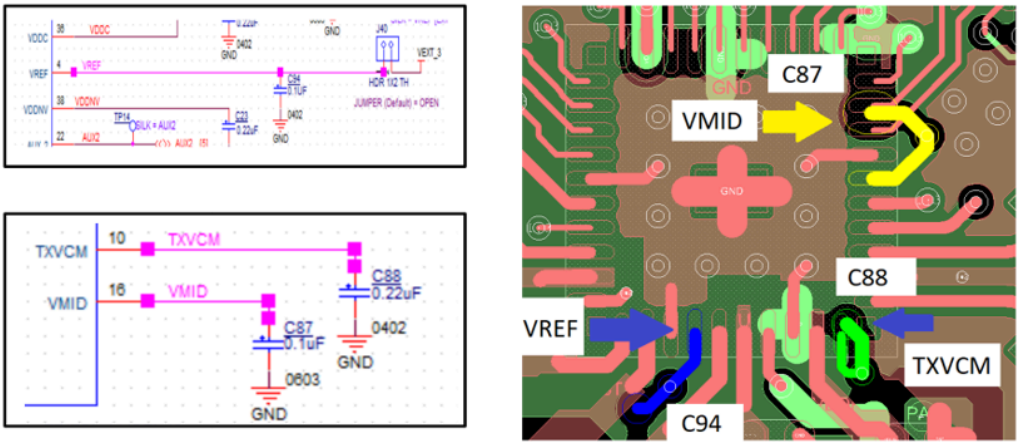
1. Place 0.1 µF cap as close as possible to VREF pad
2. Route with 20 mil trace width

VMID:

1. Place cap as close as possible to pin
2. Route with wide trace

TXVCM:

1. Place cap as close as possible to pin
2. Route with wide trace



1. Screenshot with multiple layers

Figure 30. PN5190 HVQFN layout example for VREF, VMID, and TXVCM

Table 3. PN5190 HVQFN Power supply design considerations

Keep the parasitic capacitance and inductance value lower or equal than this value.

Net name	Parasitic capacitance	Parasitic inductance (BGA pin to first node)	Max VCC	Max ICC	Routing details
VDDBOOST	3.6pF	0.21nH	6V	750mA	Cu Shape
BOOST_LX	5.0pF	0.30nH	6V	1900mA	Cu Shape / thicker track width
VBATPWR	1.6pF	0.20nH	5.5V	800mA	Cu Shape
VDDC	0.6pF	0.71nH	1.14V	30mA	10mil width
VDDNV	0.7pF	0.82nH	2.2V	150mA	10mil width
VDDPA	0.6pF	0.54nH	6V	750mA	Cu Shape
VUP	0.6pF	0.54nH	6V	750mA	Cu Shape
VREF	0.4pF	0.45nH	0.9V	1mA	Thicker track width
VMID	0.6pF	0.55nH	1.8V	20mA	Thicker track width
TXVCM	0.4pF	0.55	3V	20mA	Thicker track width

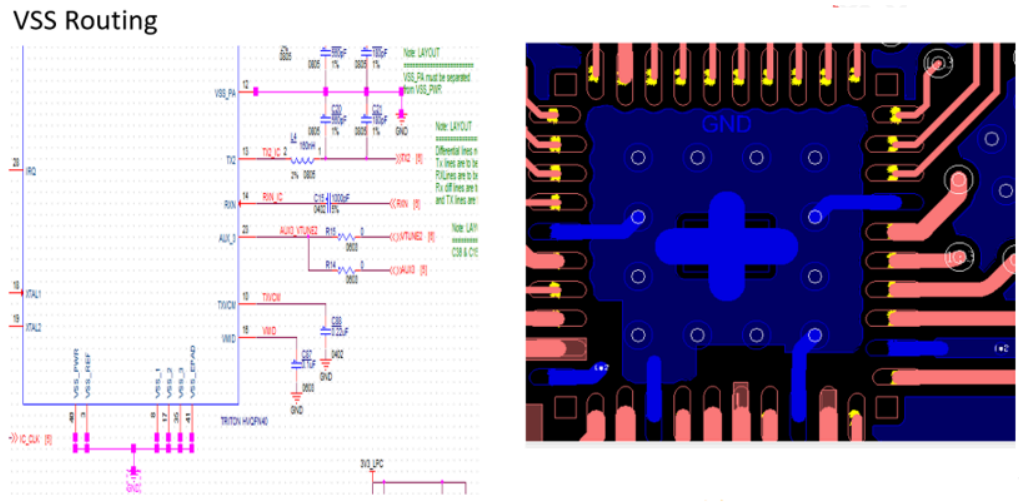
3.4.3 PN5190 HVQFN GND recommendations

VSSPWR:

Table 4. PN5190 HVQFN VSS routing

VSS routing guidance

Net name	Max ICC	Routing details
VSSPWR	1900 mA	Drop separate via to GND
VSSREF	1 mA	Connect directly to GND plane
VSSPA	400 mA	Connect directly to GND plane
VSS_EPAD		Fill copper shape and place vias



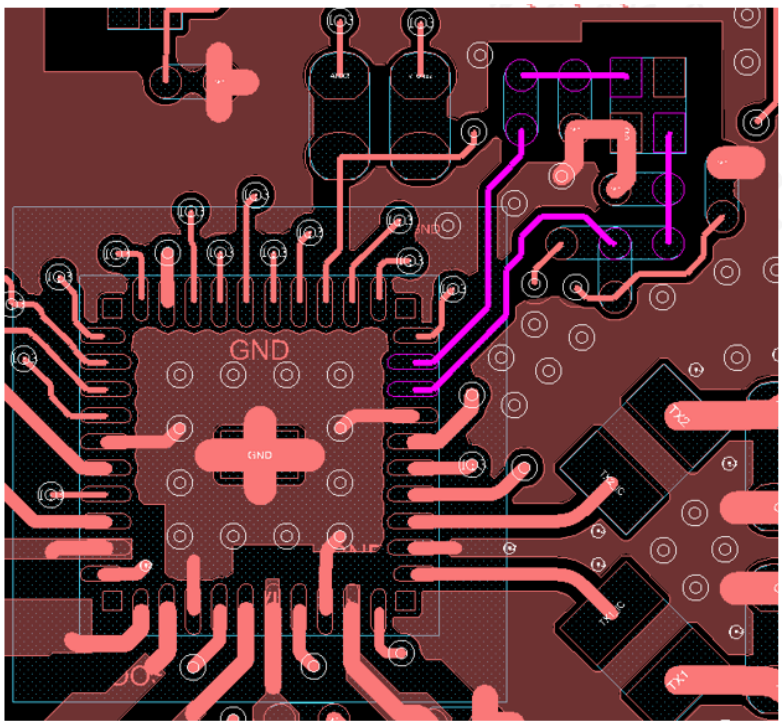
1. Screenshot with multiple layers

Figure 31. PN5190 HVQFN layout example for VSS

3.4.4 PN5190 HVQFN clock design recommendations

Clock:

- Place XTAL and the associated components as close as possible to the PN5190
- Keep traces as close as possible and keep the length equal
- Keep load capacitance close to the crystal
- Isolate the crystal away from all other signals
- Avoid vias.
- Provide proper GND isolation to avoid noise



1. Screenshot with multiple layers

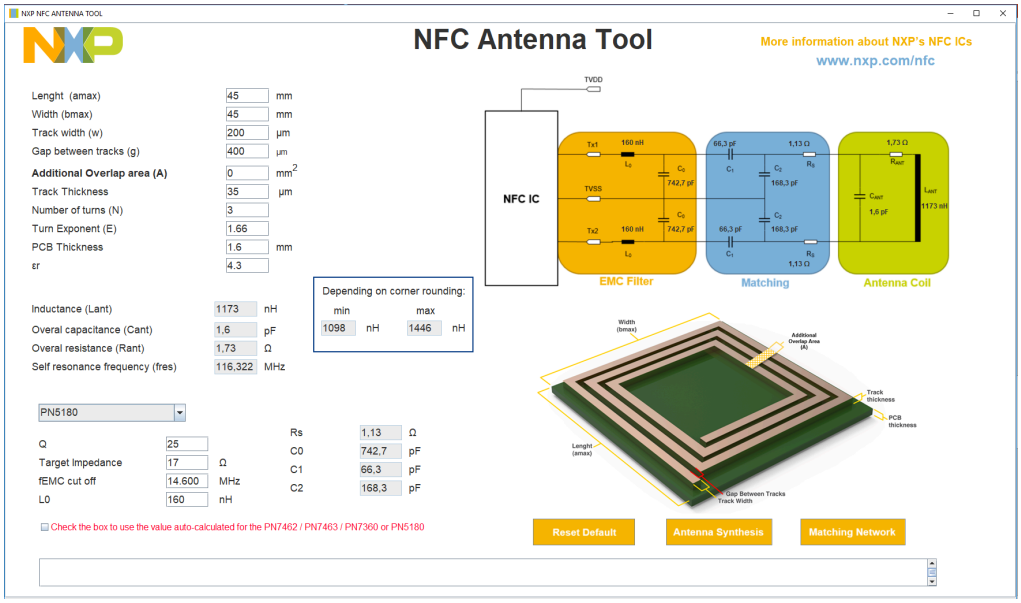
Figure 32. PN5190 HVQFN layout example for the clock

4 PN5190 antenna tuning

The following description focuses on the PCD antenna for the PN5190.

4.1 NFC antenna tool

If no other starting point is available, the NXP NFC antenna design tool on the NFC Antenna Hub (see [11]) might be helpful, as shown in Figure 33.



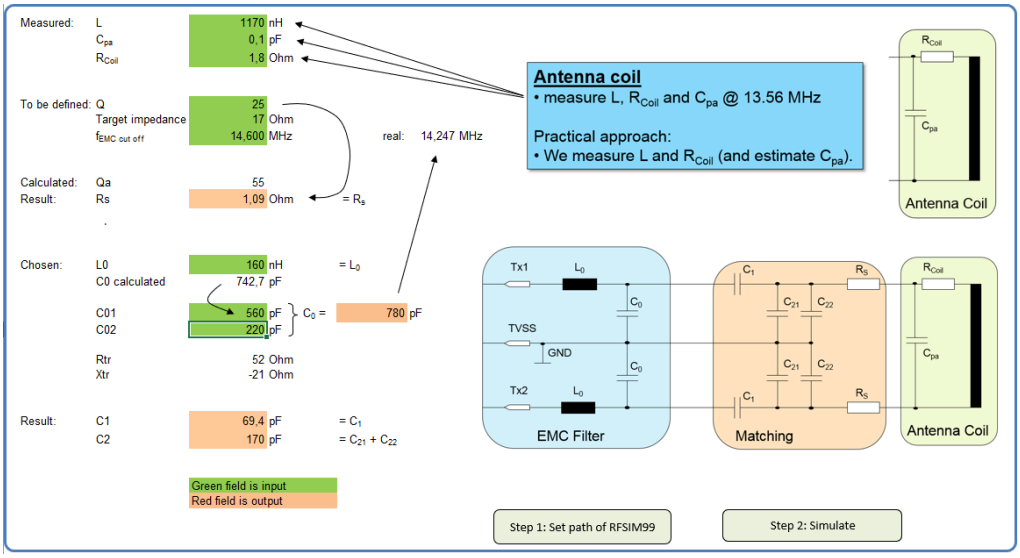
1. Choose the PN5180 as starting point.

Figure 33. NFC Antenna Tool example

The PN5180 can be chosen as NFC reader IC, which gives good starting value as such. The target impedance might be changed to a lower value, e.g. 17 Ω. The EMC filter inductor can be chosen as 160 nH.

4.2 Antenna tuning calculation excel sheet

Alternatively the known excel sheet can be used, like for the PN5180 or any other NXP NFC reader ICs. The same example from Section 4.1 is shown in Figure 34.



1. This example is showing the same tuning values as the NFC Antenna Tool, see [18]

Figure 34. Antenna calculation excel sheet example

For a simple 45 mm x 45 mm antenna with 3 turns the antenna synthesis returns:

L = 1.17 µH

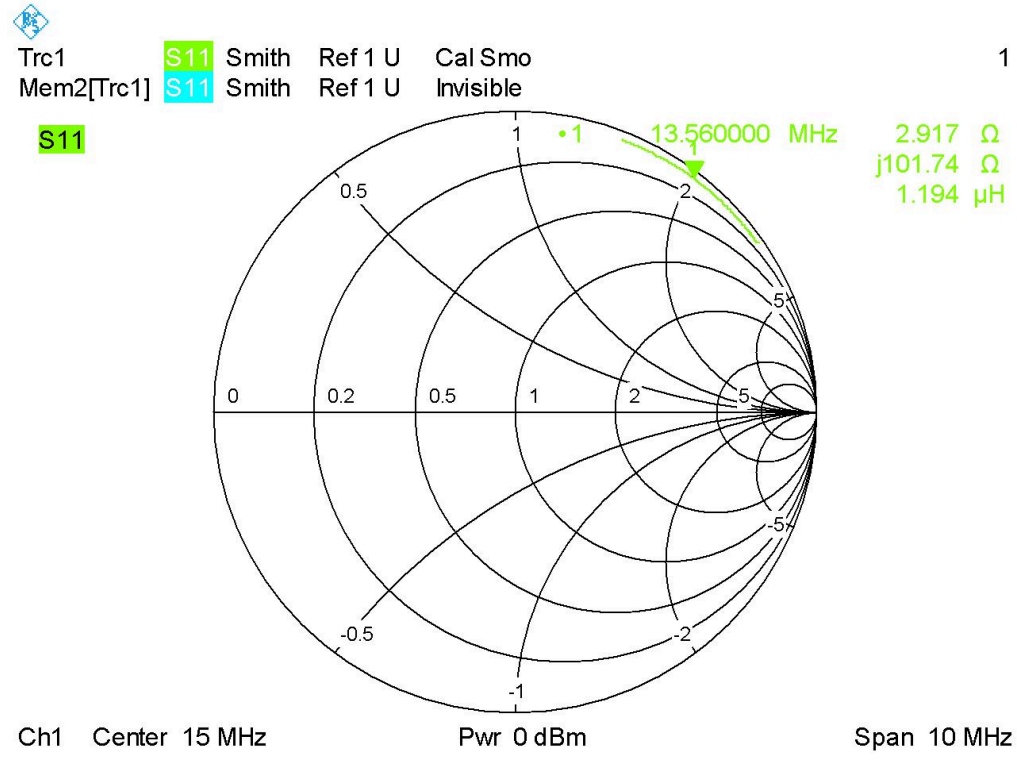
R_{Coil} = 1.7 Ω

The input values for the antenna coil itself should be taken from a simple measurement rather than only from the antenna synthesis. This antenna coil measurement is required to derive the inductance L, the resistance R_{Coil} and the capacitance C_{pa} as accurate as possible.

The easiest even though not most accurate way is to use the VNA to measure the impedance $\underline{Z}$ of the antenna coil at 13.56 MHz and to calculate L and R out of it:

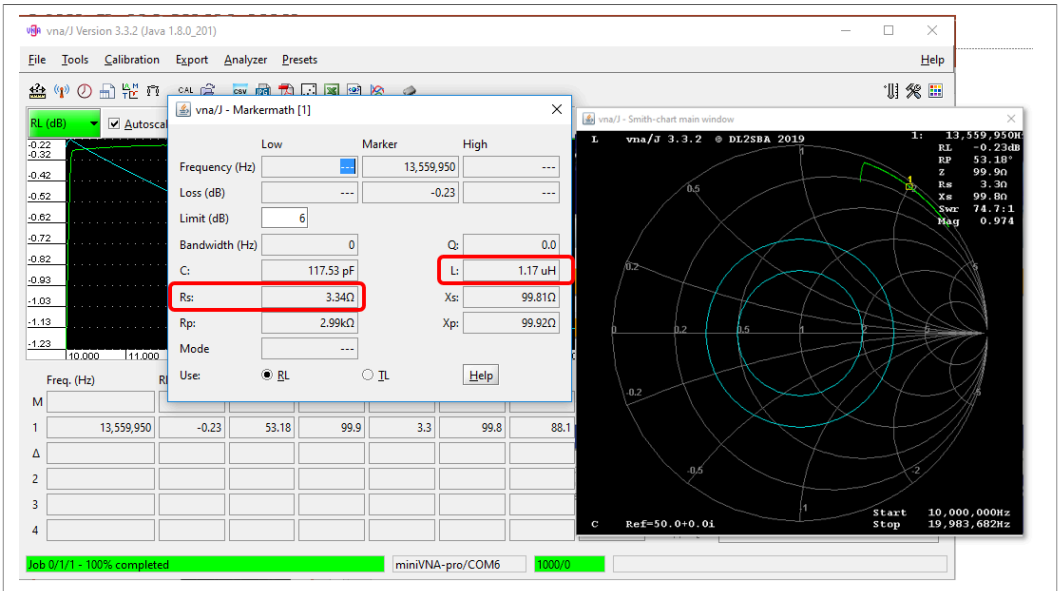
$$\underline{Z} = R + j\omega L_{Coil}$$

Typically the VNA directly can show the L and R, as shown in Figure 35 and Figure 36.



1. Measured with Rohde & Schwarz ZVL (see [7])
2. L = 1.19 µH, R = 2.9 Ω

Figure 35. Antenna coil measurement example 1



1. Measured with minVNA Pro and VNA/J (see [8] and [10])

Figure 36. Antenna coil measurement example 2

In this example, the antenna coil is measured with these values:

L = 1.17 … 1.19 µH

R_{Coil} ≈ 2.9 … 3.3Ω

C_{pa} = not measured, can be estimated

The inductance can be measured quite accurate, but the resistance is not very accurate due to the relationship between R and jωL. And the capacitance is not measured at all with this simple measurement.

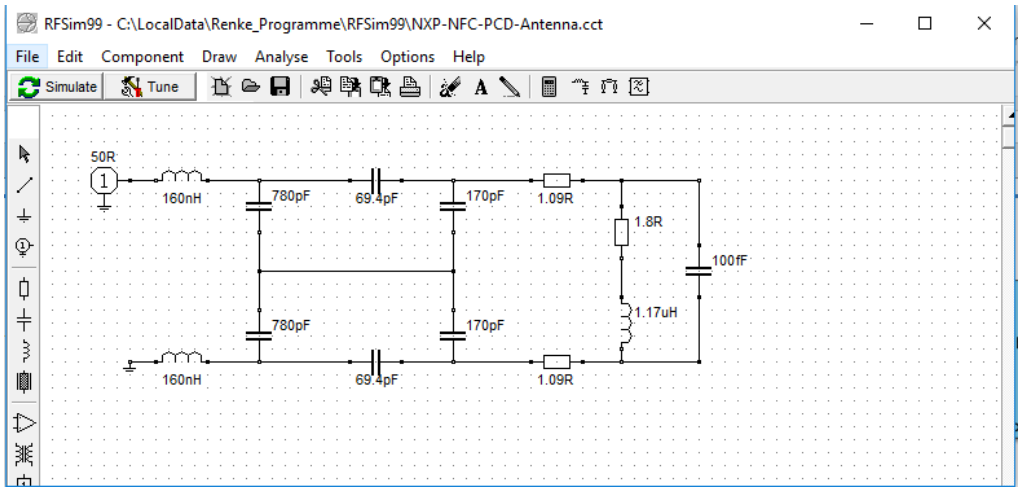
There are several ways to improve the accuracy and even further derive the capacitance, but these simple results are enough to start the tuning procedure. This tuning procedure needs to be done anyway, so there is no real need to spend more effort in measuring the antenna coil parameters more accurate.

Note: *It might be helpful to slightly adapt the Q in the given excel sheet calculation in such a way that the resulting damping resistor R_Q is calculated to be within an E-series of values (i.e. 2.7 Ω or 3.3 Ω, but not 2.845 Ω). In such case, the following calculation is more accurate, i.e. the calculation and simulation result gets closer to the measured result.*

If the RFSIM99 is used, the next step should be the simulation of the antenna circuit.

4.3 Antenna circuit simulation

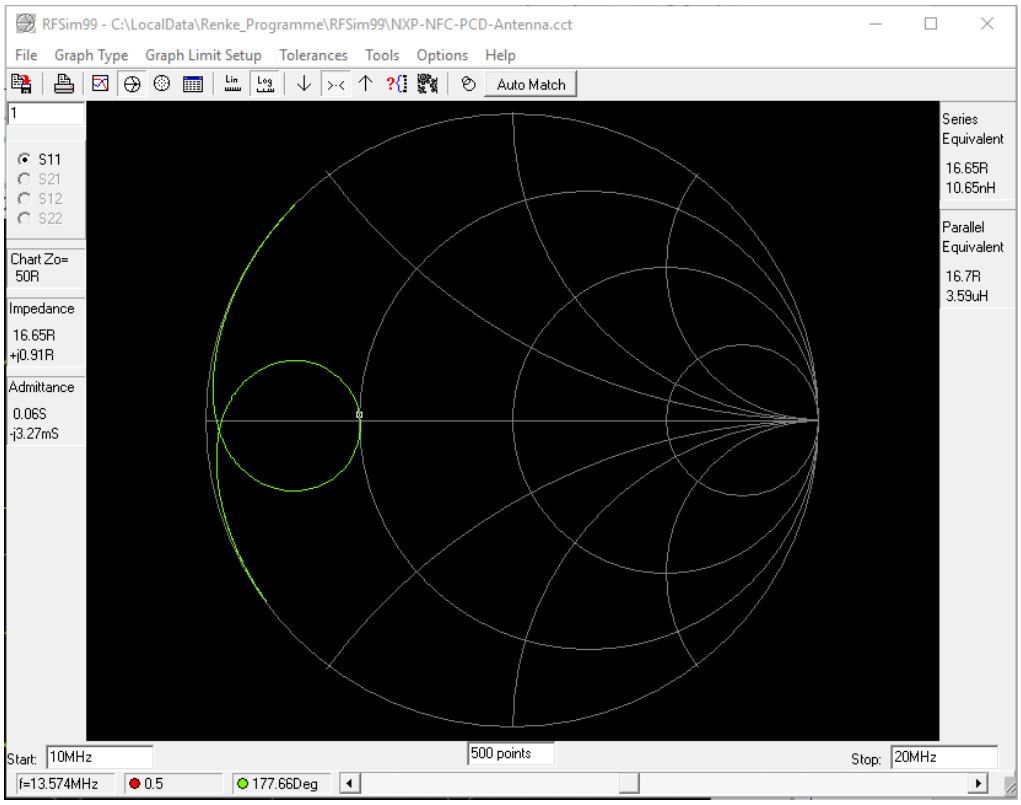
The excel sheet calculation provides a macro function, which writes the simplified netlist for the simulation tool RFSIM99 (see [9]), which then automatically is started, as shown in Figure 37 .



1. This circuit uses ideal components!

Figure 37. Circuit derived from the calculation

The impedance plot (smith chart) in Figure 38 shows the related impedance from 10 MHz to 20 MHz. The marker at (or closest to) 13.56 MHz indicates the antenna impedance at operating frequency.



1. This circuit uses ideal components!

Figure 38. RFSIM99 smith chart plot

This simulation can be used now to fine-tune the circuit with realistic components:

1. The values should fit into the given E-series. Example: Instead of C2 = 197.2 pF a value of C2 = 180 pF in parallel to 18 pF can be used.
2. The ideal inductor in the simulation indicates no losses: a first measurement will reveal that this is not realistic at all. Typically some 1…3 Ω can be added per inductor.

4.4 How to interpret the smith chart

Even though the smith chart is a well-known tool to indicate S-Parameters, and therefore the S11 simulation and measurement fits perfectly into the antenna tuning procedure, it might help to understand a few simple mechanisms of the typical NFC Antenna circuit tuning.

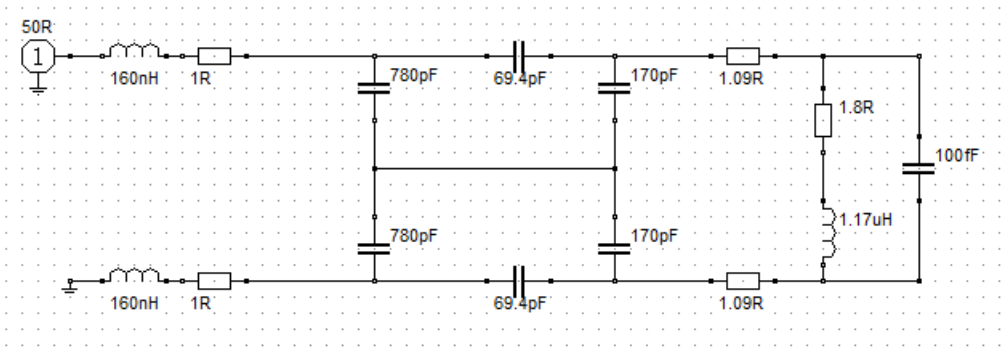
Note: *The effect of this mechanism can easily be checked with the RFSIM99.*

4.4.1 Smith chart: Inductor losses

The biggest effect in terms of losses (besides the damping resistors) comes from the EMC filter inductors. The simple circuit from the calculation uses ideal components, i.e. it does not take any inductor losses at all into account.

So the first step for the simulation is to add those losses. Instead of using a physical model of a real inductor, the Figure 39 shows the circuit including manually added losses.

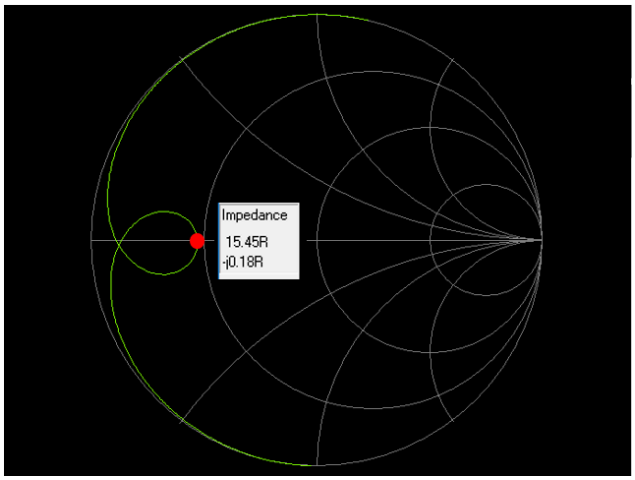
That example indicates losses of 1 Ω per inductor (at the operating frequency, which is quite realistic).



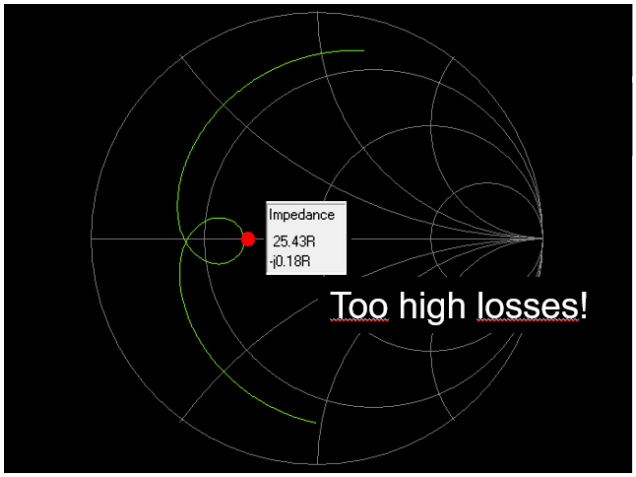
1. The L0 inductor (real component) contains losses, which are manually added.

Figure 39. Circuit derived from the Calculation including losses

The impact of those losses can be directly seen in the smith chart as shown in principle in Figure 40.



Ideal L0, no losses

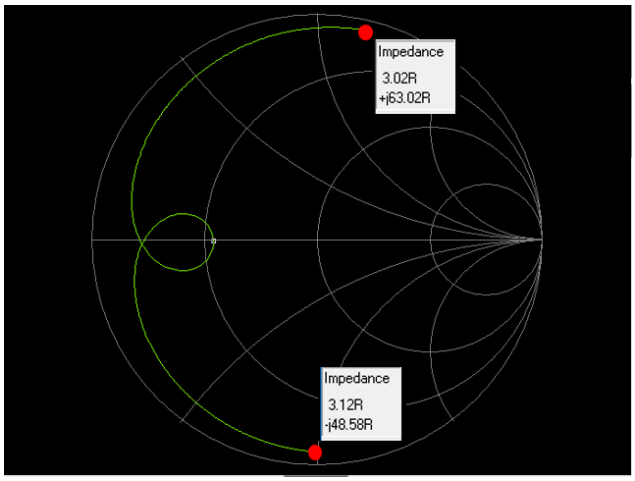


Bad L0 with 5 Ω losses at 13.56 MHz

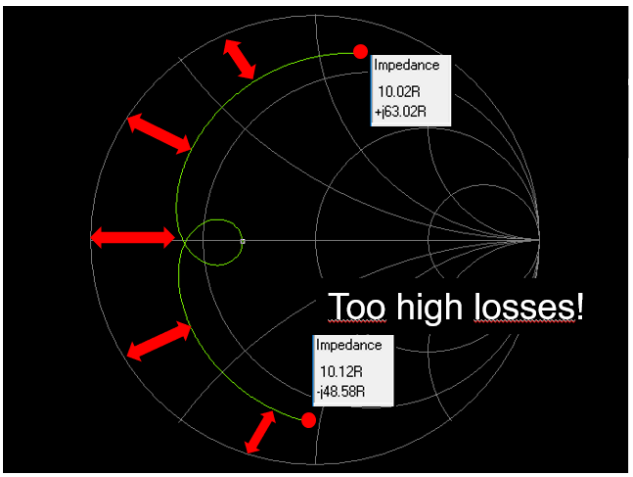
Figure 40. Impedance comparison with and without losses

Even further, the losses can be directly measured within this circuit, when moving the measurement marker to its ends, either to 10 MHz or to 20 MHz, as shown in Figure 41.

The marker directly shows the added losses of the two inductors, since all other components are either loss-free (capacitors) or do not count at these frequencies (damping resistor or antenna coil losses). So the real part of the S11 (ignore the reactive part) in Ω shows the losses of the series of the two L0.



Good L0 with R = 1.5 Ω

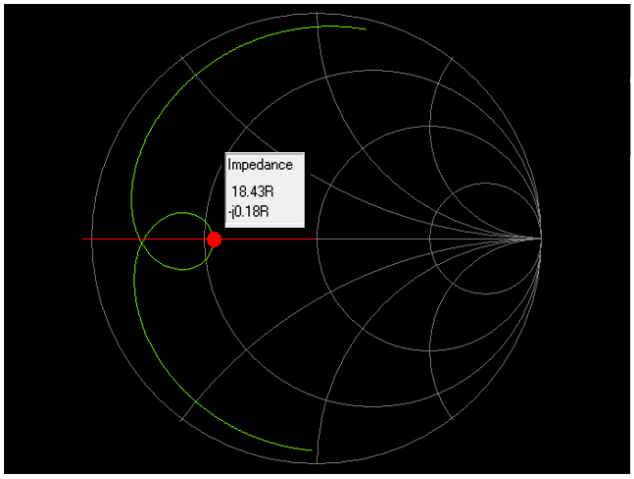


Bad L0 with R = 5 Ω

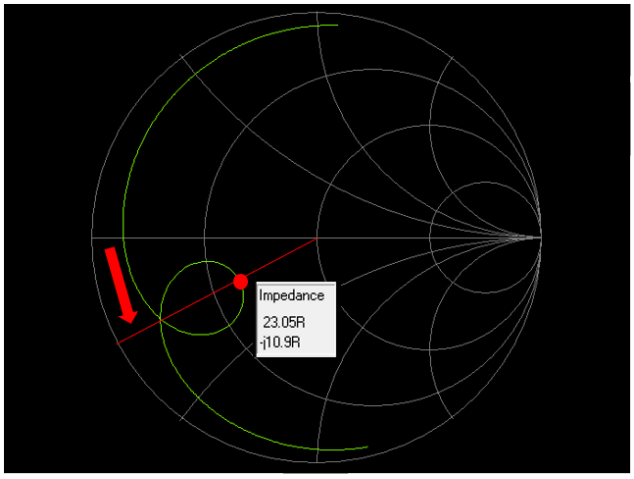
Figure 41. Measure the inductor loss

4.4.2 Smith chart: C0

The impact of the value of C0 (EMC filter capacitor) can also be read from the smith chart, as indicated in Figure 42 and Figure 43.

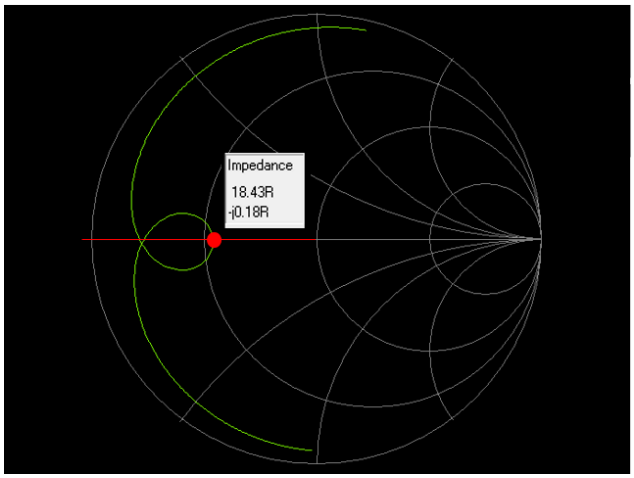


C0 ok, Cut off frequency ok

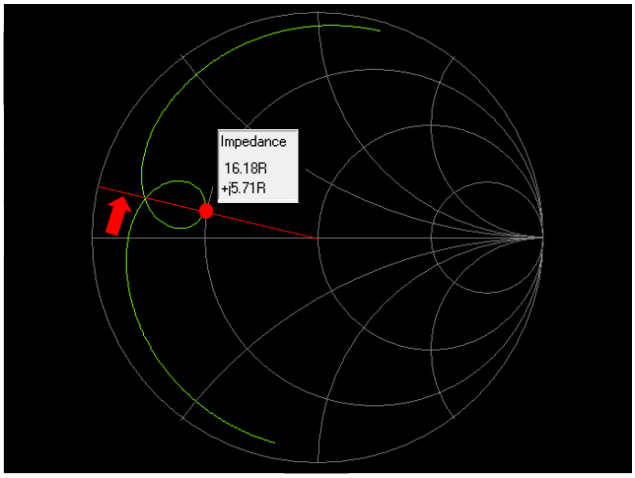


C0 too low, Cut off frequency too high

Figure 42. Smith chart: C0 too low



C0 ok, Cut off frequency ok

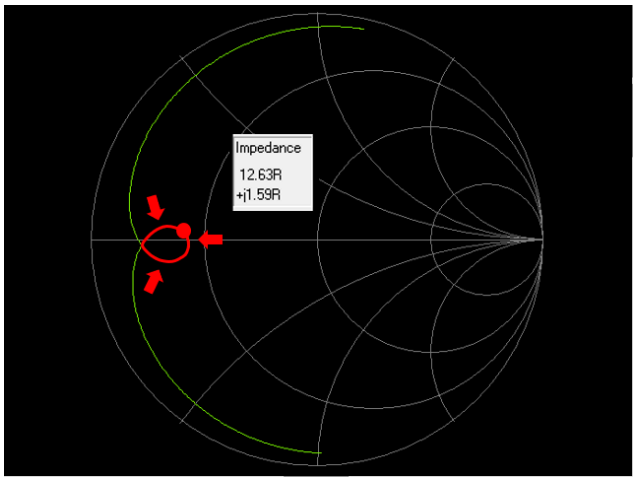


C0 too high, Cut off frequency too low

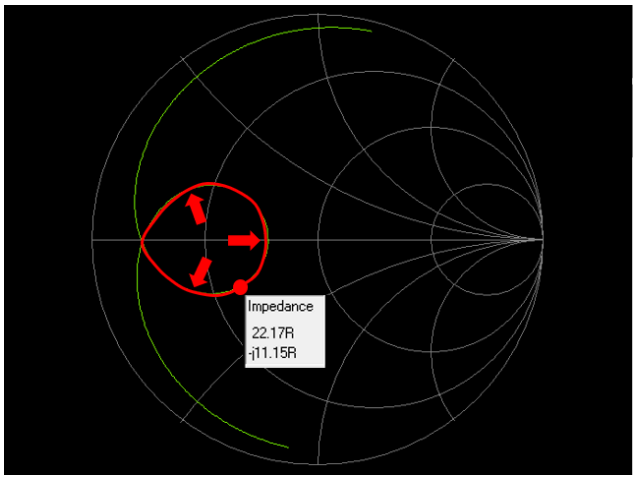
Figure 43. Smith chart: C0 too high

4.4.3 Smith chart: C1

The effect of C1 can also be estimated from the smith chart, as shown in Figure 44.



C1 too low, impedance too low

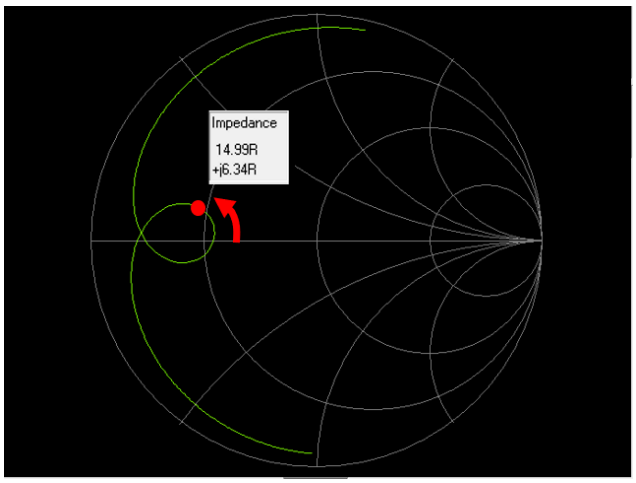


C1 too high, impedance too high

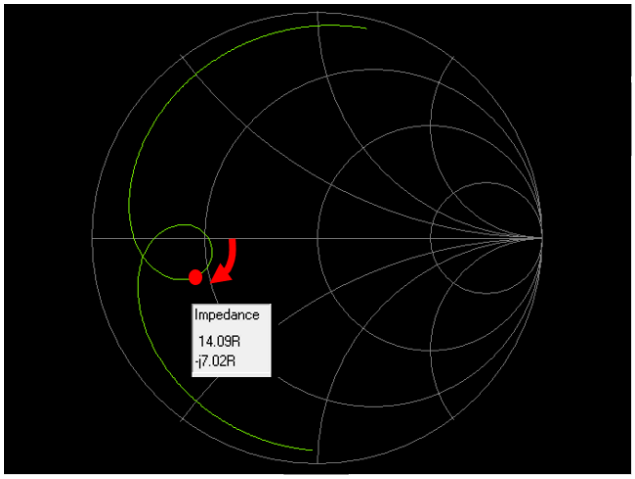
Figure 44. Smith chart: impact of C1

4.4.4 Smith chart: C2

The effect of C2 can also be estimated from the smith chart, as shown in Figure 45.



C2 too low, Impedance too inductive



C2 too high, impedance too capacitive

Figure 45. Smith chart: impact of C2

4.5 Correction of the simulated circuit

Based on the measured inductance and resistance value of the antenna, the basic tuning circuit is derived (see Section 4.2 and Section 4.3). After adding the realistic losses of L0 (see Figure 39), now the capacitance values are modified into realistic values.

C0 = 780 pF are replaced with 560 pF || 220 pF

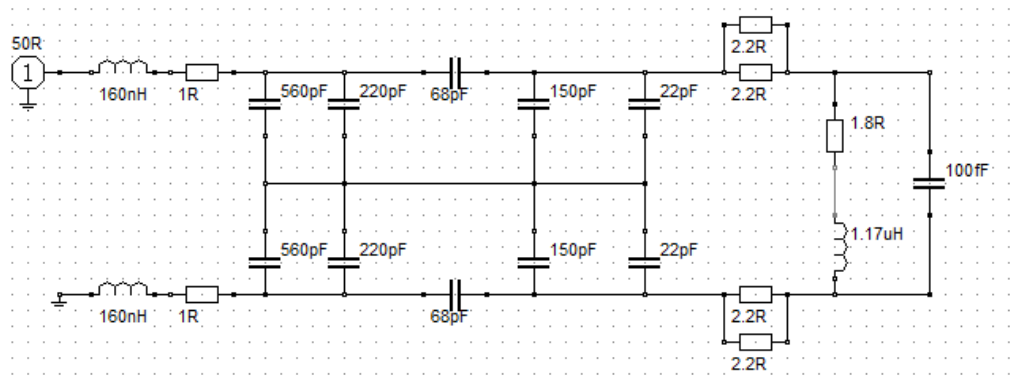
C1 = 69.4 pF is replaced with 68 pF

C2 = 170 pF is replaced with 150 pF || 22 pF

$R_{damping}$ = 1.09 Ω is replaced with 2.2 Ω || 2.2 Ω

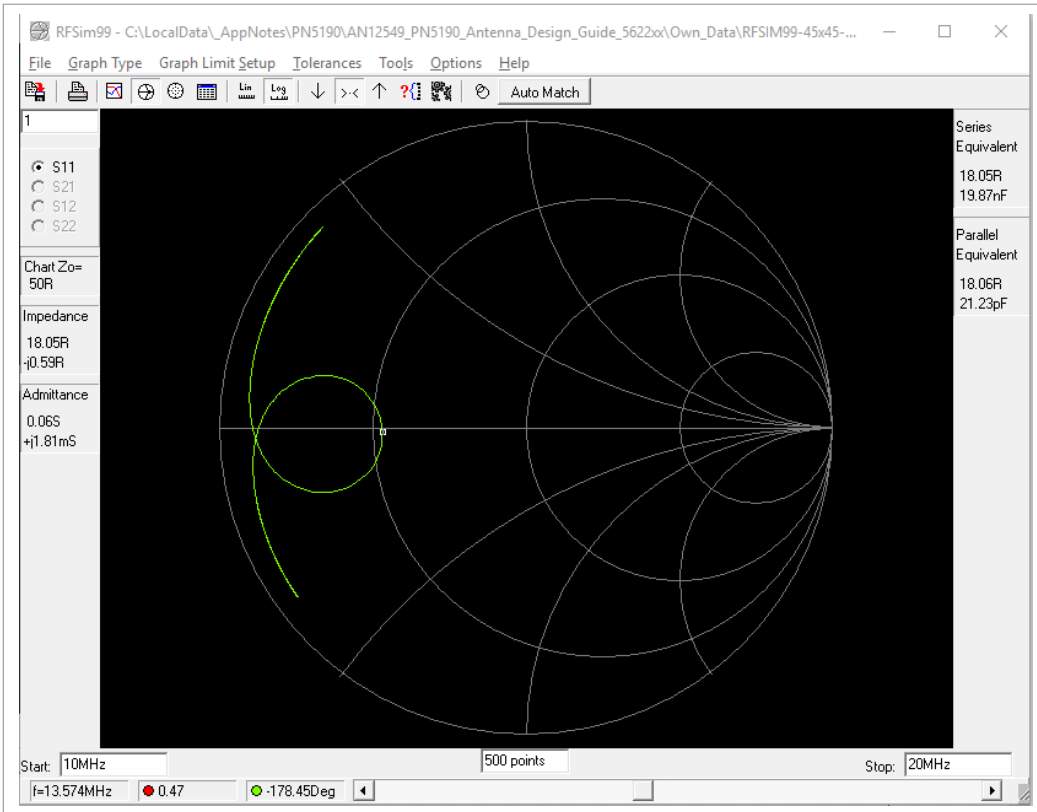
All values are tuned in such a way, that the smith chart plot shows a “symmetrical” plot with the correct target impedance at resonance.

The Figure 46 and Figure 47 show the result of that correction.



1.

Figure 46. Corrected simulation circuit



1. The simulated impedance is slightly higher than the target.

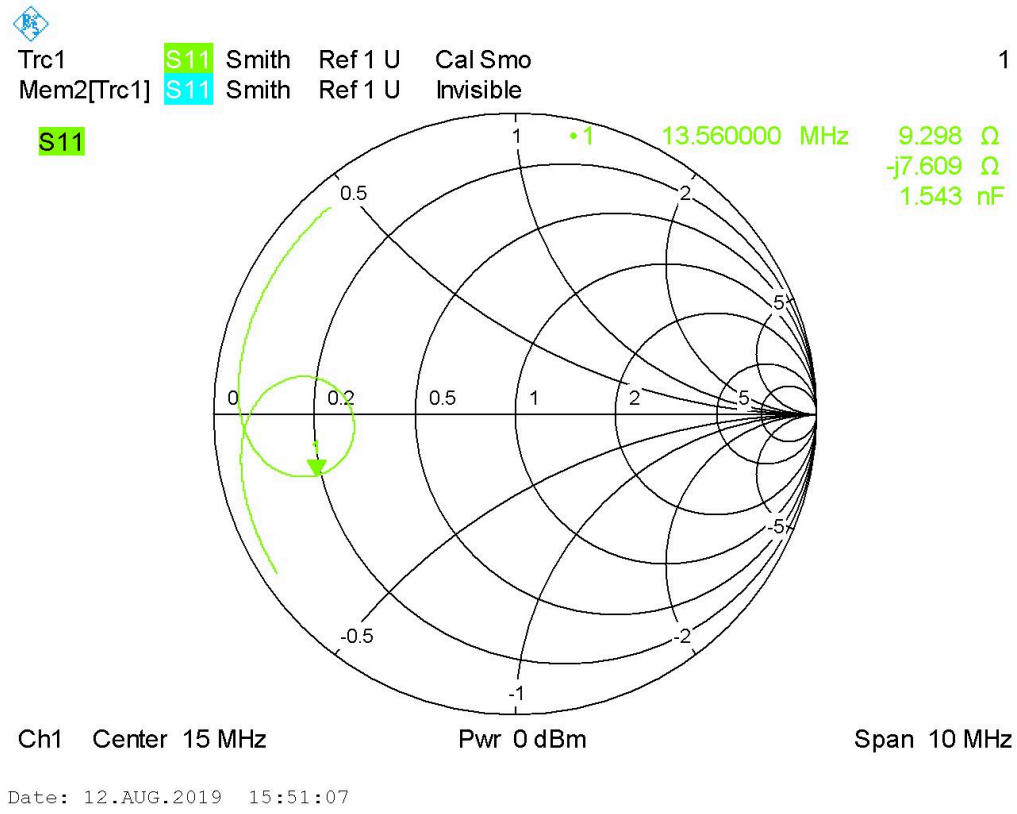
Figure 47. Smith chart plot of the corrected tuning circuit

4.6 Measure the real circuit

With these values, the tuning can be assembled now. Assuming that all the values are correct and the same as simulated the measured impedance plot must be the same like the simulated one.

However, the measurement of the antenna coil introduced some uncertainties, especially on the losses, which are not considered yet in the simulation. On top of that, the layout has some influence, too, i.e. it mainly introduces some additional parallel capacitance and some inductance due to the length of traces.

So in reality typically there is a mismatch between the measured circuit and the simulated one, as shown in the example in Figure 48.



1. First-time assembly after simulation

Figure 48. Smith chart plot of the corrected circuit

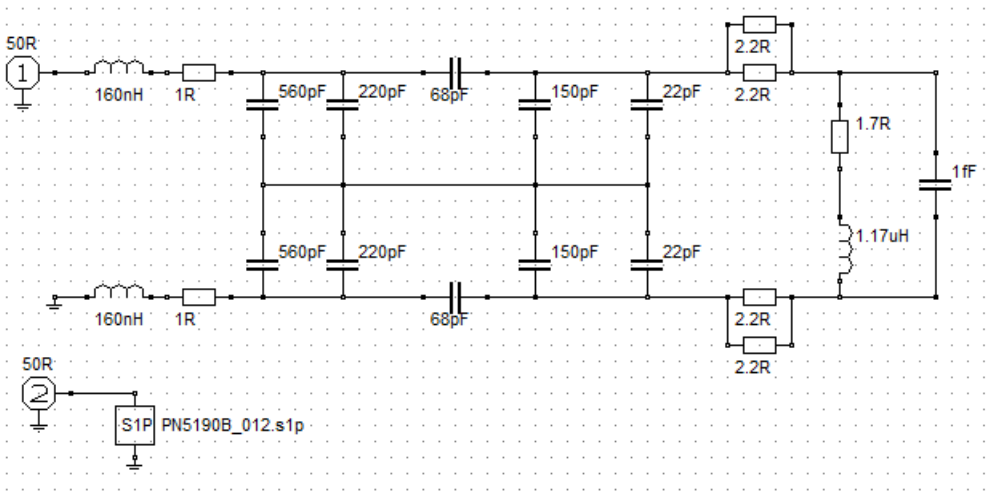
The measured smith chart indicates a too high C2, and the impedance seems to be a bit too low.

The C2 can be easily explained: the antenna coil measurement did no take any capacitance into account. There might be a few pF missing in the simulation.

The wrong impedance as such might be most likely related to the very inaccurate R_{Coil}. The calculation returned R_{Coil} = 1.7 Ω, while the measurement showed R_{Coil} = 2.9 … 3.3Ω. So should be used to derive a simulation, which takes realistic values into account, and tries to match the real measurement.

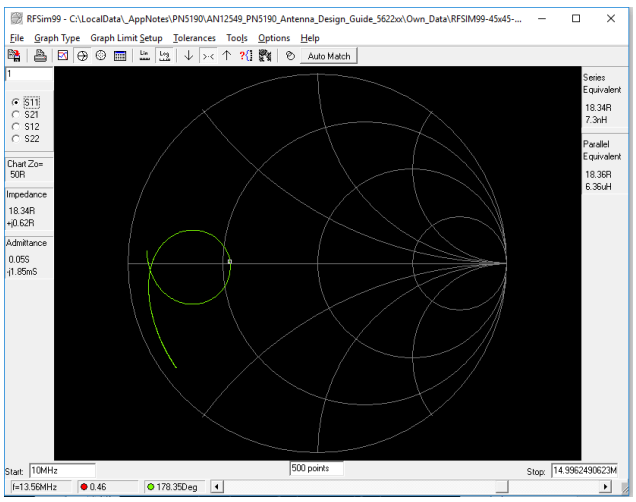
4.7 Adapt the simulation

To simplify the exercise, the measurement pot is saved S1P-file, and then added into the simulation file, as shown in

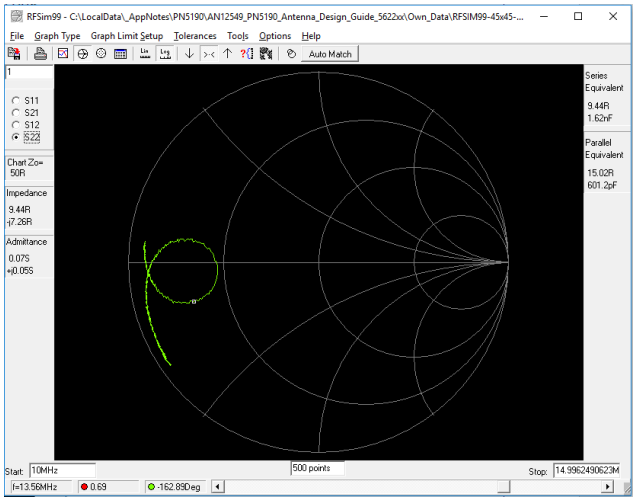


1.

Figure 49. First Assembly, simulated and measured



S11: Simulation plot



S22: measured plot

Figure 50. Comparison of simulation and measurement

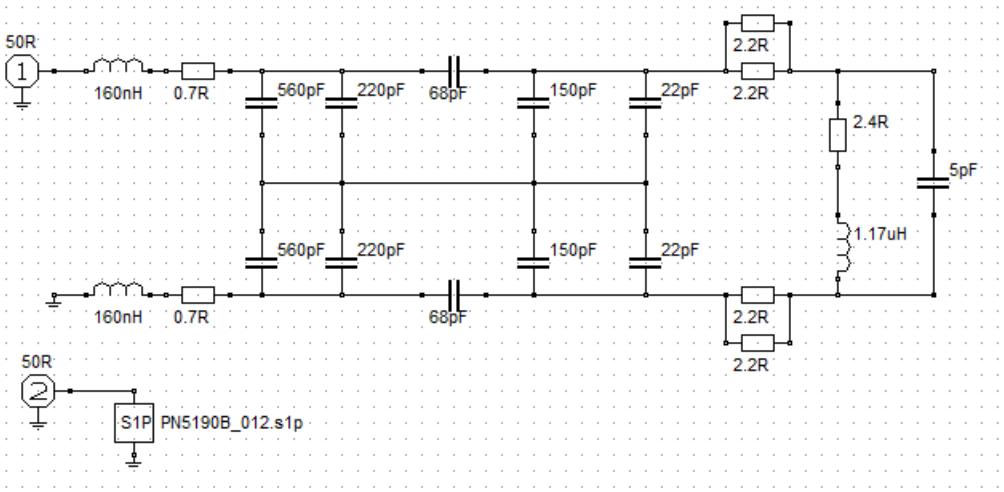
Remark: the span is automatically limited by the simulation tool due to the high number of measurement points, and therefore ends at 15 MHz. 15 MHz still is enough for the tuning purpose, so this limitation does not matter.

With the following, the changes the simulation is then adapted to match the reality:

- Increase the C_{ant} to C_{ant} = 5 pF.
- Increase the R_{Coil} to R_{Coil} = 2.4 Ω.

- It can also be shown that the estimated losses of the L0 inductors were too high. So in this case the resistance, which indicates the L0 losses, are reduced to R_{L0} = 0.7 Ω.

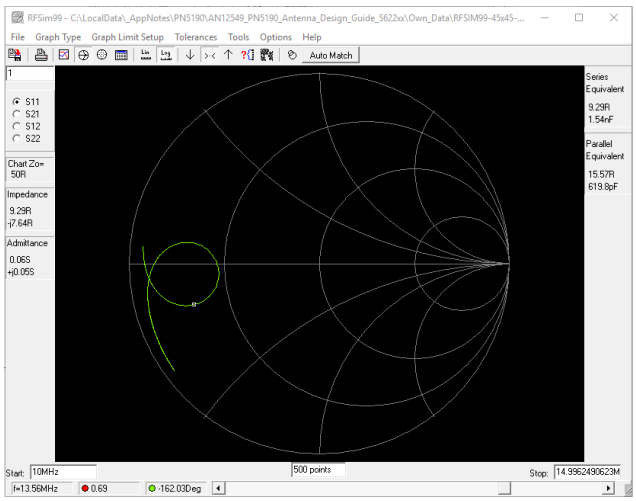
With all these three corrections the simulation plot matches the measurement, as shown in



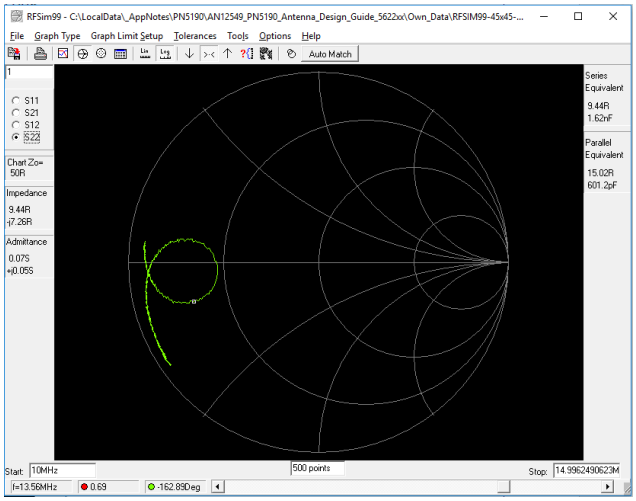
1. The antenna is not properly tuned yet!

Figure 51. Adapted simulation plot to match the measured plot

Correct the simulation



S11: simulated plot



S22: measured plot

Figure 52. Smith chart comparison after adaptation

So after this adaptation we can assume that our simulation is accurate enough to represent the reality.

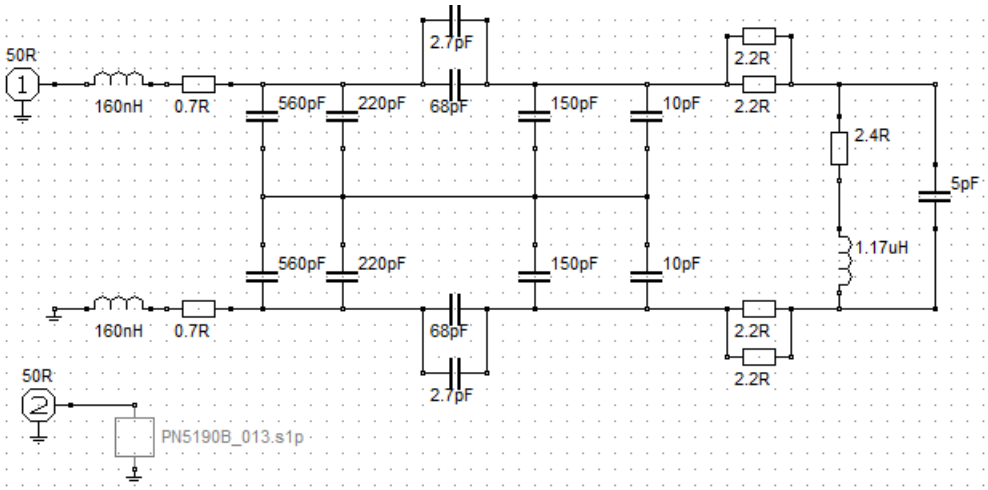
Now the last step it to retune the circuit to meet our original target: get a symmetrical plot with the parallel resonance at the target impedance.

4.8 Correct the simulation

After the unknown values have been adapted in such a way, that the simulation matches the reality, in a final step the tuning needs to be corrected in such way to get a symmetrical tuning to meet the target impedance. This is done:

- Reduce C2 to C2 = 10 pF
- Increase C1 to C1 = 68 pF || 2.7 pF

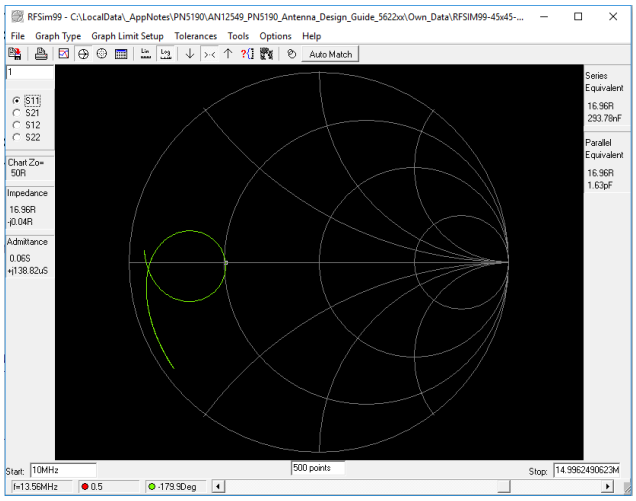
With these changes, the target impedance should be ok, as the simulation result shows in Figure 53 and Figure 54.



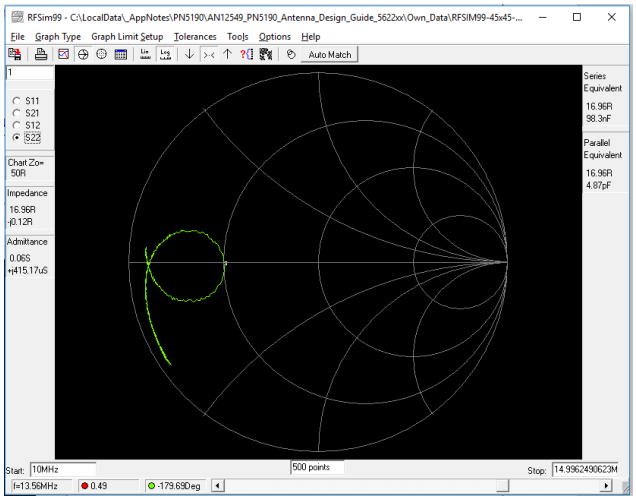
1.

Figure 53. Corrected simulation circuit to meet the target impedance

With these values, the target impedance is supposed to be at 17 Ω.



S11: Corrected simulation plot

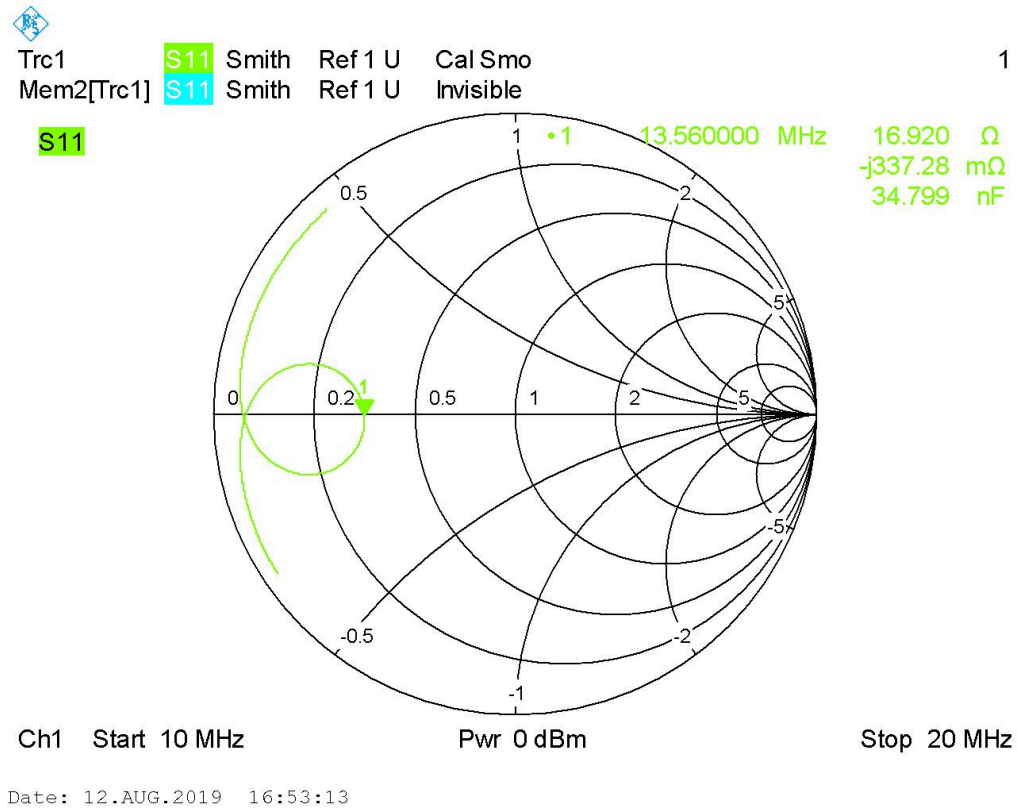


S22: measured corrected plot

Figure 54. Corrected simulation plot to meet the target impedance

4.9 Finalize tuning

The real measurement (already shown as S11-File in Figure 54) then shows the correct tuning, which is already finally tuned, as shown in Figure 55.



1. No further fine-tuning is required.

Figure 55. Final antenna tuning measurement

4.10 RX Circuit

The RX Circuit is a simple coupling of the EMC filter output to the RX inputs, providing a capacitor for DC decoupling and a resistor, as shown in Figure 56.

The value must be:

Crx = 1 nF

Rrx = 560…1500 Ω

More details tbd.

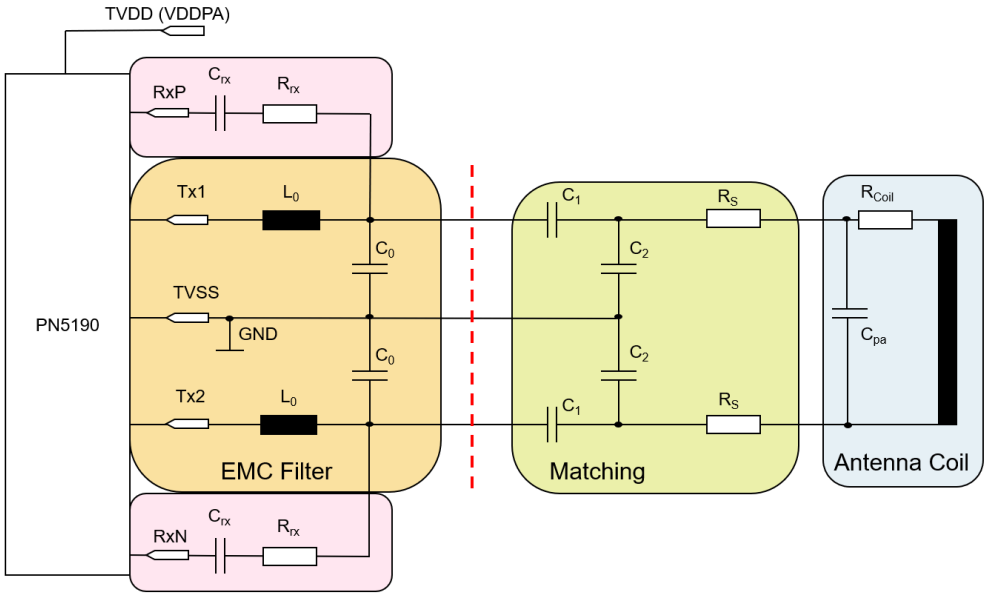


Figure 56. PN5190 complete antenna circuit (including RX)

5 PN5190 and Dynamic Power Control (DPC)

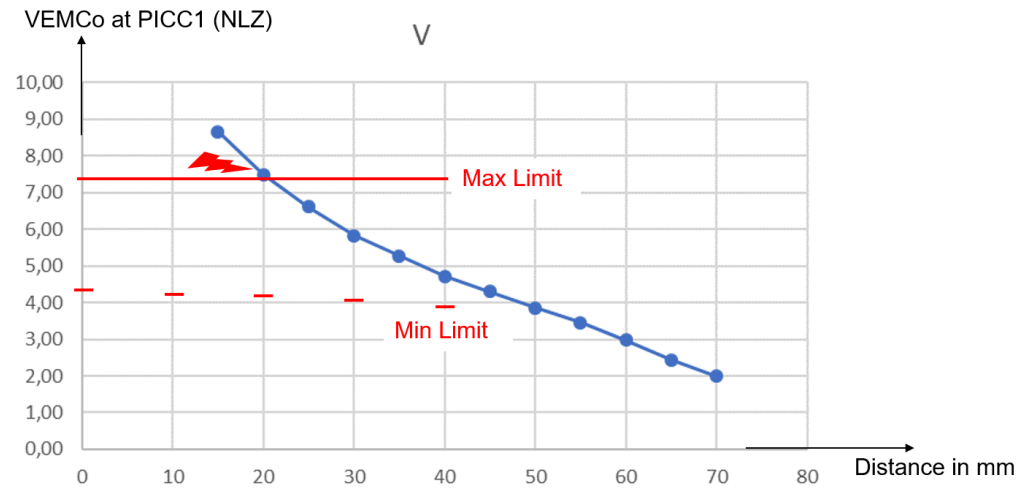
The PN5190 antenna tuning is optimized to provide a maximum power transfer for a large operating distance (related to the antenna size), i.e. it is optimized for the case of very low coupling. This provides the maximum possible power transfer operating distance.

5.1 Bad example with no DPC

However, as soon as the PICC comes closer to the PCD antenna, the loading and detuning causes an increase of the driver current ITVDD as well as an increase of the power transfer. That can easily result in too much RF field (power transfer) for the PICC as well as too much driver current (ITVDD). Examples measured with the EMVCo 3.0 TestPICC1 for the 45 mm x 45 mm antenna are shown in Figure 57 and Figure 58.

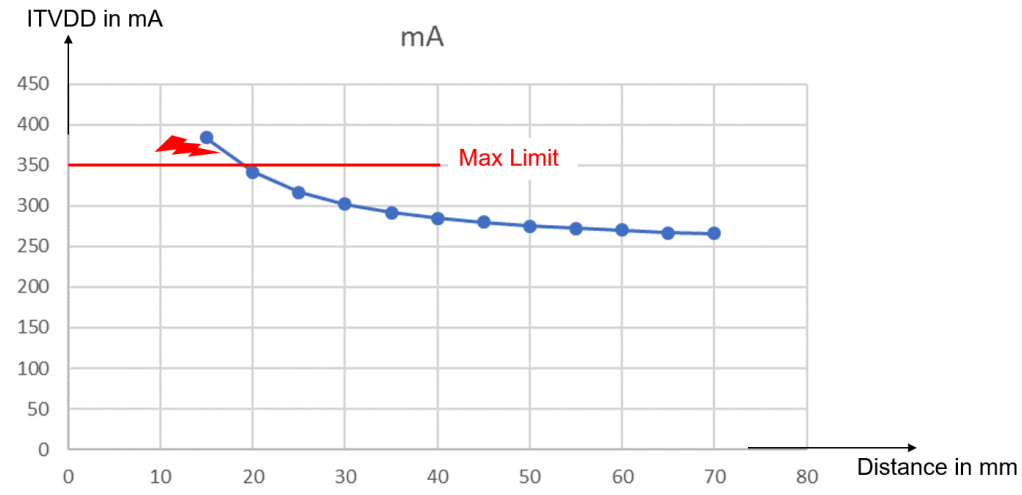
Below 20 mm the maximum power transfer is exceeded as well as the ITVDD limit of the PN5190. That might both destroy the PICC and the PCD, and at least violates the specifications.

Note: *The PN5190 has an overcurrent protection, which switches off the RF field in case of over temperature, as well as an over temperature protection, which resets the PN5190 in case of over temperature. However, in a good PCD design, these protections should never be triggered during normal operation.*



1. 45 mm x 45 mm antenna

Figure 57. EMVCo Power transfer example without DPC



1. 45 mm x 45 mm antenna

Figure 58. TX Driver current (ITVDD) example without DPC

5.2 First step of DPC: Current limiter

To avoid such kind of specification violation, the PN5190 DPC provides a current limiter function, which can be configured.

The first step of configuration is the definition of a “target current”. The PN5190 DPC automatically controls the VDDPA (supply voltage of the TX driver) from maximum 5.7 V down to 1.5 V in 43 100 mV-steps, keeping the driver current (ITVDD) constant at the target current +/- a hysteresis.

Both, the target current (DPC_TARGET_CURRENT) as well as the hysteresis (DPC_HYSTERESIS for loading and unloading) can be defined in EEPROM (see [1]).

5.2.1 DPC_TARGET_CURRENT

The target current (DPC_TARGET_CURRENT, 0x77 & 0x78) defines the nominal current, which drives the antenna. As soon as the ITVDD exceeds the target current (including a hysteresis), the VDDPA is reduced automatically. This does not only protect the PN5190, but also helps to keep the field strength limits (of ISO, NFC or EMVCO).

For EMVCo POS design, the easiest way is to measure the ITVDD with the TestPICC (e.g. TestPICC1) in 4 cm distance, and then write these values into the DPC_TARGET_CURRENT. The NFC Cockpit provides a simple interface to do that.

5.2.2 DPC_HYSTERESIS

The hysteresis (DPC_HYSTERESIS_LOADING, DPC_HYSTERESIS_UNLOADING) together with the target current (DPC_TARGET_CURRENT) defines the current limit, at which the DPC automatically decreases or increases the VDDPA.

The VDDPA is automatically reduced, as soon as the current exceeds the DPC_TARGET_CURRENT + DPC_HYSTERESIS_LOADING, and the VDDPA is automatically increased again, as soon as the current is below DPC_TARGET_CURRENT – DPC_HYSTERESIS_UNLOADING.

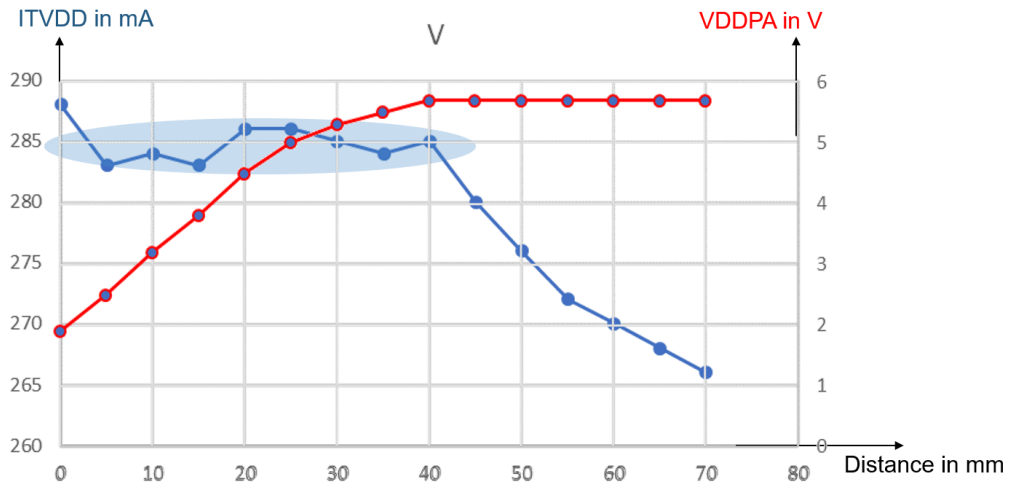
The hysteresis shall not be less than 20 dec (loading) and 10 dec (unloading). So normally the default values should not be changed – other than for test purposes.

The Figure 59 shows an example with the current ITVDD and the related TX driver supply voltage VDDPA under loading conditions. The TestPICC1 is used to load the 45 mm x 45 mm antenna. The target current is set to 285 mA, and all current reduction values in the LUT are reset to 0 (this is no default setting!).

Below 40 mm operating distance the DPC current limiter reduces the VDDPA, which then keeps the current within the defined window of 285 mA +/- 20 mA. This protects the PN5190 and the overall power supply circuit.

Note: *The default control range of the VDDPA is limited to 2.2 V … 5.7 V, using the RDON feature. Still if the loading is too strong, the current might increase above the targeted limit, since the VDDPA cannot decrease further.*

Note: *The minimum VDDPA can be set, if needed, using the TXLDOVDDPALOW (0x7D). Using the RDON feature, it is recommended to use the TXLDOVDDPALOW = 2.2 V, in all other cases the lowest setting of 1.5 V typically is the best choice. The DPC calibration should be done for the full VDDPA range from 1.5 V to 5.7 V. Then the lower limit of the VDDPA can be easily adjusted afterwards to any higher value (enabling or disabling the RDON feature), if needed, without retouching the DPC calibration as such.*

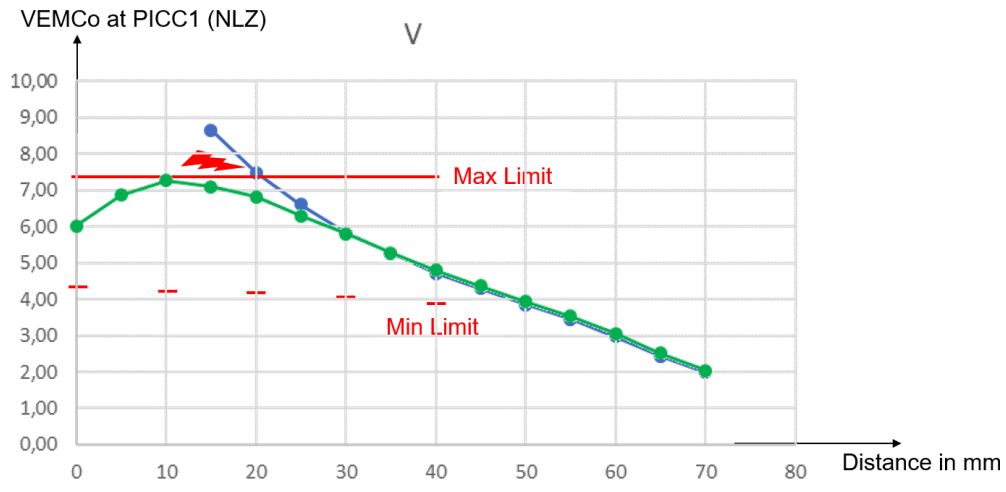


1. 45 mm x 45 mm antenna, target current = 285 mA

Figure 59. ITVDD & VDDPA with automatic current limiter

The Figure 60 shows the EMVCo Power transfer measured with the EMVCo TestPICC1, for the same use case with the current limiter as shown in Figure 59. It can be seen that the current limiter already helps to meet the EMVCo power transfer limits. However, there is no good margin in this example: at 1cm distance the maximum power limit is almost reached. So it would be useful not only to apply a current limiter, but to enable a further current reduction (= power reduction) under these loading conditions (TestPICC in the range of around 1 cm).

That introduces the next related feature to enhance the control of the power transfer, which is called “current reduction”. That is shown in the second step.



1. 45 mm x 45 mm antenna

Figure 60. EMVCo power transfer with automatic current limiter

5.3 Second step of DPC: Current reduction

As shown in Figure 60, the pure current limiter might not be good enough to properly meet the specification limits. So in addition to the current limiter (“target current”), the PN5190 DPC offers a current reduction lookup table (DPC_LOOKUP_TABLE, see [1]), which allows a reduced current for each of the 43 VDDPA steps (if TXLDOVDDPALOW = 1.5 V).

5.3.1 DPC_LOOKUP_TABLE

The DPC_LOOKUP_TABLE (DPC LUT) defines a 4 byte entry per VDDPA step, from 5.7 V down to 1.5 V (resulting in 43 entries).

BYTE 0 (LSByte): This byte defines the current reduction at this VDDPA(new). The value is an unsigned integer value: The final target current is the DPC_TARGET_CURRENT – current reduction value.

The DPC takes the current measurement and calculates a load:

Load = VDDPA(old) / ITVDD

Based on this load the “new” VDDPA = VDDPA(new) can be calculated. The VDDPA(new) would be the applied VDDPA, if no extra current reduction is defined:

VDDPA(new) = Load · target current

In a second step now the required current reduction is applied, which then results in the final VDDPA = VDDPA(target):

VDDPA(target) = Load · (target current – current reduction @ VDDPA(new))

Example:

Assumption 1: Unloaded ITVVD = 300 mA @ VDDPA = 5.7 V (due to the antenna tuning)

Assumption 2: Target current = 300 mA (set in DPC_TARGET_CURRENT)

Assumption 3: Current reduction @ 5.3 V = 20 mA (set in the related entry of DPC_LOOKUP_TABLE)

As soon as the loading changes, and the ITVDD exceeds the 320 mA, the DPC needs to switch the power level.

Load = 5.7 V / 320 mA = 17.8 Ω -> VDDPA(new) = 17.8 Ω · 300 mA = 5.3 V

VDDPA(target) = 17.8 Ω · (300 mA - 20 mA) = 5.0 V

So the DPC switches down to 5.0 V.

Attention: To get a certain ITVDD at a certain VDDPA = VDDPA(target), the current reduction value of the corresponding VDDPA(new) must be set. The VDDPA(new) is the related VDDPA value **without** current reduction.

Example above: To achieve the ITVDD = 280 mA at VDDPA = 5.0 V, the current reduction of 20 mA must be set into the LUT entry at the VDDPA = 5.3 V.

The NFC Cockpit DPC calibration provides a calculation, which creates some major LUT entries, based on a few measurements.

Attention: The current reduction for a lower VDDPA might be even higher than the one of the next higher VDDPA, as long as the calculated load (load = VDDPA / ITVDD) is equal or higher than the one of the next higher VDDPA. Otherwise the DPC might start oscillating.

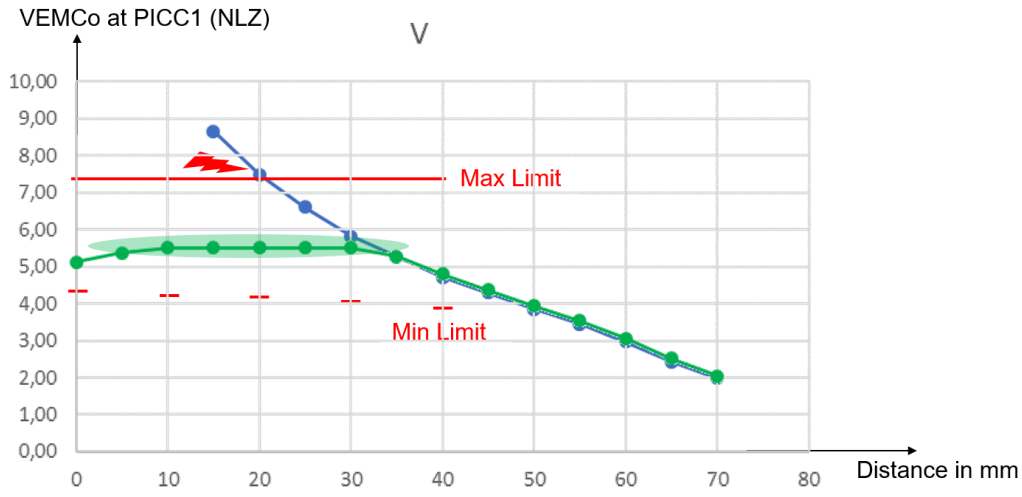
The BYTE 1, BYTE 2, and BYTE 3 are not relevant for the DPC calibration itself, so they have no impact of the power transfer. However, they are used to define a dynamic adjustment of TX Shaping parameters. The details of the TxShaping explained in AN12551.

BYTE 1: This byte defines a relative change of the modulation index. It is a signed integer value, which is added to the RESIDUAL_AMPL_LEVEL of the applied protocol.

BYTE 2: This byte defines the relative change of the rise and fall time parameter (EDGE_STYLE) of the 100 % ASK (e.g. type A 106). It is a signed integer which is added to the EDGE_STYLE of the applied protocol (in case of 100 % ASK), if the FW-based TxShaping is used.

BYTE 3: This byte defines the relative change of the rise and fall time parameter (EDGE_STYLE) of the 10 % ASK (e.g. type B 106). It is a signed integer which is added to the EDGE_STYLE of the applied protocol (in case of 10 % ASK), if the FW-based TxShaping is used.

With this feature of current reduction per VDDPA step, the power transfer can be optimized. The Figure 61 shows the power transfer measurement with **manually** adjusted current: that power transfer might be taken as the target for the DPC calibration, as described in the following.



1. 45 mm x 45 mm antenna

Figure 61. EMVCo power transfer with manual current reduction (target)

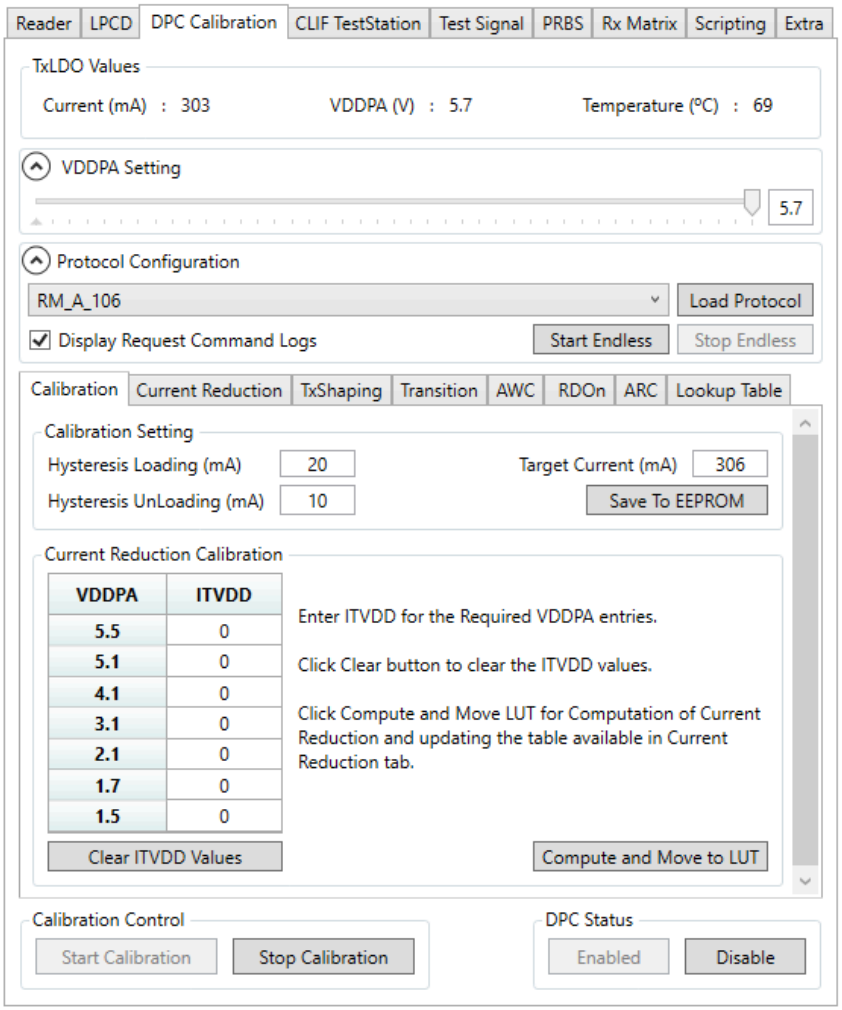
5.4 PN5190 DPC calibration

To operate the PN5190 with optimum performance, only a few settings must be defined. These settings can easily be adjusted with the NFC Cockpit.

5.4.1 Set target current

The first value is the target current:

For EMVCo POS design, the easiest way is to measure the ITVDD with the TestPICC (e.g. TestPICC1) in 4 cm distance, and then write these values into the DPC_TARGET_CURRENT. The NFC Cockpit provides a simple interface to do that, as shown in Figure 62.



1. The DPC calibration loop reads continuously the ITVDD and the temperature, and indicates the VDDA.

Figure 62. NFC Cockpit: DPC Calibration entry of target current and hysteresis

It is recommended to set the target current, but not to change the hysteresis value (other than for test purposes).

The target current should be such, that the PN5190 does not reduce the VDDPA without major loading.

For EMVCo: The TestPICC1 might be good to check the power transfer in 4 cm distance, which gives a reasonable amount of loading (depending on PCD antenna size). Typically the current ITVDD increases by 15…20mA from unloaded, as soon as the TestPICC1 is placed into position 400.

In combination with the given hysteresis, it might be a good starting point to use the target current anywhere in between the unloaded current and the ITVDD with the TestPICC in 400.

5.4.2 Set current reduction

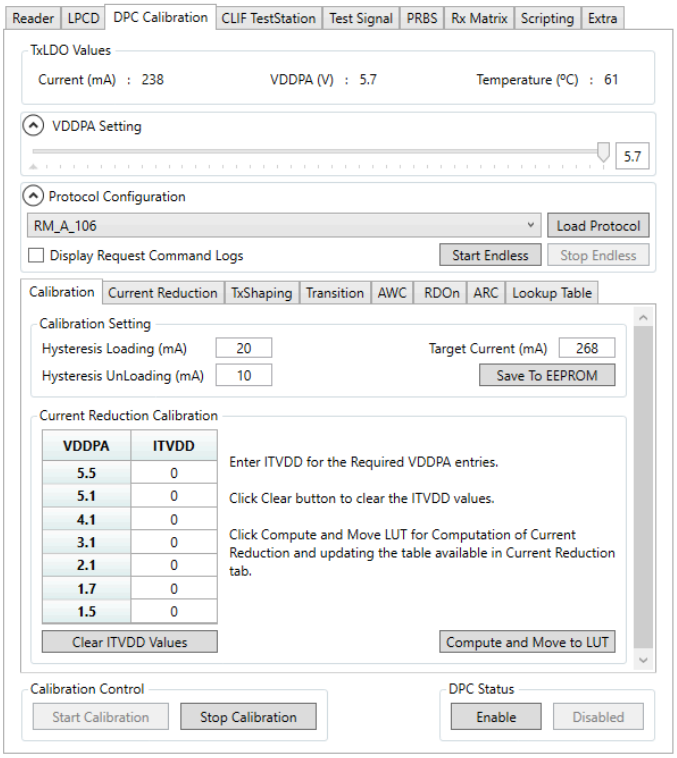
The current reduction must be carefully set to avoid a DPC oscillation. The NFC Cockpit provides a function to quickly measure the current at 7 VDDPA positions and then calculate the related current reduction values out of that. Then the remaining empty current reduction LUT entries must be filled manually with interpolation.

This is normally good enough to retrieve a nicely working DPC calibration.

However, the more accurate alternative is to use the NFC Cockpit and measure each VDDPA separately and calculate all related values.

The principle of measuring the required current reduction is the same in both methods:

1. Start DPC calibration & Disable DPC
2. Stop DPC calibration & Reset PN5190 (“Soft Reset”)
3. Restart the DPC Calibration & Load Protocol A106



1. Unloaded condition: ITVDD = 238 mA

Figure 63. DPC Calibration start with disabled DPC

Then the measurement of the required ITVDD at a certain VDDPA can be done:

1. Adjust the required VDDPA using the VDDPA slider
2. Apply the required loading, e.g. with the EMVCo TestPICC in such a way, that under the given VDDPA in whatever distance the required power transfer is achieved.
3. Read the current ITVDD.

Note: *Be aware that with disabled DPC there is no current limiter. The resulting current ITVDD depends on the loading condition, and might exceed the PN5190 limits, if not taken care by the user!*

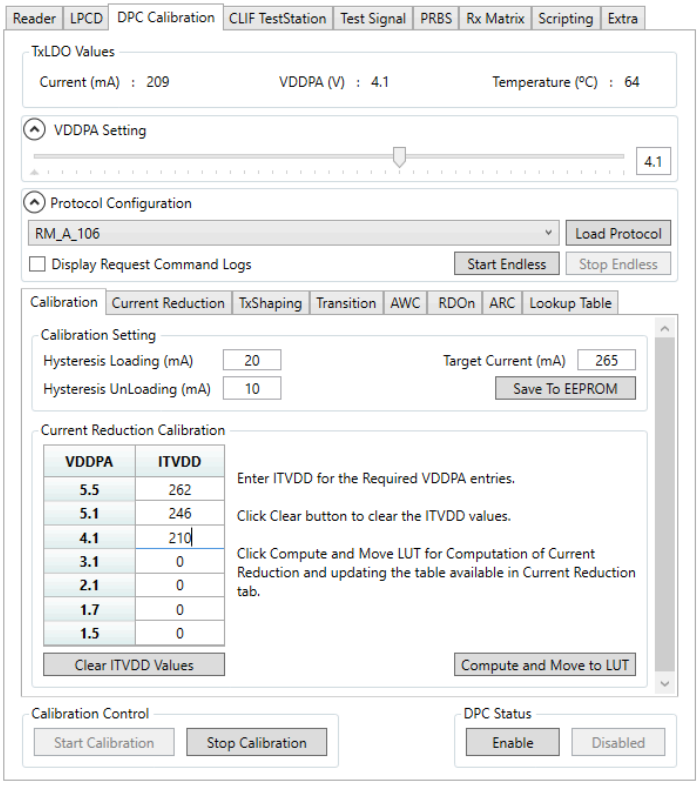
5.4.2.1 NFC Cockpit current reduction calibration fast method

The NFC Cockpit provides a simple support to calibrate the DPC. It calculates 7 LUT entries out of a measurement procedure.

The user needs to enter the target condition (= target ITVVD) for 7 different VDDPA levels.

Figure 64 shows the example measurement at VDDPA 4.1 V: the applied load (e.g. a TestPICC in a certain distance, which shows the targeted power transfer) causes an ITVDD of 208…210 mA.

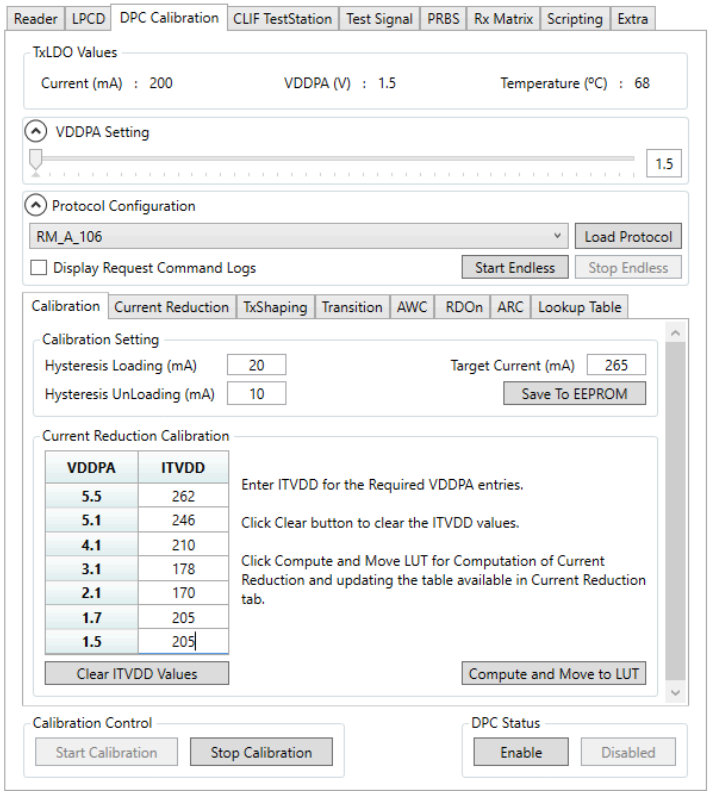
So the DPC LUT should be set in such a way that the DPC loop targets the 210 mA at 4.1 V, to achieve the same power transfer when enabling the DPC later.



1. The load applied results in ITVDD = 210 mA @ VDDPA = 4.1 V

Figure 64. DPC Calibration with NFC Cockpit, calibrating

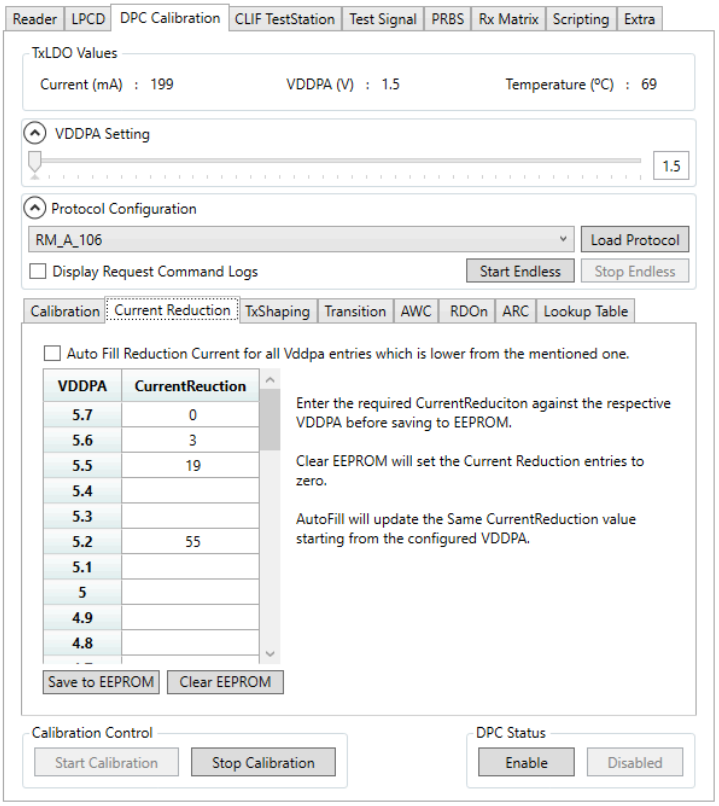
When all 7 measurements are done, the NFC Cockpit (as shown in Figure 65) can calculate the related LUT entries, clicking the <Compute and Move to LUT>.



1. All measurements done

Figure 65. DPC Calibration with NFC Cockpit, measurements done

Then the NFC cockpit switches to the second subtab, and 7 entries are indicated in the LUT as shown in Figure 66. The empty LUT entries must now be filled manually, before the complete LUT can be saved in EEPROM.

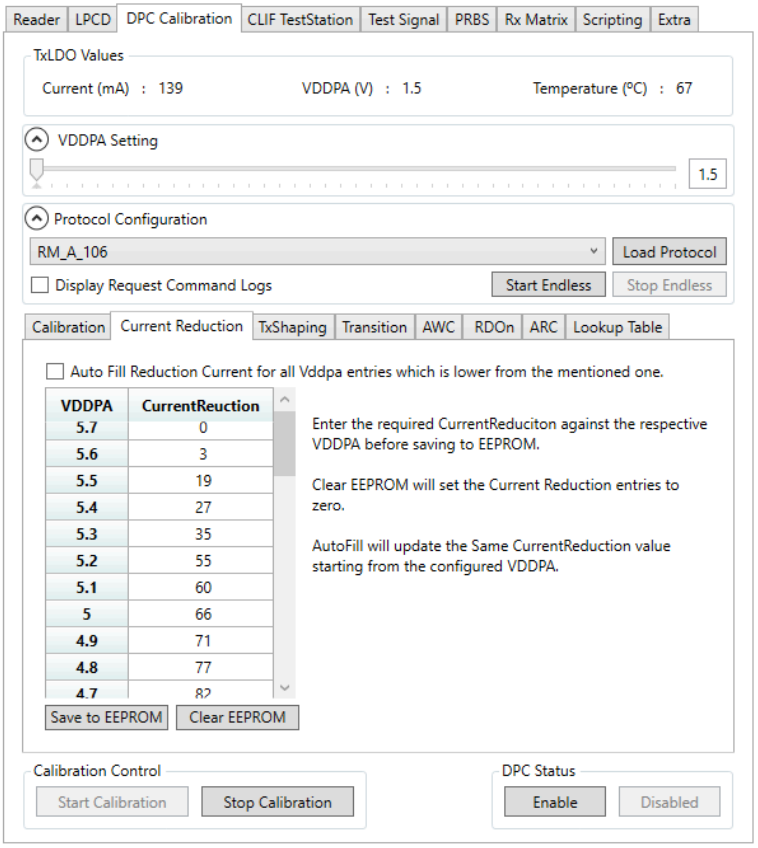


1. The empty entries need to be filled manually (interpolation).

Figure 66. DPC Calibration with NFC Cockpit, LUT start

To fill the missing LUT entries, the in-between values can simply be interpolated, like shown in Figure 67.

As soon as all LUT entries are filled, they can be saved into EEPROM, using the <Save to EEPROM> button. Then the DPC is calibrated, but only needs to be enabled again.



1. The complete LUT must be saved to EEPROM

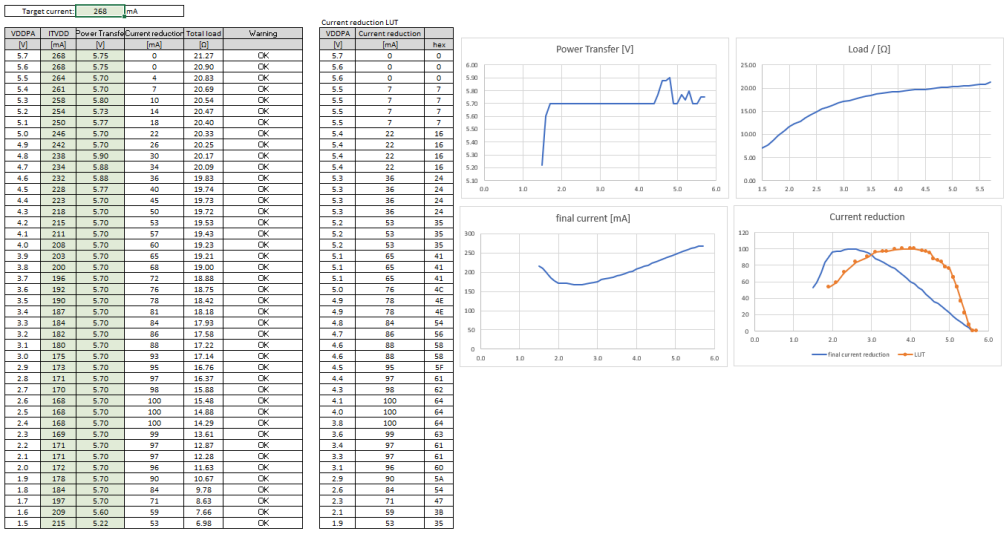
Figure 67. DPC Calibration with NFC Cockpit, all LUT entries filled

5.4.2.2 NFC Cockpit current reduction calibration accurate method

The manual interpolation normally is accurate enough. However, the LUT can be filled manually with an accurate measurement for each of the given VDDPA values, if needed.

NXP provides an excel sheet to perform the calculation and help to visualize the calibration results, as shown in Figure 68.

The way of calibrating is the same as described in Section 5.4.2.1, but instead of only 7, all 43 VDDPA steps are measured.



Target current: 268 mA

VDDPA [V]	ITVDD [mA]	Power Transfer [V]	Current reduction [mA]	Total load [Ω]	Warning
5.7	268	5.75	0	21.27	OK
5.6	268	5.75	0	20.90	OK
5.5	264	5.70	4	20.83	OK
5.4	261	5.70	7	20.69	OK
5.3	258	5.80	10	20.54	OK
5.2	254	5.73	14	20.47	OK
5.1	250	5.77	18	20.40	OK
5.0	246	5.70	22	20.33	OK
4.9	242	5.70	26	20.25	OK
4.8	238	5.90	30	20.17	OK
4.7	234	5.88	34	20.09	OK
4.6	232	5.88	36	19.83	OK
4.5	228	5.77	40	19.74	OK
4.4	223	5.70	45	19.73	OK
4.3	218	5.70	50	19.72	OK
4.2	215	5.70	53	19.53	OK
4.1	211	5.70	57	19.43	OK
4.0	208	5.70	60	19.23	OK
3.9	203	5.70	65	19.21	OK
3.8	200	5.70	68	19.00	OK
3.7	196	5.70	72	18.88	OK
3.6	192	5.70	76	18.75	OK
3.5	190	5.70	78	18.42	OK
3.4	187	5.70	81	18.18	OK
3.3	184	5.70	84	17.93	OK
3.2	182	5.70	86	17.58	OK
3.1	180	5.70	88	17.22	OK
3.0	175	5.70	93	17.14	OK
2.9	173	5.70	95	16.76	OK
2.8	171	5.70	97	16.37	OK
2.7	170	5.70	98	15.88	OK
2.6	168	5.70	100	15.48	OK
2.5	168	5.70	100	14.88	OK
2.4	168	5.70	100	14.29	OK
2.3	169	5.70	99	13.61	OK
2.2	171	5.70	97	12.87	OK
2.1	171	5.70	97	12.28	OK
2.0	172	5.70	96	11.63	OK
1.9	178	5.70	90	10.67	OK
1.8	184	5.70	84	9.78	OK
1.7	197	5.70	71	8.63	OK
1.6	209	5.60	59	7.66	OK
1.5	215	5.22	53	6.98	OK

Current reduction LUT

VDDPA [V]	Current reduction [mA]	hex
5.7	0	0
5.6	0	0
5.6	0	0
5.5	7	7
5.5	7	7
5.5	7	7
5.4	22	16
5.4	22	16
5.4	22	16
5.4	22	16
5.3	36	24
5.3	36	24
5.3	36	24
5.3	36	24
5.2	53	35
5.2	53	35
5.2	53	35
5.1	65	41
5.1	65	41
5.0	76	4C
4.9	78	4E
4.9	78	4E
4.8	84	54
4.7	86	56
4.6	88	58
4.6	88	58
4.5	95	5F
4.4	97	61
4.3	98	62
4.1	100	64
4.0	100	64
3.8	100	64
3.6	99	63
3.4	97	61
3.3	97	61
3.1	96	60
2.9	90	5A
2.6	84	54
2.3	71	47
2.1	59	3B
1.9	53	35

1. 50 mm x 30 mm antenna

Figure 68. Example of DPC Calibration, using DPC_LUT excel sheet

In this example, the EMVCo TESTPICC (EMVCo 2.6) is used to load and define the DPC current values. The measurement starts with disabled DPC, VDDPA = 5.7 and the TestPICC placed in 70 mm above. This can be seen as “unloaded”: moving the TESTPICC further away does not influence the current value.

Moving the TestPICC in steps of 5 mm, the VDDPA and the ITVDD is measured (reading from NFC Cockpit) and the EMVCo power transfer is checked (Vdc at the TestPICC) at each step.

At 40 mm distance the current value can be read: ITVDD = 268 mA. This is taken as input for the DPC_TARGET_CURRENT.

The power transfer at this point is 5.75 V, measured at the TestPICC. This value now shall be the target over the full calibration range.

When switching the VDDPA to 5.6 V, the ITVDD decreases as well as the power transfer. Correcting the operating distance, shows that at a slightly lower distance, with the same current the same power transfer can be achieved. So the target current for VDDPA = 5.6 V is 268 mA, too.

When switching the VDDPA to 5.5 V, the ITVDD decreases as well as the power transfer. Correcting the operating distance, shows that at a slightly lower distance, the current to achieve the same power transfer is slightly less than before. So the target current for VDDPA = 5.5 V is 264 mA.

Stepping down the VDDPA step by step, for each VDDPA the current is noted down, which is required to achieve the power transfer of ≈ 5.75 V.

It can be seen, that at VDDPA = 5.3 V, the current of 255 mA, which is required to achieve the power transfer of 5.75 V, cannot be taken, since with that combination of VDDPA and ITVDD the load increases at lower VDDPA. That would lead to an undefined DPC condition and shall be avoided. So the current must be increased, until the load = VDDPA / ITVDD is lower than the previous one.

For the VDDPA = 5.3 V, the current is raised here to 258 mA.

This measurement needs to be done for all VDDPA steps. For each step, the conditions are:

1. the power transfer is at its target,
2. the load is lower than the load in the previous (higher) VDDPA step.

The example is shown in Table 5.

Table 5. Current reduction LUT example

In case of ambiguity, the higher current is taken.

VDDPA / [V]	ITVDD / [mA]	Load / [Ω]	LUT VDDPA	Current reduction
5.7	268	21.27	5.7	0
5.6	268	20.90	5.6	0
5.5	264	20.83	5.6	0
5.4	261	20.69	5.5	7
5.3	257	20.62	5.5	7 (instead of 11)
5.2	254	20.47	5.5	7 (instead of 14)
5.1	250	20.40	5.5	7 (instead of 18)
5.0	246	20.33	5.4	22
4.9	242	20.25	5.4	22 (instead of 26)
4.8	238	20.17	5.4	22 (instead of 30)
4.7	234	20.09	5.4	22 (instead of 34)
4.6	232	19.83	5.3	36
4.5	228	19.74	5.3	36 (instead of 40)
4.4	223	19.73	5.3	36 (instead of 45)
4.3	218	19.72	5.3	36 (instead of 50)
4.2	215	19.53	5.2	53
4.1	211	19.43	5.2	53 (instead of 57)
4.0	208	19.23	5.2	53 (instead of 60)
3.9	203	19.21	5.1	65
3.8	200	19.00	5.1	65 (instead of 68)
3.7	196	18.88	5.1	65 (instead of 72)
3.6	192	18.75	5.0	76
3.5	190	18.42	4.9	78
3.4	187	18.18	4.9	78 (instead of 81)
3.3	184	17.93	4.8	84
3.2	182	17.58	4.7	86
3.1	180	17.22	4.6	88
3.0	175	17.14	4.6	88 (instead of 93)
2.9	173	16.76	4.5	95
2.8	171	16.37	4.4	97

Table 5. Current reduction LUT example*...continued*

In case of ambiguity, the higher current is taken.

VDDPA / [V]	ITVDD / [mA]	Load / [Ω]	LUT VDDPA	Current reduction
2.7	170	15.88	4.3	98
2.6	168	15.48	4.1	100
2.5	168	14.88	4.0	100
2.4	168	14.29	3.8	100
2.3	169	13.61	3.6	99
2.2	171	12.87	3.4	97
2.1	171	12.28	3.3	97
2.0	172	11.63	3.1	96
1.9	178	10.67	2.9	90
1.8	184	9.78	2.6	84
1.7	197	8.63	2.3	71
1.6	209	7.66	2.1	59
1.5	215	6.98	1.9	53

It can be seen that in this example the current even increases again at lower VDDPA. That is possible, since the load always decreases at lower VDDPA.

With these inputs, the current reduction LUT entries can be calculated:

$$LUT\ \ VDDPA = VDDPA \big/ ITVDD \cdot TargetCurrent$$

$$Current\ \ reduction = target\ \ current - ITVDD$$

With

- LUT VDDPA: entry field for the corresponding current reduction
- VDDPA = VDDPA, as set during the calibration measurement
- ITVDD = current, as measured via TXLDO_VOUT_CURR register
- Target current = DPC_TARGET_CURRENT
- Current reduction = decimal value for the LUT

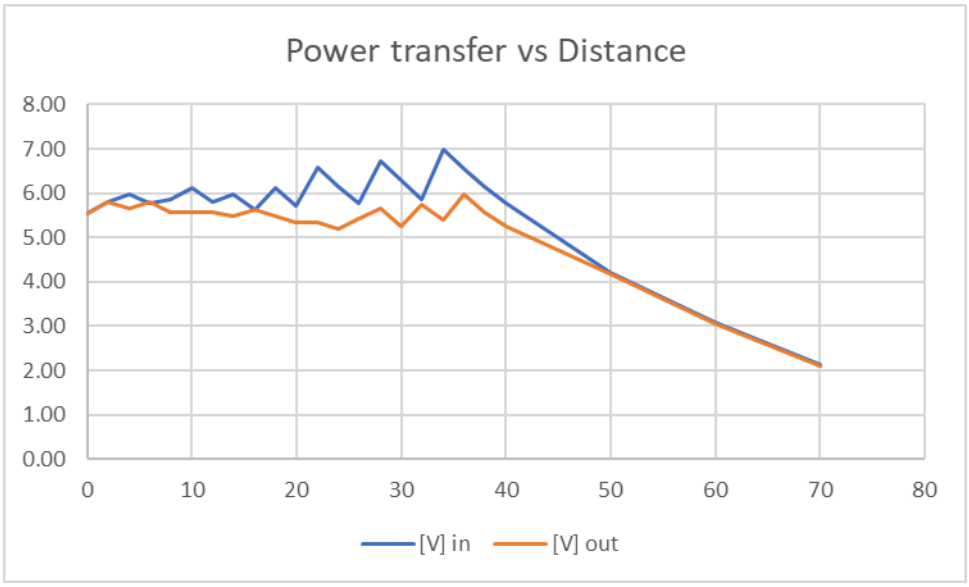
It might happen that different current reduction values are applied to the same VDDPA entry, which of course does not work. In those cases, the first value (which results in the highest ITVDD) should be chosen to avoid ambiguities.

Note: *There might be still some few "empty" LUT entries, which then require a manual interpolation, like VDDPA = 4.2 in the above example, which then can be interpolated with 99.*

With these values written into the DPC_LOOKUP_TABLE, the DPC is properly calibrated. The final measurement with the EMVCo 2.6 TestPICC moving into the field (blue curve) and moving back out of the field (orange curve) can be seen in Figure 69.

With these settings, the overall power transfer with all 3 TestPICCs of EMVCo 3.0 can be met.

Note: *The calibration for EMVCo can be done with either of the TestPICCs. Even the old EMVCo 2.6 TestPICC can be taken (as shown in this example). However, the different voltage limits have to be considered, since all PICCs show different loading and different voltage levels.*



1. Distance in mm, power transfer in V, measured at the EMVCo 2.6 TestPICC
2. 50 mm x 30 mm antenna
3. Blue = moving in; orange = moving out

Figure 69. EMVCo 2.6 power transfer example with final DPC

6 PN5190 RX

The PN5190 receiver itself is completely different than the known RX of PN5180 or CLRC663. It uses DSP with matched filters, providing a higher sensitivity and better robustness. The build Contactless Test Station (CTS) can be used to optimize settings and performance, and for debugging.

However, the overall external circuitry looks the same like known before, as shown in the Figure 70.

So for the optimum performance, only the values of Crx and Rrx must be defined.

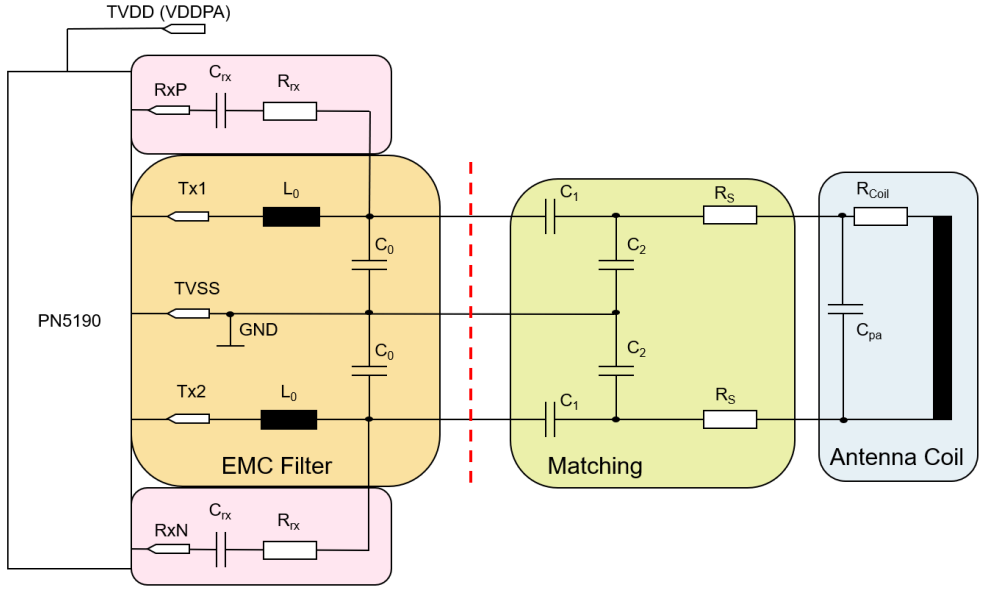


Figure 70. PN5190 antenna circuit including the RX path

C_{RX} = 1 nF

R_{RX} ≈ 560 … 1500 Ω (see below)

Note: *The RX layout shall be symmetrical, as shown in Figure 12.*

6.1 Correct RX coupling

The best value of R_{Rx} can easily be determined with the NFC Cockpit, using this procedure:

1. DPC: <Start Calibration>
2. <Load Protocol>
3. Use unloaded antenna (typical VDDPA = 5.7 V)
4. Read H_ATT_VALUE, RX_CONTROL_STATUS register (0x28), bit 3…8

The target HF_ATT_VALUE should be 40 dec.

Increase R_{Rx}, if the HF_ATT_VALUE is too high.

Decrease R_{Rx}, if the HF_ATT_VALUE is too low.

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Date of release: 23 April 2021
Document identifier: AN12549
Document number: 562211