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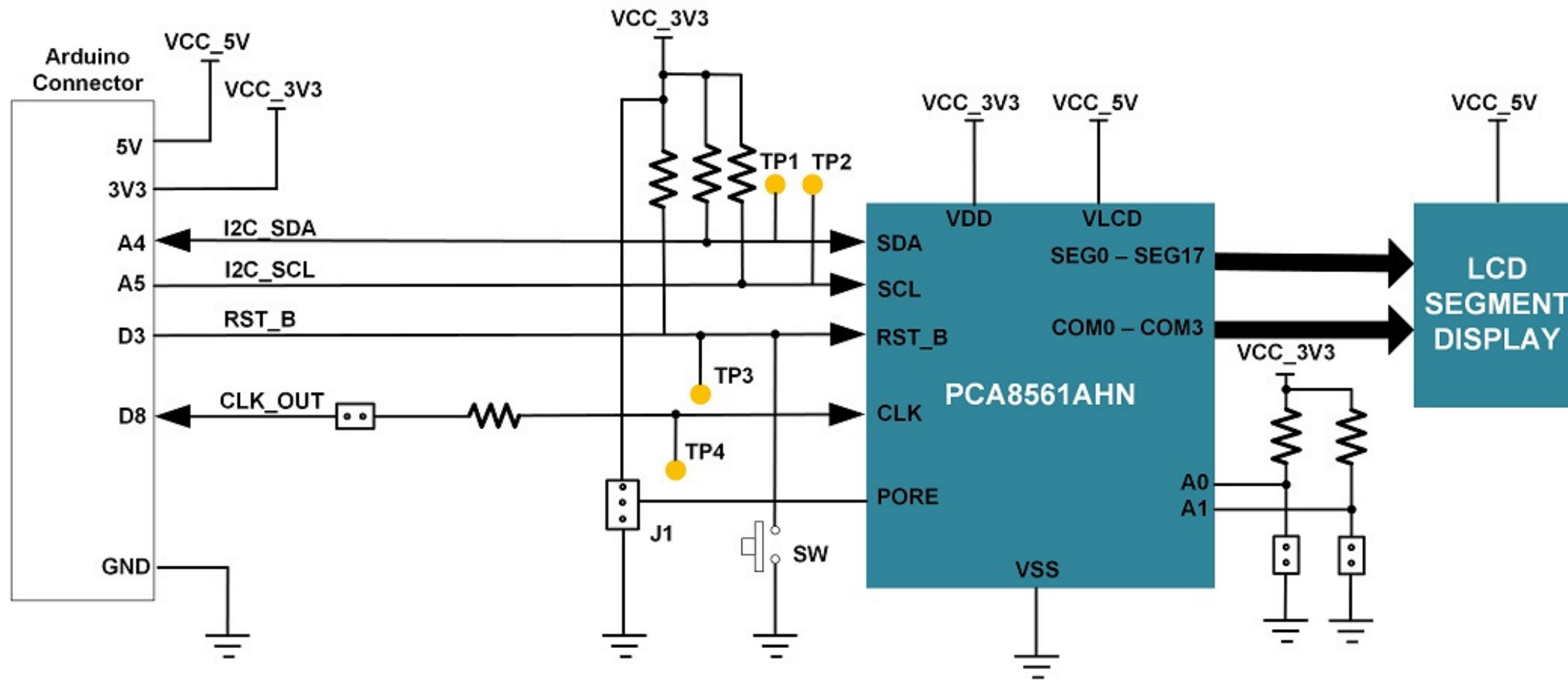
Revisions			
Rev	Description	Date	Approved
X1	First draft (development)	24-JAN-20	Giovanni Genna
A	Final draft (pilot production)	06-FEB-20	Giovanni Genna
B	Release to production	26-FEB-21	Giovanni Genna

PCA8561AHN-ARD

<Core Design>

		Analog Sensor Product Group 6501 William Cannon Drive West Austin, TX 78735-8598	
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Approved: Giovanni Genna	Size B	Document Number SCH-46661 PDF: SPF-46661	Rev B
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BLOCK DIAGRAM



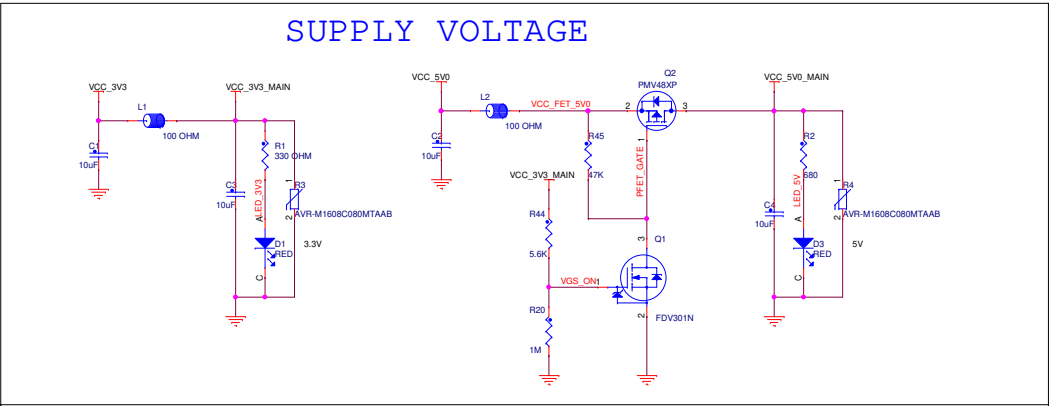
Jumper Table

REF DES	JUMPER(DEFAULT)	JUMPER(OPTION1)	PAGE NAME
J9	1-2 - POR ENABLE	2-3: POR DISABLE	P03_LCD_SEGMENT_DRIVER
J7	2-3 - A0=0	1-2 - A0=1	P03_LCD_SEGMENT_DRIVER
J8	2-3 - A1=0	1-2 - A1=1	P03_LCD_SEGMENT_DRIVER
J10	OFF - INTERNAL CLOCK	ON - EXTERNAL CLOCK	P03_LCD_SEGMENT_DRIVER

<Core Design>

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ARDUINO CONNECTOR



U2									
SEG 0	R ₂₆	0	LCD SEG0	1	S11F1E1D				
SEG 1	R ₂₆	0	LCD SEG1	2	S22F2E2D				
SEG 8	R ₂₆	0	LCD SEG8	5	S33F3E3D				
SEG 14	R ₂₆	0	LCD SEG14	7	S44F4E4D				
					S55F5E5D				
					S66F6E6D				
					S77F7E7D				
					S88F8E8D				
						1H1G1L1M	36	LCD SEG3	R ₂₆ SEG 3
						2H2G2L2M	34	LCD SEG1	R ₂₆ SEG 7
						3H3G3L3M	32	LCD SEG1	R ₂₆ SEG 11
						4H4G4L4M	30	LCD SEG1	R ₂₆ SEG 15
						5H5G5L5M	28		
						6H6G6L6M	26		
						7H7G7L7M	24		
						8H8G8L8M	22		
SEG 1	R ₂₆	0	LCD SEG1	2	1I1J1K1N				
SEG 2	R ₂₆	0	LCD SEG2	4	2I2J2K2N				
SEG 9	R ₂₆	0	LCD SEG9	6	3I3J3K3N				
SEG 13	R ₂₆	0	LCD SEG13	8	4I4J4K4N				
					5I5J5K5N				
					6I6J6K6N				
					7I7J7K7N				
					8I8J8K8N				
						1A1B1C1P	35	LCD SEG2	R ₂₆ SEG 2
						2A2B2C2P	33	LCD SEG2	R ₂₆ SEG 10
						3A3B3C3P	31	LCD SEG1	R ₂₆ SEG 10
						4A4B4C4P	29	LCD SEG14	R ₂₆ SEG 14
						5A5B5C5P	27		
						6A6B6C6P	25		
						7A7B7C7P	23		
						8A8B8C8P	21		
COM0	R ₂₆	0	LCD COM0	20	COM0NC0NC0				
COM1	R ₂₆	0	LCD COM1	19	COM0NC0NC0				
COM2	R ₂₆	0	LCD COM2	18	NC0NC0COM3NC				
COM3	R ₂₆	0	LCD COM3	17	NC0NC0COM4				

MISCELLANEOUS

Test Points

The diagrams illustrate the placement of test points (TPs) for different power supply rails:

- TP5:** Located on the 3V3 rail, connected to VCC_3V3 and 3V3_MAIN.
- TP7:** Located on the 3V3_MAIN rail, connected to 3V3_MAIN and 3V3.
- TP9:** Located on the GND rail, connected to GND and GND.
- TP6:** Located on the 5V0 rail, connected to VCC_5V0 and 5V0_MAIN.
- TP11:** Located on the 5V0_MAIN rail, connected to 5V0_MAIN and 5V0.
- TP10:** Located on the GND rail, connected to GND and GND.