

AN12339

Antenna design guide for NTAG 5 boost

Rev. 1.1 — 30 January 2020
523911

Application note
COMPANY PUBLIC

Document information

Info	Content
Keywords	NTAG 5 boost, Antenna Theory, Antenna Design, Measurement Methods, Antenna Design Procedure
Abstract	NTAG 5 boost needs to be connected to an antenna to access NTAG 5 via NFC interface. This application note provides guidance for designing such antenna.



Revision history

Rev	Date	Description
1.1	20200130	Antenna matching calculation sheet added in the document
1.0	20200116	First release

Contact information

For more information, please visit: <http://www.nxp.com>

1. Introduction

NTAG 5 family is ISO/IEC 15693 and NFC Forum Type 5 Tag compliant, with an EEPROM, SRAM and I²C host interface. This Application note helps to easily design and match antennas for NTAG 5 boost with active load modulation.

2. Antenna basics

2.1 Series and parallel equivalent circuits

2.1.1 Series equivalent circuit of the antenna

The antenna can be described by an inductance L_{sc} in series to a loss resistance R_{sc} . The antenna capacitance C_c is in parallel to this series circuit. This capacitance consists of the inter-turn capacitance and a possibly designed tag capacitance C_{IC} .

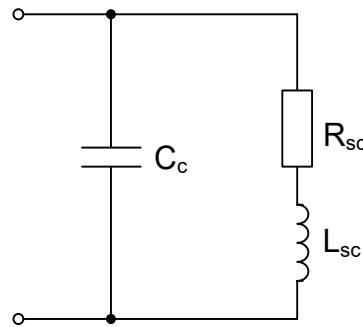


Fig 1. Series equivalent circuit of the antenna

The antenna quality factor is calculated by

$$Q_{sc} = \frac{2 \cdot \pi \cdot f_{op} \cdot L_{sc}}{R_{sc}}$$

with operating frequency $f_{op} = 13.56$ MHz.

2.1.2 Parallel equivalent circuit of the antenna

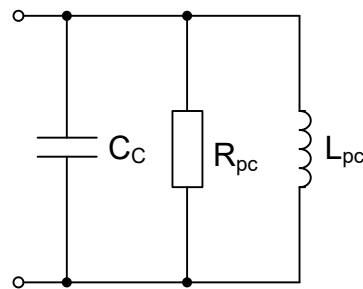


Fig 2. Parallel equivalent circuit of the antenna

The following applies:

$$L_{pc} = \frac{R_{sc}^2 + (2 \cdot \pi \cdot f_{op} \cdot L_{sc})^2}{(2 \cdot \pi \cdot f_{op})^2 \cdot L_{sc}} = L_{sc} \cdot \frac{1 + Q_{sc}^2}{Q_{sc}^2}$$

$$R_{pc} = \frac{R_{sc}^2 + (2 \cdot \pi \cdot f_{op} \cdot L_{sc})^2}{R_{sc}} = R_{sc} \cdot (1 + Q_{sc}^2)$$

$$Q_{pc} = \frac{R_{pc}}{2 \cdot \pi \cdot f_{op} \cdot L_{pc}} = Q_{sc}$$

For the further calculations, the parallel equivalent circuit was chosen to simplify the resonance circuit. This makes calculation easier.

2.2 Q factor adjustment

To get a proper shaping in terms of fall a rise time of the pulse the Q-factor needs to be optimized. The Target Q-factor should not be above 14. The Q-factor should also not be too low as this reduces the performance. To check the proper size of the damping resistors, check the answer shaping (see Fig 3). The target hear is to have a proper shaping as shown on the right signal (Fig 3).

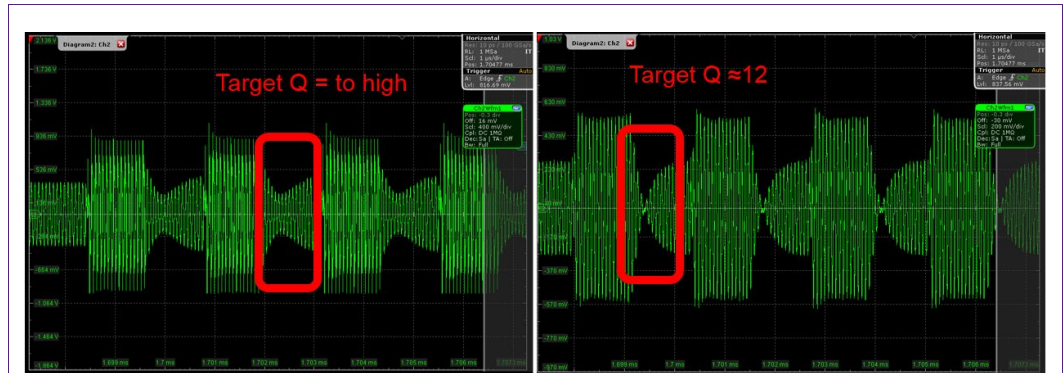


Fig 3. ALM answer shaping

2.3 Antenna sizes

Depending on possible antenna sizes, NTAG 5 link/switch with passive load modulation (PLM) and NTAG 5 boost with active load modulation (ALM) will be used. NTAG 5 boost should be used for antennas smaller or equal class 6. For larger antennas NTAG 5 link/switch should be used (see Fig 4). The active load modulation additionally can be changed from ASK to BPSK mode to increase the response strength even further for smallest antenna sizes.

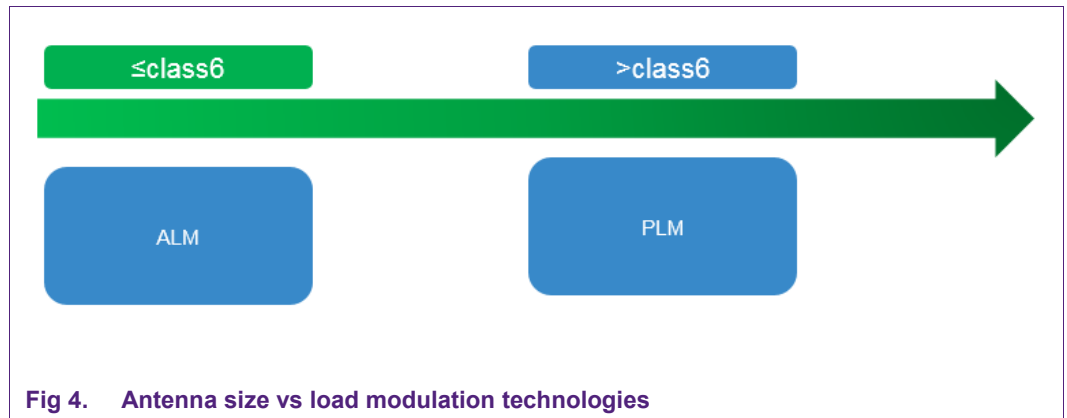


Fig 4. Antenna size vs load modulation technologies

2.4 Antenna design

After fixing the antenna outline, the number of turns shall be chosen in a way to meet the inductance target value. The antenna inductance can be calculated with the NFC antenna design tool available for download on NXP website.

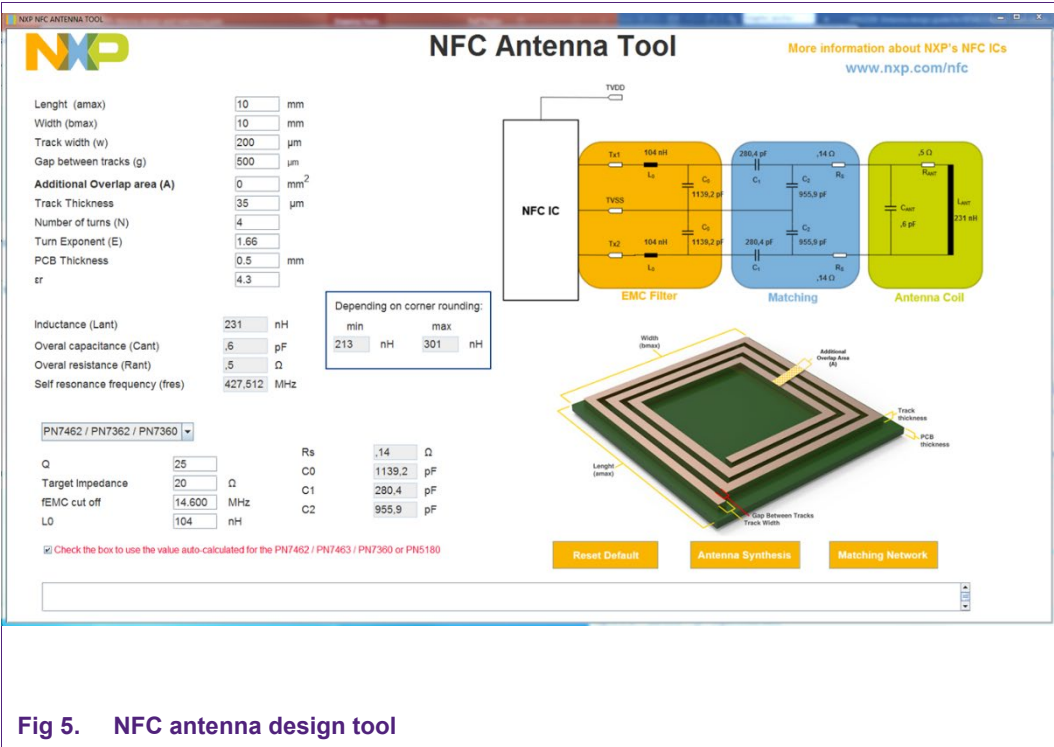


Fig 5. NFC antenna design tool

The tool calculates the inductance with the given size and shaping a big influence has also the rounding of the edges to the inductance.

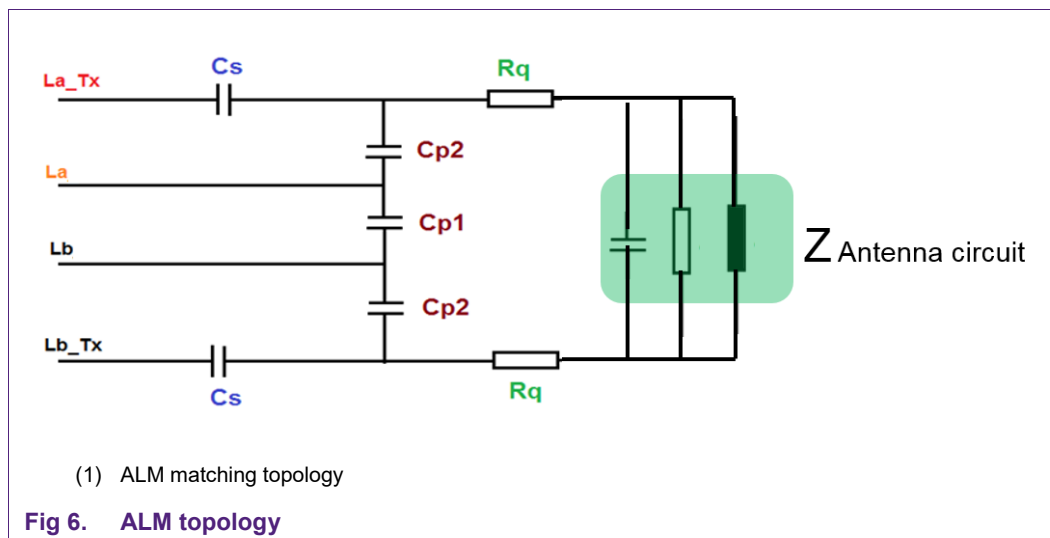
In this case an inductance between 213 nH and 301 nH is calculated.

In this case it is within our targeted range so the antenna prototype can be produced, and the measurement and matching can be done on the prototype.

3. Antenna matching

3.1 Matching topology

The ALM matching topology contains a capacitive voltage divider to guarantee a maximum voltage at the La/Lb Rx pins below 1.4Vp.



3.2 General antenna matching procedure and preparation

For a proper antenna design the antenna impedance must be measured using an impedance analyzer or VNA (vector network analyzer). Such a VNA can be a high-end tool from Agilent or Rohde & Schwarz (like the R&S ZVL), as normally used in this document), but might be a cheap alternative with less accuracy like e.g. the miniVNA Pro (see). In any case the analyzer needs to be able to measure the impedance in magnitude and phase (vector).

Such VNA can be used to measure the antenna coil as well as the antenna impedance including the matching circuit.

The antenna matching is done with the following steps:

1. Measure the antenna equivalent circuit parameters
2. Calculate the matching components
3. Simulate the matching
4. Assembly and measurement
5. Adaptation of simulation
6. Correction and assembly

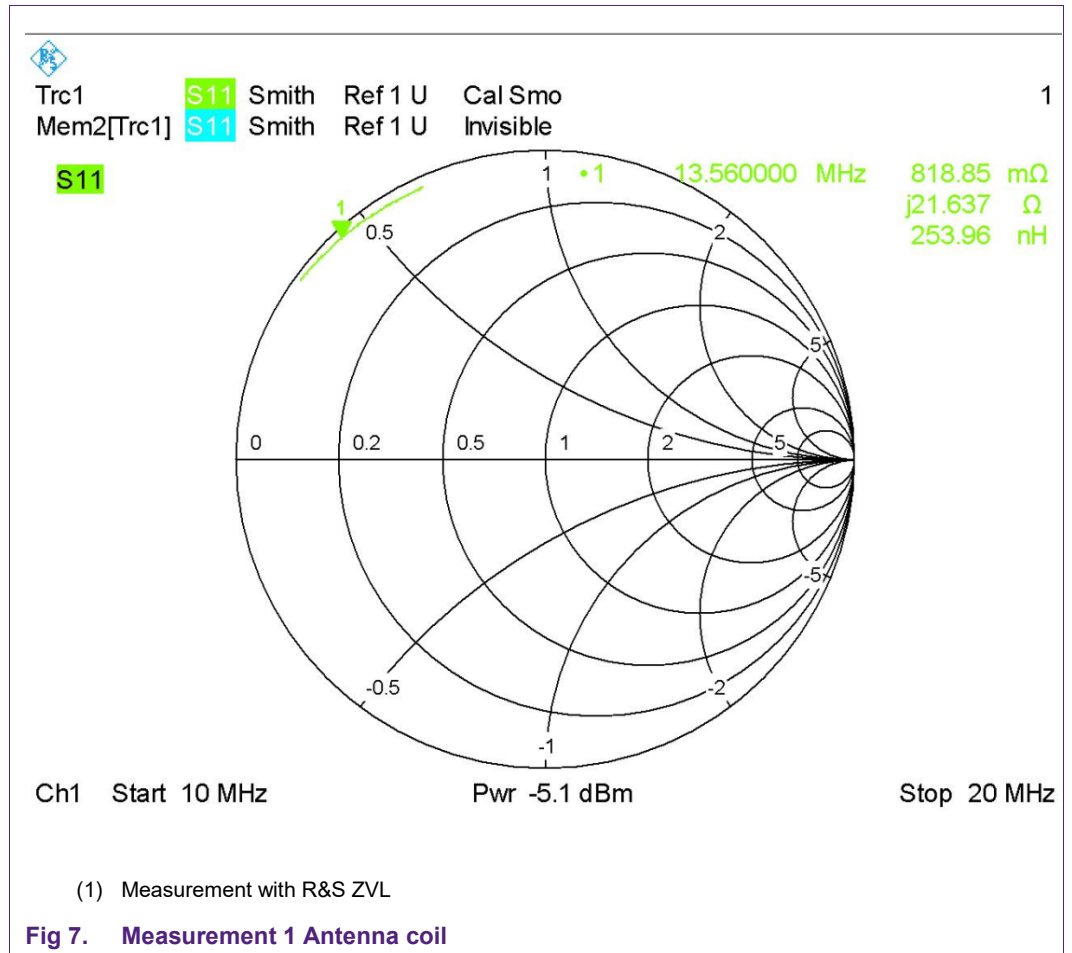
3.2.1 Measure the antenna equivalent circuit parameters

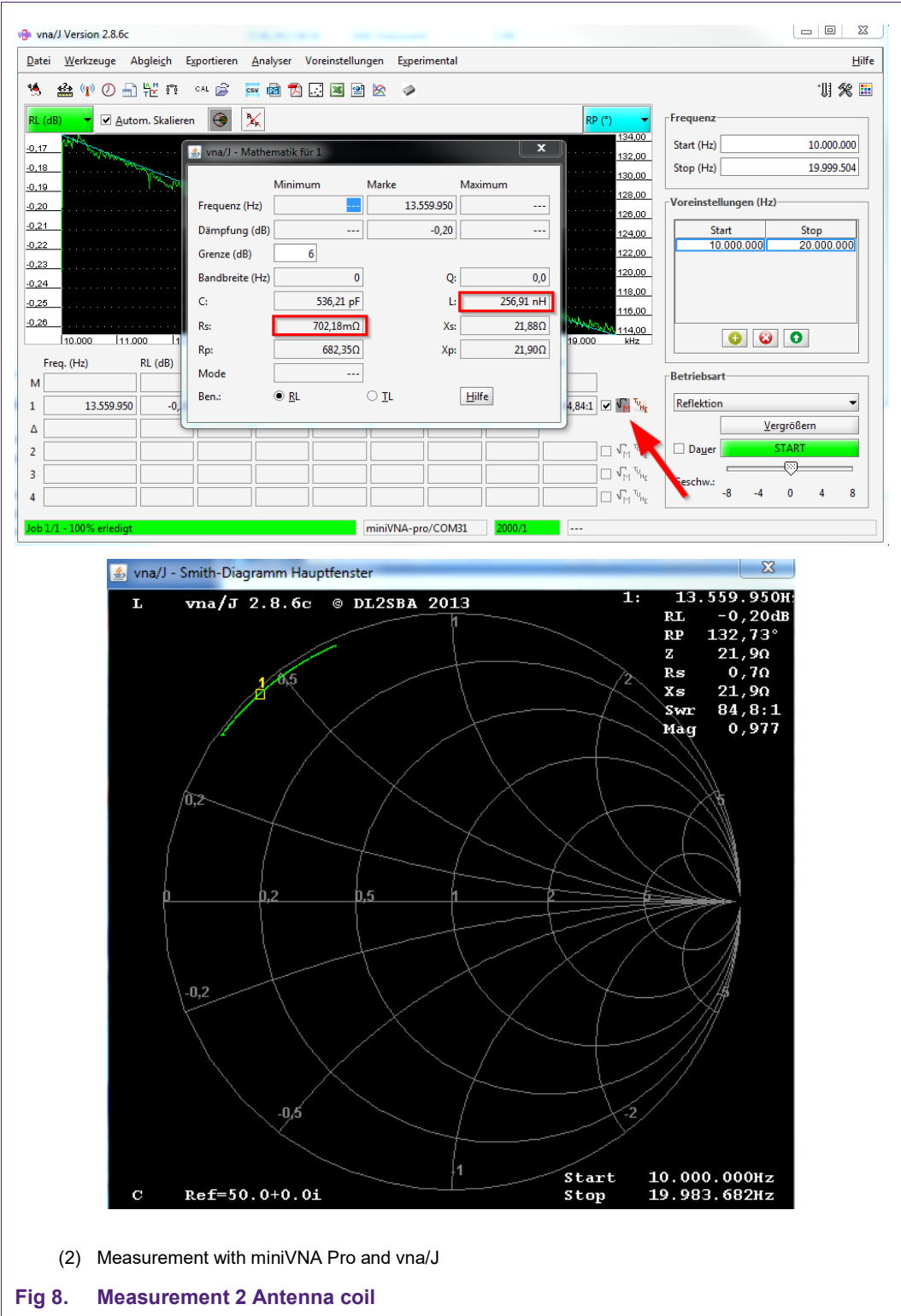
The antenna coil must be designed as described in section 2 be measured. The measurement is required to derive the inductance L , the resistance R_{Coil} and the capacitance C_{pa} as accurate as possible.

The easiest even though not most accurate way is to use the VNA to measure the impedance \underline{Z} of the antenna coil at 13.56MHz and to calculate L and R out of it:

$$\underline{Z} = R + j\omega L_{Coil} \quad (1)$$

Typically, the VNA directly can show the L and R , as shown in Fig 7 and Fig 8.





In this example the antenna coil is measured with these values:

$$L = 253\text{nH}$$

$$R_{\text{Coil}} = 0,7 \dots 0,82\Omega$$

C_{pa} = not measured, can be estimated (typical in the range of 1-8pF)

The inductance can be measured quite accurate, but the resistance is not very accurate due to the relationship between R and $j\omega L$. And the capacitance is not measured at all with this simple measurement.

There are several ways to improve the accuracy and even further derive the capacitance, but these simple results are enough to start the tuning procedure. This tuning procedure needs to be done anyway, so there is no real need to spend more effort in measuring the antenna coil parameters more accurate.

3.3 Antenna matching

3.3.1 Matching circuit calculation

The next step is to calculate the values of the matching circuit.

For the ALM the additional capacitive voltage divider needs to be calculated. This divider guarantees that the voltage at the LA / LB pins, during the active pulse, are in the range of max 1.4V.

To generate the matching values the measured antenna values must be inserted in the first part of the calculation sheet (see Fig 11):

1 Measured" values:

$L_a = L = 250\text{nH}$ (measured antenna coil inductance)

$C_a = C_{\text{pa}} = 0.1\text{pF}$ (estimated parallel capacitance of the antenna coil)

$R_a = R_{\text{Coil}} = 1\Omega$ (measured antenna coil resistance)

Enter the values in the first part of the calculation sheet (Fig 11)

Enter the antenna physical parameters in the second part of the excel sheet (Fig 11)

2. Calculating matching values:

The first step:

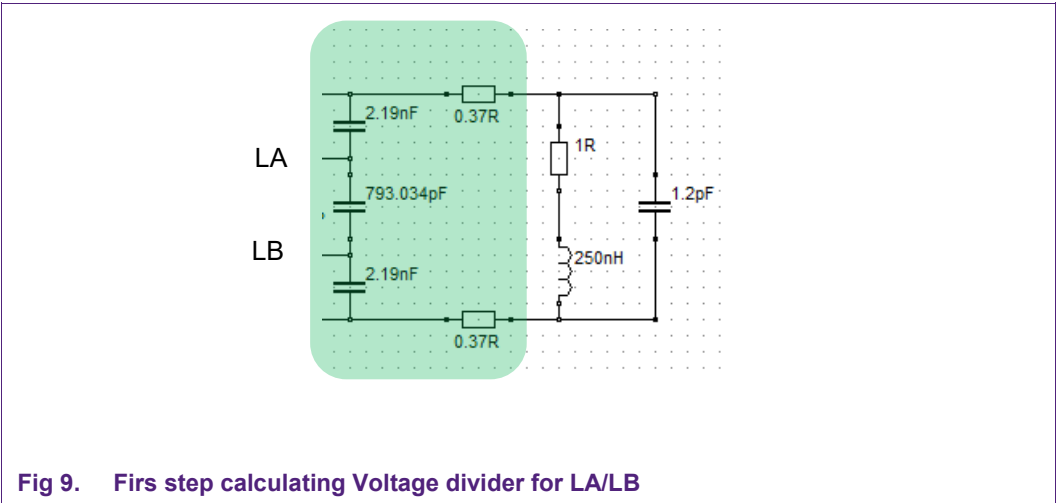
Calculate the Voltage divider based on the assumed max and min field strength (Table 1). This voltage divider is the mayor part for the matching as it limits the Voltage for the Receiver pins to 1,8V. To proper calculate the Voltage divider the Antenna parameters needed to be added in the Excel sheet as it is the base for the Voltage calculation on the Antenna, based on the min and max field strength that should be covered.

Table 1. Matching target values for voltage divider

Name	Value	
Target Q-factor	12,30	
Target Impedance	50,00	Ω
Receiver Resonance Freq	14,84	MHz
Min. H-Field Support	0,22	A/m (rms)
Max. H-Field Support 10% modulation	6,00	A/m (rms)
RX Division Ratio	0,58	

(defined Q-factor, see [chapter 2](#)).

The blue marked values are used to calculate the voltage divider for L A/B. These values should not be touched if there is no change in the max field strength.



Second Step

Calculate the series Capacitor for LA/B_Tx based on the values for the Voltage divider. In this case the resulting impedance is limited due to the voltage divider which is the focus of the matching. The series capacitor is calculated in such a way that the impedance is around the real axis at 13.56MHz (Fig 10). To change the impedance the voltage divider needs to be recalculated at first. Due to that reason the target impedance is not incorporated as in standard reader matching.

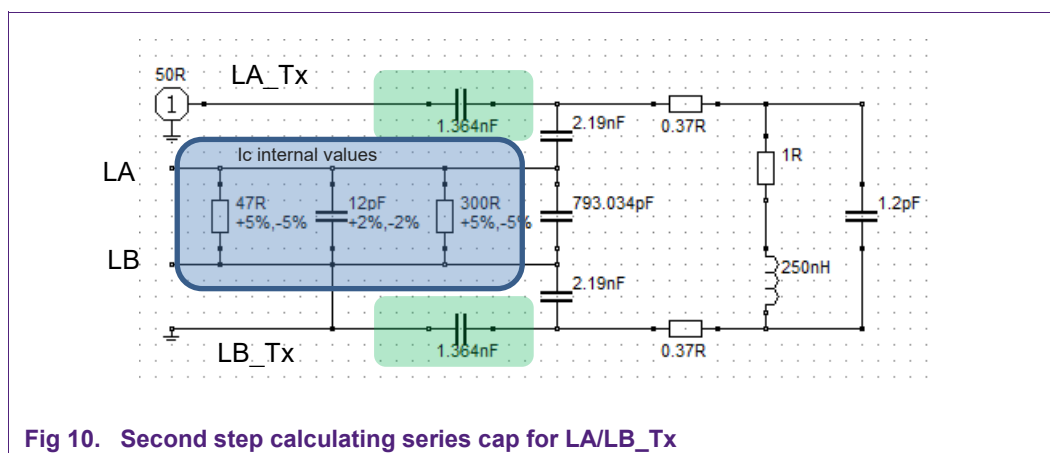


Fig 10. Second step calculating series cap for LA/LB_Tx

With these values the matching components can be calculated using the excel sheet.

3 Calculated Values and components using excel sheet:

Components ALM

The matching capacitors are calculated:

$$R_{ext} = R_Q = 0,37\Omega$$

$$C_s = 1,364nF$$

$$C_{p1} = 793pF$$

$$C_{p2} = 2,190nF$$

Antenna Electrical Parameters		
Inductance	250.00	nH
Resistance	1.00	Ω
Parasitic capacitance	0.10	pF
Antenna Physical parameters		
Antenna Width	10.00	mm
Antenna Length	10.00	mm
No. of Turns	4.00	
Matching Target		
Target Q-factor	12.30	
Target Impedance	50.00	Ω
Receiver Resonance Freq	14.84	MHz
Min. H-Field Support	0.22	A/m (rms)
Max. H-Field Support 10% modulation	6.00	A/m (rms)
RX Division Ratio	0.58	
Matching Circuit		
Damping Resistance (Rq)	0.37	Ω
Cp1	793.03	pF
Cp2	2190.284561	pF
Cs	1363.95	pF

(1) ALM calculation sheet

Excel sheet is included in this document as attachment, see [section 5.3](#)

Fig 11. Antenna matching calculation ALM

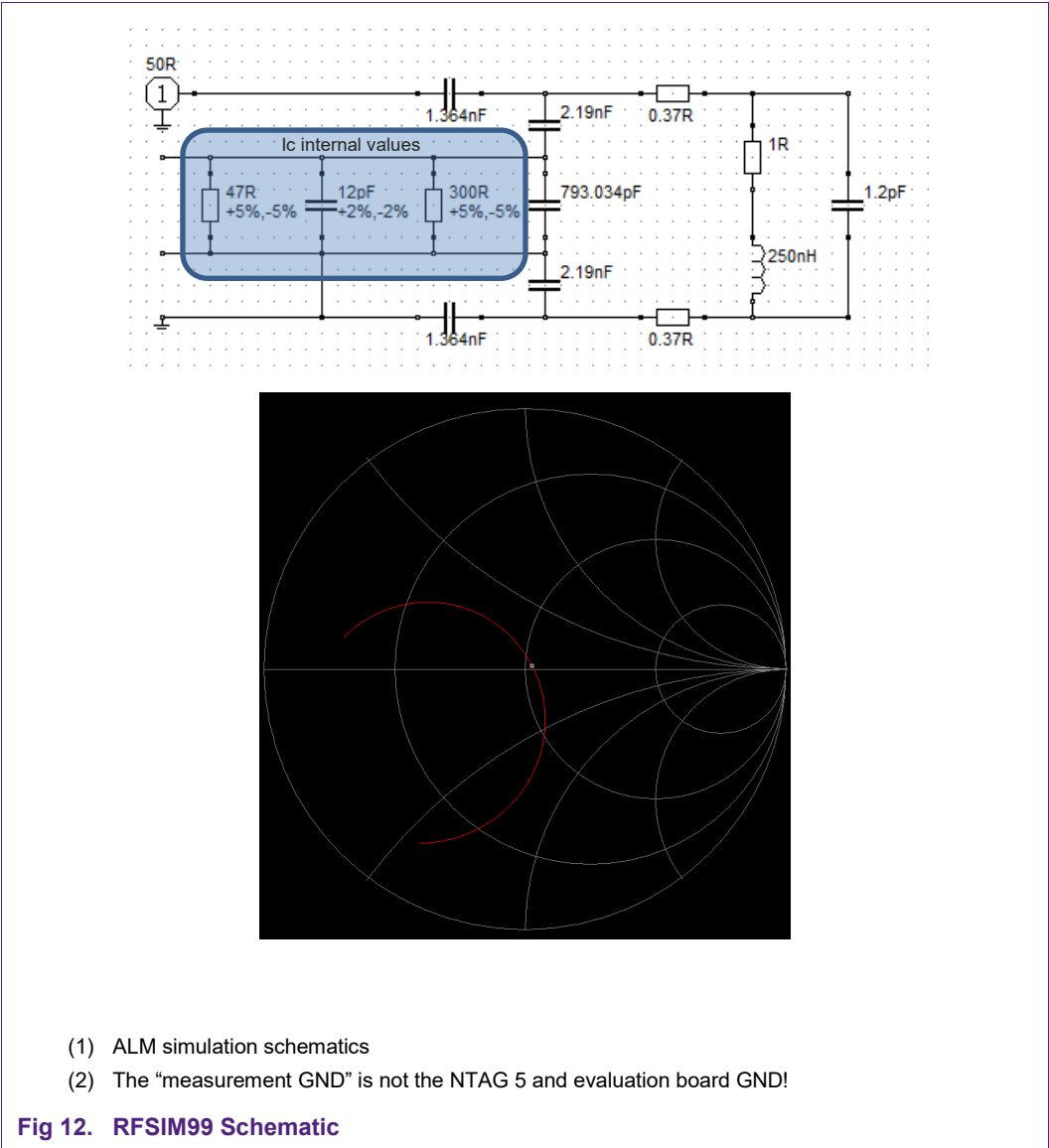
3.3.2 Simulate the matching

The measurement of the antenna coil itself typically is not very accurate. Therefore a (fine) tuning of the antenna normally is required, which might become easier in combination together with a simulation.

A simple matching simulation tool like e.g. RFSIM99 can be used to support the antenna tuning. The simulation input and the result based on the above given start values for the antenna matching is shown in Fig 12 and Fig 13.

With these values the assembly can be done, even though the result is not yet optimum, as shown in Fig 14. The overall impedance is slightly below 40 Ω and capacitive ($-j4\Omega$).

Note: The result is not as calculated, since not the exact calculated values of the capacitors are taken for assembly.

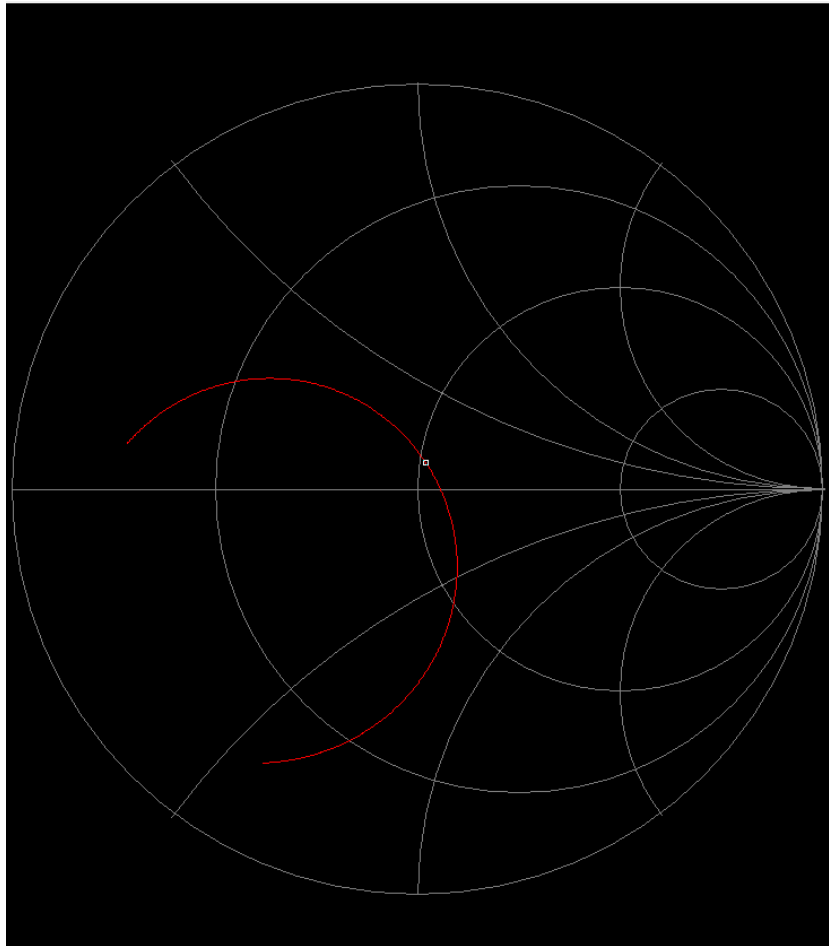


3.3.3 Assembly and measurement (based on ALM example)

After the first assembly the impedance measurement must be done.

If the measurement result does not meet the requirements, i.e. it needs to be retuned.

The measurement result is typically slightly different than the simulation result, since the accuracy of the original antenna coil measurement is limited.



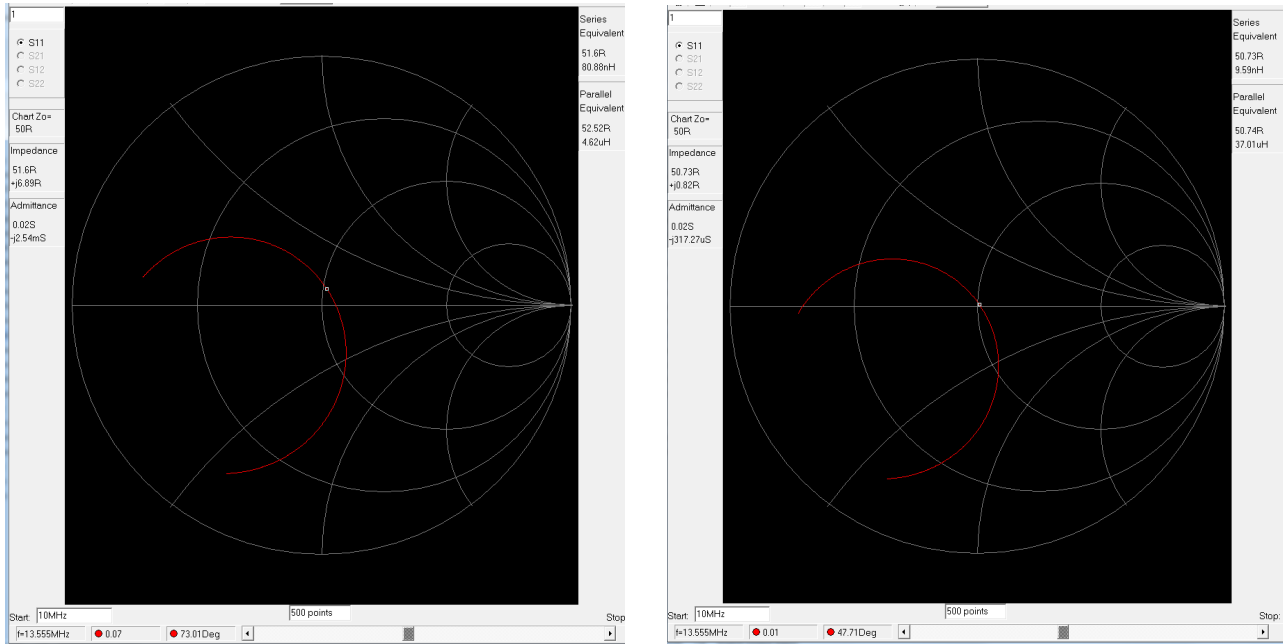
(3) This matching does not meet the requirements. It must be corrected and retuned.

Fig 13. Measurement result of first assembly

3.3.4 Impedance fine tuning

The easiest and fastest way to (fine) tune the antenna is to first of all adapt the simulation in such a way that it shows the same result as the reality. The parameters of the antenna coil are the parameters to be changed, since these parameters are not measured (or estimated) correctly.

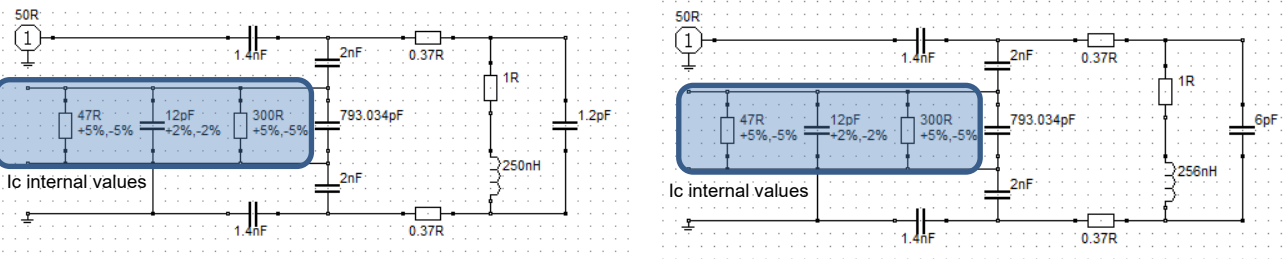
So with the values of L , C_{pa} , and R_{Coil} the simulation is tuned from Fig 13a to Fig 13b. The changed values can be seen in Fig 14b.



a. Impedance first step

b. Impedance after adaptation

Fig 14. Impedance adaptation in the simulation (result)



a. Circuit first step

b. Circuit after adaptation

Fig 15. Impedance adaptation in the simulation (circuit)

With these adapted values the antenna coil the last step of the final tuning can be done:

$$L_a = L = 256 \text{ nH}$$

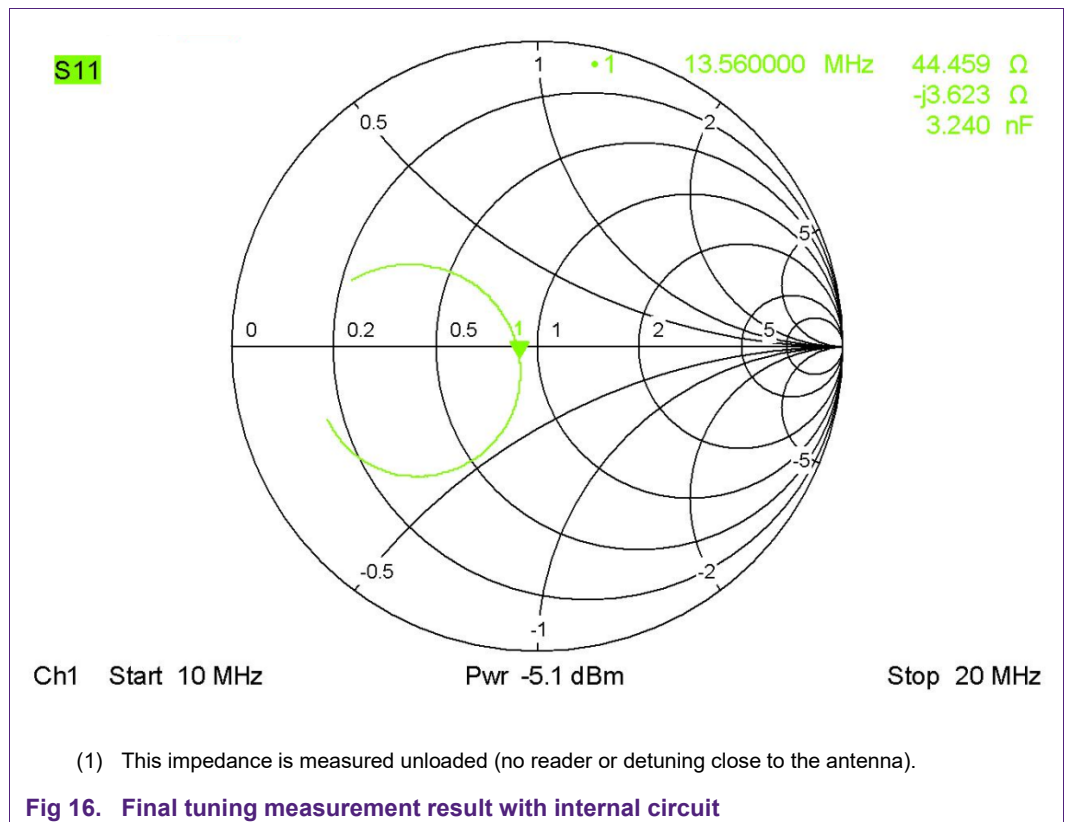
$$C_a = C_{pa} = 6 \text{ pF}$$

$$R_a = R_{Coil} = 1 \Omega$$

The tuning of the impedance is now corrected with the values of Cp1 and Cp2.

These values are assembled, and the impedance is measured. The result is shown in Fig 16.

Note: For the measurements the internal resistance as well as the capacitance need to be considered (can be added with an additional small board connected during the measurement)



3.4 ALM LUT

The ALM look up table (LUT) is a dynamic setting of the TX power which is used to change the strength of the answer signal. This is used to stay within the NFC limits and reduce the power in close coupling condition, if needed. The ALM LUT is always used if ALM is enabled and the threshold for each step is fix and cannot be changed.

The LUT contains 16 entries' starting at address 41h up to 44h. each address contains 4 Bytes so 4 entry's per address. (see Fig 17)

Block Address		Byte 0	Byte 1	Byte 2	Byte 3
NFC	I ² C				
40h	1040h	ALM_CONF_00	ALM_CONF_01	ALM_CONF_02	ALM_CONF_03
41h	1041h	ALM_LUT_00	ALM_LUT_01	ALM_LUT_02	ALM_LUT_03
42h	1042h	ALM_LUT_04	ALM_LUT_05	ALM_LUT_06	ALM_LUT_07
43h	1043h	ALM_LUT_08	ALM_LUT_09	ALM_LUT_10	ALM_LUT_11
44h	1044h	ALM_LUT_12	ALM_LUT_13	ALM_LUT_14	ALM_LUT_15

Fig 17. LUT address range

The LUT entry is configured depending on the field strength and is switched due to the value at the field digitalization register (first 4 bit of the ALM_STATUS_REG adr. ACh Byte2). Each byte of the ALM LUT contains the option to change the answer strength as well as adjust the bit phase (normally not needed), if necessary. The strength of the answer signal can be adjusted by changing the RON (fine adjustment with small steps) or by changing from BPSK to ASK (substantial change). The RON can be combined with BPSK and ASK mode. (see Fig 18)

Bit	Name	Value	Description
7 to 5	Dynamic phase adjust	xxx _b	adjust phase in 11.25° steps
4	Enable BPSK	0 _b	ASK
		1 _b	BPSK
3 to 0	RON	0000 _b	1574 Ω
		0001 _b	716 Ω
		0010 _b	414 Ω
		0011 _b	248 Ω
		0100 _b	123 Ω
		0101 _b	82 Ω
		0110 _b	62 Ω
		0111 _b	49 Ω
		1000 _b	41 Ω
		1001 _b	35 Ω
		1010 _b	31 Ω
		1011 _b	27 Ω
		1100 _b	25 Ω
		1101 _b	22 Ω
		1110 _b	21 Ω
		1111 _b	17 Ω

Fig 18. ALM LUT value content

The values of the ALM LUT are used according to the field digitization value. That means if the field digitization value is 5 the same ALM LUT value is used. This link is fixed and cannot be changed.

The values of the field digitization are linked to the field strength ([Fig 19](#)). The values shown are based on the 10x10mm antenna and corresponding matching, which is part of the development kit. These values vary depending on the matching and antenna size, therefore they can be different depending on the setup. The corresponding measurement is done on the receiver pins and up to 1,15V a Voltage measurement is done and above the current is measured.

Code	Level	Code	Level
0	<0.22V	7	1mA
1	0.22V	8	6mA
2	0.40V	9	7.5mA
3	0.57V	10	10.5mA
4	0.74V	11	13mA
5	0.93V	12	15mA
6	1.15V	13	17mA
		14	18mA

Fig 19. Measured field vs field digitization code

The default entries of the ALM LUT can be used and only need to be changed if the card answer is too strong, in respect to the field strength during the certification test.

3.5 LUT Values for 10mmx10mm antenna

The LUT values need to be set according to antenna size and the supply

Below are the default values for the 10x10 mm antenna of the evaluation board

Table 2. LUT for 3.3V supply with 10x10mm antenna

Address (I ² C)	Byte 0	Byte 1	Byte 2	Byte 3
1041h	0x1F	0x1F	0x17	0x14
1042h	0x13	0x13	0x12	0x12
1043h	0x10	0x10	0xF0	0xF0
1044h	0xF0	0xF0	0xF0	0xF0

Table 3. LUT for 1.62V supply with 10x10mm antenna

Address (I ² C)	Byte 0	Byte 1	Byte 2	Byte 3
1041h	0x1F	0x1F	0x1F	0x1F
1042h	0x1F	0x1F	0x1F	0x12
1043h	0x10	0x10	0x10	0x10
1044h	0x10	0x10	0x10	0x10

4.

4. List of abbreviations

This document uses the following list of abbreviations:

A_c	Average antenna area
A_{Active}	Active antenna area
A_i	Area of antenna winding i
a_{avg}, b_{avg}	Average dimensions of the antenna
a_{max}, b_{max}	Maximum dimensions of the antenna
a_o, b_o	Overall dimensions of the antenna
C_c	Antenna capacitance
C_{br}	Bridge capacitance
C_{Con}	Capacitance due the connection NTAG 5 IC – antenna
C_{IC}	NTAG 5 IC input capacitance
C_{ICT}	NTAG 5 IC input capacitance for threshold condition
C_{in}	Designed inlet capacitance
C_{it}	Inter turn capacitance of the antenna
C_{pl}	Parallel equivalent capacitance of the inlet
C_{plT}	Parallel equivalent capacitance of the inlet for threshold condition
d	Antenna wire diameter
f	Frequency
f_{op}	Operating frequency
f_R	Resonance frequency of the inlet
f_{RT}	Threshold resonance frequency of the inlet
g	Gap between the tracks
H_T	Threshold field strength
H_{Tmin}	Minimal threshold field strength
H_{Top}	Threshold field strength at operating frequency
I_1	Reader antenna current
L_{calc}	Inductance calculated out of the geometrical antenna parameters
L_o	Objective inductance of the antenna
L_{pc}	Parallel equivalent inductance of the antenna
L_{sc}	Serial equivalent inductance of the antenna
M	Mutual inductance between the inlet antenna and reader antenna
N_c	Number of turns of the antenna
p	Turn exponent
Q	Quality factor of the inlet
Q_{pc}	Quality factor of the antenna for parallel equivalent circuit
Q_{sc}	Quality factor of the antenna for serial equivalent circuit
Q_T	Threshold quality factor of the inlet
R_{Con}	Resistance of the connection NTAG 5 IC – antenna
R_{IC}	NTAG 5 IC input resistance
R_{ICT}	NTAG 5 IC input resistance for threshold condition

R_{pc}	Parallel equivalent resistance of the antenna
R_{pl}	Parallel equivalent resistance of the inlet
R_{plT}	Parallel equivalent resistance of the inlet at threshold condition
R_{sc}	Serial equivalent resistance of the antenna
t	Track thickness
V_{LA-LB}	NTAG 5 IC input voltage
$V_{LA-LB\ min}$	Minimal voltage level for NTAG 5 IC operation
w	Track width

5. Reference documentation

NXP provides several documents to support the development of customized antennas.

5.1 Data sheets

NXP provides the following data sheet:

- NTA5332 - NTAG 5 boost, NFC Forum-compliant I2C bridge for tiny devices, doc.no. 544730
<https://www.nxp.com/docs/en/data-sheet/NTA5332.pdf>

5.2 Application notes

NXP provides the following application note:

- AN12428 - NTAG 5 design recommendations for FCC and CE certifications
<https://www.nxp.com/docs/en/application-note/AN12428.pdf>

5.3 Included antenna matching calculation excel sheet

As attachment you will find a ZIP file containing the antenna matching calculator.

The Excel file is enclosed in a ZIP file which has the file extension .nxp. To access the Excel file, you can do the following:

1. Open the attachment by clicking the paperclip in the left margin.
2. You will find a .nxp file added to this PDF as an attachment. Right-click the file and click Save Attachment. Store it at a permanently available (network) storage location.
3. Open the location where you saved the attachment.
4. Rename the file. Change the extension from .nxp into .zip.
5. Now you can open the zip file which contains the Excel file.

6. Legal information

6.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

6.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out of the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US\$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

6.3 Licenses

Purchase of NXP ICs with NFC technology

Purchase of an NXP Semiconductors IC that complies with one of the Near Field Communication (NFC) standards ISO/IEC 18092 and ISO/IEC 21481 does not convey an implied license under any patent right infringed by implementation of any of those standards. Purchase of NXP Semiconductors IC does not include a license to any NXP patent (or other IP right) covering combinations of those products with other products, whether hardware or software.

6.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

NTAG — is a trademark of NXP B.V.

PC-bus — logo is a trademark of NXP B.V.

AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamiQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, µVision, Versatile — are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved.

7. List of figures

Fig 1.	Series equivalent circuit of the antenna	4
Fig 2.	Parallel equivalent circuit of the antenna	4
Fig 3.	ALM answer shaping	5
Fig 4.	Antenna size vs load modulation technologies ..	6
Fig 5.	NFC antenna design tool	7
Fig 6.	ALM topology	8
Fig 7.	Measurement 1 Antenna coil	9
Fig 8.	Measurement 2 Antenna coil	10
Fig 9.	Firs step calculating Voltage divider for LA/LB ..	12
Fig 10.	Second step calculating series cap for LA/LB_Tx	13
Fig 11.	Antenna matching calculation ALM	14
Fig 12.	RFSIM99 Schematic	15
Fig 13.	Measurement result of first assembly	16
Fig 14.	Impedance adaptation in the simulation (result)	17
Fig 15.	Impedance adaptation in the simulation (circuit)	17
Fig 16.	Final tuning measurement result with internal circuit	18
Fig 17.	LUT address range	19
Fig 18.	ALM LUT value content	20
Fig 19.	Measured field vs field digitization code.....	20

8. List of tables

Table 1. Matching target values for voltage divider..... 12

Table 2. LUT for 3,3V supply with 10x10mm antenna ..21

Table 3. LUT for 1.62V supply with 10x10mm antenna 21

9. Contents

1.	Introduction	3
2.	Antenna basics	4
2.1	Series and parallel equivalent circuits	4
2.1.1	Series equivalent circuit of the antenna	4
2.1.2	The antenna can be described by an inductance Lsc in series to a loss resistance Rsc. The antenna capacitance Cc is in parallel to this series circuit. This capacitance consists of the inter-turn capacitance and a possibly designed tag capacitance CIC	4
2.1.3	Parallel equivalent circuit of the antenna	4
2.2	Q factor adjustment	5
2.3	Antenna sizes	6
2.4	Antenna design	6
3.	Antenna matching	8
	Matching topology	8
3.1	8	
3.2	General antenna matching procedure and preparation	8
3.2.1	Measure the antenna equivalent circuit parameters	9
3.3	Antenna matching	11
3.3.1	Matching circuit calculation	11
3.3.2	Simulate the matching	14
3.3.3	Assembly and measurement (based on ALM example)	16
3.3.4	Impedance fine tuning	17
3.4	ALM LUT	19
3.5	LUT Values for 10mmx10mm antenna	21
4.	List of abbreviations	22
5.	Reference documentation	24
5.1	Data sheets	24
5.2	Application notes	24
6.	Legal information	25
6.1	Definitions	25
6.2	Disclaimers	25
6.3	Licenses	25
6.4	Trademarks	25
7.	List of figures	26
8.	List of tables	27
9.	Contents	28