MIMXRT1060-EVKB

Table of Content

Revision History

Rev. Code	Date	By	Description
A	2020-11-27	Shawn Shi	Initial Release
B	2021-03-17	Shawn Shi	1.Add R432,R433 for SD power switch 2.Change R232 from 10K to 100K 3.Swap I2C3_SCL and I2C3_SDA 4.Add R434,R435 for I2C signal pull-up 5.DNP R252, R345.Populate R160,R162,R164,R167,R176,R382,R390,R396,R415
B1	2021-06-03	Albert Li	No Layout change compared to RevB, only BOM update: 1.DNP R368,R376,R347,R349,R365,R363 2.Add note in page05 to populate resistors for M.2 SDIO App.

REF DES	JUMPER(DEFAULT)	PAGE NAME
J40	5-6	03 MAIN POWER
J44,J29,J27,J25,J30,J26	1-2	04 POWER DOMAIN
J41,J35,J37,J36	1-2	09 AUDIO
J5,J6,J13,J9,J11,J3,J10,J4	1-2	15 FREELINK

REF DES	SWITCH(DEFAULT)	PAGE NAME
SW3,SW2	off,off,off,off	17 BOOT
SW4	off,off,on,off	17 BOOT

1. Unless Otherwise Specified:

   All resistors are in ohms, 1/16 Watt,0402
   All capacitors are in uF,0402
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: PUBI:

Designer: Shawn Shi	Drawing Title: MIMXRT1060-EVKB	
Drawn by: Shawn Shi	Page Title: COVER	
Approved: Yes	Size C	Document Number SCH-47858, PDF: SPF-47858 Rev B1
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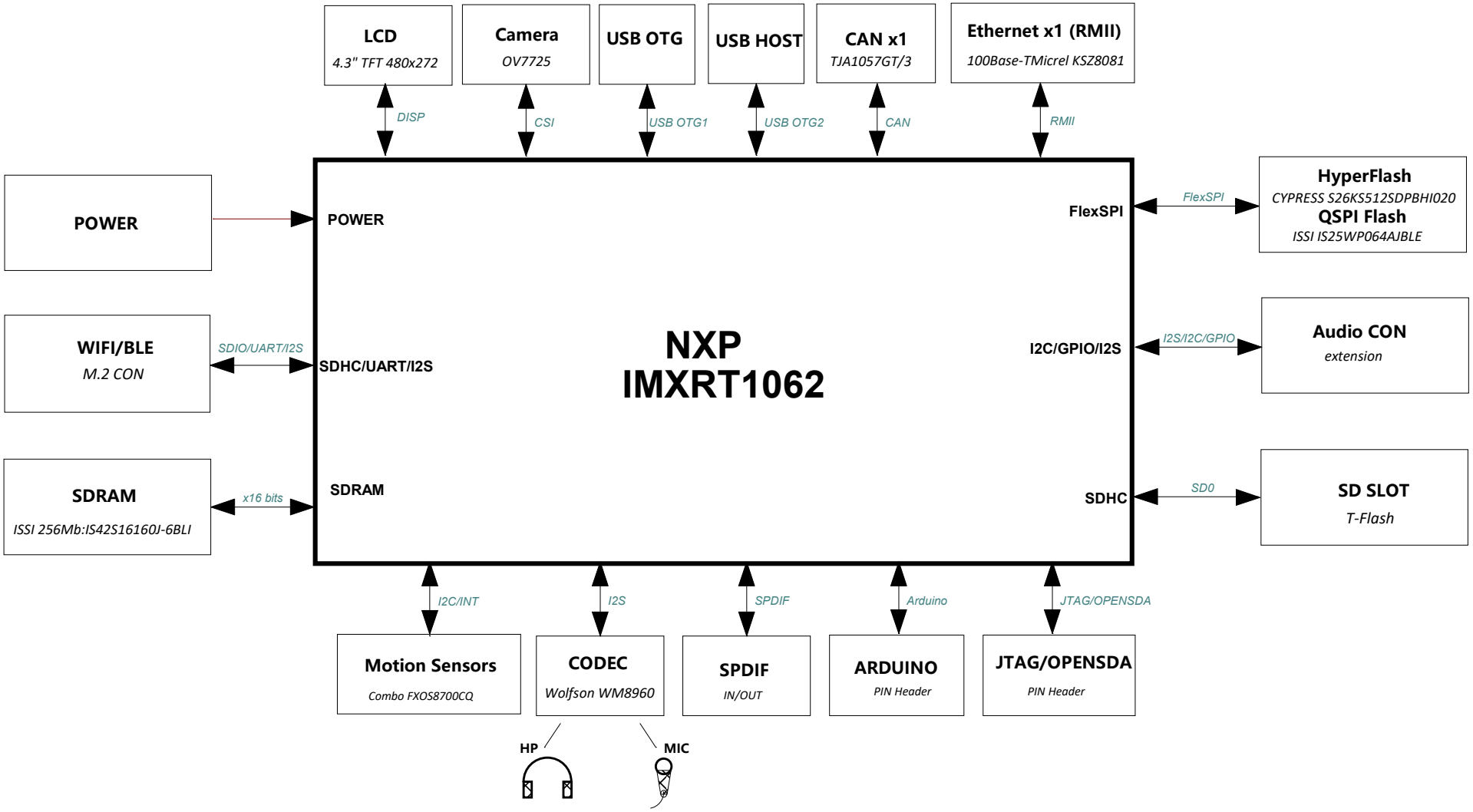
Blcok Diagram Rev B#####

MIMXRT1060-EVKB



ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: MIMXRT1060-EVKB

Page Title: BLOCK DIAGRAM

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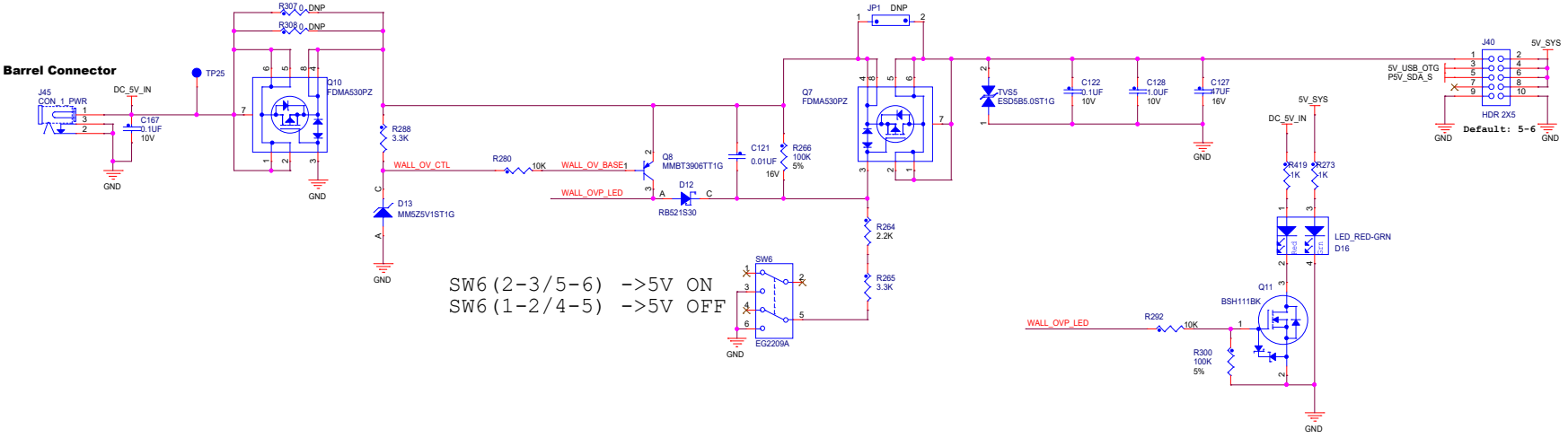
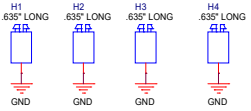
Main Power



Board Mounting Holes



Ground TPs

Layout Note: Place Ground TPs
to assist signal measurement.

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Page Title:	MAIN POWER	
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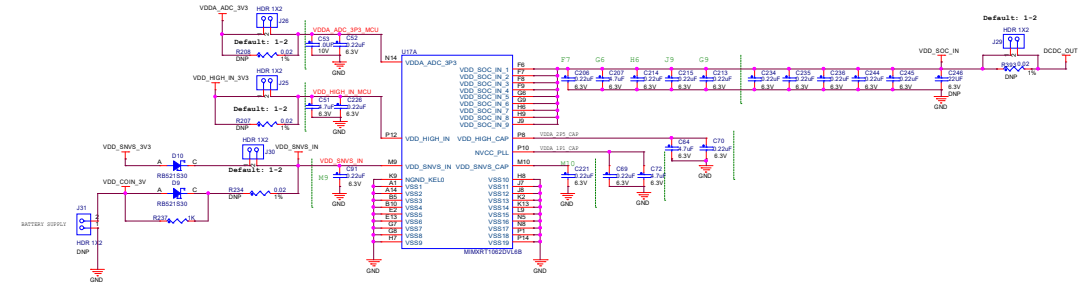
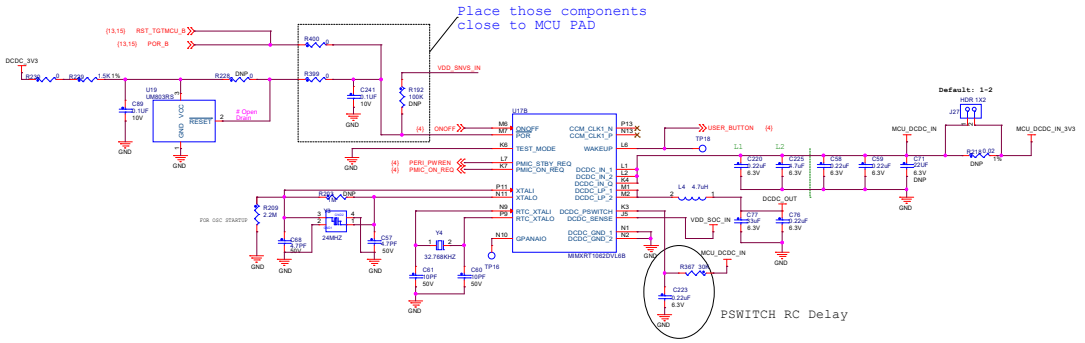
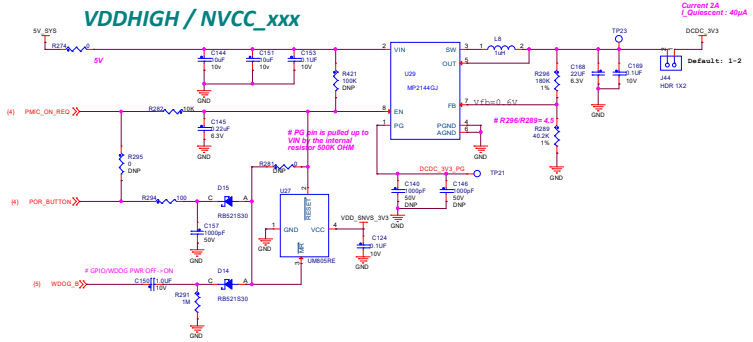




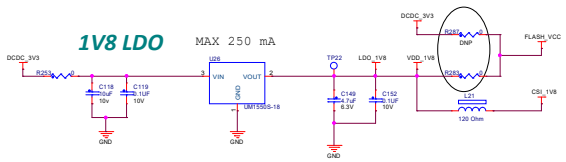
VDDHIGH / NVCC_xxx



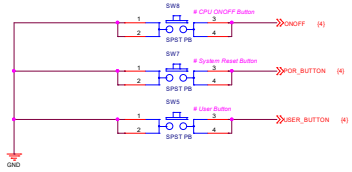
FLASH VCC

1V8 LDO

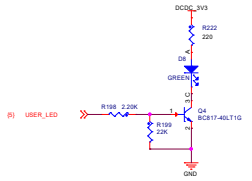
MAX 250 mA



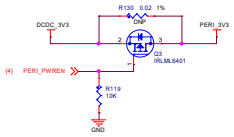
BUTTONS



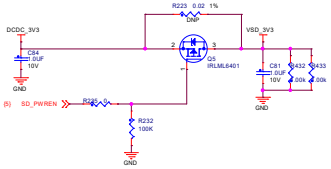
USER LED



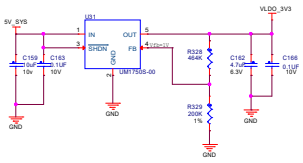
LCD 3V3 POWER SWITCH



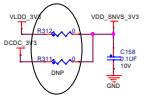
SD CARD POWER SWITCH



3V3 LDO for SNVS

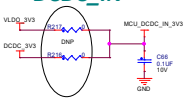


SNVS

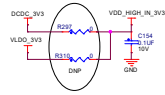


ADC

DCDC_IN

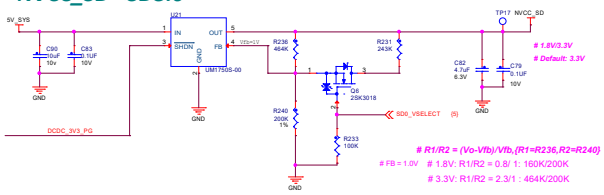


VDD_HIGH_IN



NVCC_SD <SD3.0>

MAX 350 mA



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Drawing Title:	MIMXRT1060-EVKB
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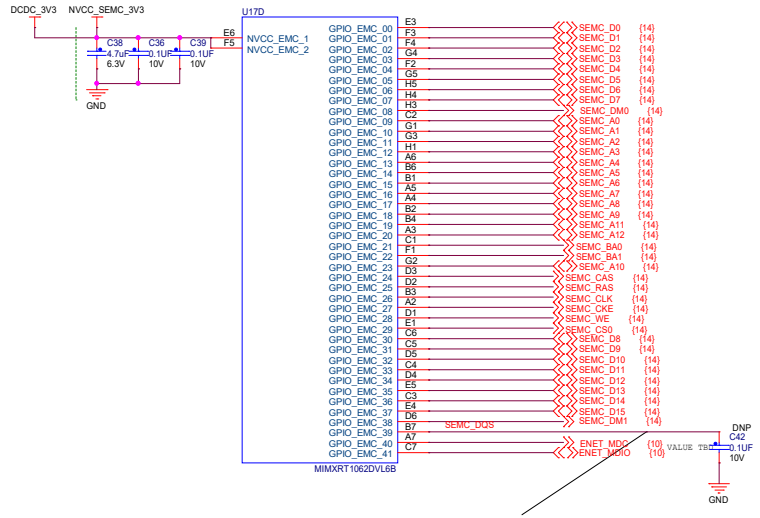
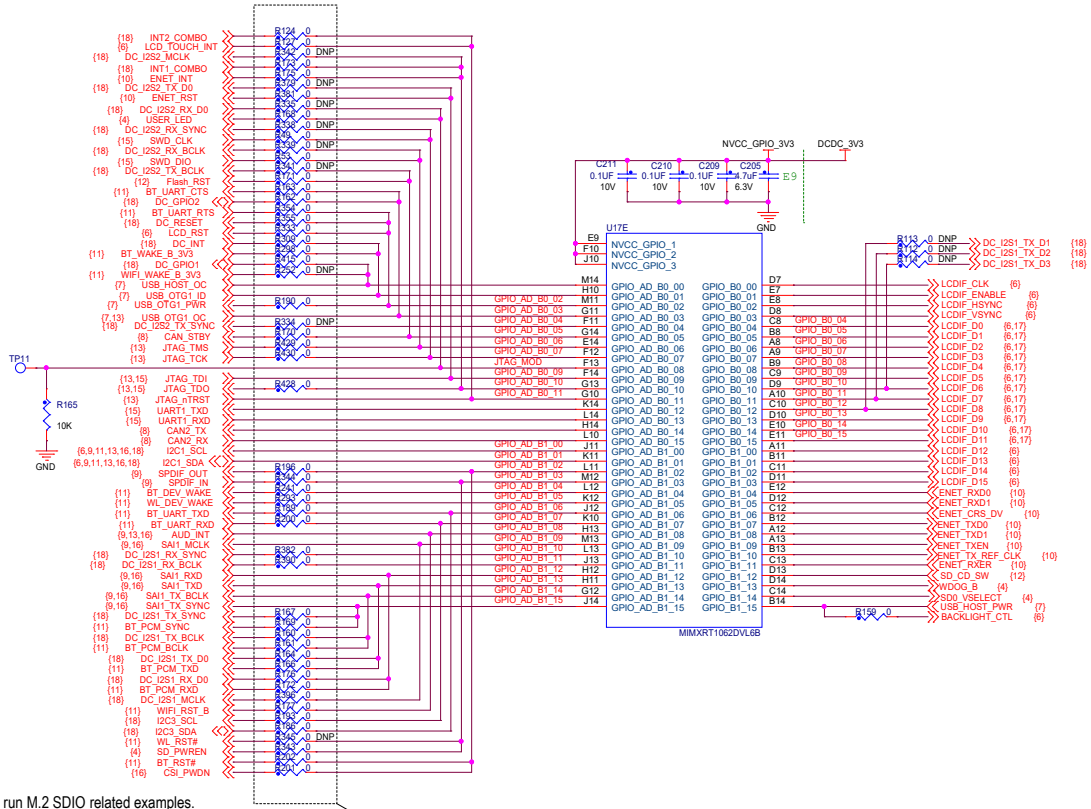
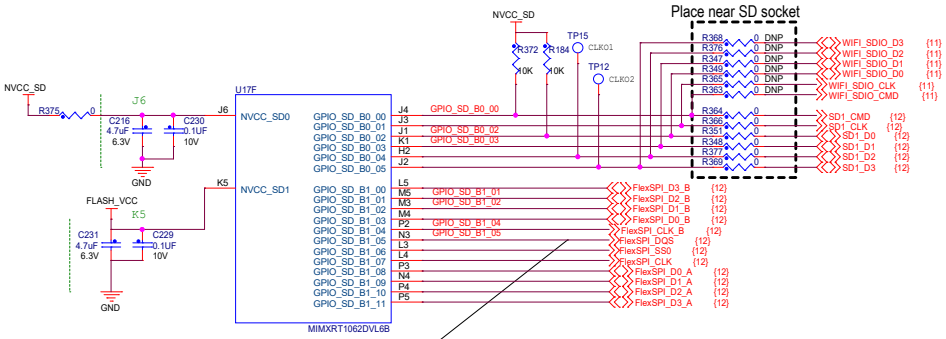
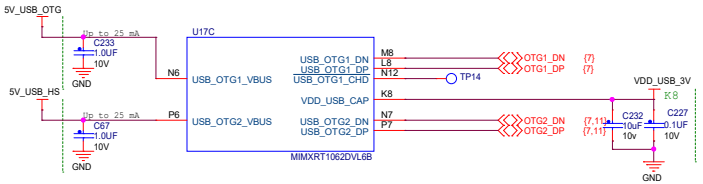
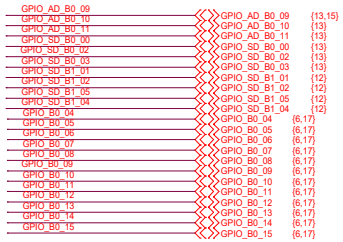


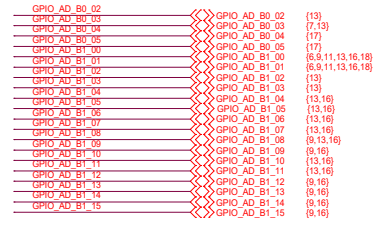


Note: Populate R368,R376,R347,R349,R365,R363 when run M.2 SDIO related examples.









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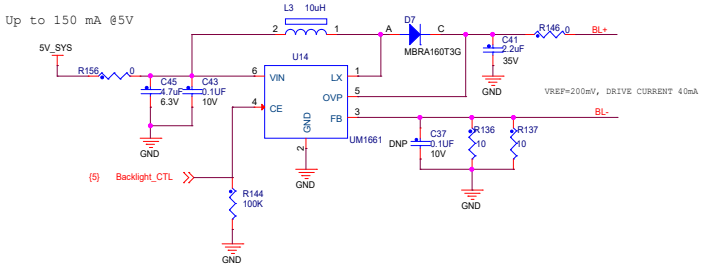
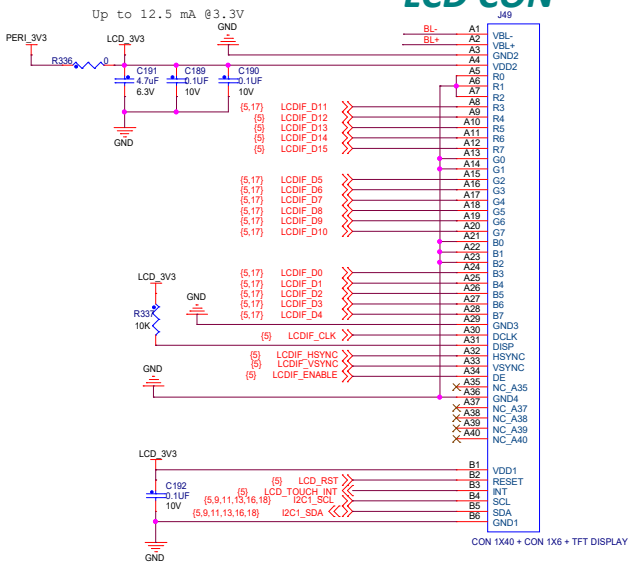
Backlight Control



LCD CON



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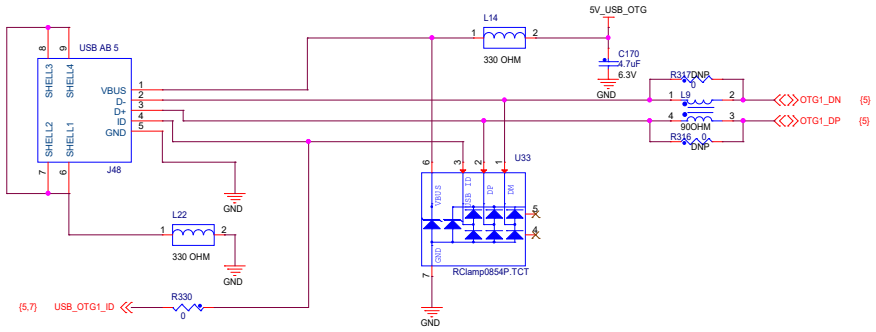
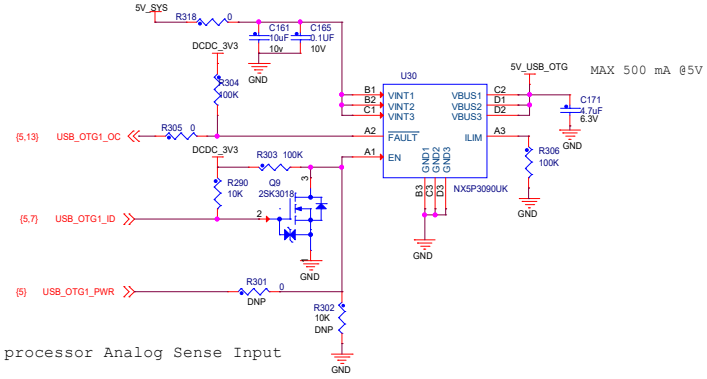
USB OTG



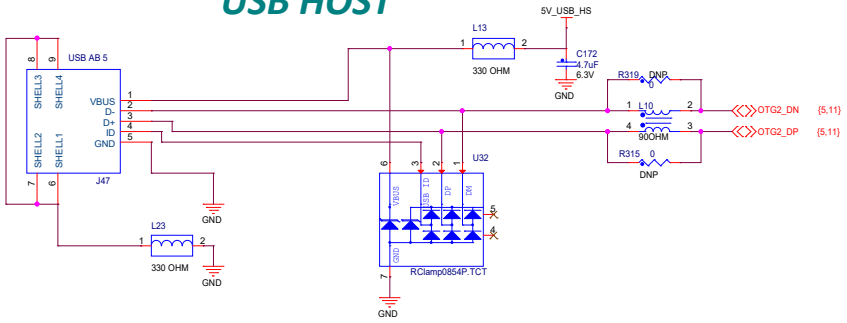
USB POWER

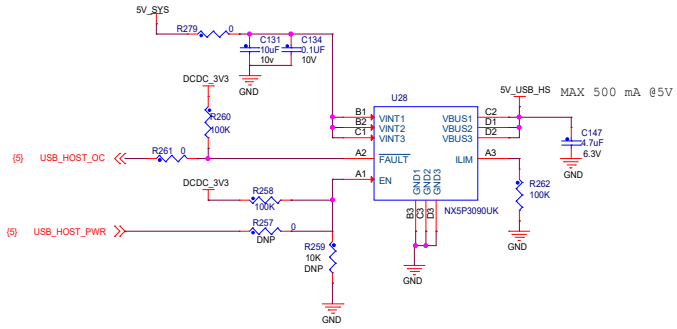


USB ID is a processor Analog Sense Input

Host --> ID = GND
Device --> ID = Floating

USB HOST





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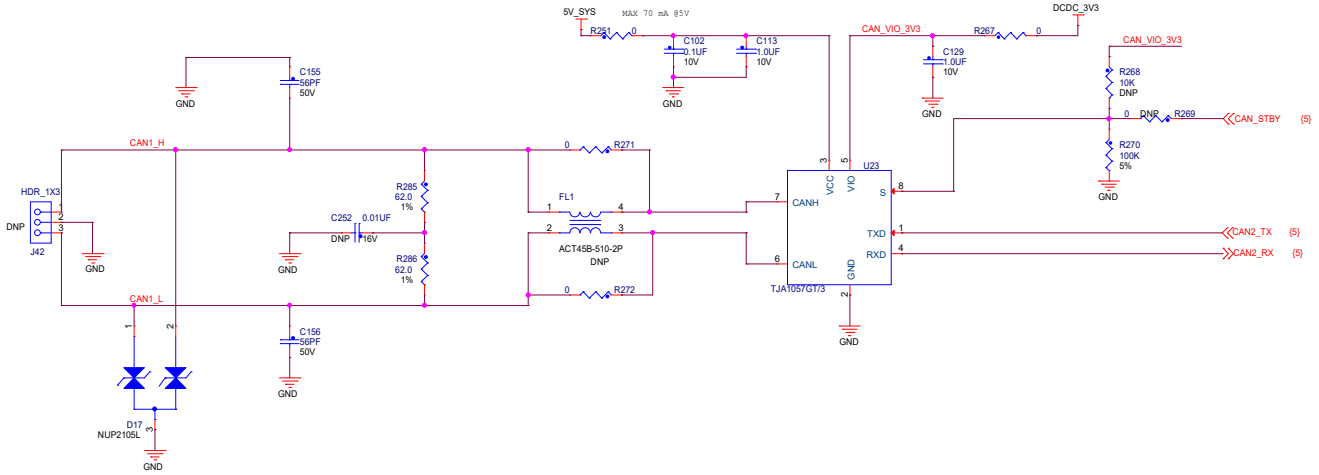
CAN BUS



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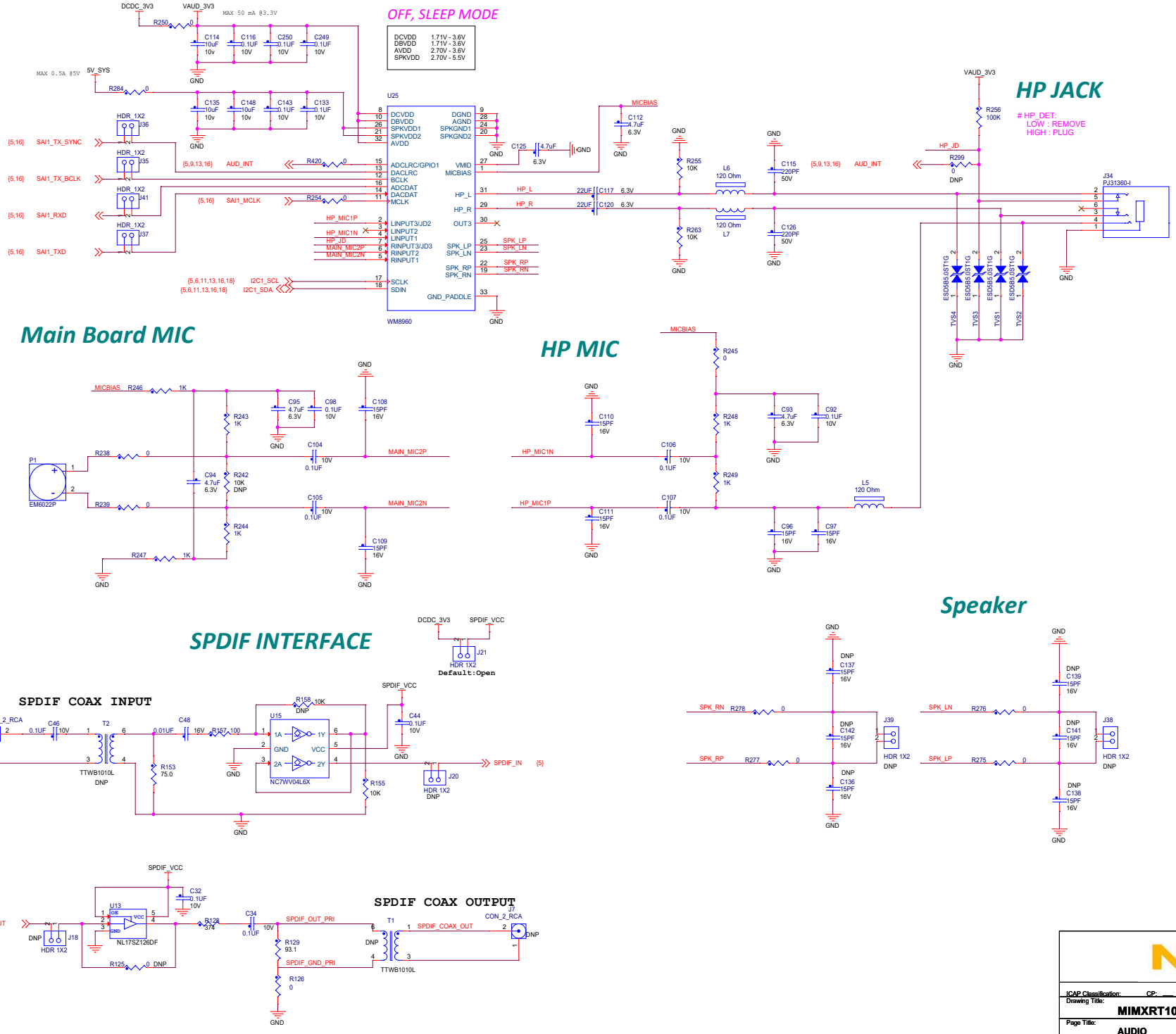
OFF, SLEEP MODE
DCVDD 1.71V - 3.6V
DBVDD 1.71V - 3.6V
AVDD 2.70V - 3.6V
SPKVDD 2.70V - 5.5V
WM8960
HP JACK
HP_DET:
LOW : REMOVE
HIGH : PLUG
Main Board MIC
HP MIC
Speaker
SPDIF INTERFACE
SPDIF COAX INPUT
SPDIF COAX OUTPUT
Default:Open
ICAP Classification: CP: ___ IUO: X PUBI: ___
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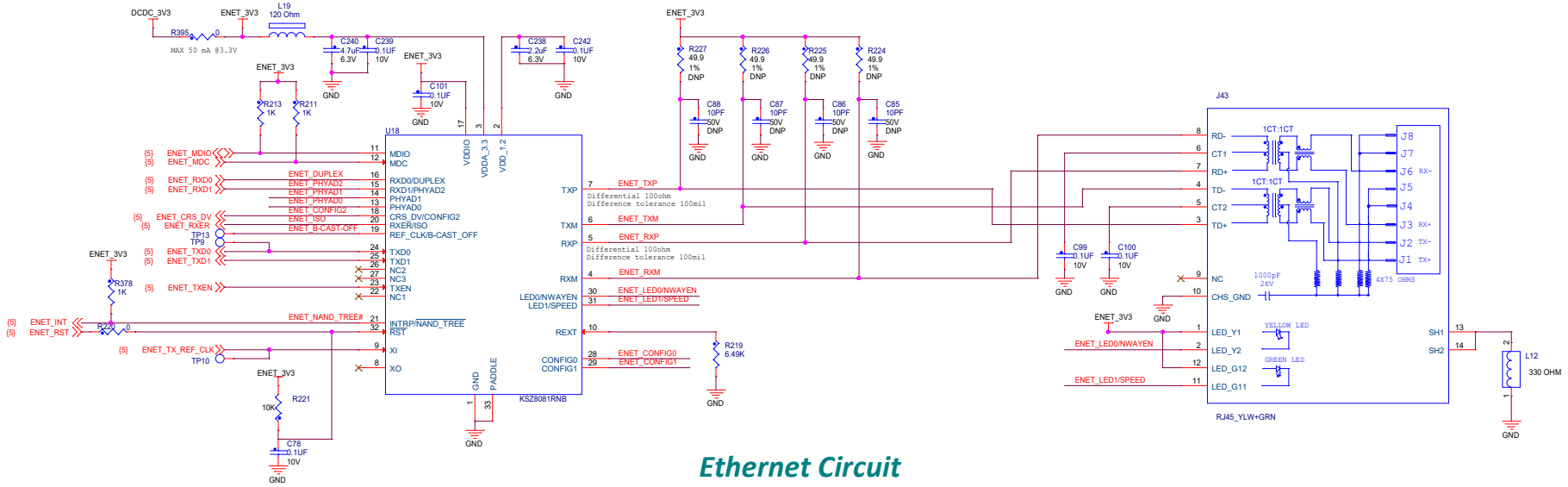
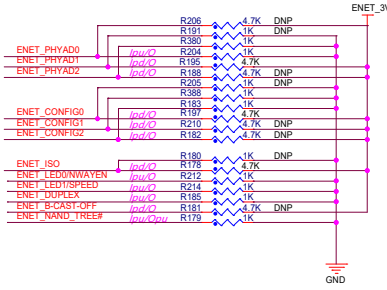


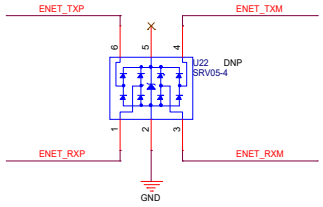
Ethernet Circuit



# CFG	Description
PHYAD[2:0]	PHY ADDR 00-XXX (00010 DEFAULT)
CONFIG[2:0]	IF MODE 001 RMII 101 RMII Back-to-Back xxx Reserved-not used
ISO	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable
SPEED	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps

# CFG	Description
DUPLEX	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex
NWAYEN	Nway Auto-Negotiation Pull-up (default) = Enable Pull-down = Disable
B_CAST_OFF	Broadcast Off - for PHY Address 0 Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY addr
NAND_TREE#	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable

ESD PROTECTION



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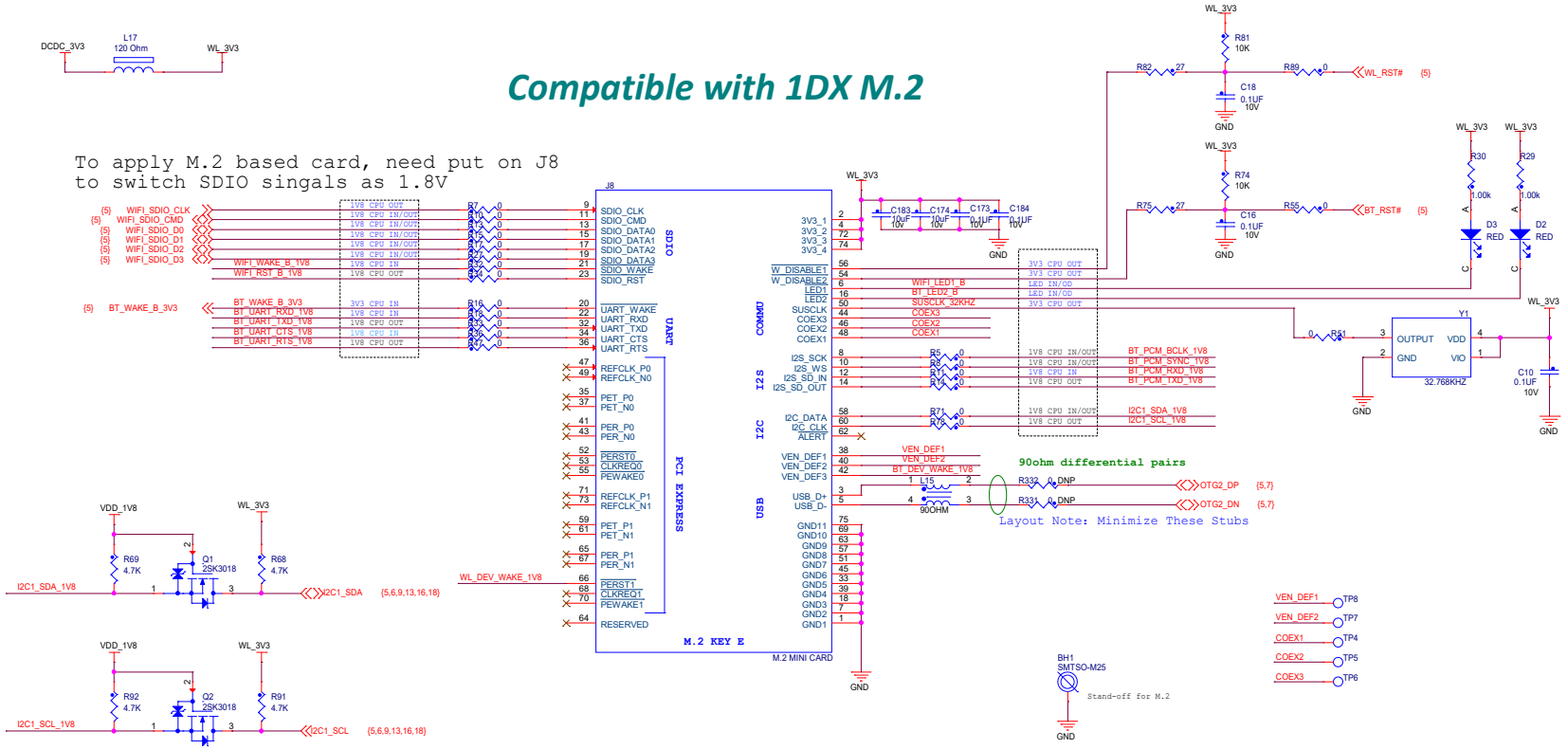
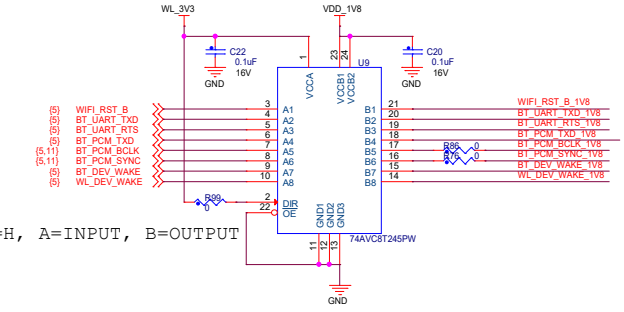
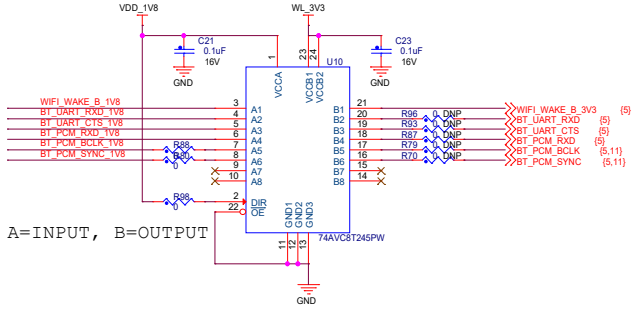
Compatible with 1DX M.2

To apply M.2 based card, need put on J8
to switch SDIO singals as 1.8V





DIR=H, A=INPUT, B=OUTPUT



DIR=H, A=INPUT, B=OUTPUT

ICAP Classification:	CP: ___	IUO: X	PUBI: ___
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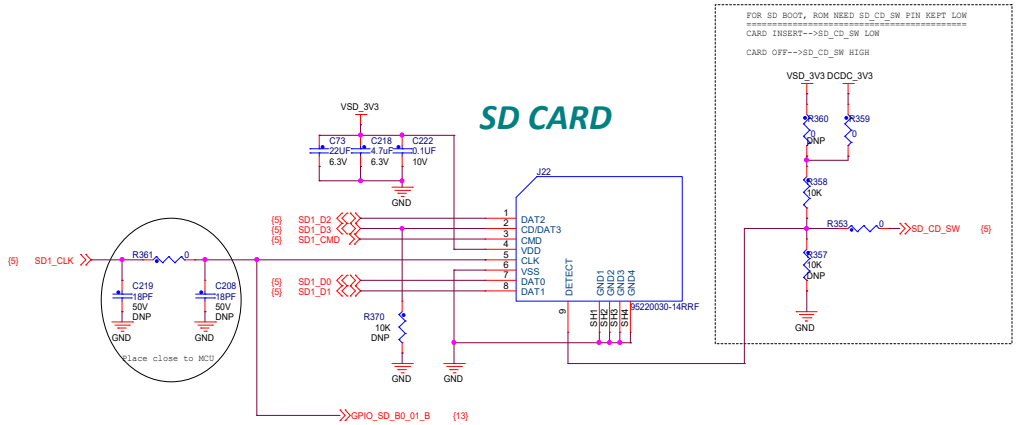
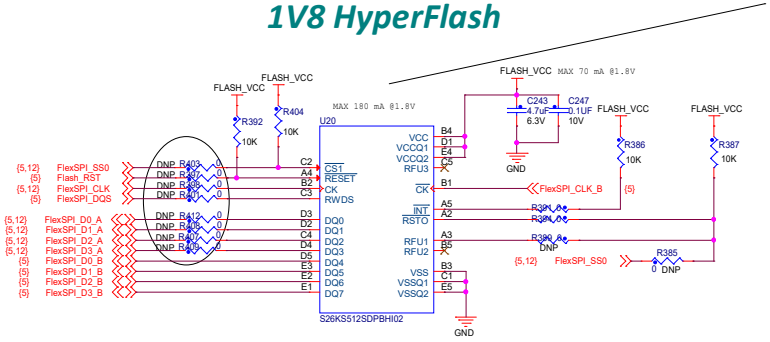
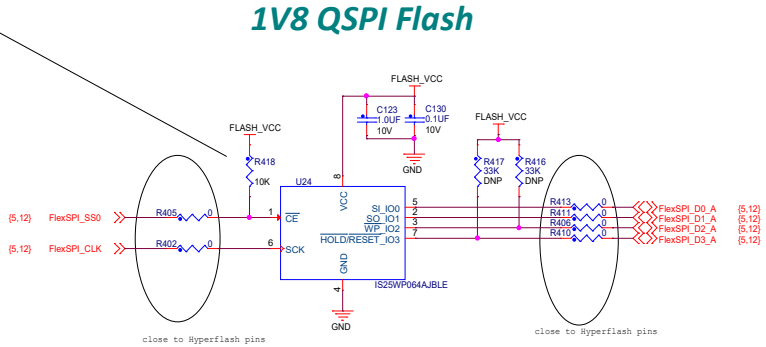


OPTION1: USE Hyperflash(DNP R402,R405,R406,R410,R411,R413, Mount R403,R398,R401,R407,R408,R409,R412)
OPTION2(DEFAULT): USE QSPI FLASH(Mount R402,R405,R406,R410,R411,R413, DNP R403,R398,R401,R407,R408,R409,R412)





Share the same package with S27KS0641DPBHI023
(if HYPERRAM is replaced, then DNP R391,R394, Mount R385,R389)

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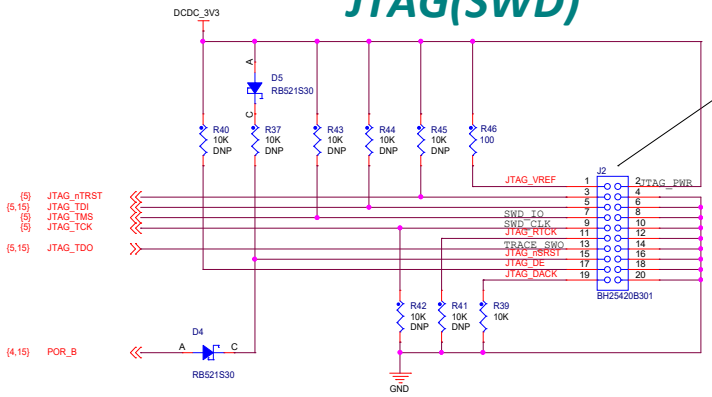
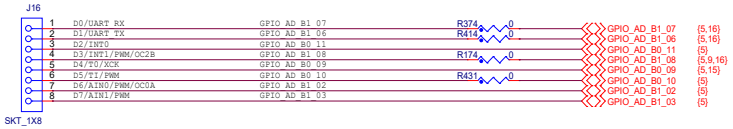
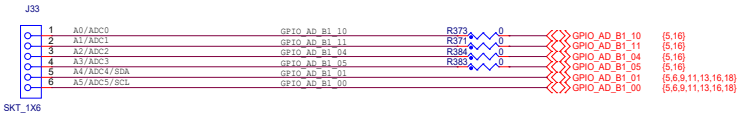
JTAG(SWD)

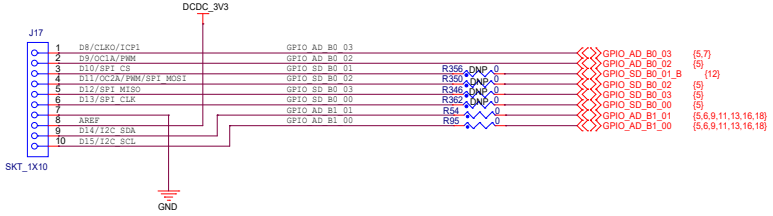
1.SWD debug is enabled by default
2.Board rework and fuse programming are needed to support JTAG debug

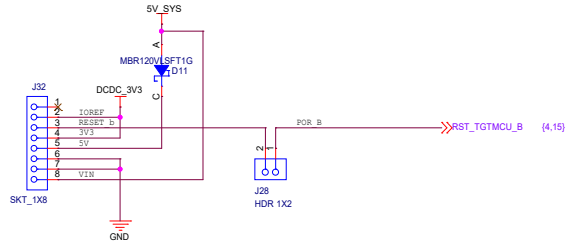


Arduino Interface









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Drawing Title:	MIMXRT1060-EVKB		
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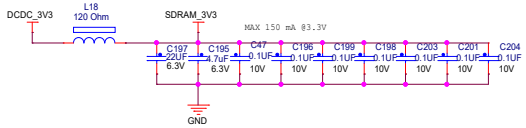
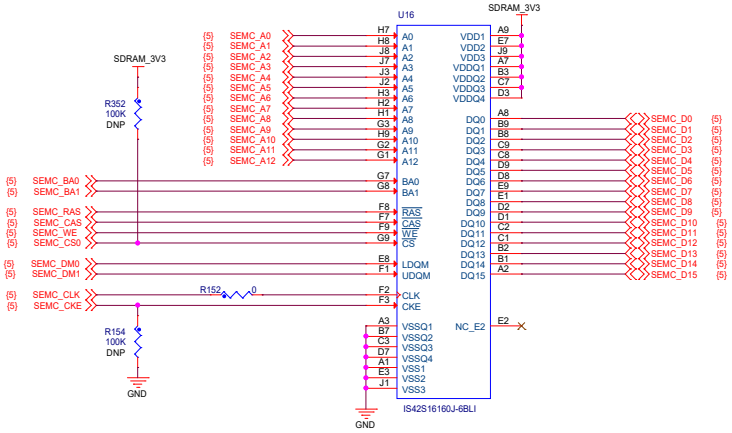
SDRAM





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Drawing Title:	MIMXRT1060-EVKB		
Page Title:	SDRAM		
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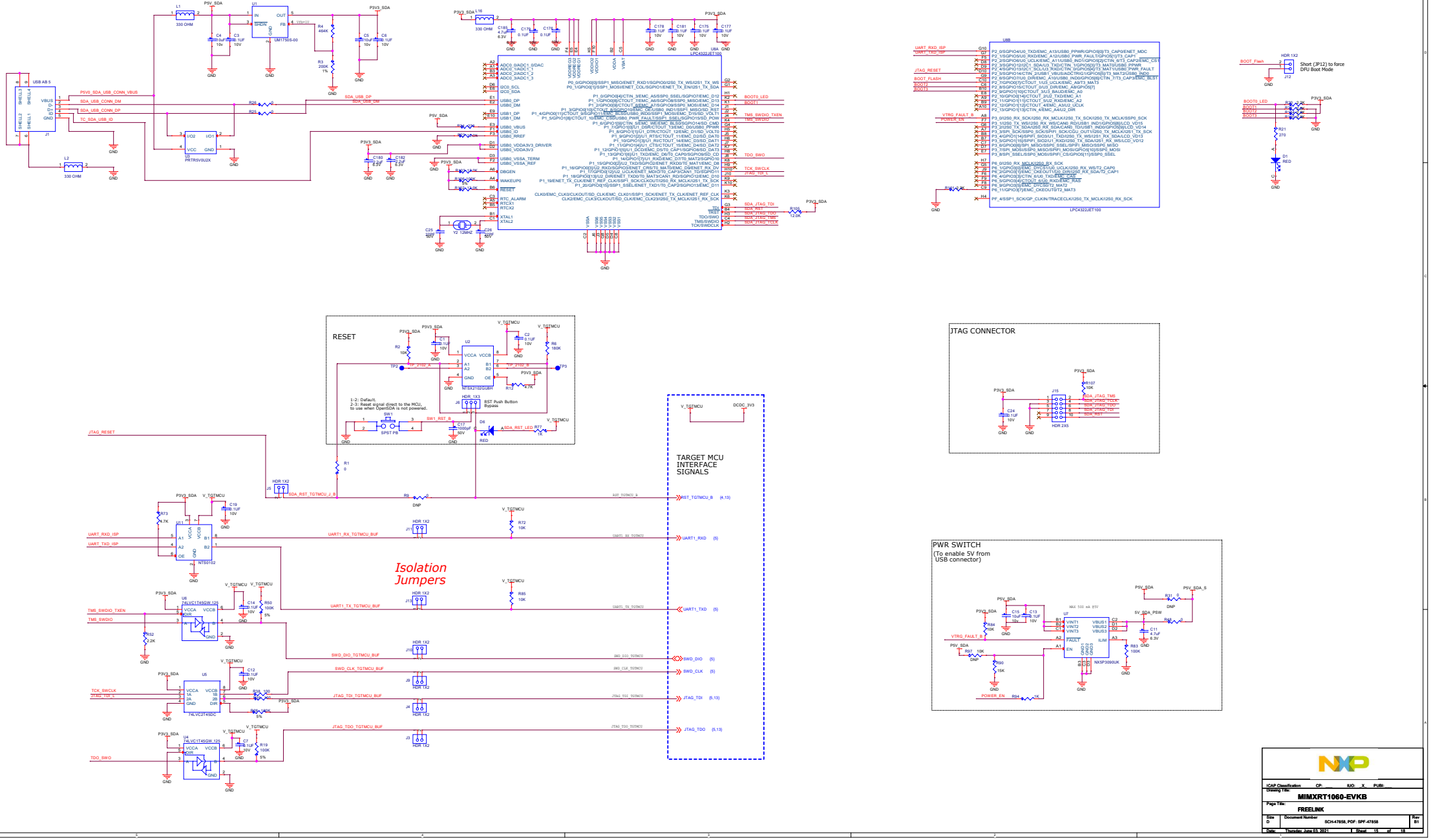
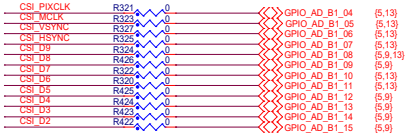
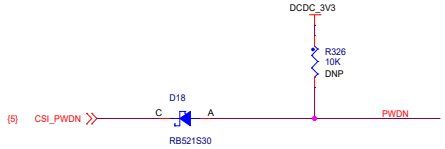
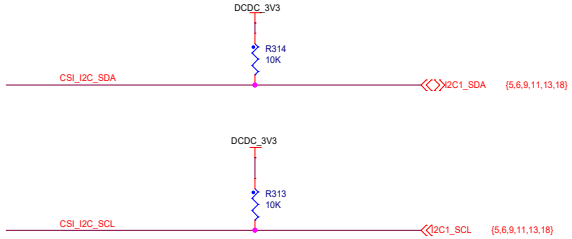
Freelink Interface



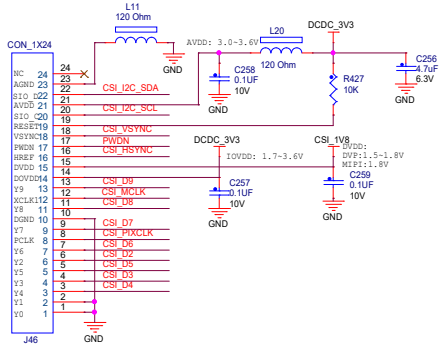
Camera Signals







FPC FOR MT9M114/OV7725 MODULE



ICAP Classification: CP: ___ IUO: X PUBI: ___

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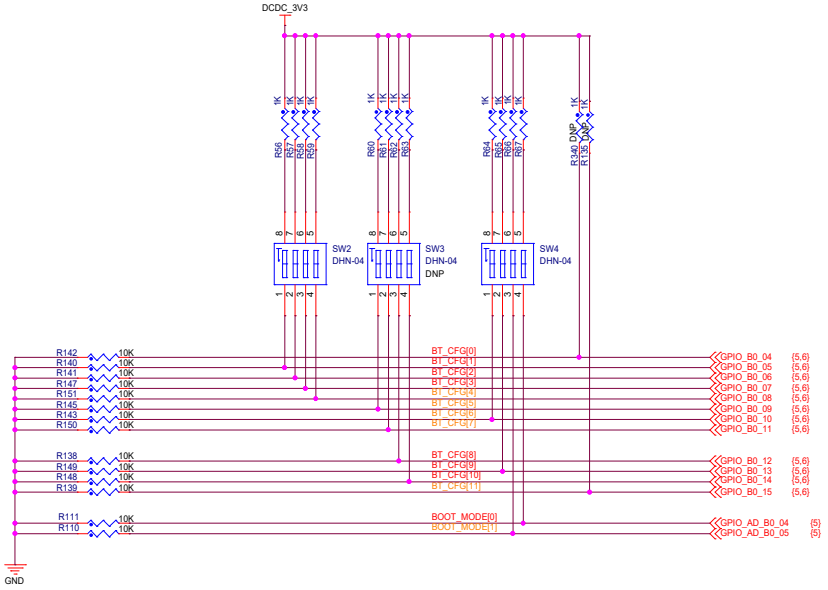
BOOT CONFIG TABLE

	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
TYPE	**BOOT_CFG[11]**	**BOOT_CFG[10]**	**BOOT_CFG[9]**	**BOOT_CFG[8]**	**BOOT_CFG[7]**	**BOOT_CFG[6]**	**BOOT_CFG[5]**	**BOOT_CFG[4]**	**BOOT_CFG[3]**	**BOOT_CFG[2]**	**BOOT_CFG[1]**	**BOOT_CFG[0]**
FlexSPI1 - Serial NOR	*Infinit-Loop: (Debug USE only) 0 - Disable 1- Enable*	*FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR*			*0*	*0*	*0*	*0*	*HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms*		*EncryptedXIP 0 - Disabled 1- Enabled*	*Reserved*
SD	*Infinit-Loop: (Debug USE only) 0 - Disable 1- Enable*	*Reserved*	*Bus Width: 0 - 1-bit 1 - 4-bit*	*SD1 VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V*	*0*	*1*	*SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104*		*SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad*	*SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD '1' - direct*	*Port Select: 0 - eSDHC1 1 - eSDHC2*	*Fast Boot: 0 - Regular 1 - Fast Boot*



ICAP Classification: CP: ___ IUO: X PUBI: ___

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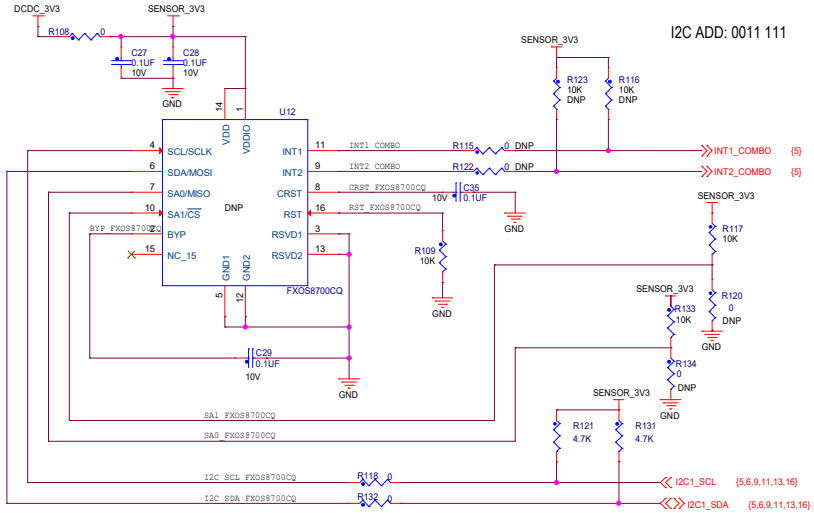
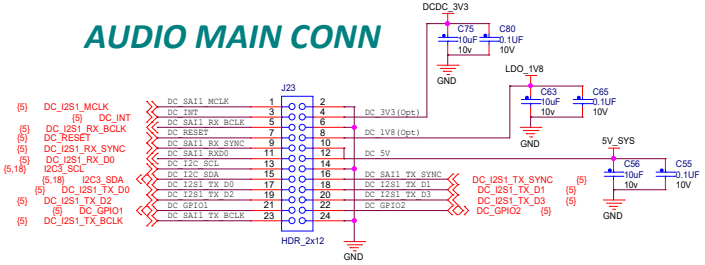
COMBO SENSOR



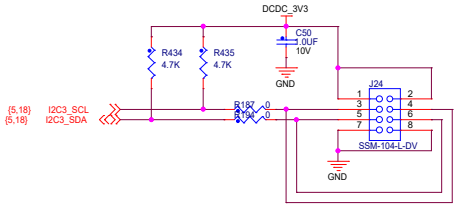
FXOS8700CQ COMBO SENSOR

AUDIO MAIN CONN

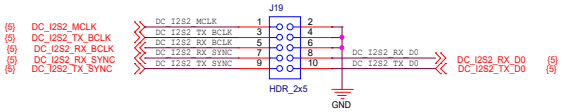


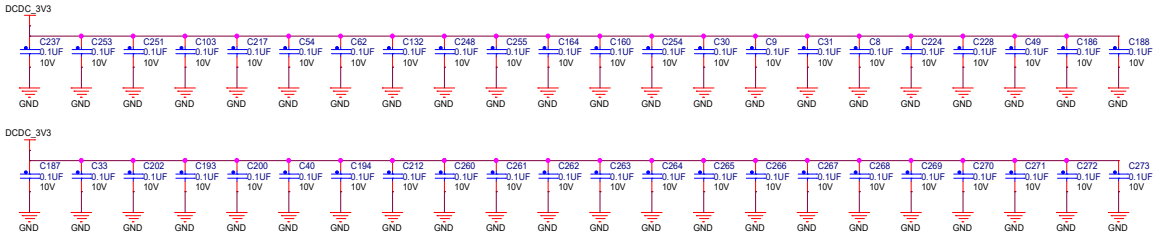
If Audio aux conn (J19) is used, please mount resistors below,
R334,R335,R338,R339,R379,R341,R342

MFI CONN



AUDIO AUX CONN





ICAP Classification:	CP: ___ IUO: X PUBI: ___	
Drawing Title:	MIMXRT1060-EVKB	
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