

Table of Contents	
1	TITLE, TOC & REV
2	NOTES
3	FS86TRK
4	VMON, DEBUG
5	FRDM MCU

Revisions			
Rev	Description	Date	Approved
	Initial draft	May 15th, 2020	Lucie Hernandez
X1	A055, PPL Released	May 18th, 2020	Lucie Hernandez
	A070 Released	May 29th, 2020	Lucie Hernandez
X2	R157 & D20 Added J26 Net names swapped and Default jumpers added J15 Default jumper changed from 1-2 to 2-3 SW4 & SW5 Mfg. part numbers changed. J28 All shorted.	Jun 10th, 2020	Lucie Hernandez
X3	FS0b, MCU signal to FRDM K25Z J1-10 pin (instead of J2-1).	Jun 15th, 2020	Lucie Hernandez
A	A085 (Final SCH, BOM) Prototype Release	July 16th, 2020	Lucie Hernandez
AX1	-R32 changed from 5.1K to 10K -R40 changed from 5.1K to 10K -R36 changed from 1.1K to 0 Ohm -10nF(C66) Added between BAT_SW and GND -10nF(C67) Added between Q7-2 and VSUP -2K(R158) Added between Q7-2 and GND	July 27th, 2020	Lucie Hernandez
B	- In Page3 VSUP net position changed. And Near Q1 Two more nets added before Q1 is VPI net name and after Q1 is VPRE_IN net name's updated. - J29 Removed from the design. - TP7, TP9 & TP11 Test points removed from the design - R2 & R3 Resistor value changed from 6.57k to 6.65k - J28 Jumper removed from the design A085 (Final SCH, BOM) Prototype Release	Sep 10th, 2020	Lucie Hernandez
BX1	As per shared file, Design updated	Jan 5th, 2021	Lucie Hernandez
C	A085 (Final SCH, BOM) Release	Jan 19th, 2021	Lucie Hernandez
D	LBO1 Changed from 180-79539 to 180-79136 A085 (Final SCH, BOM) Release	Feb 23rd, 2021	Lucie Hernandez

KITFS86TRKFRDMEM

Truck Soldered Board

		Analog Sensor Product Group 6501 William Cannon Drive West Austin, TX 78725-8598	
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.			
Designer: Lucie Hernandez	Drawing Title: KITFS86TRKFRDMEM	ICAP Classification: CP:	IND: X PUR:
Drawn by: Ramakrishna	Page Title: TITLE, TOC & REV		
Approved: Dider Pagnoux	Size C	Document Number SCH-47408 PDF: SPF-47408	Rev D
Date: Tuesday, March 09, 2021	Sheet 1 of 5		

Board Configuration

This board is meant to be fully configurable. However, we propose bellow a configuration exemple :

REG	Switching frequency	Output voltage	Max output current	Input	Monitoring
Vpre	455 kHz	4.1V	10A	Vsnp	VMON8_RES
Buck	2.22 MHz	3.3V	2.5A	Vpre	VMON7_RES
Boost	2.22 MHz	6V	1A	Vpre	VMON9_RES
LDO1	-	3.3V	400mA	Vpre	VMON5_RES
LDO2	-	5V	400mA	Vboost	VMON6_RES

Vpre & Pi Filter Coil Selection :

For Vpre 15 Amps :
- PiFilter : SPM7054VT-1R0M-D Isat 19.3A / Itemp@40°C 14.9A (7.5 x 7mm)
- Vpre 455kHz : SPM12565VT-4R7M-D Isat 22.2 / Itemp@40°C 14A (13 x 12.5mm) / DCR 7.1 mOhm

Alternate Parts for Vpre 10 Amps :
- PiFilter : SPM6545VT-1R0M-D Isat 17.9A / Itemp@40°C 13.3A (7 x 6.5mm)
- Vpre 455kHz : SPM10065VT-4R7M-D Isat 19.3A / Itemp 11.7A (10 x 10.5mm) / DCR 9.2 mOhm

Alternate Parts for Vpre 6 Amps :
- PiFilter : SPM6545VT-1R0M-D Isat 17.9A / Itemp@40°C 13.3A (7 x 6.5mm)
- Vpre 455kHz : SPM7054VT-4R7M-D Isat 11.2A / Itemp 7.8A (7.5 x 7mm) / DCR 16.6 mOhm

Alternative parts for 2.22MHz (fit with 455KHz inductors footprint for evaluation purpose) :
- Vpre 2.22MHz : SPM10040T-2R2M-HZ Isat 13A / Itemp@40°C 16.7A (10.7 x 10mm) / DCR 6.8 mOhm
- Vpre 2.22MHz : SPM7054VT-2R2M-D Isat 14.1A / Itemp 12A (7.5 x 7mm) / DCR 7.4 mOhm

Vpre MOS Optimization :

Vpre 455kHz :
For Vpre 15 A (40V max):
- HS : BUK9M9R5-40H
- LS : BUK9M3R3-40H
For Vpre 10 Amps (60V max):
- HS : BUK9M42-60E
- LS : BUK9M12-60E

Vpre 2.22MHz :
For Vpre 6A and 40V max:
- HS : BUK9M20-40H
- LS : BUK9M20-40H

Table 1. Jumper Settings

REF DES	JUMPER	PAGE NAME
J11,J8,J9,J7	DEFAULT(1-2)	03-FS86TRK
J32,J15	DEFAULT(2-3)	03-FS86TRK
J13	DEFAULT(7-8)	03-FS86TRK
J4	DEFAULT(OPEN)	03-FS86TRK
J31,J12,J3	OPEN	03-FS86TRK
J26	DEFAULT(1-2) (3-4) (5-6) (7-8)	04-VMON, DEBUG
J19,J20,J18,J17,J27	DEFAULT(1-2)	04-VMON, DEBUG
J24	DEFAULT(2-3)	04-VMON, DEBUG
J25	OPEN	04-VMON, DEBUG

Table 2. DNP Components

REF DES	ASSY OPT	PAGE NAME
R159,C68,R11,CPRE2,CSUP5,R6,C18,C17,C4,R7,CSUP6,D3,D21,R2,C69,C19,CPI3,CPRE3,R42,C20,R13	DNP	03-FS86TRK
R151,R149	DNP	04-VMON, DEBUG
C70	DNP	05-FRDM MCU

Table 3. SWITCH DEFAULT Settings

REF DES	SWITCH	PAGE NAME
SW2	DEFAULT(OPEN)	03-FS86TRK
SW3	OFF	03-FS86TRK
SW1	ON	03-FS86TRK
SW5,SW4	DEFAULT ALL ON	03-FS86TRK

Table 4. Solder Jumper Setting

REF DES	SHORT	PAGE NAME
SJ2	OPEN	03-FS86TRK
SJ3,SJ4,SJ6,SJ1,SJ5	SHORT	03-FS86TRK

Alternate Parts for Vpre 10 Amps :
- Vpre 455KHz : XAL1010-682 Isat 21.8A / Itemp 14A (10x11.3mm)
- Vpre 2.22MHz : XAL6030-182ME Isat 18.2A / Itemp@20C 10A

For Vpre 6 Amps :
- Vpre : XAL6060-682ME



EAP Classification: CP: BUC: PUB:			
Drawing Title: KITFS86TRKFRDMEM			
Page Title: NOTES			
Size C	Document Number	SCH-47408 PDF: SPF-47408	Rev D
Date:	Tuesday, March 09, 2021	Sheet 2 of 5	

Fixed Voltage Monitoring

VMONs Fixed Resistor Bridges		
Monitoring		
	VMON_3V3	VMON_5V
Voltage	3.3V	5V
RH	37.4K	105K
RL	12K	20K

VMON_08V

Flexible Voltage Monitoring

VMONs Flexible Resistor Bridges

	Monitoring		
	VMON7	VMON8	VMON9
Voltage	0.8V -> 3.9V	2.4V -> 5.5V	3.9V -> 7V
RH	POT 20K	10K + POT 20K	20K + POT 20K
RL	5.1K	5.1K	5.1K

VMON7

VMON8

VMON9

VMON7_RES 3

VMON8_RES 3

VMON9_RES 3

VMON_08V

[illegible]

FS8600 Signals

Signal	Pin	Signal	Pin
3 ERRMON	1	VDD	2
3.4.5 INT#	3	4	4
3 FOUT	5	6	6
3.4.5 FOUT	7	8	8
3 AMUX	9	10	10
3 XFALL	11	12	12
3 RST#	13	14	14
3.4 PGOOD	15	16	16
3.5 FBIN_OU	17	18	18
3 FCCU	19	20	20
3 FCCU	19	21	21
		22	22
		23	23
		24	24
		25	25

OPEN

GND

FS8600 Monitored Signal

Diagram showing the pin connections for the FS8600 Monitored Signal. The connector is labeled J26.

Signal	Pin	Signal	Pin
VPRE	1	VMON8	2
VBOOST	3	VMON5	4
BUCK	5	VMON7	6
LDO1	7	VMON5_VDD	8
LDO2	9	VMON5_VDD	10
EXT_RSG1	11	EXT_RSG2	12
EXT_RSG2	13	EXT_RSG3	14
EXT_RSG3	15	EXT_RSG4	16
EXT_RSG4	17	EXT_RSG5	18
EXT_RSG5	19	EXT_RSG6	20

Additional connections shown:

- VPRE, VBOOST, BUCK, LDO1, LDO2, EXT_RSG1, EXT_RSG2, EXT_RSG3, EXT_RSG4, EXT_RSG5, EXT_RSG6, EXT_RSG7, EXT_RSG8, EXT_RSG9, EXT_RSG10 are connected to a common VBUS line.
- EXT_RSG1, EXT_RSG2, EXT_RSG3, EXT_RSG4, EXT_RSG5, EXT_RSG6, EXT_RSG7, EXT_RSG8, EXT_RSG9, EXT_RSG10 are connected to a common GND line.
- EXT_RSG1, EXT_RSG2, EXT_RSG3, EXT_RSG4, EXT_RSG5, EXT_RSG6, EXT_RSG7, EXT_RSG8, EXT_RSG9, EXT_RSG10 are connected to a common GND line.

Legend:

- VPRE, VBOOST, BUCK, LDO1, LDO2, EXT_RSG1, EXT_RSG2, EXT_RSG3, EXT_RSG4, EXT_RSG5, EXT_RSG6, EXT_RSG7, EXT_RSG8, EXT_RSG9, EXT_RSG10
- VMON8, VMON5, VMON7, VMON5_VDD, VMON5_VDD
- EXT_RSG1, EXT_RSG2, EXT_RSG3, EXT_RSG4, EXT_RSG5, EXT_RSG6, EXT_RSG7, EXT_RSG8, EXT_RSG9, EXT_RSG10

Default connections: DEFAULT (1-2) (3-4) (5-6) (7-8) (9-10)

POWER

MON1_DAC 3
MON2_DAC 3
MON3_DAC 3
MON4_RNT 3

3.4.5 VPRE

GND

GND

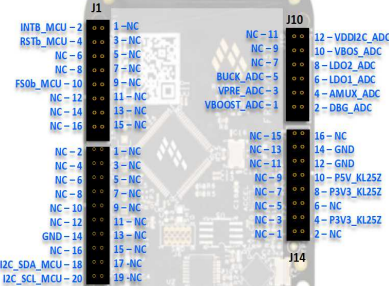
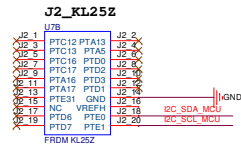
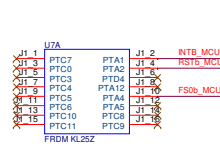
GND

CON_1X4

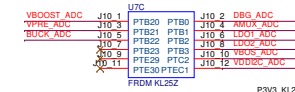
- * for VPRE <10A , use pins 2 and 3 *
- * For VPRE >10A , use pins 1,2,3 and 4 *

FRDM KL25Z – pinout

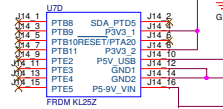
© 2012 FREESCALE



J10_KL25Z



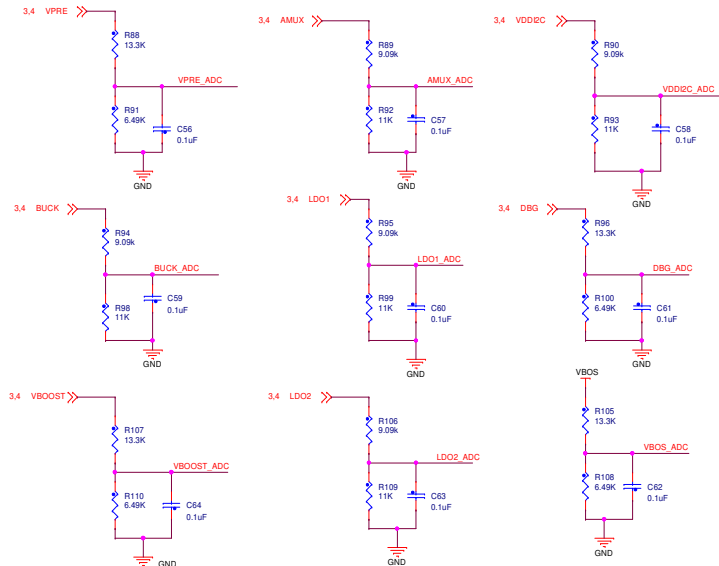
J14_KL25Z



KL25Z Decoupling Caps

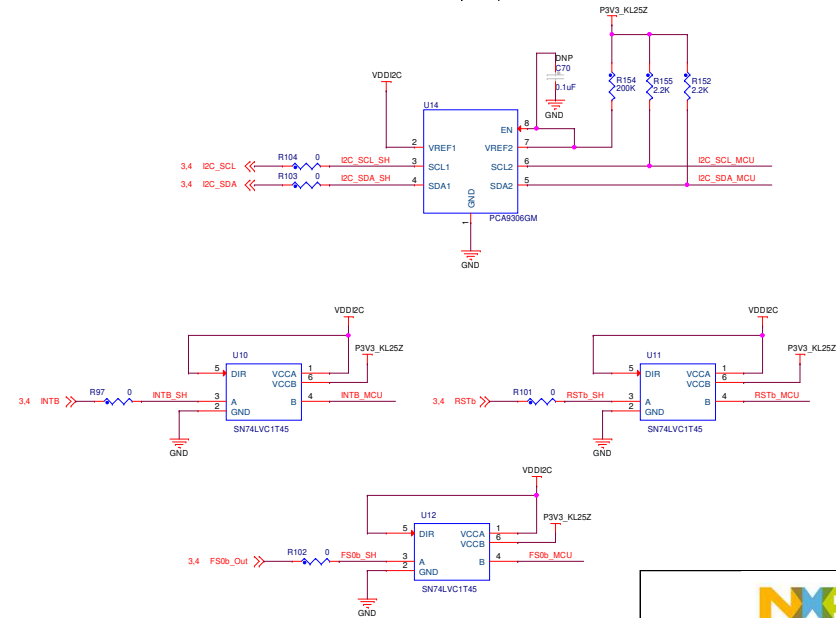
CAD NOTE:
Please place these capacitors
near each respective CPU pin
(VREFH to VREFL
and VDDA to VSSA).
Decoupling capacitors
shall be used for these
pins: VDD1, VDD2, VDDA.

Analog Inputs



Level Shifter (1.65V / 5.5V)

Fail Safe Outputs / I2C



ICAP Classification:		CP:	BUO:	PUB:
Drawing Title: KITFS86TRKFRDMEM				
Page Title: FRDM MCU				
Size C	Document Number SCH-47408 PDF: SPF-47408			Rev D
Date:	Tuesday, March 09, 2021		Sheet	5 of 5