8MPLUSLPD4-PWR

(i.MX8M Plus Reference Board)

Table of Content

Revision History

Rev. Code	Date	By	Description
A	2020-01-22	Frank, Elyon	Initial version
A1	2020-11-02	Elyon	1. Update the block diagram, change "OTG" to "Dual Role". 2. Change R74 to 4.7M, and change the state from DNP to populate. 3. Change several Boot Mode configurations on page 11 to "Reserved". 4. Change R208 to 0.4 OHM for VDD_USB_0V8 measurement. 5. Change R76 to 1.0 OHM for VDD_PLL_ANA_0V8 measurement. 6. Change R225 to 1.0 OHM for VDD_LVDS_1V8 measurement. 7. Change R227 to 1.0 OHM for VDD_PCI_1V8 measurement. 8. Change R129 to 0.05 OHM for LPD4_VDD2 measurement. 9. Change R209 to 0.4 OHM for VDD_PCI_0V8 measurement. 10. Update U1 part number from "MIMX8ML8DVNLZAA" to "MIMX8ML8DVNLZAB". 11. Update U1 symbol: Change USB1_ID to USB1_DNU, USB2_ID to USB2_DNU, MIPI_VREG2_CAP to MIPI_TEST_DNU; Remove DDR3L option for DDR interface. 12. Remove the signal connections for USB1_DNU(USB1_ID), USB2_DNU(USB2_ID). 13. DNP the decoupling capacitor C106 for MIPI_TEST_DNU(MIPI_VREG2_CAP), can be floating for normal use. 14. Update the Power Sequence and Operating Range Table on Page 11. 15. Change R77 to 0.4 OHM for VSYS_5V small current range measurement. 16. Change R80 to 1.0 OHM for VDD_SOC small current range measurement. 17. Change R95 to 2.0 OHM for NVCC_DRAM_1V1 small current range measurement. 18. Change R87 to 2.0 OHM for LPD4_VDDQ small current range measurement. 19. Change R94 to 1.0 OHM for VDD_PLL_ANA_1V8 large current range measurement.

1. Interrupted lines coded with the same letter or letter combinations are electrically connected.

2. Device type number is for reference only. The number varies with the manufacturer.

3. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

4. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

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This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

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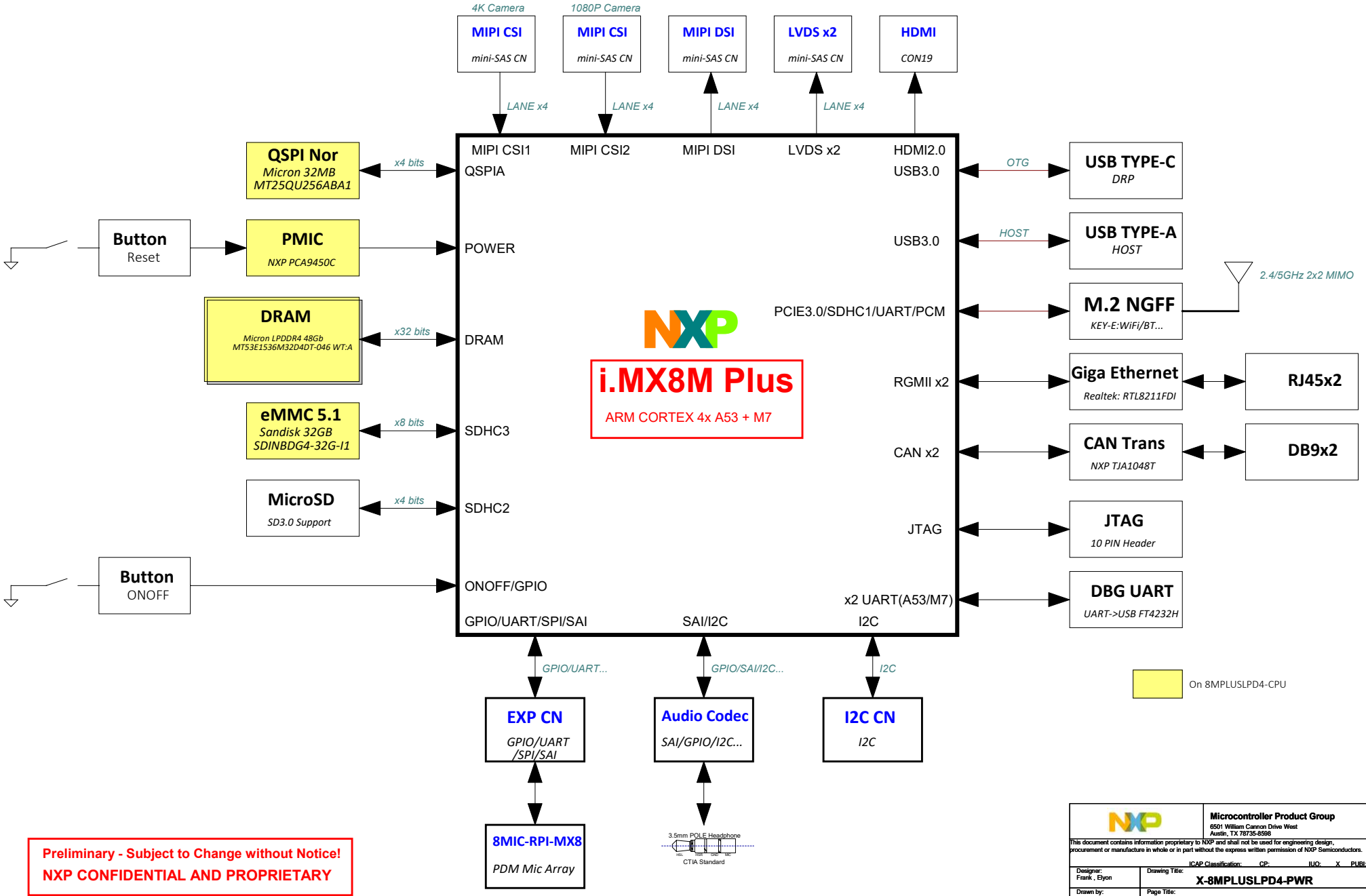
Designer: Frank , Elyon	Drawing Title: X-8MPLUSLPD4-PWR		
Drawn by: Frank , Elyon	Page Title: Title and Rev History		
Approved: <Approver>	Size C	Document Number SCH-46881 PDF:SPF-46881	Rev A1
	Date: Wednesday, November 04, 2020	Sheet 1 of 14	

IMX8MPLUSLPD4-EVK Block Diagram



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8MPLPD4-EVK PWR TREE

Base Board → VSYS *5V*

PMIC: PCA9450C

SEQ	REG	TYP	Max Capability(mA)
1	LDO1	1.8	10
2	RTC_CLK	--	--
3	BUCK1/3	0.85/0.95	6000
4	BUCK2	0.85/0.95/1.0	3000
5	LDO3	1.8	300
6	BUCK5	1.8	2000
7	BUCK6	1.1	2000
8	BUCK4	3.3	3000
8	MUXSW	3.3	400
9	LDO5	3.3/1.8	150
10	POR_B	--	--

CPU: i.MX8M Plus

SEQ	PWR/Signal	TYP	Required(mA)
1	NVCC_SNVS_1V8	1.8	10
2	32K_INTERNAL	--	--
3	VDD_SOC	0.85/0.95	5000
4	VDD_ARM	0.85/0.95/1.0	2200
5	VDDA_1V8	1.8	300
6	VDD_1V8/NVCC_xxx	1.8	NxCxVx(0.5xF)
7	NVCC_DRAM_1V1	1.1	NxCxVx(0.5xF)
8	VDD_3V3/NVCC_xxx	3.3	NxCxVx(0.5xF)
8	VSD_3V3	3.3	300
9	NVCC_SD2	3.3/1.8	10
10	POR_B	--	--

LPDDR4
VDD1
VDD2/VDDQ

QSPI
VCC

eMMC
VCCQ
VCC

WiFi/BT
VBAT
VIO

Base Board Peripherals

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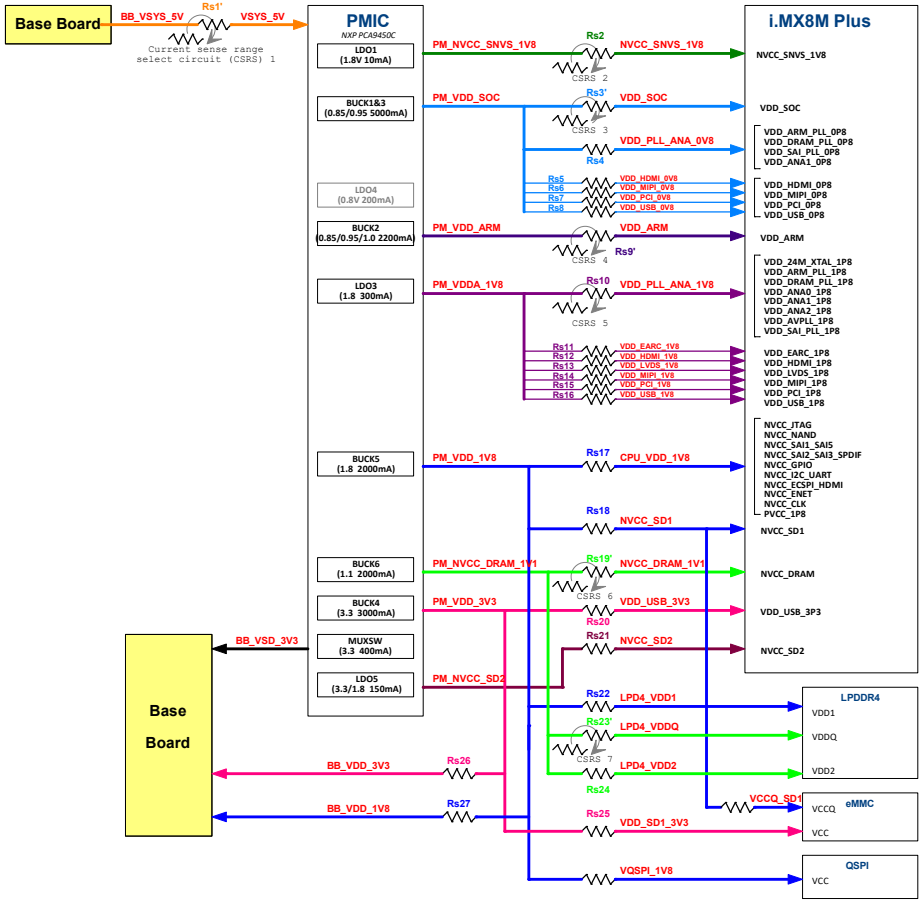
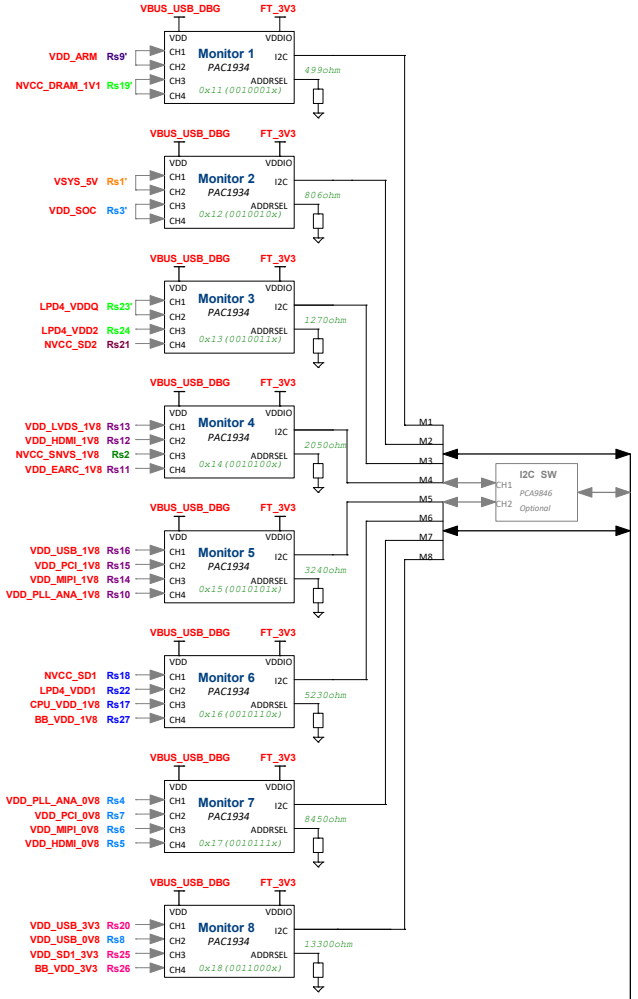
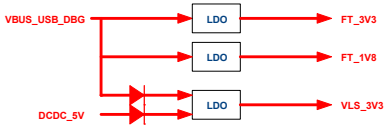
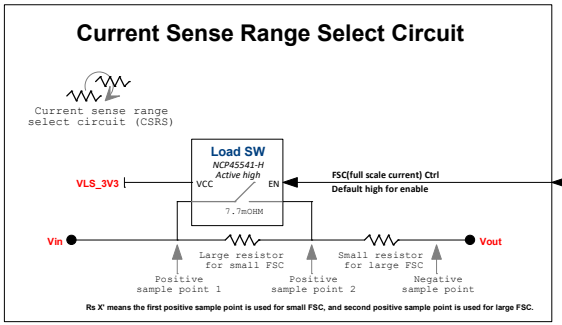
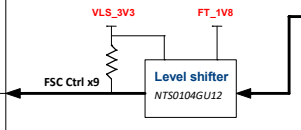
i.MX8M Plus EVK Power Measurement Diagram

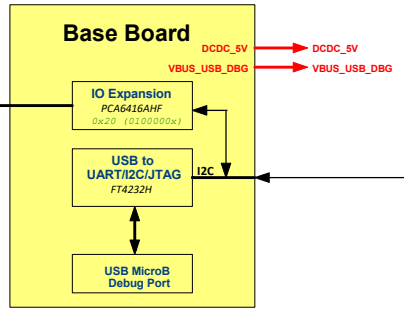












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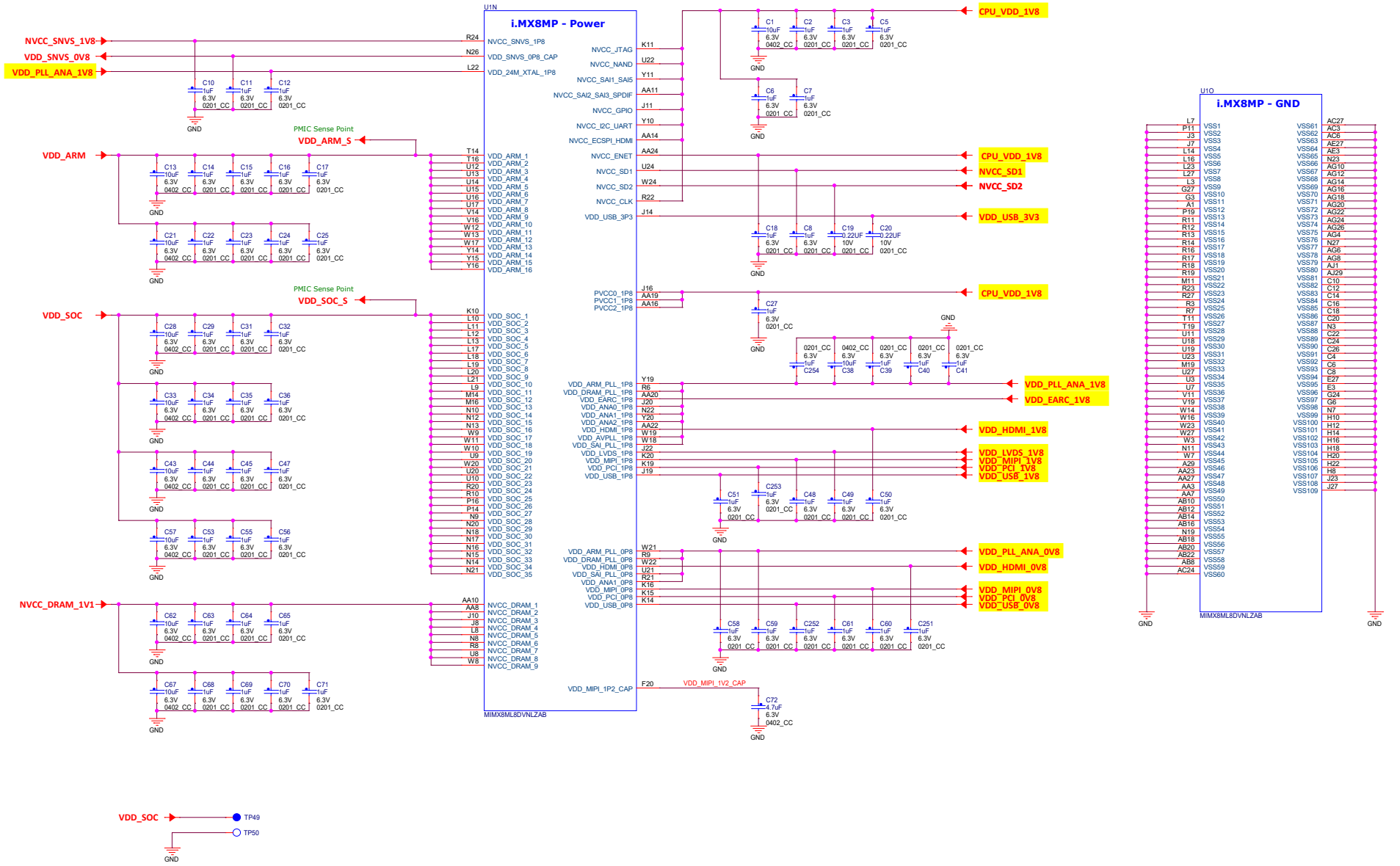
X-8MPLUSLPD4-PWR
PWR MEASUREMENT DIAGRAM

i.MX8M Plus PWR



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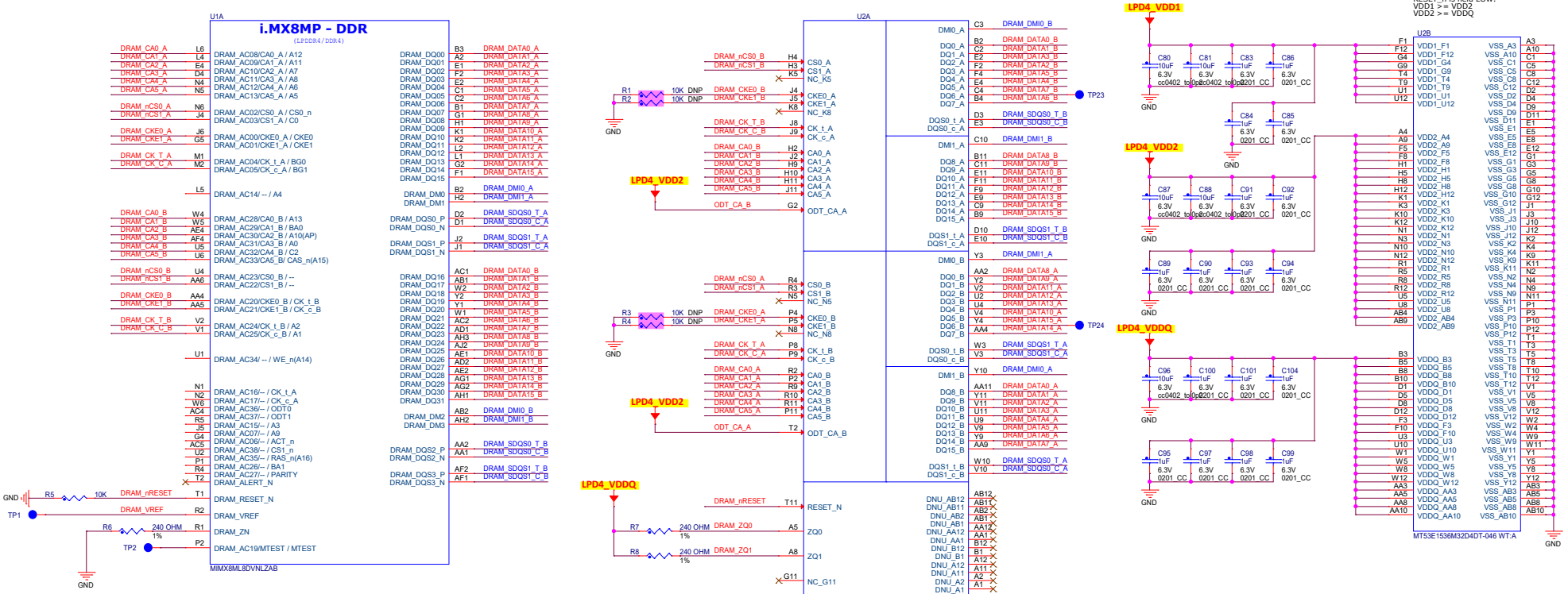
LPDDR4 6GB



Data Bus

Pin Name	LPDDR4	DDR4
DRAM_DQS0_P	DQS0_t_A	DQSL_t_A
DRAM_DQS0_N	DQS0_c_A	DQSL_c_A
DRAM_DM0	DMI0_A	DML_n_A / DBIL_n_A
DRAM_DQ00	DQ0_A	DQL0_A
DRAM_DQ01	DQ1_A	DQL1_A
DRAM_DQ02	DQ2_A	DQL2_A
DRAM_DQ03	DQ3_A	DQL3_A
DRAM_DQ04	DQ4_A	DQL4_A
DRAM_DQ05	DQ5_A	DQL5_A
DRAM_DQ06	DQ6_A	DQL6_A
DRAM_DQ07	DQ7_A	DQL7_A
DRAM_DQS1_P	DQS1_t_A	DQSU_t_A
DRAM_DQS1_N	DQS1_c_A	DQSU_c_A
DRAM_DM1	DMI1_A	DMU_n_A / DBIU_n_A
DRAM_DQ08	DQ8_A	DQU0_A
DRAM_DQ09	DQ9_A	DQU1_A
DRAM_DQ10	DQ10_A	DQU2_A
DRAM_DQ11	DQ11_A	DQU3_A
DRAM_DQ12	DQ12_A	DQU4_A
DRAM_DQ13	DQ13_A	DQU5_A
DRAM_DQ14	DQ14_A	DQU6_A
DRAM_DQ15	DQ15_A	DQU7_A
DRAM_DQS2_P	DQS0_t_B	DQSL_t_B
DRAM_DQS2_N	DQS0_c_B	DQSL_c_B
DRAM_DM2	DMI0_B	DML_n_B / DBIL_n_B
DRAM_DQ16	DQ0_B	DQL0_B
DRAM_DQ17	DQ1_B	DQL1_B
DRAM_DQ18	DQ2_B	DQL2_B
DRAM_DQ19	DQ3_B	DQL3_B
DRAM_DQ20	DQ4_B	DQL4_B
DRAM_DQ21	DQ5_B	DQL5_B
DRAM_DQ22	DQ6_B	DQL6_B
DRAM_DQ23	DQ7_B	DQL7_B
DRAM_DQS3_P	DQS1_t_B	DQSU_t_B
DRAM_DQS3_N	DQS1_c_B	DQSU_c_B
DRAM_DM3	DMI1_B	DMU_n_B / DBIU_n_B
DRAM_DQ24	DQ08_B	DQU0_B
DRAM_DQ25	DQ09_B	DQU1_B
DRAM_DQ26	DQ10_B	DQU2_B
DRAM_DQ27	DQ11_B	DQU3_B
DRAM_DQ28	DQ12_B	DQU4_B
DRAM_DQ29	DQ13_B	DQU5_B
DRAM_DQ30	DQ14_B	DQU6_B
DRAM_DQ31	DQ15_B	DQU7_B

Command/Address

Pin Name	LPDDR4	DDR4
DRAM_RESET_N	RESET_N	RESET_n
DRAM_ALERT_N	MTEST1	ALERT_n / MTEST1
DRAM_AC00	CKE0_A	CKE0
DRAM_AC01	CKE1_A	CKE1
DRAM_AC02	CS0_A	CS0_n
DRAM_AC03	CS1_A	C0
DRAM_AC04	CK_t_A	BG0
DRAM_AC05	CK_c_A	BG1
DRAM_AC06	/	ACT_n
DRAM_AC07	/	A9
DRAM_AC08	CA0_A	A12
DRAM_AC09	CA1_A	A11
DRAM_AC10	CA2_A	A7
DRAM_AC11	CA3_A	A8
DRAM_AC12	CA4_A	A6
DRAM_AC13	CA5_A	A5
DRAM_AC14	/	A4
DRAM_AC15	/	A3
DRAM_AC16	/	CK_t_A
DRAM_AC17	/	CK_c_A
DRAM_AC19	MTEST	MTEST
DRAM_AC20	CKE0_B	CK_t_B
DRAM_AC21	CKE1_B	CK_c_B
DRAM_AC22	CS1_B	/
DRAM_AC23	CS0_B	/
DRAM_AC24	CK_t_B	A2
DRAM_AC25	CK_c_B	A1
DRAM_AC26	/	BA1
DRAM_AC27	/	PARITY
DRAM_AC28	CA0_B	A13
DRAM_AC29	CA1_B	BA0
DRAM_AC30	CA2_B	A10 / AP
DRAM_AC31	CA3_B	A0
DRAM_AC32	CA4_B	C2
DRAM_AC33	CA5_B	CAS_n / A15
DRAM_AC34		WE_n / A14
DRAM_AC35	/	RAS_n / A16
DRAM_AC36	/	ODT0
DRAM_AC37	/	ODT1
DRAM_AC38	/	CS1_n
DRAM_ZN	ZQ	ZQ
DRAM_VREF	VREF	VREF

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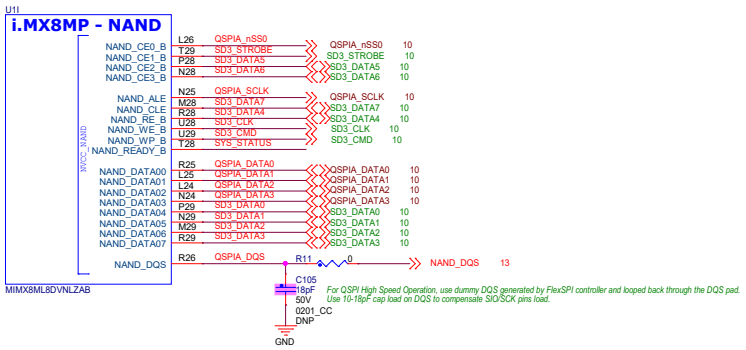
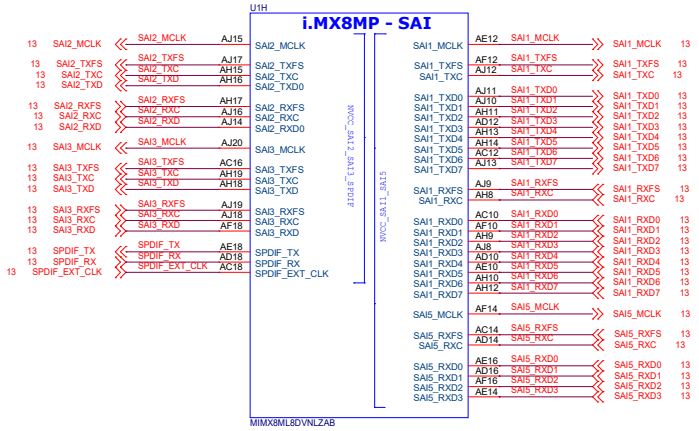
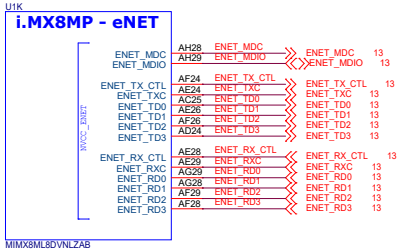
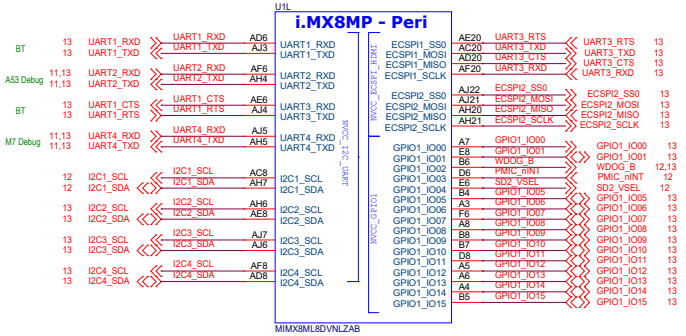
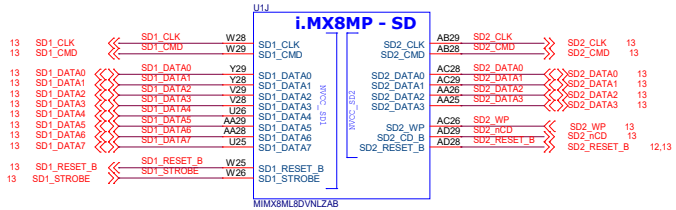
i.MX8M Plus IO Interface

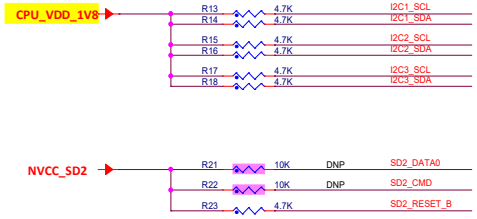


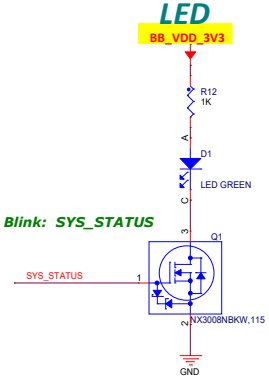












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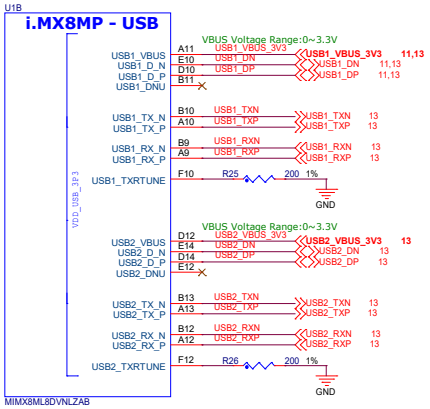
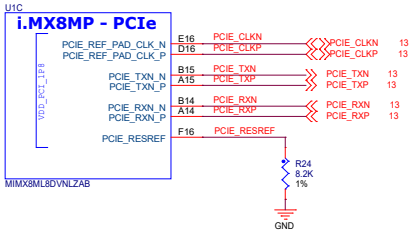
i.MX8M Plus PHYs

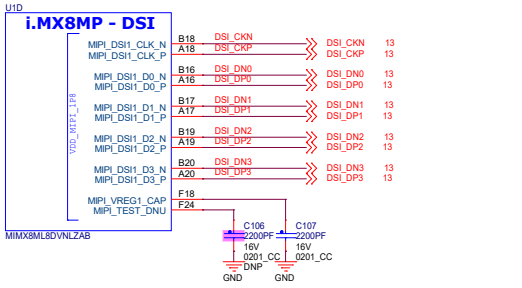


Note:

1. USB1_DNU, USB2_DNU are not functional, if USB ID function is needed, use common GPIO.

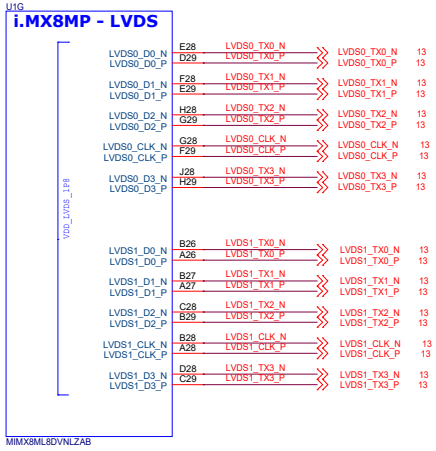
2. If USB connector is MicroAB or MicroB, USBx_VBUS MUST not connect directly to the 5V VBUS voltage of connector; Instead, this pin must be isloated with an external 30K 1% resistor.

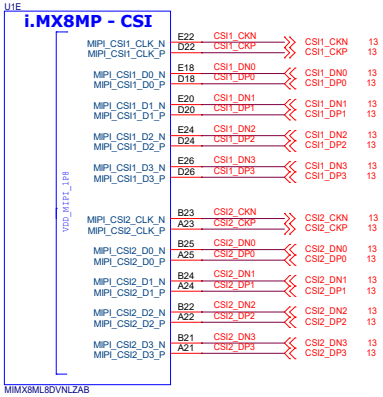


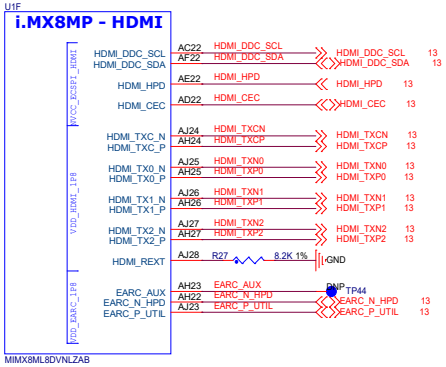


Note:

MIPI_TEST_DNU is for internal test, can be floating for normal use.







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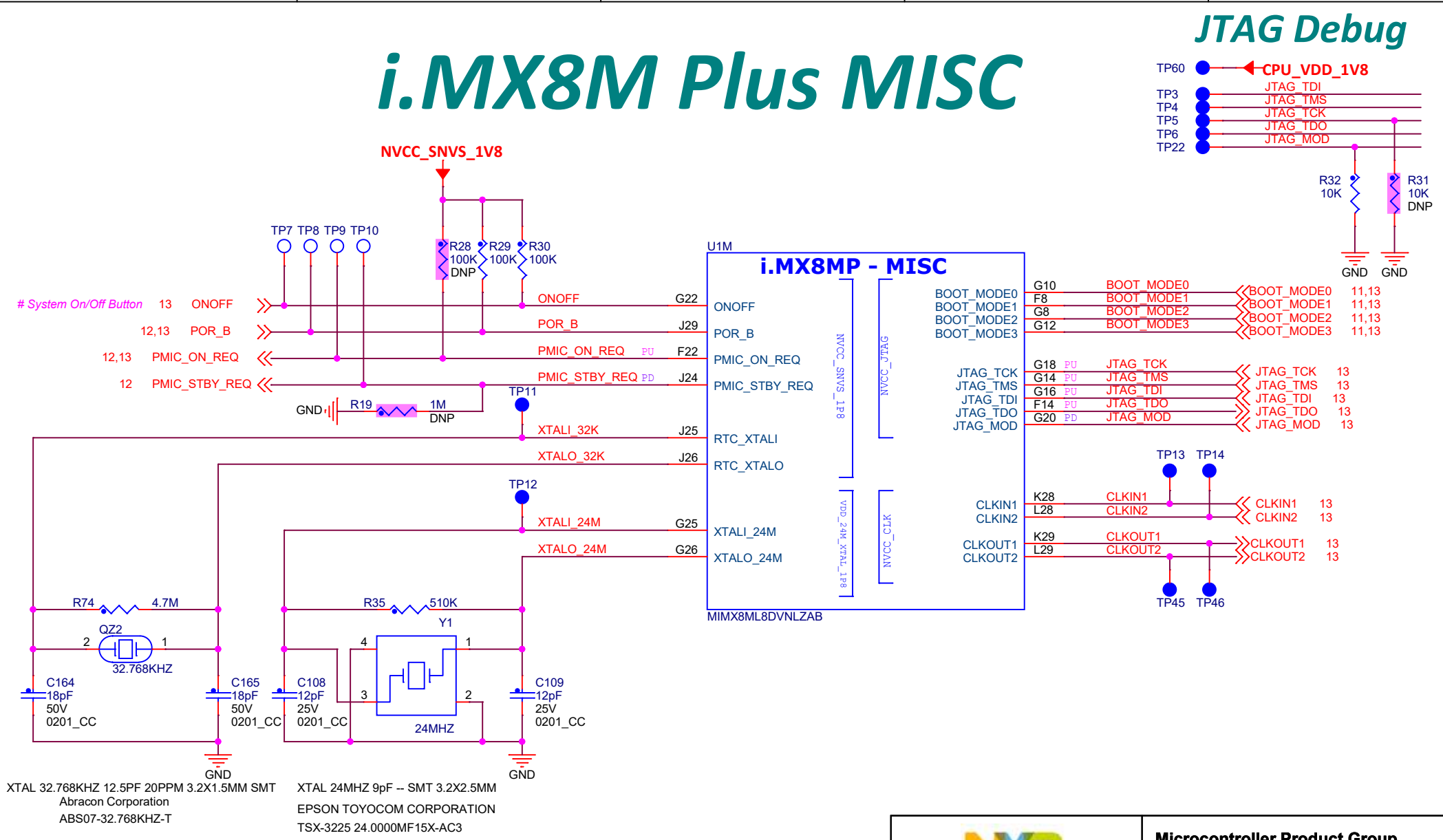
i.MX8M Plus MISC



Caution:

BOOT_MODE0, BOOT_MODE1, BOOT_MODE2, BOOT_MODE3, JTAG_MOD and POR_B must be pulled to "111111" for i.MX8M Plus to enter Boundary Scan mode.

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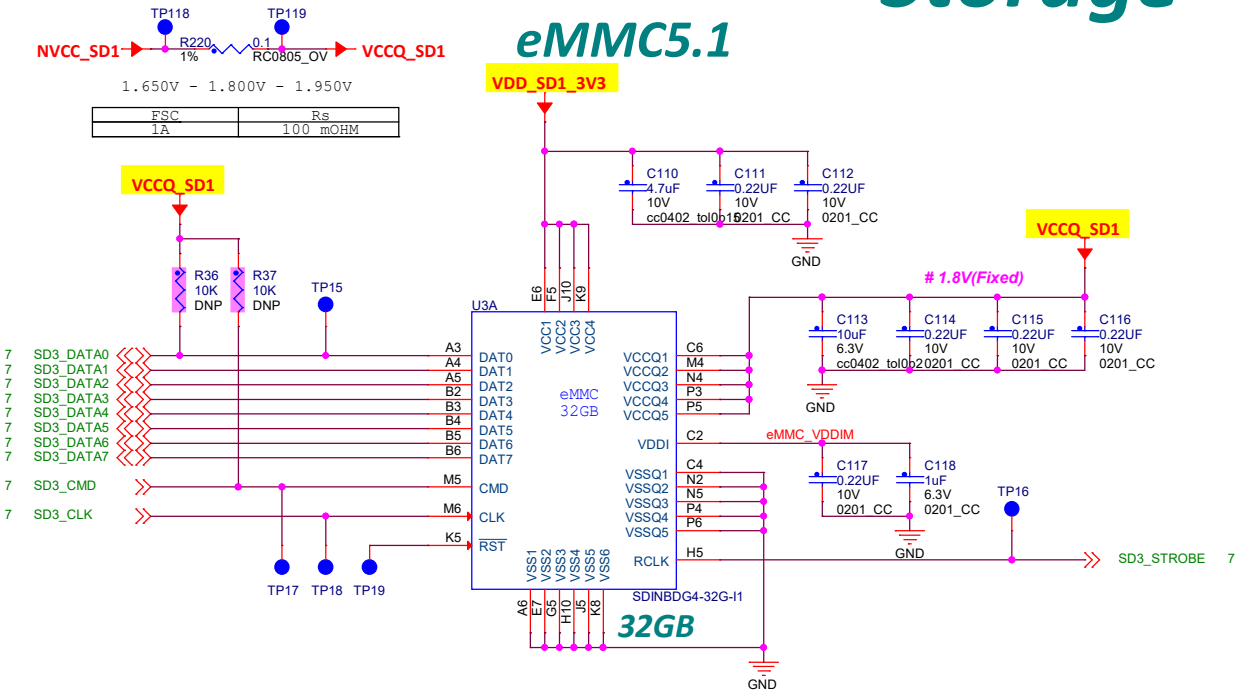
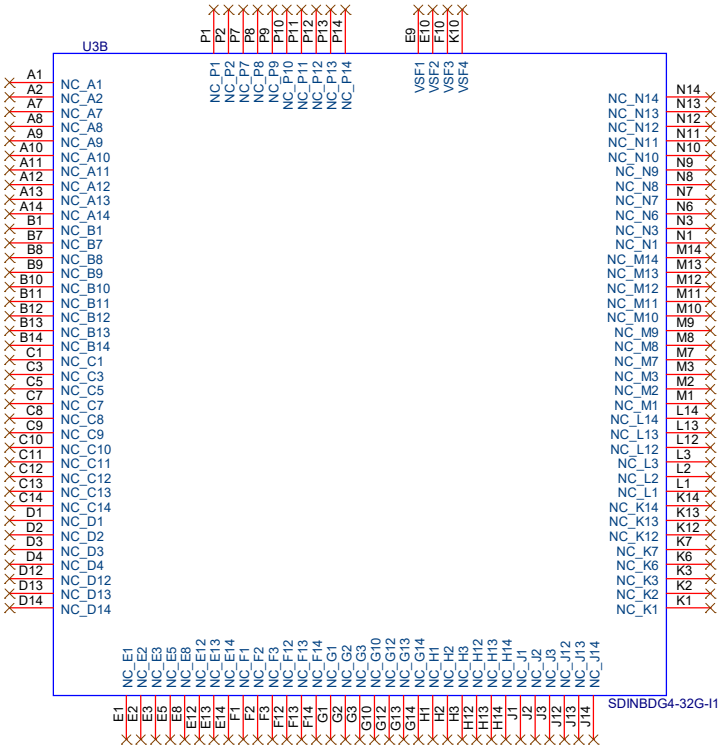
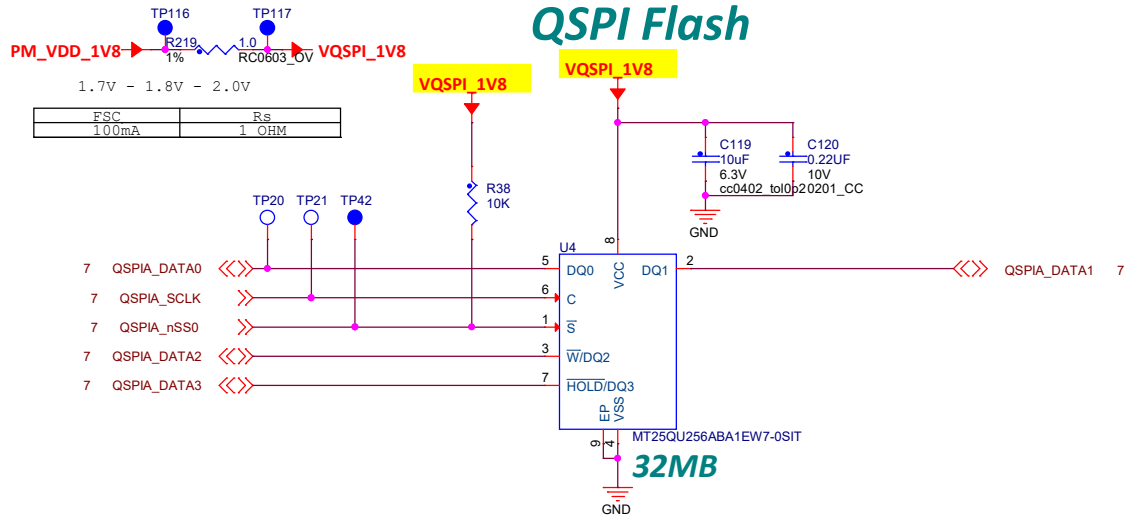
Storage

eMMC5.1





QSPI Flash



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Boot Mode and CFG Switch

i.MX8M Plus ROM Fuse

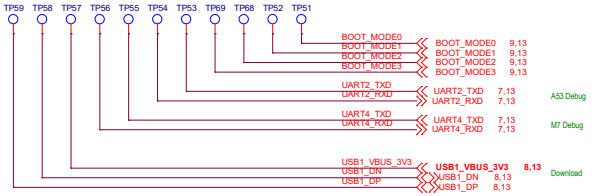
Full Line Address	Physical Address	7	6	5	4	3	2	1	0
0x470[15:0]	0x470[7:0]	OVERRIDE_NAND_PG_PER_BLK_VAL 00 - 32 pages 01 - 64 pages 10 - 128 pages 11 - 32 pages		OVERRIDE_FLEXSPI_BT_SEL 0 - Do not overriude 1 - Override	OVERRIDE_FLEXSPI_BT_SEL_VAL 00 - FlexSPI (Hyperflash 1.8V) 01 - FlexSPI (Flash with 4B READ(1x13 default supported) 10 - Default Octal mode (Micron, supported on 8QXP B0 already) 11 - Default Octal mode (Mxic, Nice to have)	FLEXSPI_AUTO_PROBE_EN 0 - Disable 1 - Enable	FLEXSPI_AUTO_PROBE_TYPE 00 - QuadSPI NOR 01 - MxicOctal 10 - MicronOctal 11 - AdestoOctal	
0x480[15:0]	0x480[7:0]	Reserved	FLEXSPI_DUMMY_CYCLE_SEL				FLEXSPI_FEQ_SEL 000 - 100 MHz 001 - 133 MHz 010 - 166 MHz 011 - 200 MHz 100 - 80 MHz 101 - 20 MHz		
0x480[31:16]	0x480[23:16]	NOC_ID_REMAP_BYPASS	ROM_NO_LOG if blown, ROM will not log event to log buffer	SDP_DISABLE Disable USB serial download	FORCE_BT_FROM_FUSE Boot from programmed fuses, not Boot Mode Pins	FLEXSPI_HOLD_TIME_SEL 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		WDOG_TIMEOUT_SELECT 00 - 2.0s 01 - 1.5s 10 - 1.0s 11 - 0.5s	
0x490[15:0]	0x490[7:0]	USDHC_PWR_EN 0 - No power cycle 1 - Enabled via	EMMC_FAST_BT 0 - Regular 1 - Fast Boot	SDMMC_BUS_WIDTH 00 - 8-bit 01 - 4-bit 10 - 8-bit DDR (MMC 4.4) 11 - 4-bit DDR (MMC 4.4)	SD_SPEED: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104	EMMC_SPEED: 00 - Normal 01 - High	USDHC_VOL_SEL For Normal Boot Mode IO Voltage 0 - 3.3V 1 - 1.8V	USDHC_MFG_VOL_SEL For Mfg Mode IO Voltage 0 - 3.3V 1 - 1.8V	
0x490[31:16]	0x490[23:16]	RECOVERY_SDMMC_BOOT_DIS 0 - Enable 1 - Disable	IMG_CNTN_SET1_OFFSET			USDHC_PAD_SION_EN 0 - Disable 1 - Enable	BT_RDC_DISABLE	USDHC_DLL_EN 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/eMMC	
0x4A0[15:0]	0x4A0[7:0]	SD_CALI_STEP '00' - 1 TBD	USDHC_PWR_INTERVAL 00 - 20ms 01 - 10ms 10 - 5ms 11 - 2.5ms		USDHC_PWR_DELAY 0 - 5ms 1 - 2.5ms	USDHC_PWR_POLARITY 0 - Low 1 - High	USDHC_OVRD_PAD_SETTING_UP1	EMMC_FAST_BT_ACK 0 - Boot Ack Disabled 1 - Boot Ack Enabled	
0x4A0[31:16]	0x4A0[23:16]	Reserved							
0x4B0[15:0]	0x4B0[7:0]	Reserved	NAND_GPMI_DDR_DLL_VAL (GPMI Read DDR DLL Target Value) 0000 - 7 0001 - 1 0111 - 0 1111 - 15				USB_SS_ENABLE	NAND_CS_NUM (Nand Number Of Devices) 00 - 1 01 - 2 10 - 4 11 - Reserved	
0x4B0[31:16]	0x4B0[23:16]	Reserved	FlexSPI NAND Busy Bit Offset Override		FlexSPI NAND CS Interval 00-100ns 01-200ns 10-400ns 11-50ns		FlexSPI NAND Column Address Width 00-12 01-13 10-14 11-15		

Full Line Address	Physical Address	7	6	5	4	3	2	1	0
0x470[15:0]	0x470[15:8]	BOOT_MODE_FUSES BootRom will retrieve boot mode from these fuses instead of BOOT_MODE pins if * BOOT_MODE_PINS=0x0 or * BT_FUSE_SEL blown				OVERRIDE_USDHC_BT_SEL 0 - Do not override 1 - Override	OVERRIDE_USDHC_BT_SEL_VAL 00 - uSDHC1 SD 01 - uSDHC1 eMMC 10 - uSDHC2 eMMC 11 - uSDHC3 SD		OVERRIDE_NAND_PG_PER_BLK 0 - Do not override 1 - Override
0x480[15:0]	0x480[15:8]	BT_LPB (Core/DDR/Bus) '00'/'01' - LPB Disable '10' - Div by 2 '11' - Div by 4		BT_LPB_POLARITY (GPIO polarity)	ICACHE_DIS L1 I-Cache DISABLE	TZASC_EN	WDOG_EN '0' - Disabled '1' - Enabled	BT_FREQ_SEL (ARM/DDR) 0 - 800 / 800 MHz 1 - 400 / 400 MHz	DCACHE_DIS Disable L1 and L2 D-Cache
0x480[31:16]	0x480[31:24]	ECSPI_PORT_SEL 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3		ECSPI_ADDR_SEL 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)	ECSPI_CS_SEL(SPI only) 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		RECOVER_ECSPI_BOOT_EN '0' - Disabled '1' - Enabled		DCACHE_BYPASS_DIS
0x490[15:0]	0x490[15:8]	USDHC_DLL_SEL 0 - DLL Slave Mode for 1 - DLL Override Mode	SDMMC_DLL_DLY[6:0] Delay target for USDHC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						
0x490[31:16]	0x490[31:24]	USDHC_OVRD_PAD_SETTING_LOW8[7:0]							
0x4A0[15:0]	0x4A0[15:8]	BT_TOGGLE_MODE	NAND_FCB_SERCH_COUNT 00 - 2 01 - 2 10 - 4 11 - 8		NAND_TG_PREAMBLE_RD_LATENCY (Toggle Mode 33MHz Preamble Delay, Read Latency) '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111' - 15 GPMICLK cycles			NAND_RST_TIME
0x4A0[31:16]	0x4A0[31:24]	NAND_OVERRIDE_PAD_SETTING[7:0]							
0x4B0[15:0]	0x4B0[15:8]	NAND_READ_RETRY_SEQ_ID[3:0] 0000 - don't use read retry(RR) sequence embedded in ROM 0001 - Micron 20nm RR sequence 0010 - Toshiba A19nm RR sequence 0011 - Toshiba 19nm RR sequence 0100 - SanDisk 19nm RR sequence 0101 - SanDisk 1ynmRR sequence 0110 - Hynix 20nm A Die RR sequence 0111 - Hynix 26nm RR sequence 1000 - Hynix 20nm B Die RR sequence 1001 - Hynix 20nm C Die RR sequence Others - Reserved				NAND_ROW_ADDR_BYTES 00 - 3 01 - 2 10 - 4 11 - 5		Reserved	Reserved
0x4B0[31:16]	0x4B0[31:24]	RNG_TRIM[7:0]							

i.MX8M Plus Boot Mode

BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0	Boot Modes
0	0	0	0	Boot From Internal Fuses
0	0	0	1	USB Serial Download
0	***0***	***1***	***0***	***USDHC3 (eMMC boot only, SD3 8-bit) Default***
0	0	1	1	USDHC2 (SD boot only, SD2)
0	1	0	0	NAND 8-bit single device 256 page
0	1	0	1	NAND 8-bit single device 512 page
0	1	1	0	QSPI 3B Read
0	1	1	1	QSPI Hyperflash 3.3V
1	0	0	0	ecSPI Boot
1	0	0	1	Reserved
1	0	1	0	FLEXSPI Serial NAND 2k page
1	0	1	1	FLEXSPI Serial NAND 4k page
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Manufacturing Test



BOOT_MODE1	BOOT_MODE0	Boot Modes
1	***0***	***USDHC3 (eMMC boot only, SD3 8-bit)***
0	1	USB Serial Download

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Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

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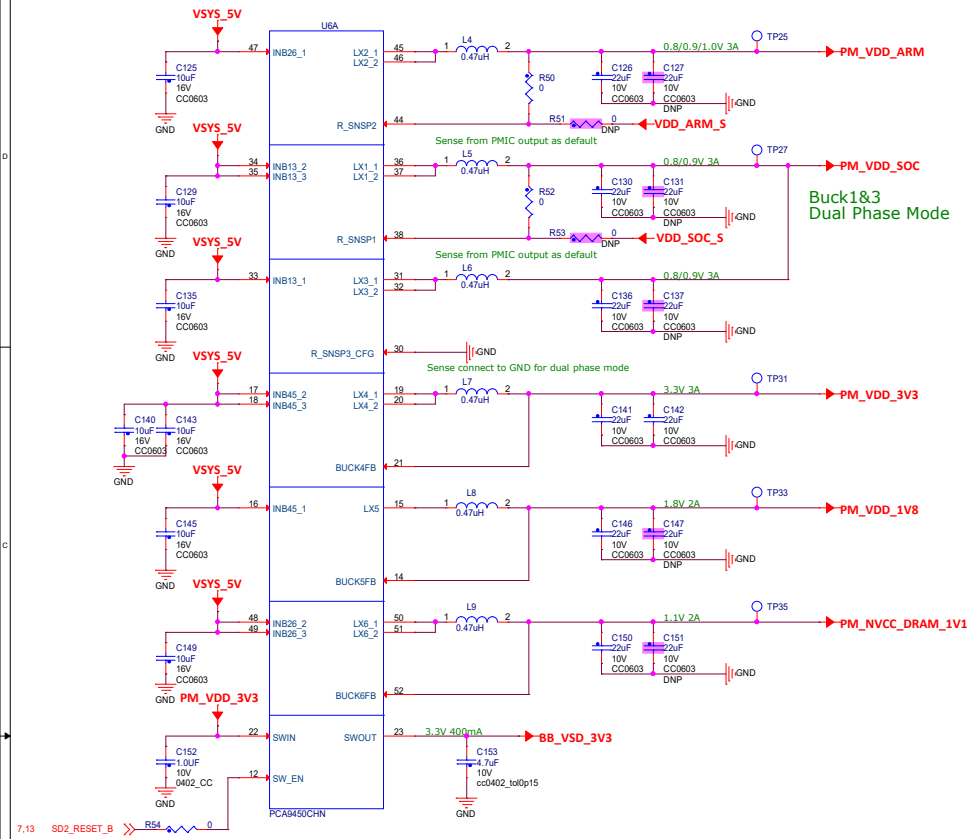
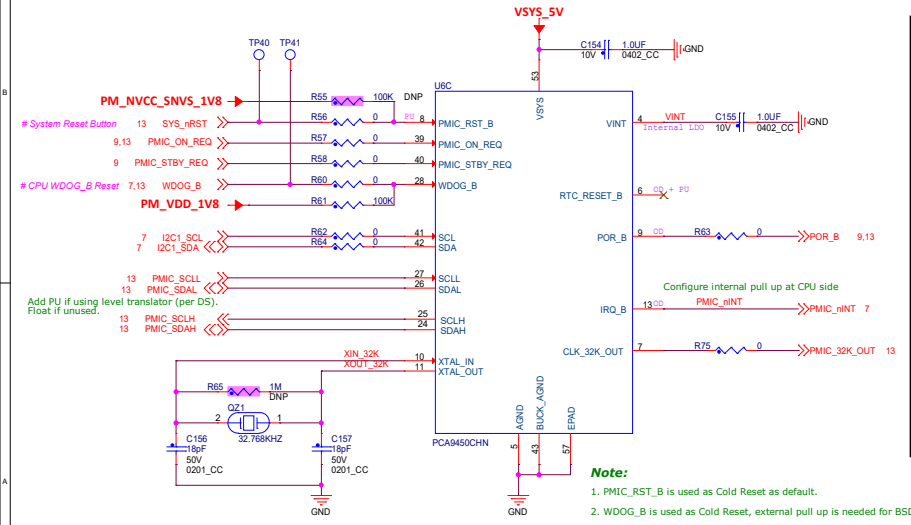
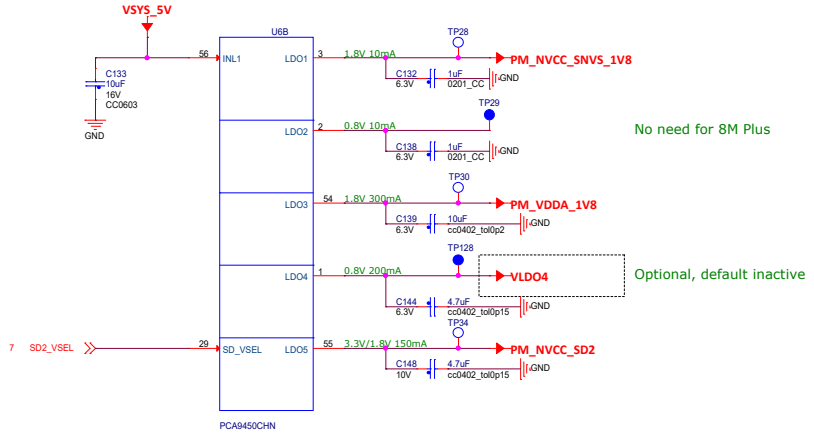
Drawn by: Frank , Elyon	Page Title:	BOOT_CFG
Approved: <Approver>	Size A2	Document Number SCH-46881 PDF:SPF-46881 Rev A1
	Date: Wednesday, November 04, 2020	Sheet 11 of 14

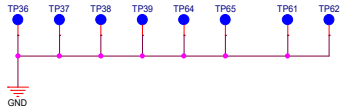
SYS PMIC



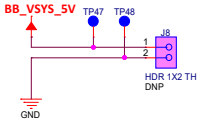




GND Testpoints



Backup PWR Supply



i.MX8M Plus LPDDR4 EVK Power Sequence and Operating Range

SEQ	PWR/Signal	REG	MIN	TYP	MAX	Max Current(mA)
1	NVCC_SNVS_1V8	LDO1	1.71	1.8	1.95	10
2	32K_INTERNAL	RTC_CLK	--	--	--	--
3	VDD_SOC	BUCK1/3	0.805/0.9	0.85/0.95	0.9/1.0	6000
4	VDD_ARM	BUCK2	0.805/0.9/0.95	0.85/0.95/1.0	0.9/1.0/1.05	3000
5	VDDA_1V8	LDO3	1.71	1.8	1.89	300
6	VDD_1V8/NVCC_xxx	BUCK5	1.65	1.8	1.95	2000
7	NVCC_DRAM_1V1	BUCK6	1.045	1.1	1.155	2000
8	VDD_3V3/NVCC_xxx	BUCK4	3	3.3	3.6	3000
8	VSD_3V3	MUXSW	3	3.3	3.6	400
9	NVCC_SD2	LDO5	3.0/1.65	3.3/1.8	3.6/1.95	150
10	POR_B	POR_B	--	--	--	--

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Drawn by: Frank , Elyon	Page Title: PMIC		
Approved: <Approver>	Size C	Document Number SCH-46881 PDF:SPF-46881	Rev A1
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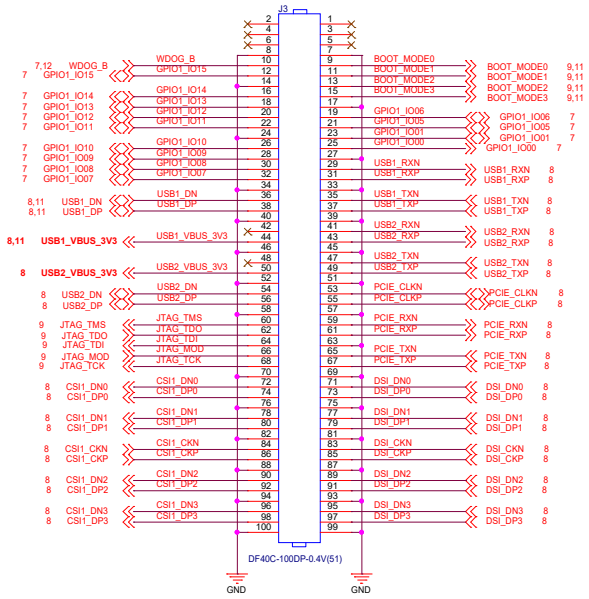
B2B Connector for CPU Board

Header



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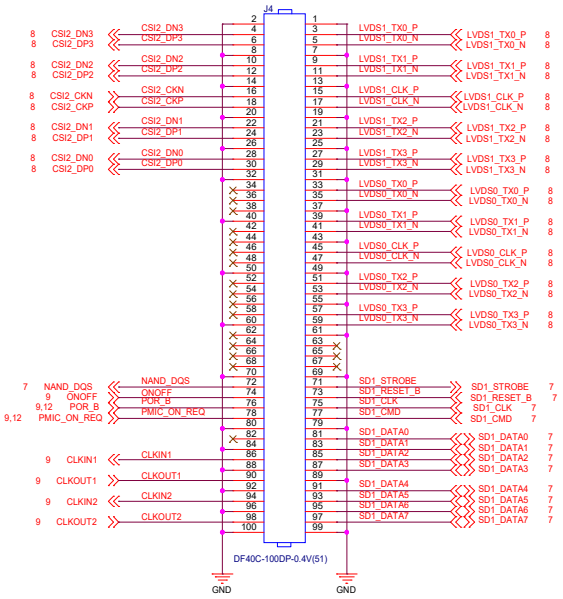

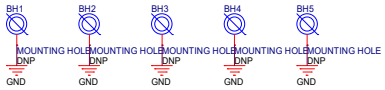

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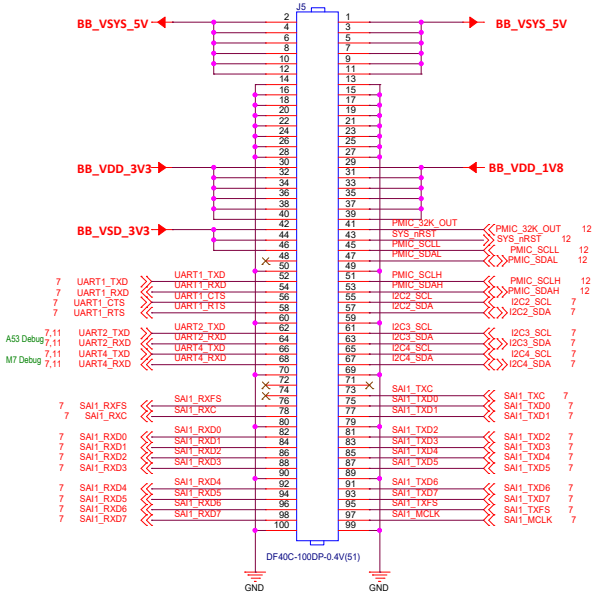

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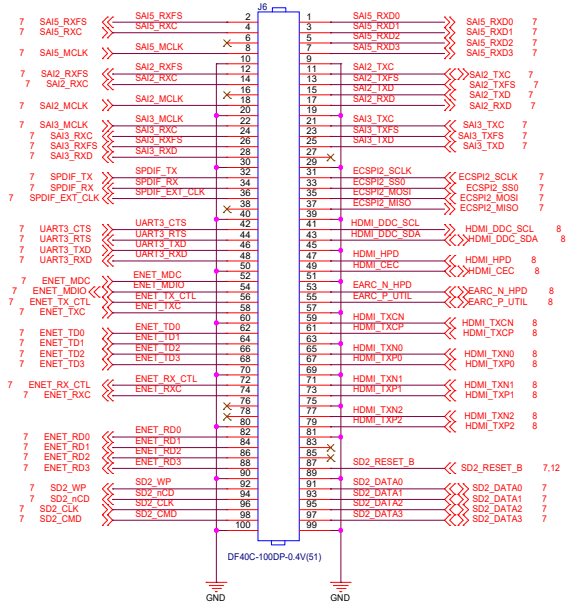

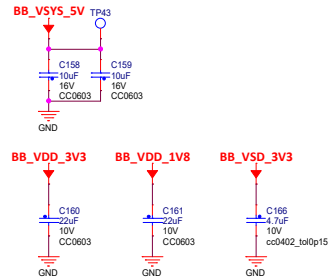

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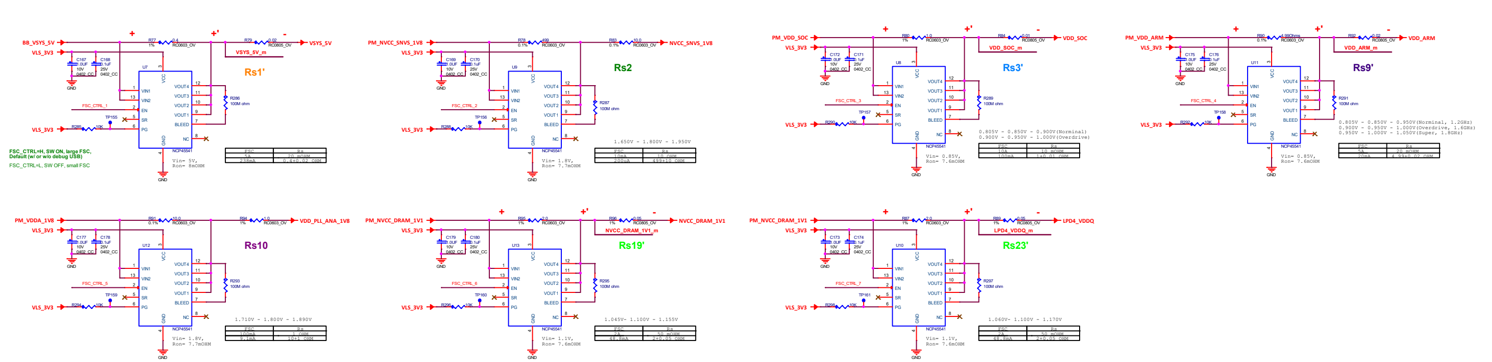
Designer: Frank , Elyon	Drawing Title: X-8MPLUSLPD4-PWR		
Drawn by: Frank , Elyon	Page Title: SOM Interface		
Approved: <Approver>	Size C	Document Number SCH-46881 PDF:SPF-46881	Rev A1
	Date: Wednesday, November 04, 2020	Sheet 13 of 14	

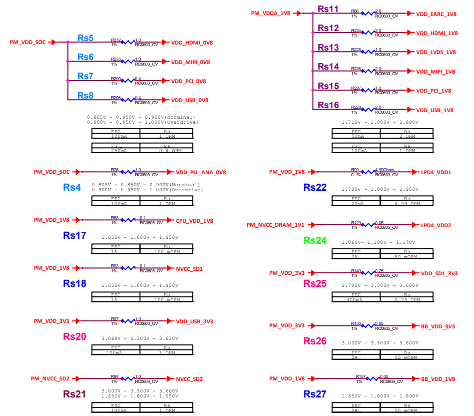
Current Sense Range Select Circuit



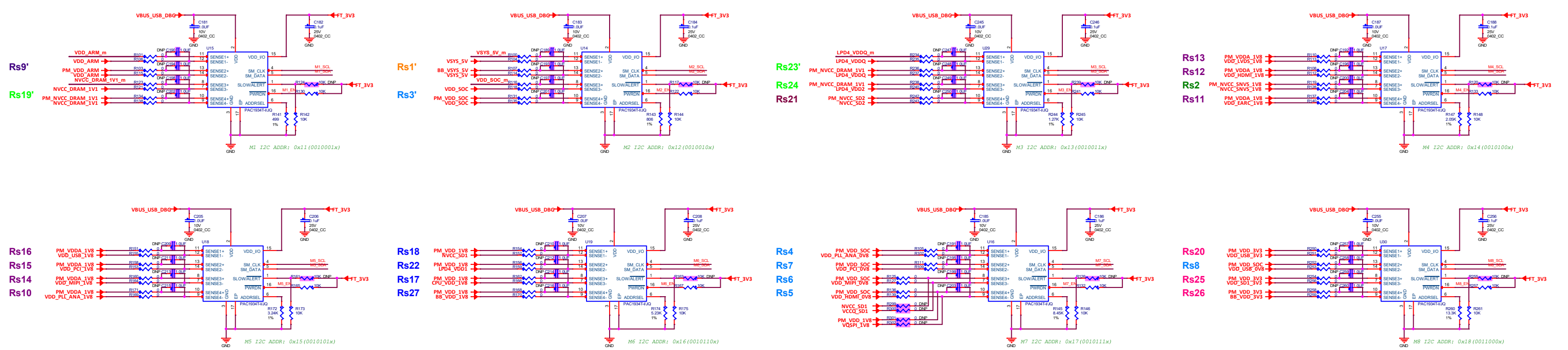
Note:

Be careful of using BLEED(Discharge), should not impact the accuracy of low power measurement!
Rs1', Rs3', Rs9', Rs19', Rs23' have second positive sensing point for high current measurement!

Fixed Current Sense Resistors



Monitors



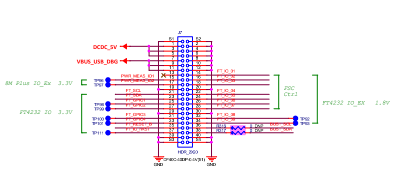
Power Measurement Equations:

I_sense = Vsense / Rs
Vout = Vsense- = V(sense+) - Vsense
Power1 = I_sense x Vout
Power2 = I_sense x Vout_typ(Theoretical Value)
Power3 = I_sense x V(sense+)

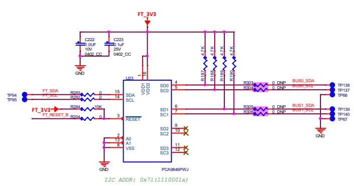
FT4232 I2C Address Table

Part	Type	Device	Address	Voltage
U15	M1	PAC1934T	0x11(0010001x)	3.3V
U14	M2	PAC1934T	0x12(0010010x)	3.3V
U29	M3	PAC1934T	0x13(0010011x)	3.3V
U17	M4	PAC1934T	0x14(0010100x)	3.3V
U18	M5	PAC1934T	0x15(0010101x)	3.3V
U19	M6	PAC1934T	0x16(0010110x)	3.3V
U16	M7	PAC1934T	0x17(0010111x)	3.3V
U30	M8	PAC1934T	0x18(0011000x)	3.3V
U28	EEPROM	AT24C32D	0xA0(1010000x)	3.3V
U23	I2C Switch	PCA9846	0x71(1110001x)	3.3V
U70(BB)	IO_EX	PCA6416A	0x20(0100000x)	3.3V
U80(BB)	EEPROM	AT24C16C(DNP)	0x57(1011111x)	3.3V

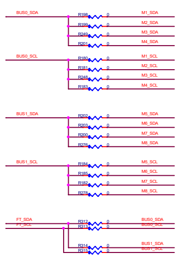
Power Measurement Interface



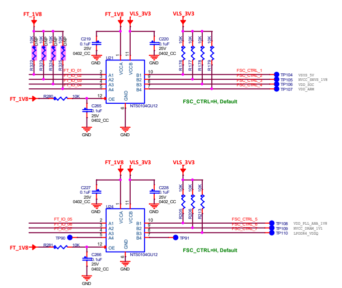
I2C Expansion



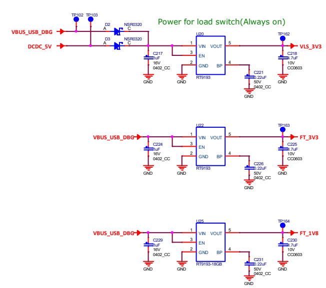
I2C Bus to Monitors



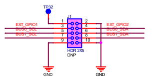
FSC Ctrl Lever Shifter



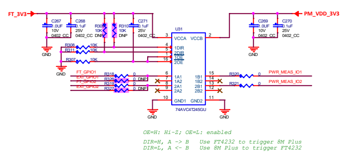
Power



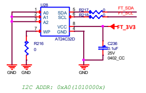
External Interface



Level Shifter



System ID



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ICAP Classification: CP: IUO: A PUBI:

Designer: Frank , Elyon	Drawing Title: X-8MPLUSLPD4-PWR		
Drawn by: Frank , Elyon	Page Title: CURRENT SENSE		
Approved: <Approver>	Size E	Document Number SCH-46881 PDF:SPF-46881	Rev A1
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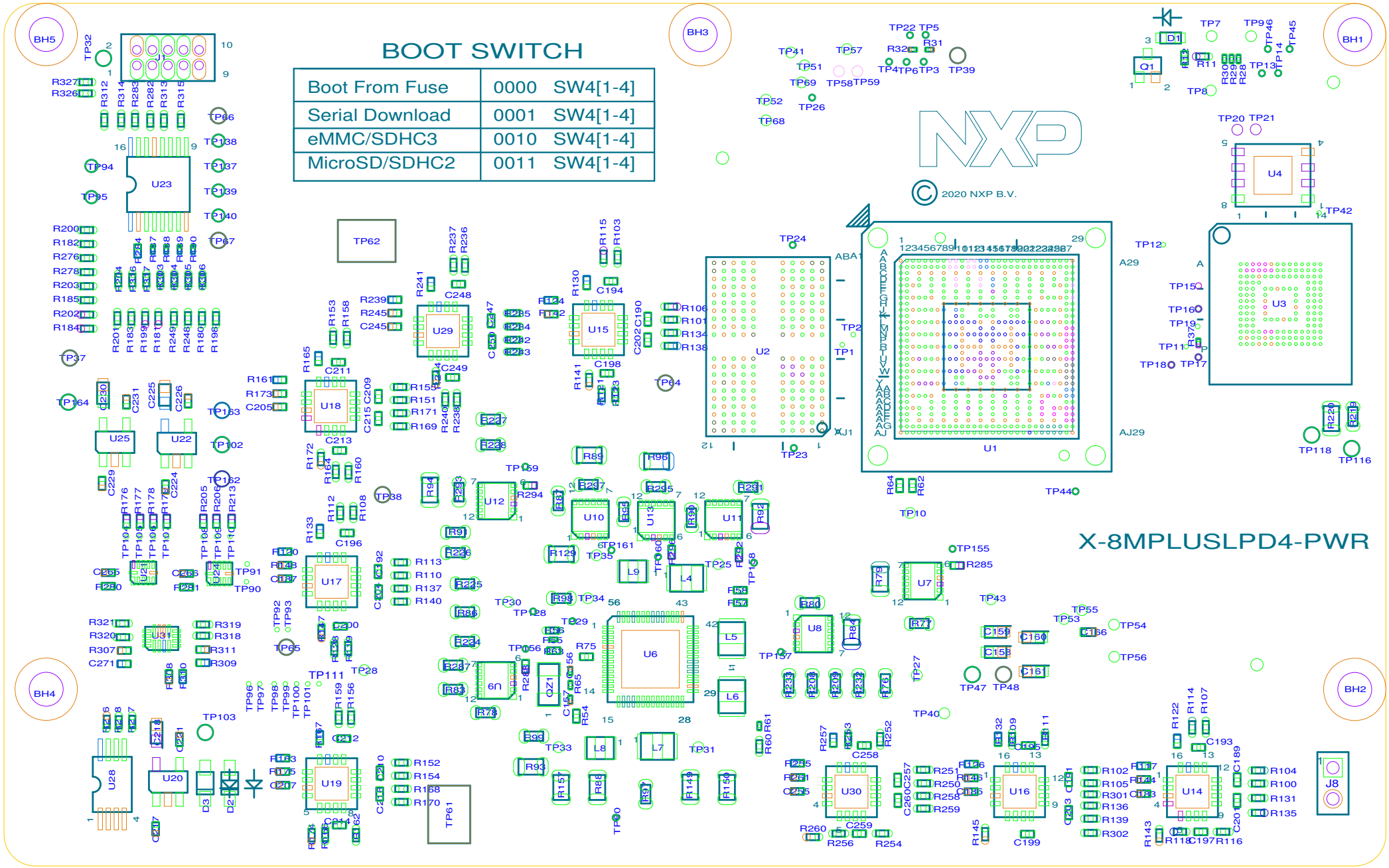
BOOT SWITCH
Boot From Fuse 0000 SW4[1-4]
Serial Download 0001 SW4[1-4]
eMMC/SDHC3 0010 SW4[1-4]
MicroSD/SDHC2 0011 SW4[1-4]
NXP
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X-8MPLUSLPD4-PWR
BH1
BH2
BH3
BH4
BH5
U1
U2
U3
U4
U6
U10
U11
U12
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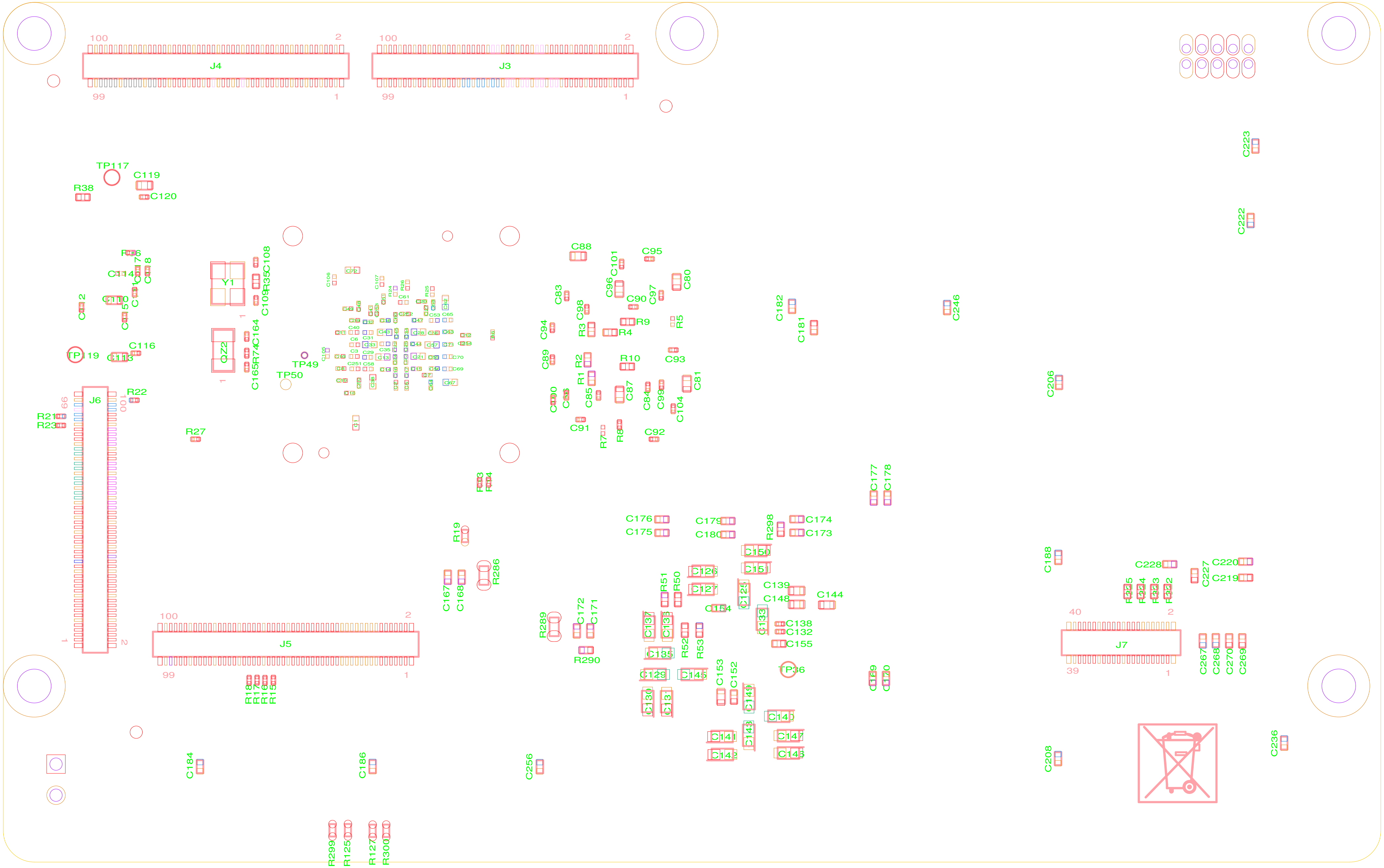
U30
U31
J8



J4
J3
J5
J6
J7
Y1
TP117
TP49
TP50
C119
C120
R38
C116
C88
C95
C101
C80
C96
C97
C90
C83
C98
R9
R5
R3
R4
C94
R10
C93
C89
R2
R1
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C228
C220
C219
C227
C267
C268
C270
C269
C184
C186
C256
C208
C236
R299
R125
R127
R300
R27
R22
R21
R23
C164
C165
C108
R35
C109

8MPLUS-BB

i.MX8M Plus Reference Base Board

Table of Content

1. Interrupted lines coded with the same letter or letter combinations are electrically connected.

2. Device type number is for reference only. The number varies with the manufacturer.

3. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

4. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

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This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

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Revision History

Rev. Code	Date	By	Description
A	2019-11-04	Frank	Initial version
A1	2020-04-28	Frank	1. Change R452 to 1K, to get the correct output level of VPCIe_3V3. 2. Update PMIC PCA9450C I2C address to "0x25", according to latest datasheet. 3. Update "ENET0" naming to "ENET2", to meet with latest fusemap and software definition. 4. Change R51 to 324K, to meet the new requirement for VBUS detect threshold (>=3.7V) from USB Type-C Functional Test Specification since 2019 5. Change several Boot Mode configurations to "Reserved". 6. Update the block diagram, change "OTG" to "Dual Role". 7. Change U48 from PCA9617ADP to PCA9509ADP for better compatibility of HDMI monitors, R185 needs be populated.
A2	2020-10-10	Frank	1. Change D2, D4 from NSR0320 to BAT54HT1 to reduce the reverse leakage current for Type-C Quadramax Load Test. 2. Change R186 from 10K to 100K, D9, D32 from NSR0320 to BAT54HT1 to reduce the leakage current on CEC line. HDMI CTS requires <=1.8uA on CEC line. 3. Change R333, R334 from 4.7K to 1.5K, for better drive strength of I2C signals. 4. Change U30 from PCMF1USB3S to PCMF1HDMI2S, which is dedicated for HDMI application. **5. DNP R432 and R433, remove the signal connections for USB1_DNU(USB1_ID), USB2_DNU(USB2_ID), these pins CAN'T be used, according to latest I.MX8M Plus datasheet.**
A3	2021-01-11	Frank	1. Change "X-8MPLUS-BB" to "8MPLUS-BB" for mass production. 2. Remove the text "NXP CONFIDENTIAL AND PROPRIETARY" on each page. 3. Change R452 to 0ohm, to improve load transient response for high power consumption M.2 devices. 4. Change U56 from NTB0104 to NTS0104, which can support bigger capacitive load.
B	2021-03-12	Frank	1. Remove Q3, add U81 and related components to reduce the output delay of PCIE external reference clock. 2. Remove R432, R433, as USB1_DNU(USB1_ID), USB2_DNU(USB2_ID) are not used. 3. Add R142, provide the connection for M.2 PCIE_DIS2, DNP as default. 4. Add R163, provide the option to control PWDN of each camera module separately, DNP as default.
B1	2021-05-13	Elyon	1. Change C120 and C121 to 0.22uF (150-79999) to meet the spec requirement for PCIe Gen3 TX AC coupling capacitance (175~265nF).

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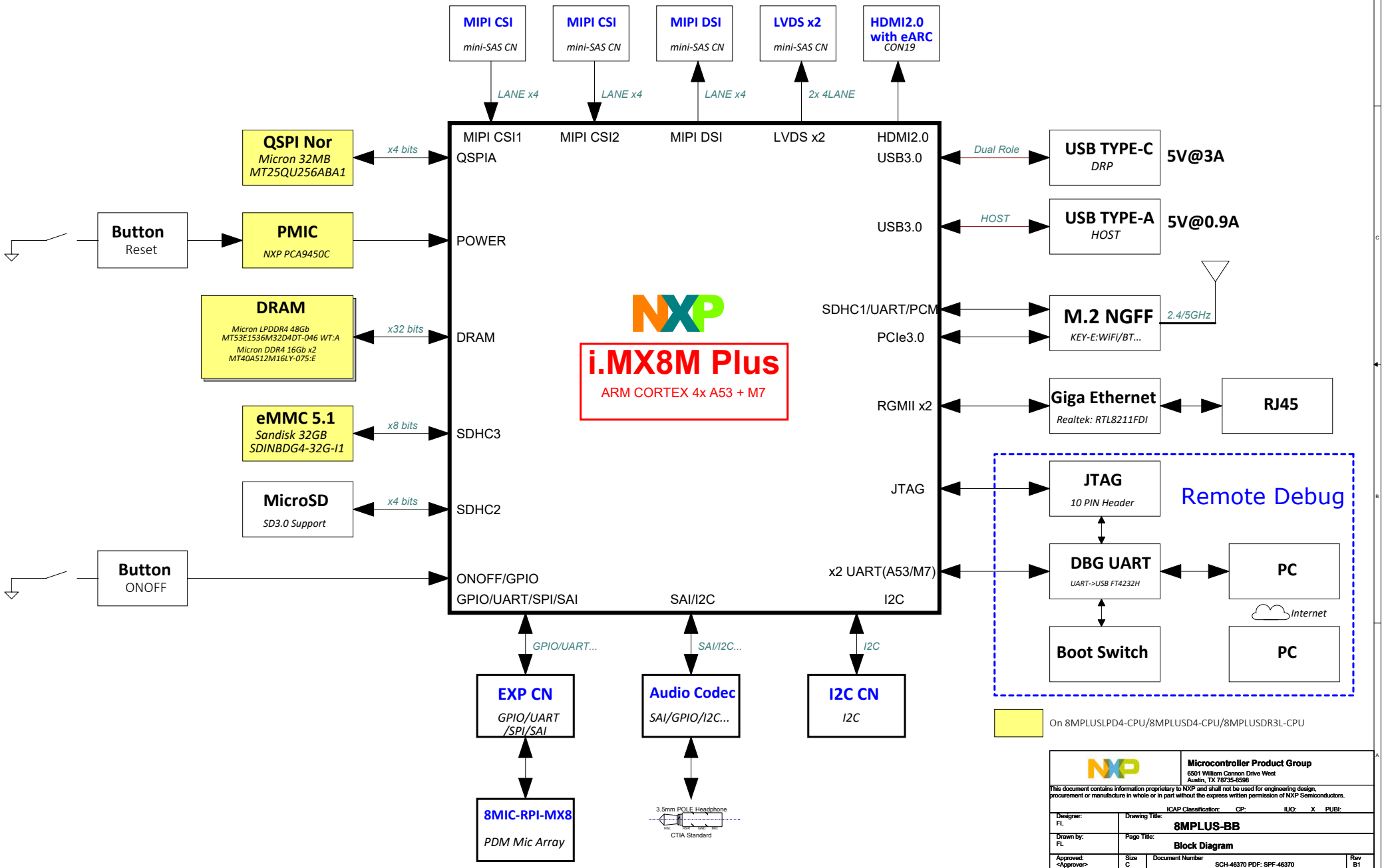
IMX8MPLUSLPD4 - EVK

Block Diagram

8MPLUSLPD4 - EVK	46371
8MPLUSLPD4-CPU	46368
8MPLUS-BB	46370

8MPLUSDR4 - EVK	
8MPLUSDDR4 - CPU	47568
8MPLUS - BB	46370



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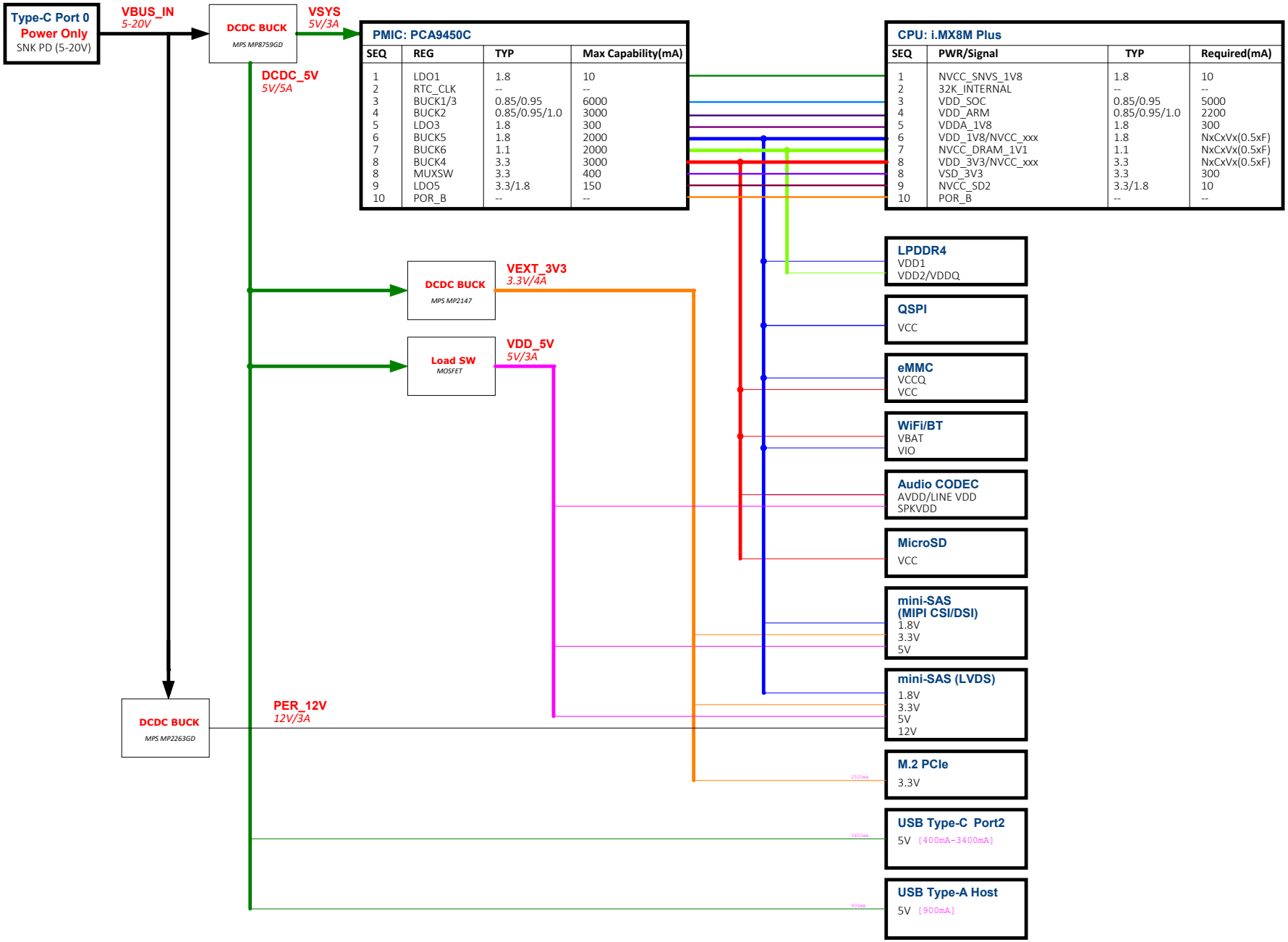
IMX8MPLUSLPD4-EVK PWR TREE



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Approved: <Approver>	Size: Custom	Document Number: SCH-46370 PDF: SPF-46370 Rev: B1
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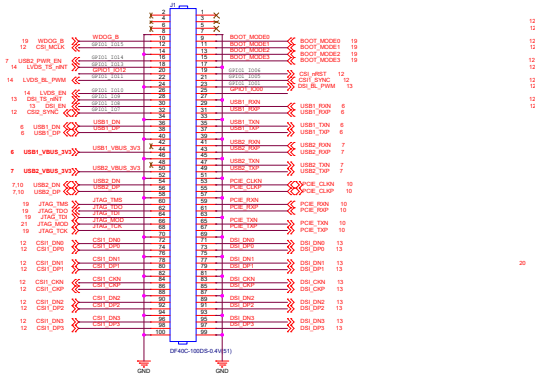
IO Connector

Receptacle



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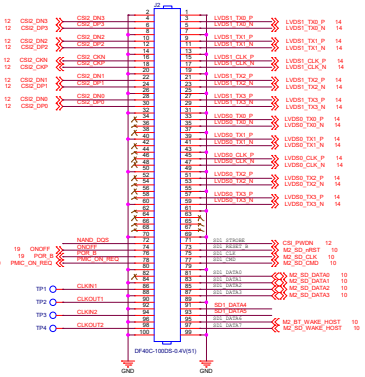

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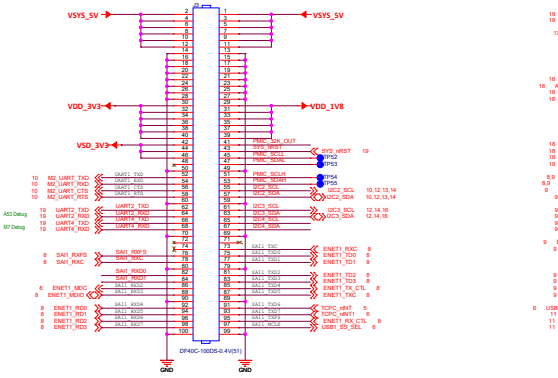

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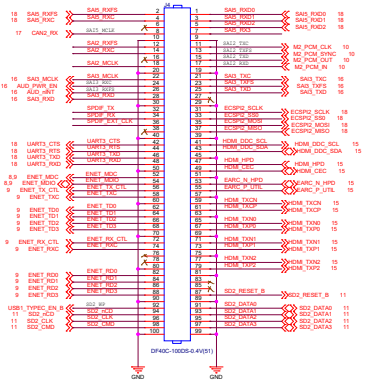
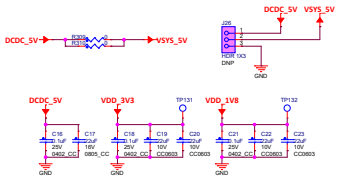




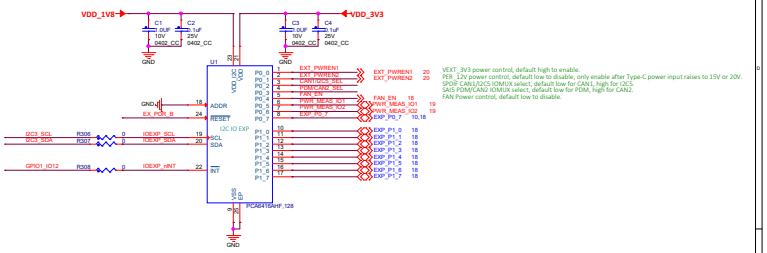
SAI Usage

Port	Usage
SAI1	RGMII ENET1, IO
SAI2	M.2 BT
SAI3	Audio Codec
SPDIF	CAN1/I2C5
SAI5	PDM MIC/CAN2

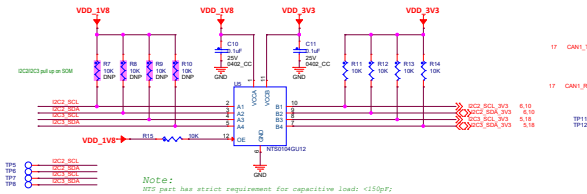
I2C Address Table

Port	Type	Device	Address	Voltage
I2C1	PMIC	PCA9450C	0x25(0100101x)	1.8V
I2C2	LVDS0	IT6263	0x4C(1001100x)	1.8V
	DSI-HDMI	ADV7535	0x3D(0111101x)	1.8V
	M.2 Clock	9FGV0241A	0x68(1101000x)	3.3V
	Type-C1	PTN5110	0x50(1010000x)	3.3V
	Type-C1	NX20P3483UK	0x72(1110010x)	3.3V
	CSI1			1.8V
	M.2			1.8V
I2C3	LVDS1	IT6263	0x4C(1001100x)	1.8V
	Type-C0	PTN5110	0x50(1010000x)	3.3V
	CODEC	WM8960	0x1A(0011010x)	1.8V
	IO_EX	PCA6416A	0x20(0100000x)	1.8V
	CSI2			1.8V
	EX_CN			3.3V
I2C5	I2C_CN			3.3V

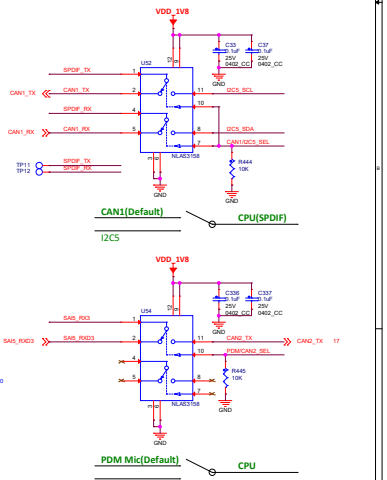
IO Expansion



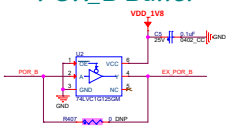
I2C Level shifter



CAN Selection



POR_B Buffer



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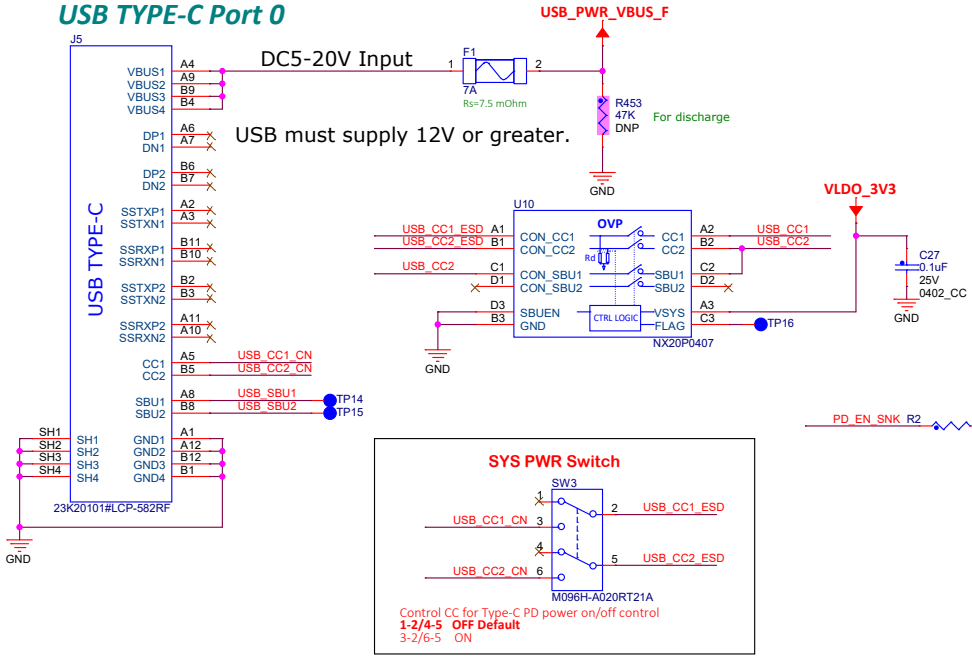
USB Type-C Power Supply

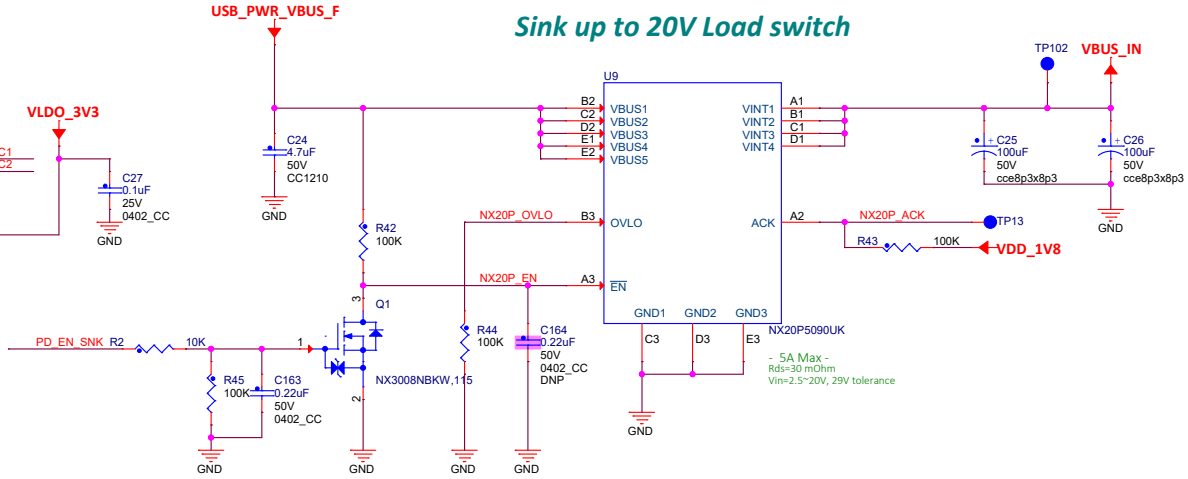
This is the power supply, must be ON for system running!

USB TYPE-C Port 0

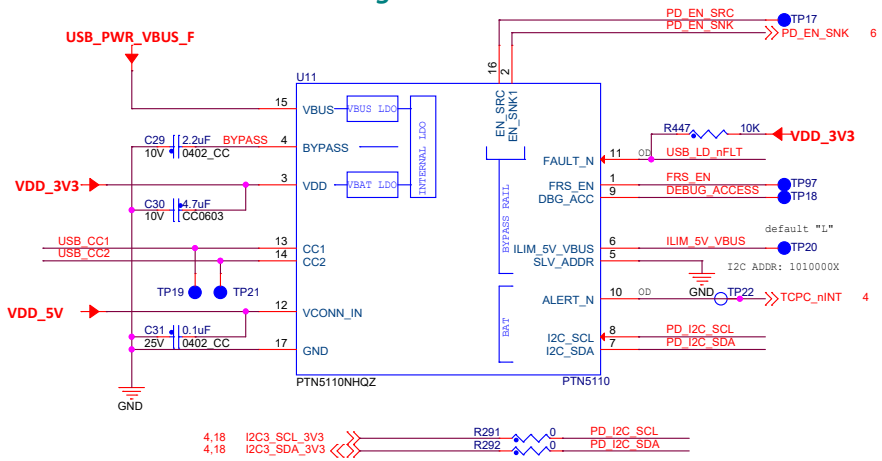


SYS PWR Switch

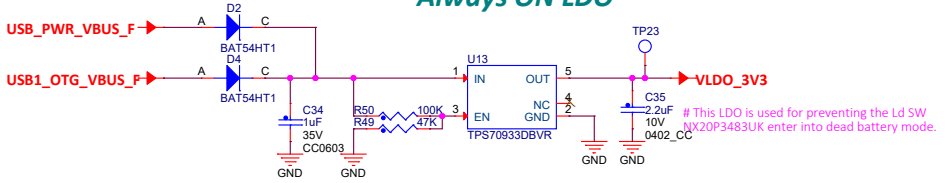
Sink up to 20V Load switch



CC Logic Detection



Always ON LDO



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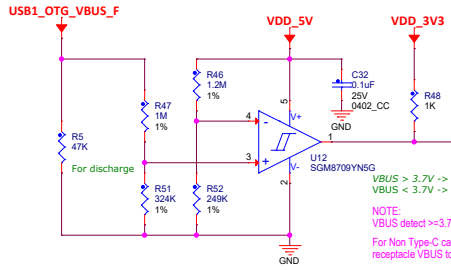
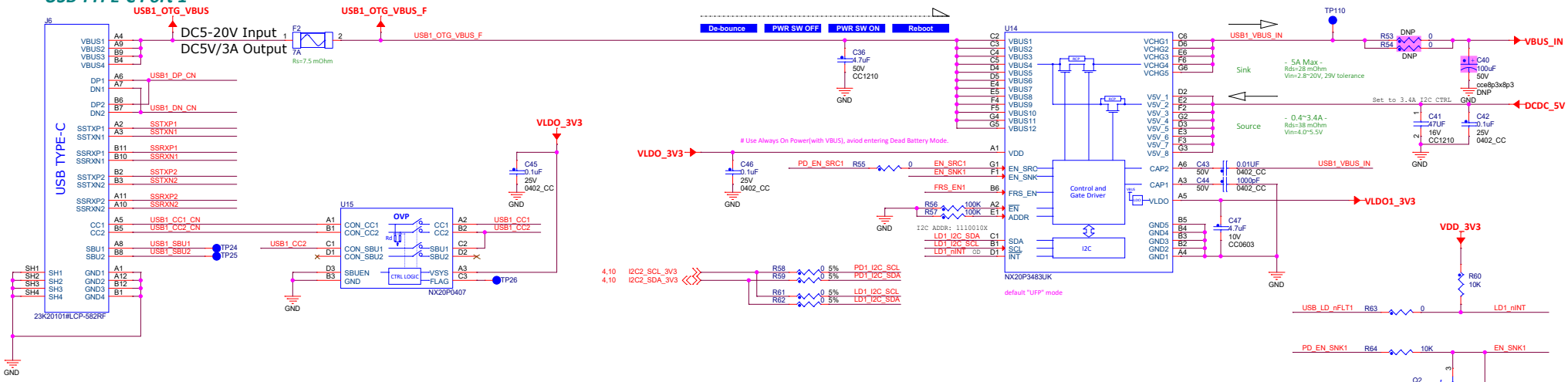
USB3.0 Type-C

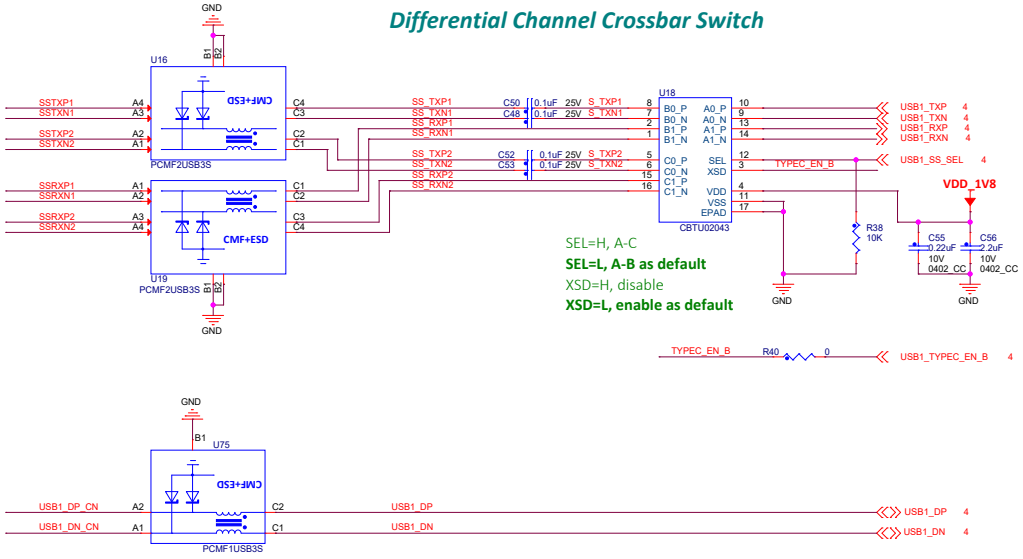


This is NOT the power supply!

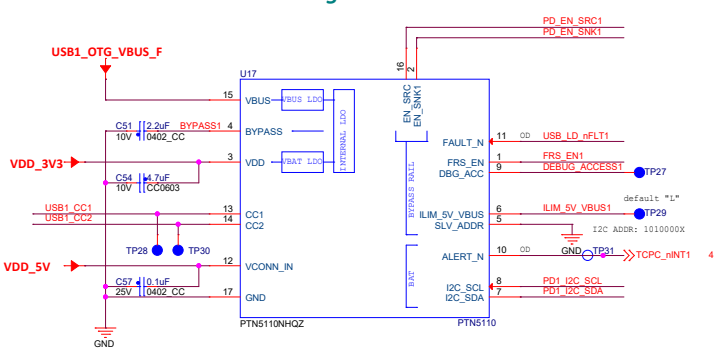
USB TYPE-C Port 1



Differential Channel Crossbar Switch



CC Logic Detection



TP45 USB1_DNU(USB1_ID)

Caution:
I.MX8M Plus USBx_ID pins are changed to USBx_DNU, CAN'T be used.
Recommend to use common GPIO if USB Identification is needed.

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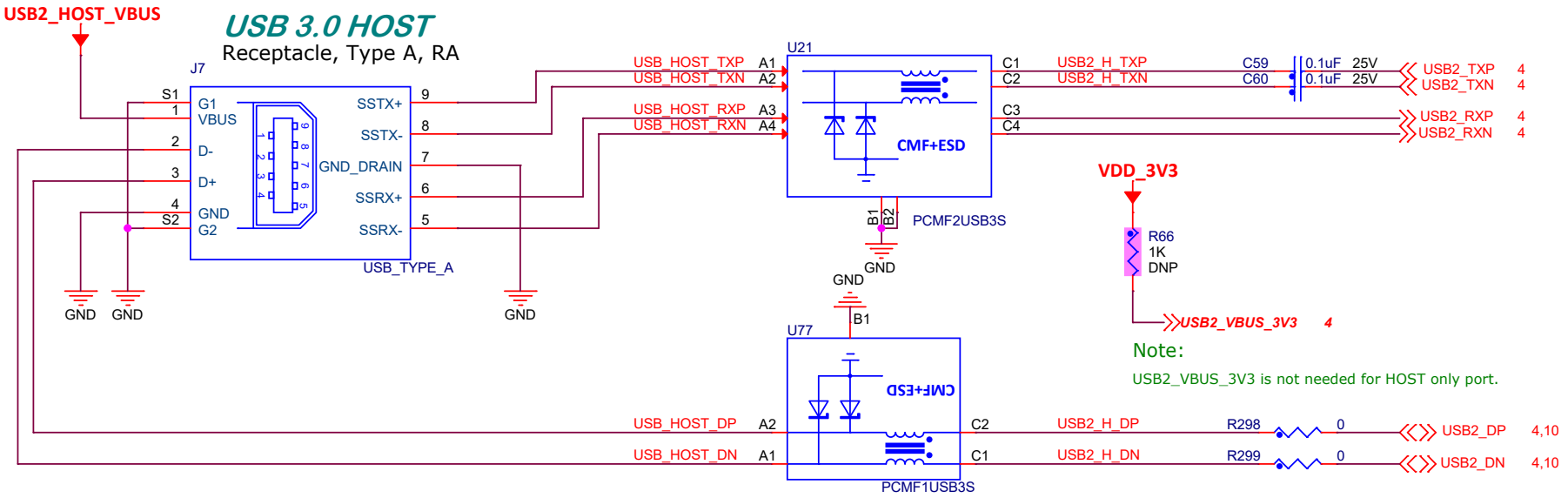
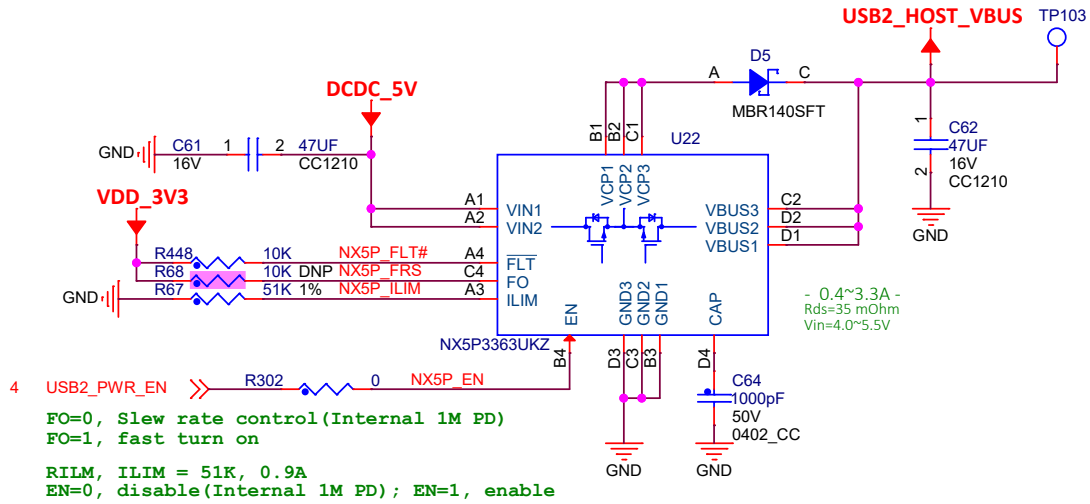
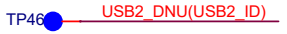
USB3.0 HOST



5V Source Load Switch





Caution:

I.MX8M Plus USBx_ID pins are changed to USBx_DNU, CAN'T be used. Recommend to use common GPIO if USB Identification is needed.

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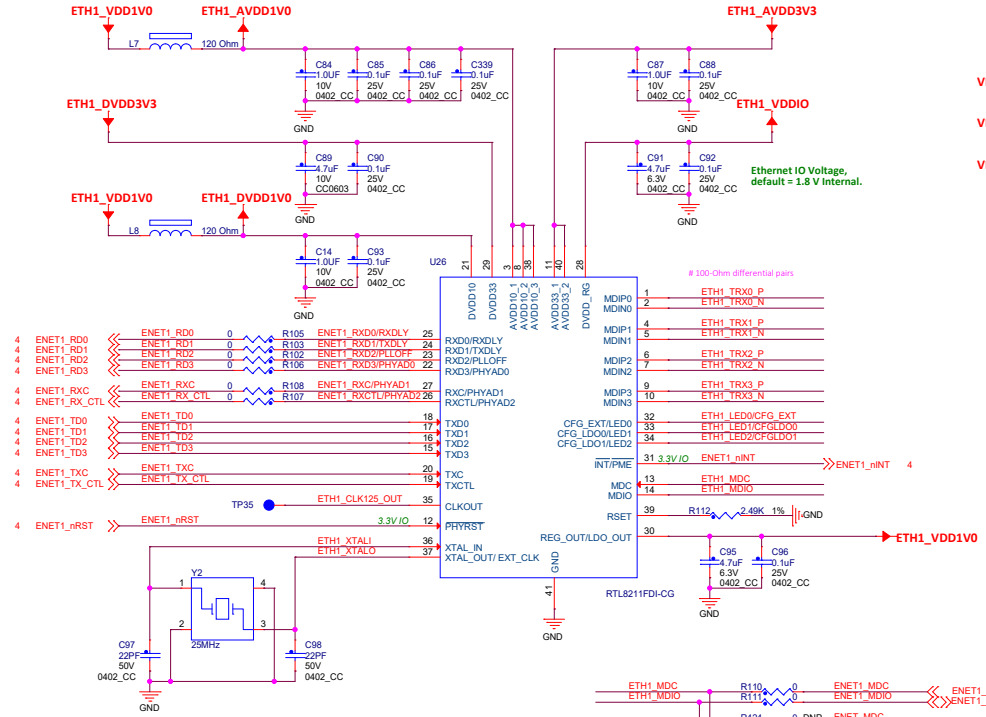
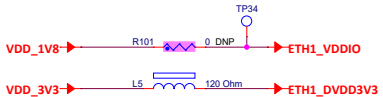
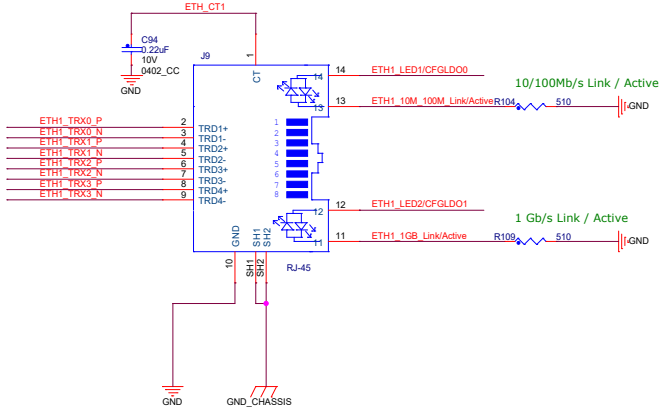
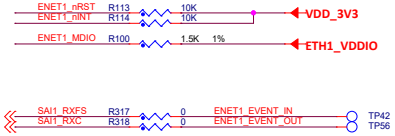
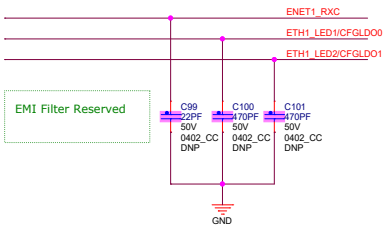
RGMII 10/100/1000Mbps Ethernet



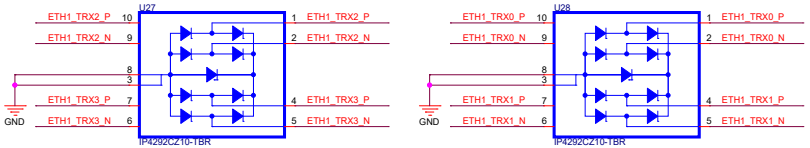




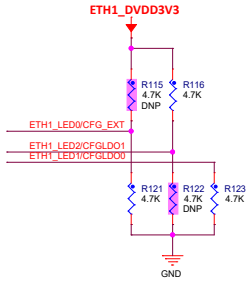




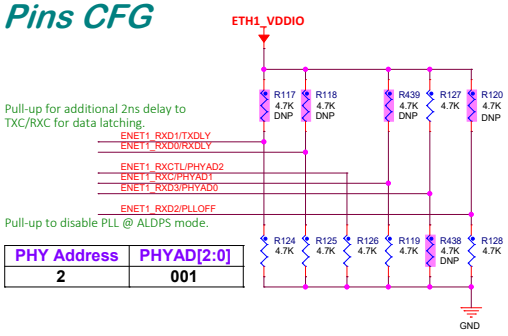
ESD protection



Power-on Strapping Pins CFG



RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1	00
External 2.5V	1	01
External 1.8V	1	10
External 1.5V	1	11
Internal 2.5V	0	01
Internal 1.8V(Default)	0	10
Internal 1.5V	0	11



PHY Address	PHYAD[2:0]
2	001

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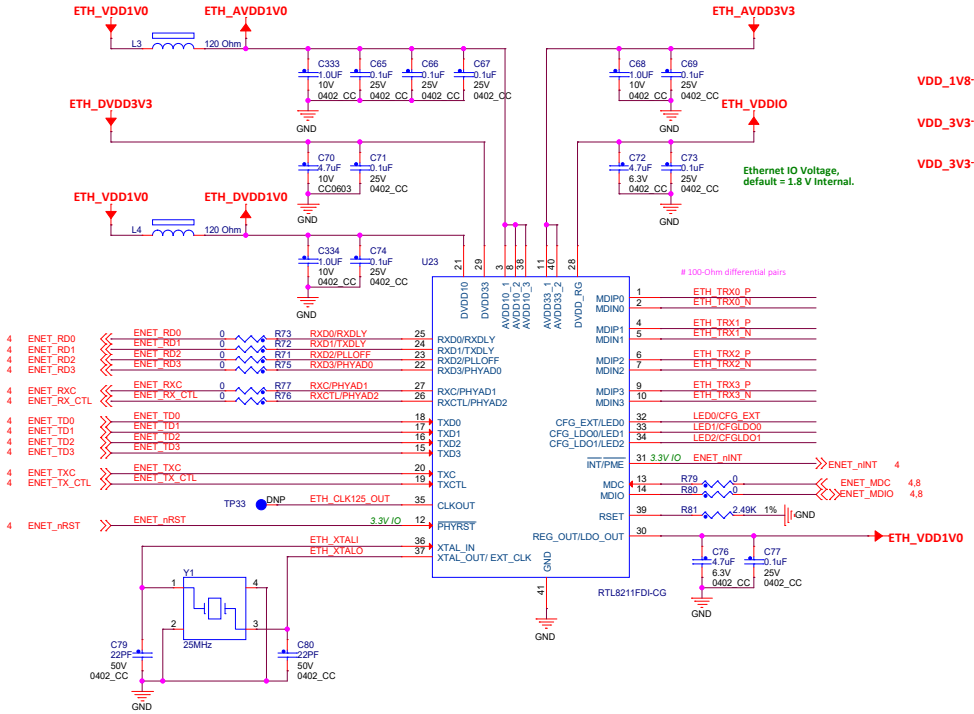
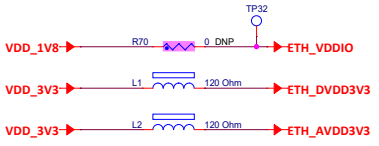
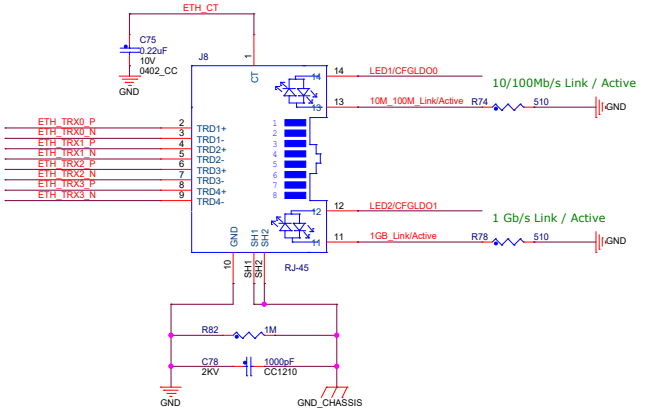
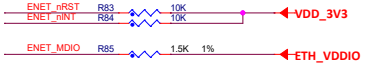
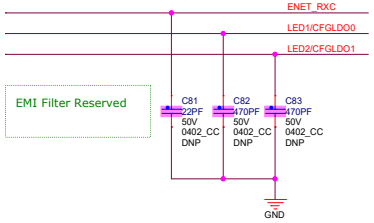
RGMII 10/100/1000Mbps Ethernet TSN supported



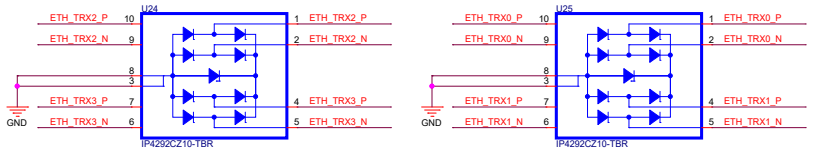




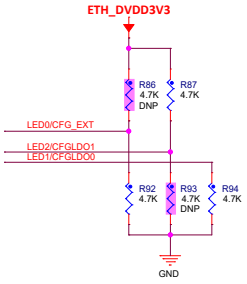




ESD protection



Power-on Strapping Pins CFG



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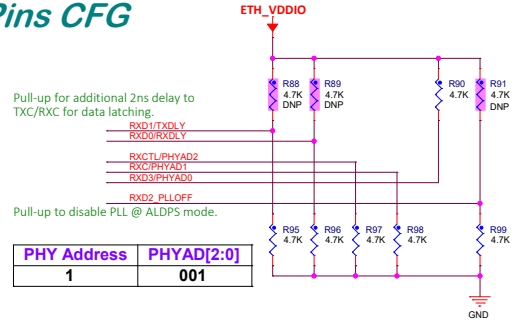
External 2.5V	1	01
External 1.8V	1	10
External 1.5V	1	11
Internal 2.5V	0	01
Internal 1.8V(Default)	0	10
Internal 1.5V	0	11



PHY Address	PHYAD[2:0]
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ICAP Classification: CP: IUO: X PUBI:

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PCIe3.0 M.2/NGFF

PCIe MEMS OSC

U29 9FGV0241AKLF

Standoff for M.2

BH1 SMTSO-M25 — BH9 SMTSO-M25 — BH10 SMTSO-M25

2230 3030 — 2242 3042 — 2260

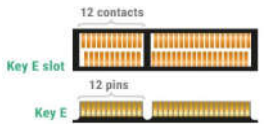
M.2 PWR

M.2 (NGFF) CN

J10 M.2 / NGFF KEY E

CON_MINI CARD_RA

MDT420E01001



NOTE:
Use external clock as default.
When using internal clockpopulate R135, R136, remove R131, R132, R137, R138.

NOTE:
This component share PCB package
When use 9FGV0241 PIN5: GND;PIN7:1.8V
When use PI6CFGL201BZDIEX PIN5:1.8V;PIN7:3.3V

1. For L1 Sub-states: Uses a bidirectional open-drain clock request (CLKREQ#) signal for entry and exit this state.

2. Clock delay should be smaller than 400ns, according to M.2 spec, so CLKREQ# should be connected to OE pins instead of PD pin.

VDIO For some modules

PMIC_32K_OUT as default PU as default

Enable internal PU of CPU

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Approved: <Approver>	Size A3	Document Number SCH-46370 PDF: SPF-46370	Rev B1
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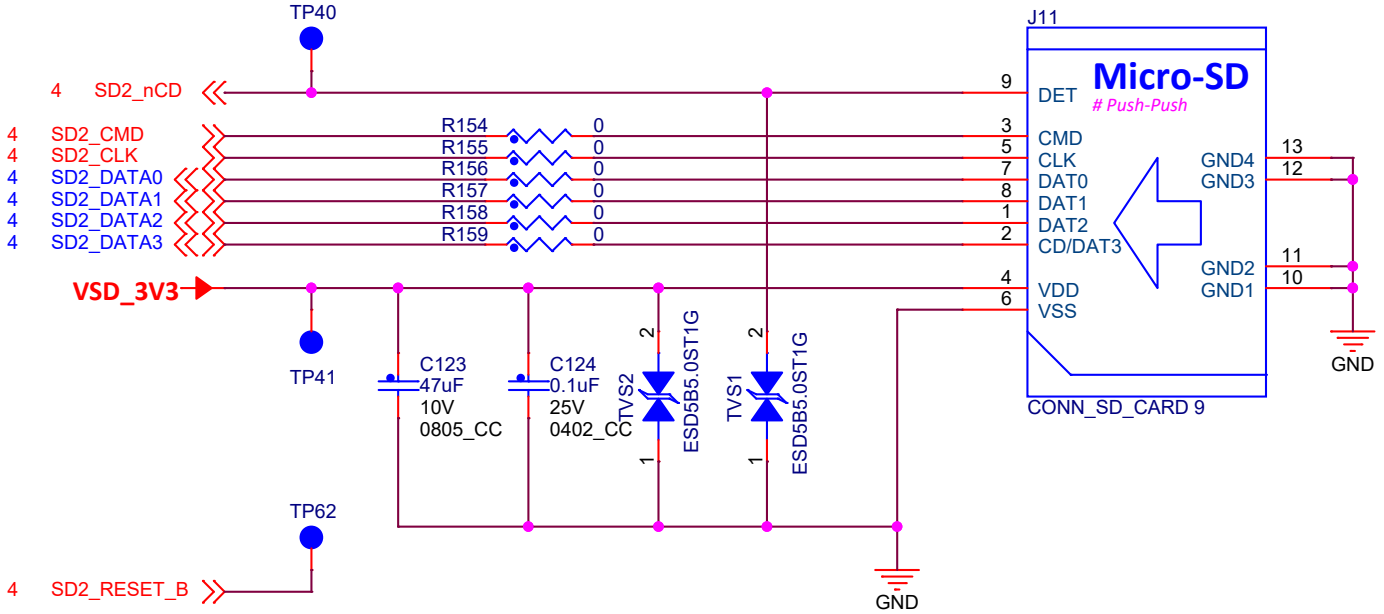
MicroSD 3.0



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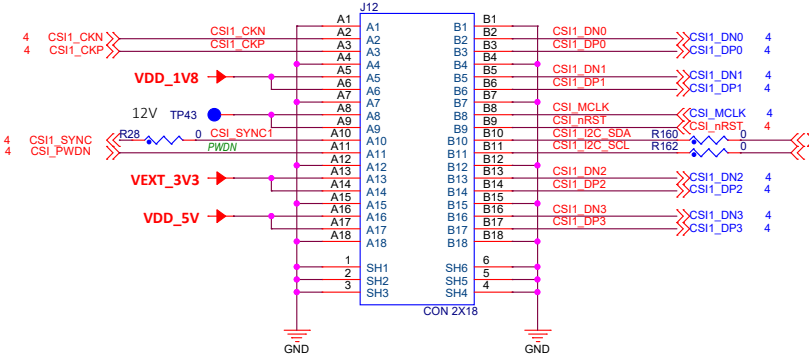
Drawn by: FL	Page Title: **MicroSD**
Approved: <Approver>	Size A / Document Number SCH-46370 PDF: SPF-46370 / Rev B1
	Date: Thursday, May 13, 2021 / Sheet 11 of 21

Camera CSI Interface

Camera 1#



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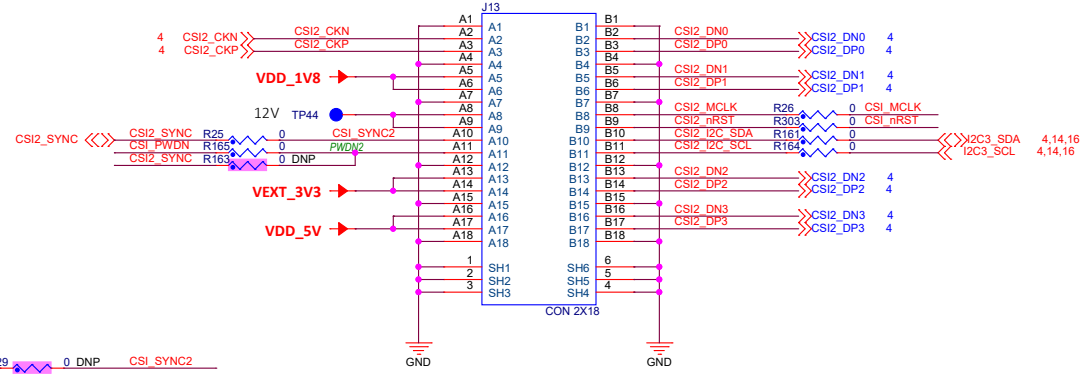
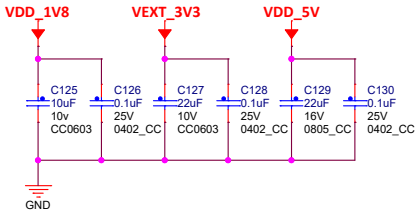
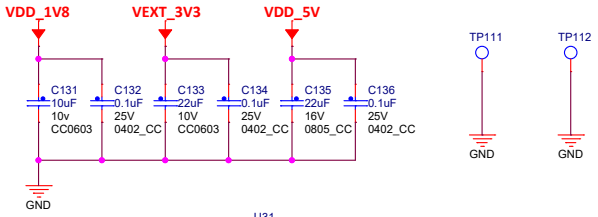


CSI_SYNC1 R29 0 DNP CSI_SYNC2

SYNC signal comes from one sensor to another.





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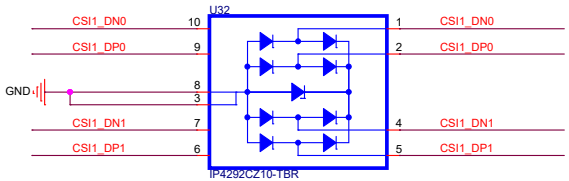

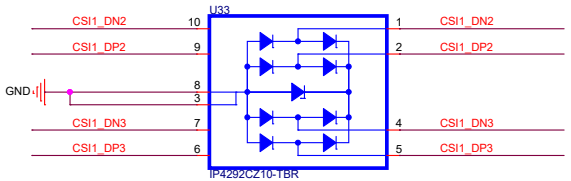

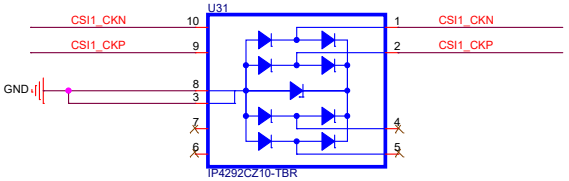

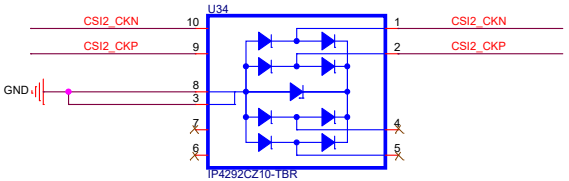

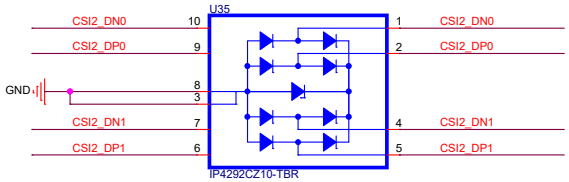

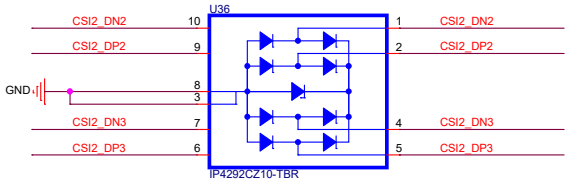

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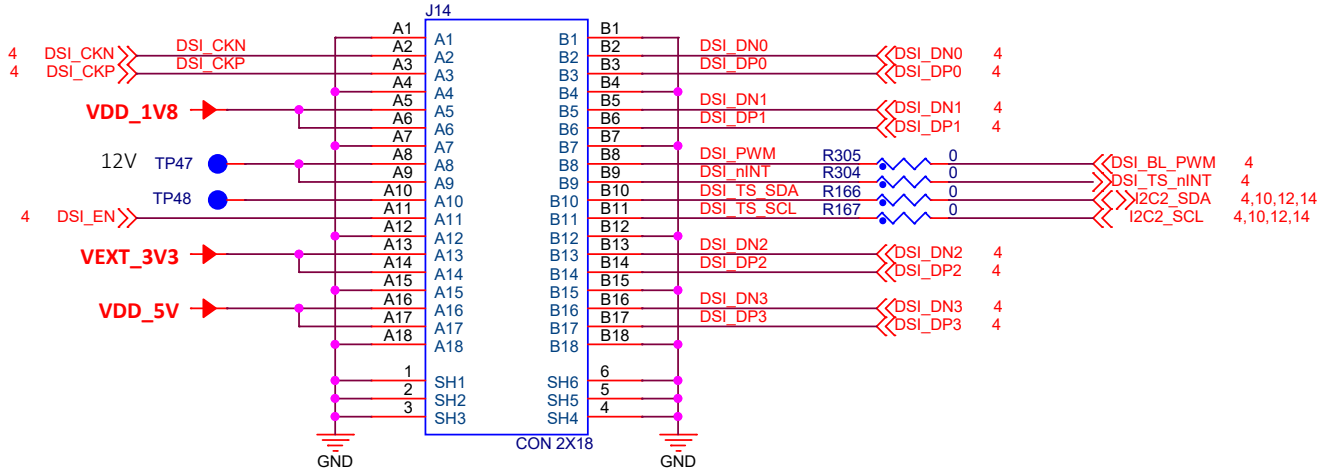
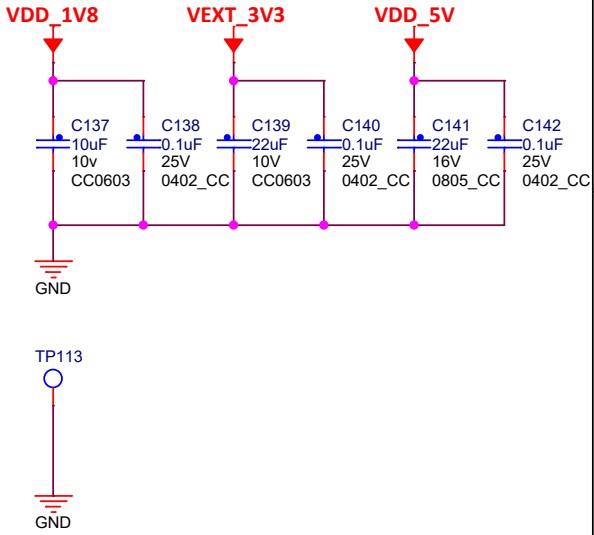
DSI Display





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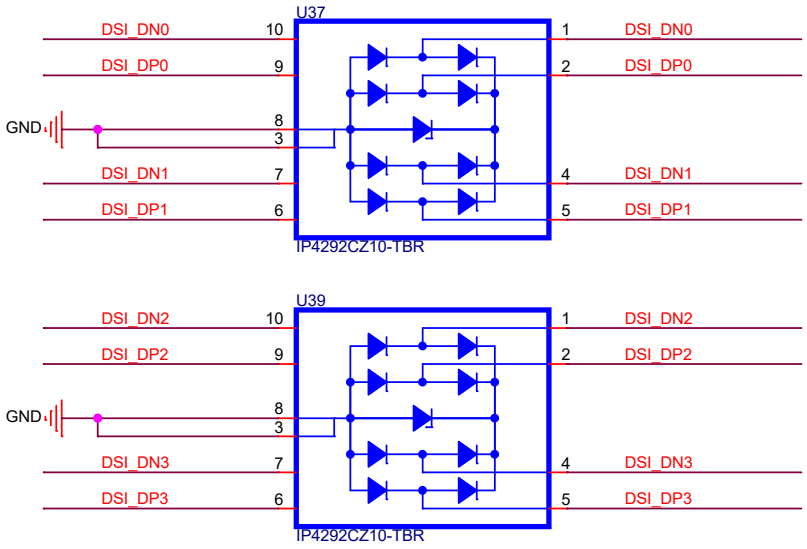

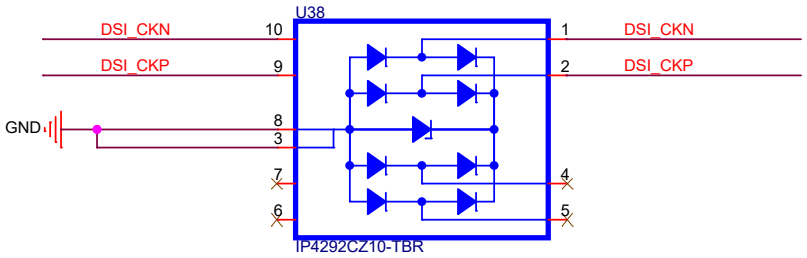

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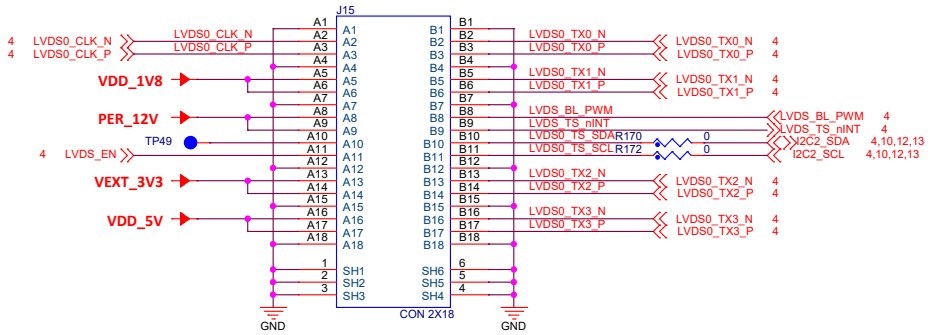
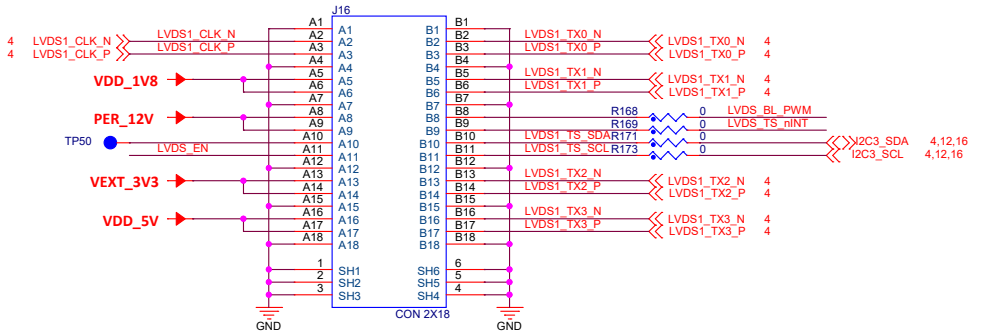
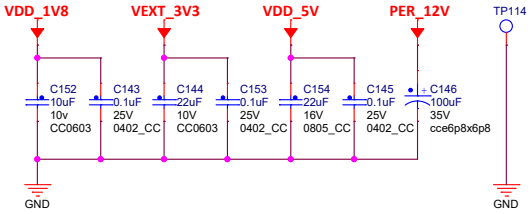
LVDS Display

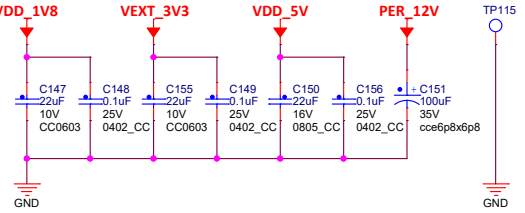
LVDS0 Display



LVDS1 Display







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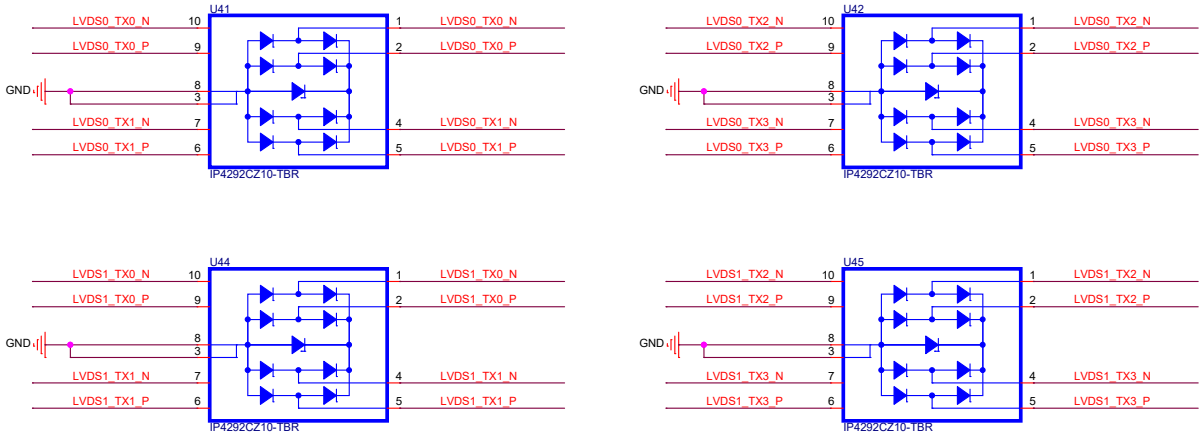

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Drawn by: FL	Page Title: **LVDS DISPLAY**		
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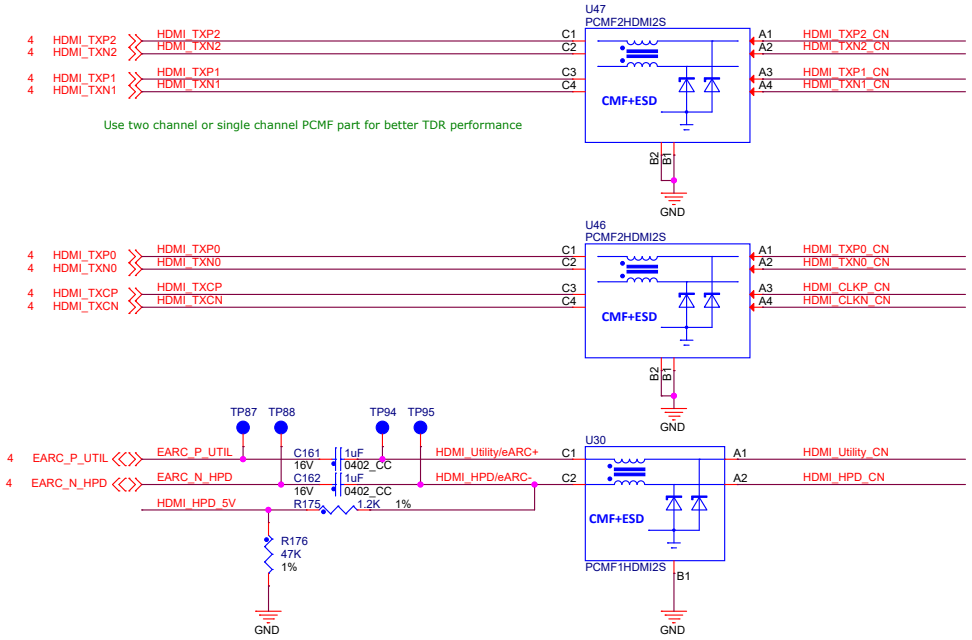
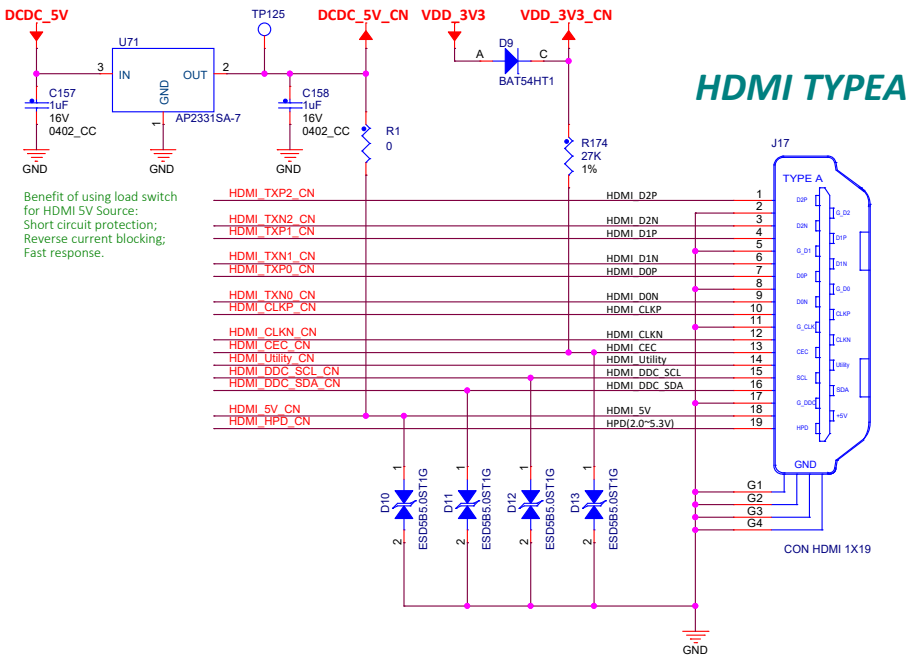
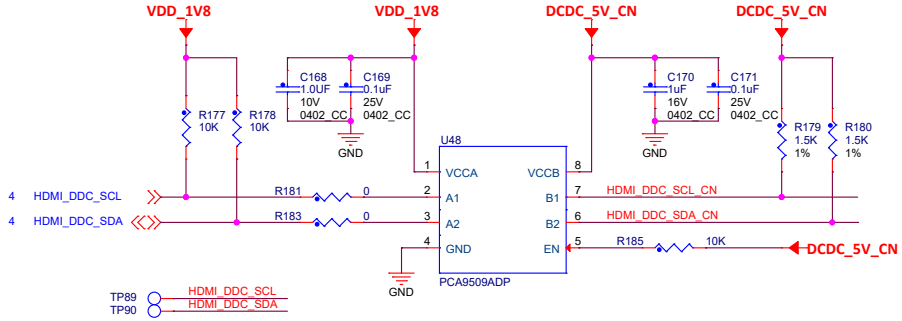
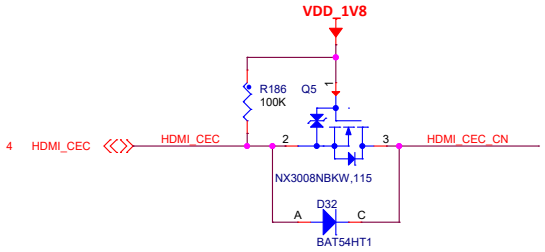
HDMI2.0 Display with eARC RX

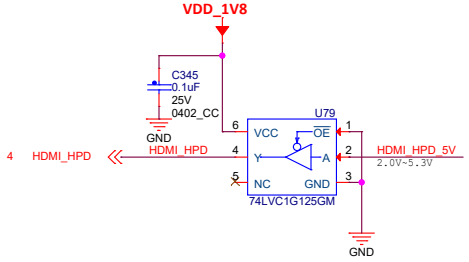




Level shifter







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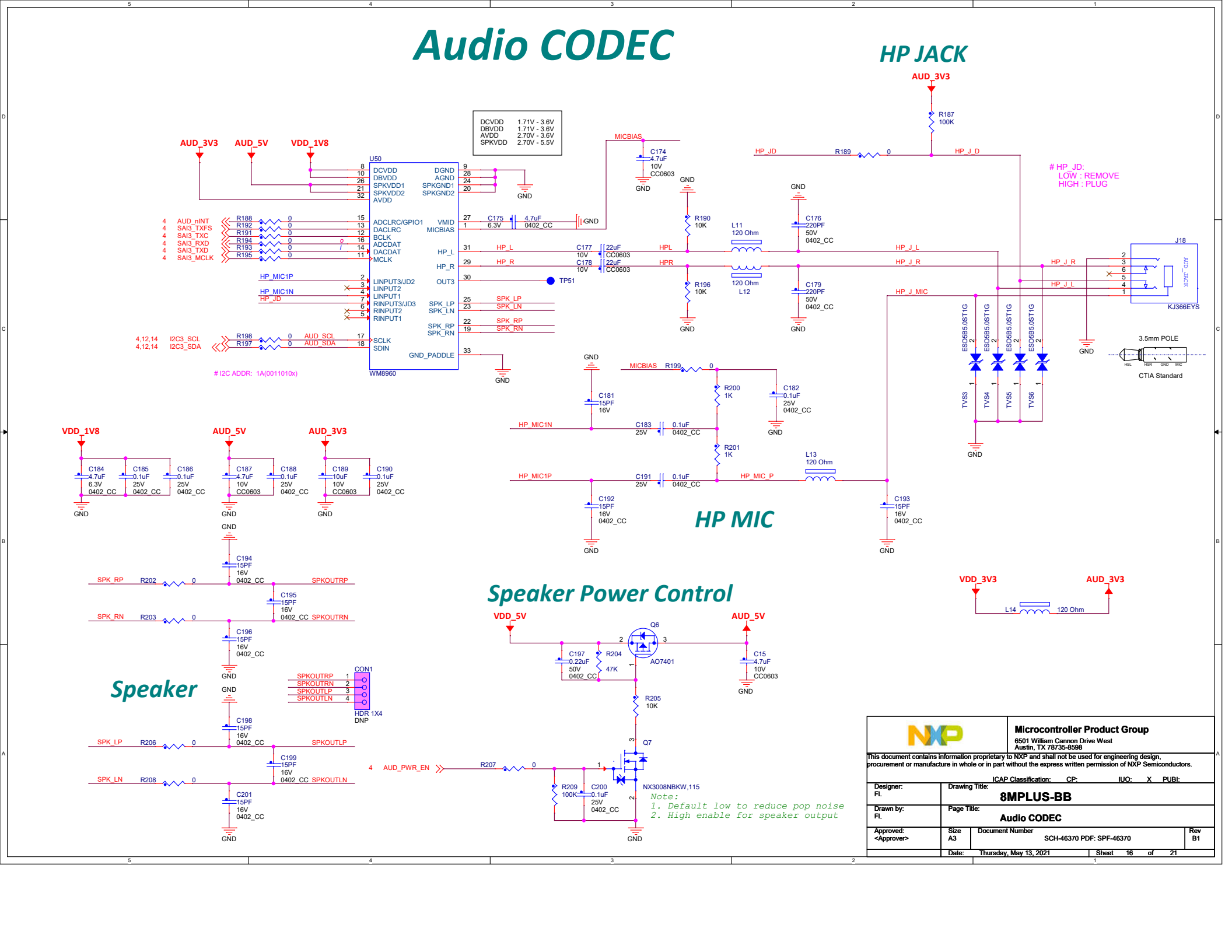
Audio CODEC



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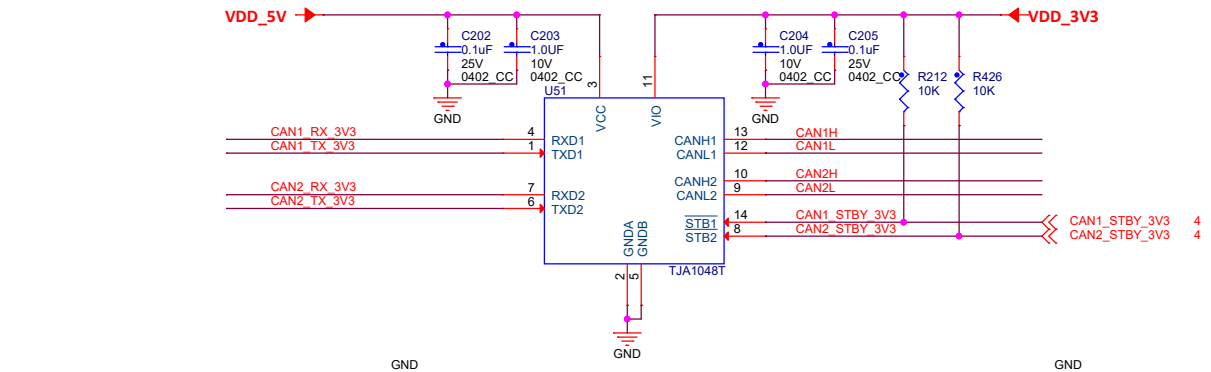
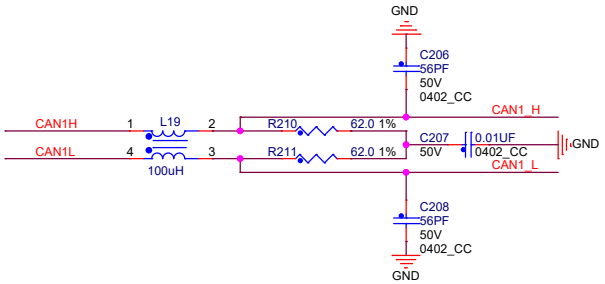
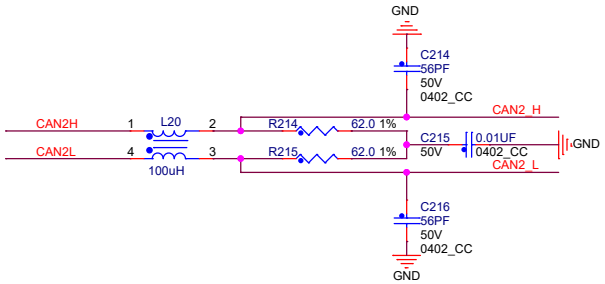
CAN Bus

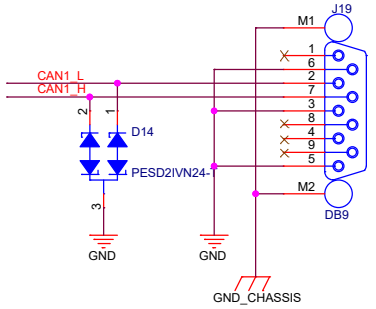
Dual CAN FD



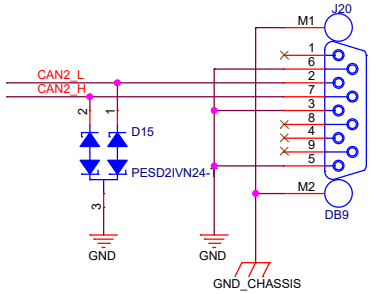




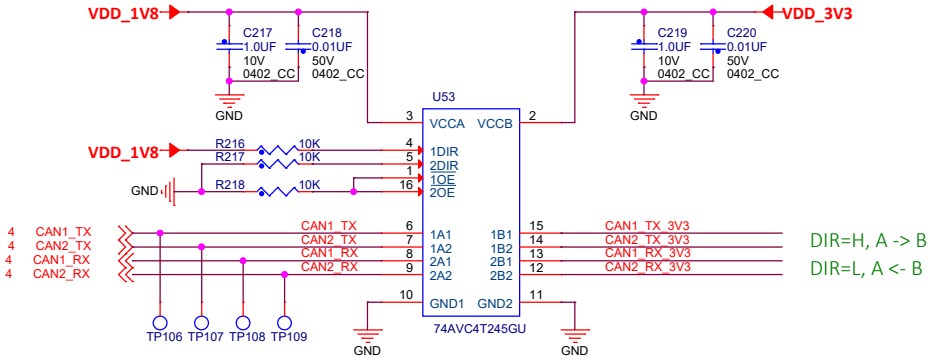
DB9 Female



DB9 Female



Level shifter



DIR=H, A -> B
DIR=L, A <- B

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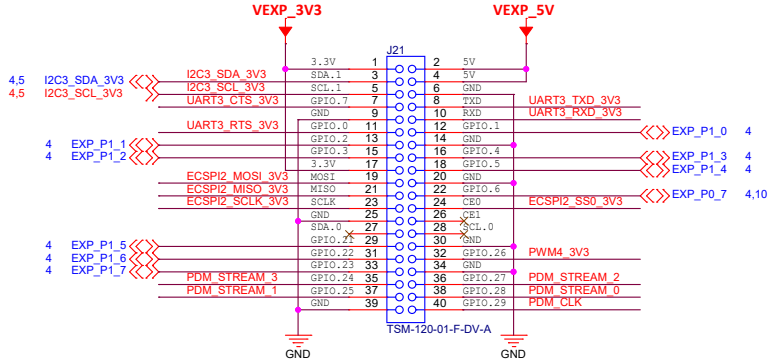
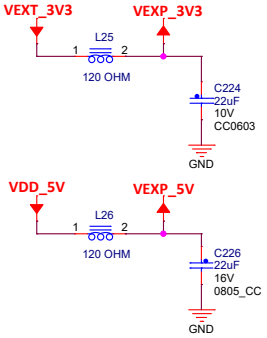
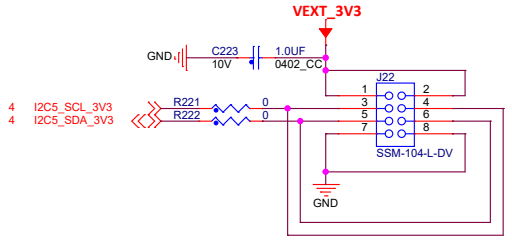
Expansion Connectors

EXP CN

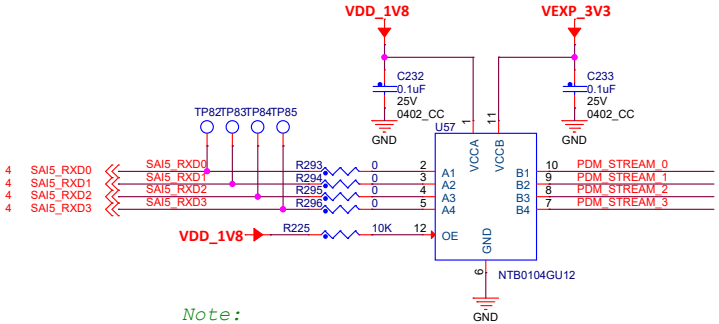




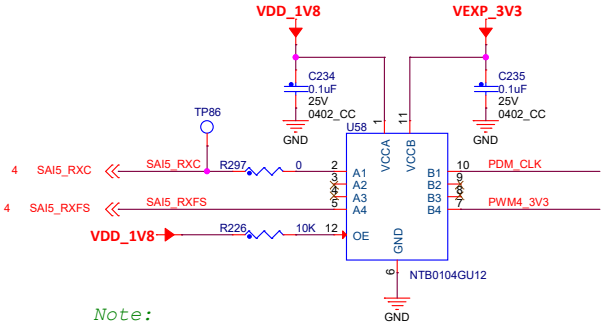
I2C CN



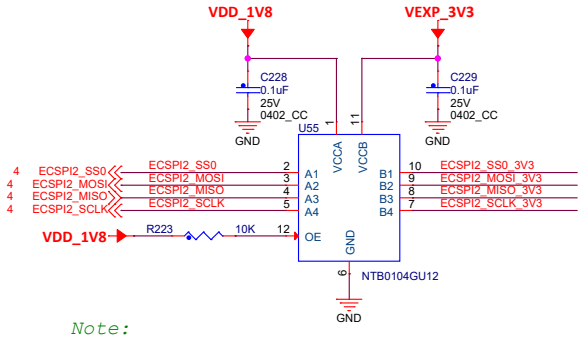
Level Shifter



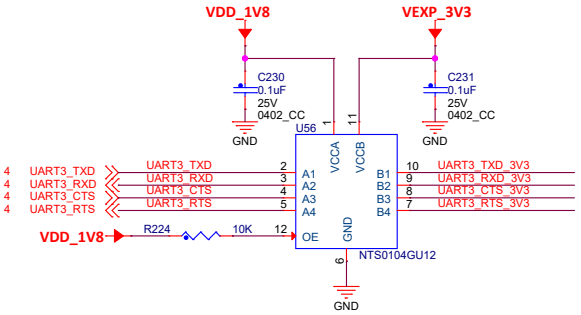
Note:
NTB part has strict requirement for capacitive load: <70pF



Note:
NTB part has strict requirement for capacitive load: <70pF

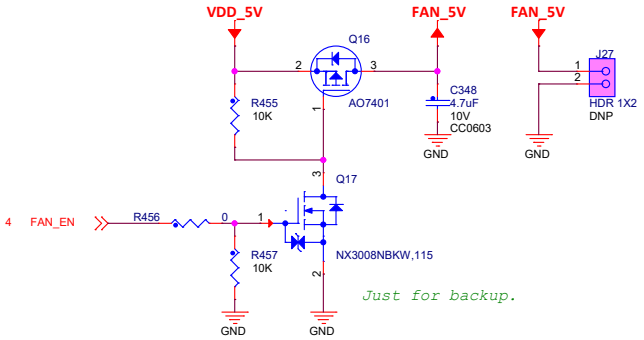


Note:
NTB part has strict requirement for capacitive load: <70pF



Note:
NTS part has strict requirement for capacitive load: <150pF;
Use NTS part instead of NTB part for UART, will have
better capacitive load support w/o performance degradation.

FAN Power Control



Just for backup.

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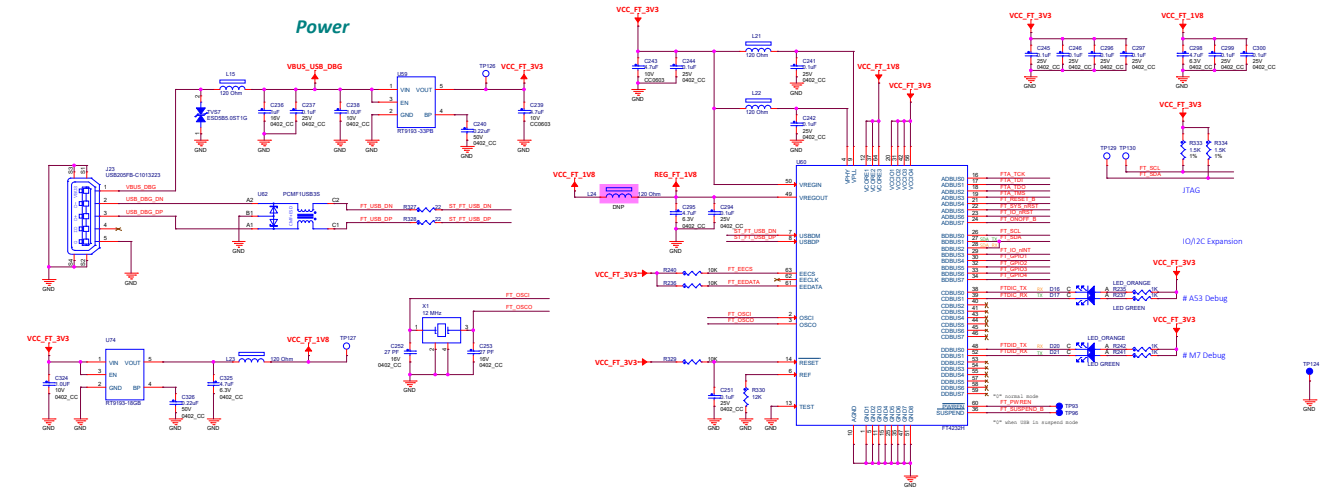
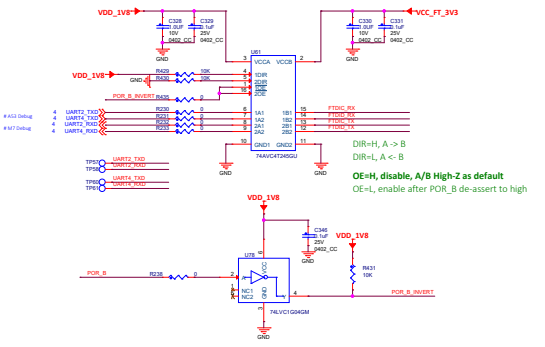
UART-USB Remote Debug

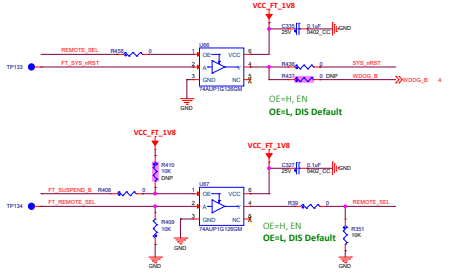
Power



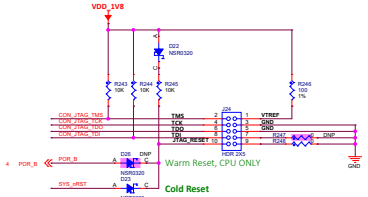
UART Level Shifter



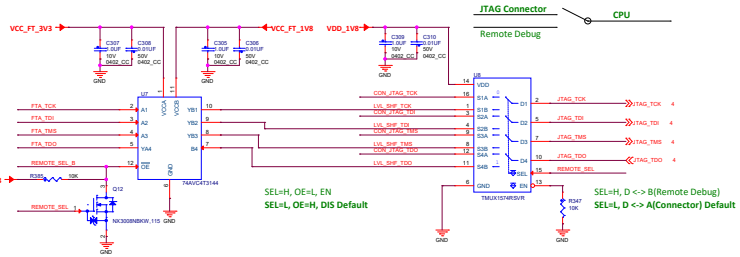
Misc Remote Control



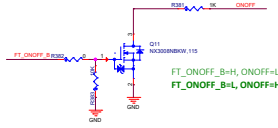
JTAG Interface



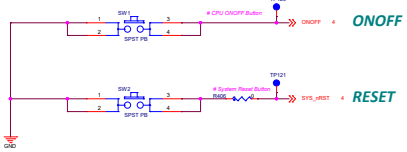
JTAG Remote Control



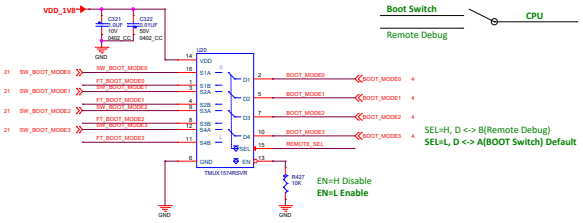
ONOFF Remote Control



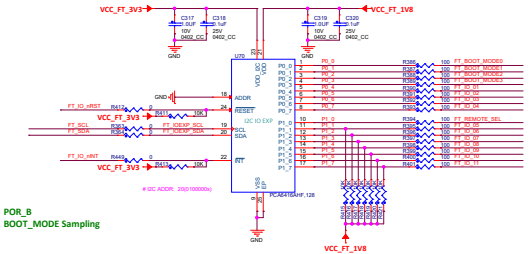
Buttons



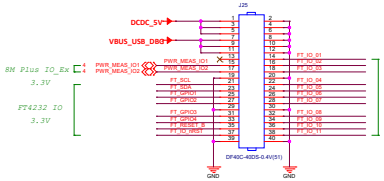
Bootmode Remote Control



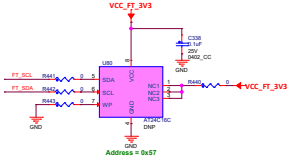
IO Expansion



Expansion Interface for Power Measurement Board Receptacle



System ID



FT Conencted First --> FT_3V3/1V8 ON --> FT_BOOT_MODE Input --> REMOTE_SEL HIGH --> Board Power/Repower --> VDD_1V8 ON --> POR_B
FT_BOOT_MODE Output Switch enable BOOT_MODE Sampling
Connection switch to Remote Debug

CPU Power ON First --> VDD_1V8 ON --> POR_B
Switch enable BOOT_MODE Sampling
Switch select to Local Switch

Designer: PL	Drawing Title: 8MPLUS-BB		
Drawn by: PL	Page Title: Debug		
Approved: <Approver>	Size: A1	Document Number: SCH-46370 PDF: SPF-46370	Rev: B1
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Microcontroller Product Group
6501 William Cannon Drive West
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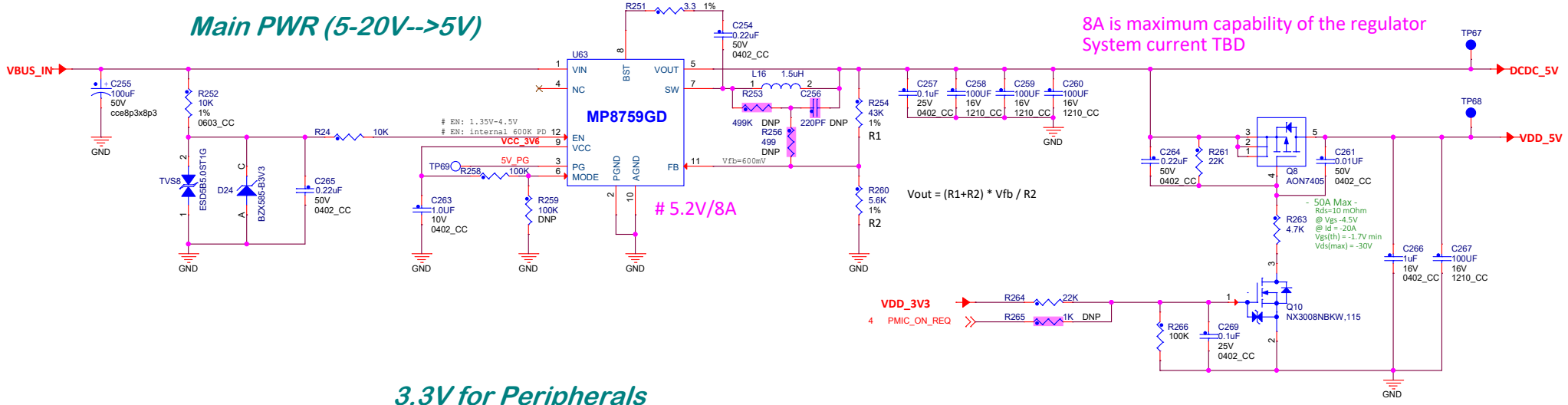
ICAP Classification: CP: BID: X PUB:

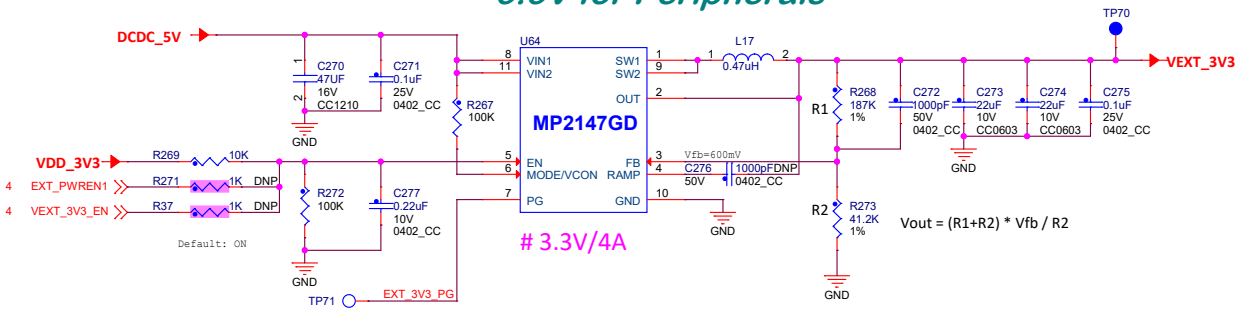
SYSTEM POWER

Main PWR (5-20V-->5V)

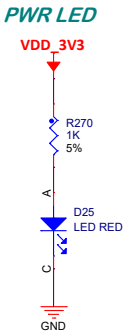


8A is maximum capability of the regulator
System current TBD

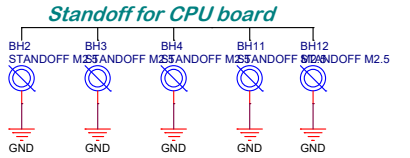
3.3V for Peripherals



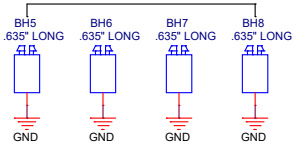
PWR LED



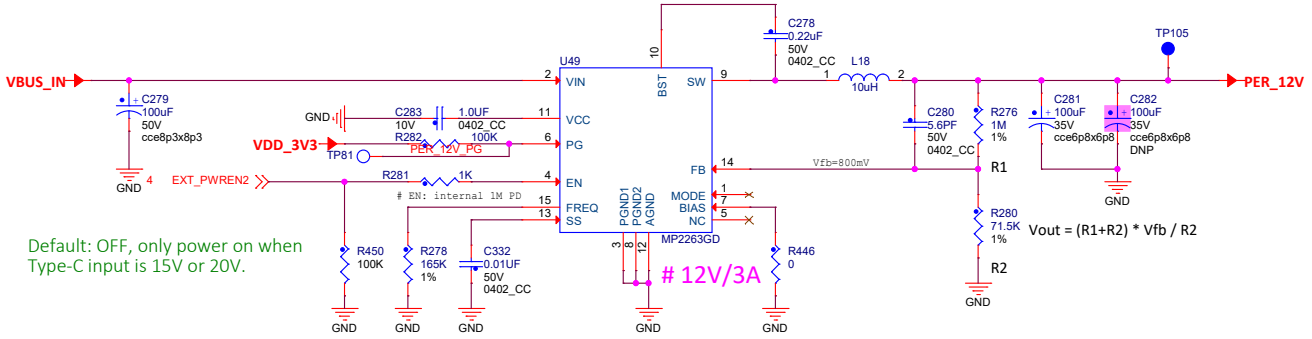
Standoff for CPU board



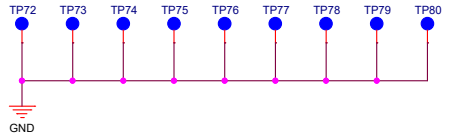
Base board screw holes



12V for Peripherals



GND Testpoints



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6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

Designer: FL	Drawing Title: 8MPLUS-BB		
Drawn by: FL	Page Title: Power		
Approved: <Approver>	Size A3	Document Number SCH-46370 PDF: SPF-46370	Rev B1
	Date: Thursday, May 13, 2021	Sheet 20 of 21	

Boot Mode and CFG Switch

i.MX8M Plus ROM Fuse

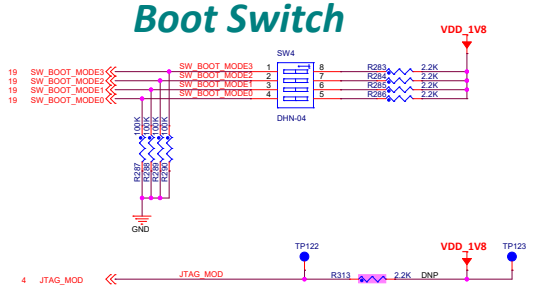
Full Line Address	Physical Address	7	6	5	4	3	2	1	0
0x470[15:0]	0x470[7:0]	OVERRIDE_NAND_PG_PER_BLK_VAL 00 - 32 pages 01 - 64 pages 10 - 128 pages 11 - 32 pages		OVERRIDE_FLEXSPI_BT_SEL 0 - Do not overriude 1 - Override	OVERRIDE_FLEXSPI_BT_SEL_VAL 00 - FlexSPI (Hyperflash 1.8V) 01 - FlexSPI (Flash with 4B READ(1x13 default supported) 10 - Default Octal mode (Micron, supported on 8QXP B0 already) 11 - Default Octal mode (Mxic, Nice to have)	FLEXSPI_AUTO_PROBE_EN 0 - Disable 1 - Enable	FLEXSPI_AUTO_PROBE_TYPE 00 - QuadSPI NOR 01 - MxicOctal 10 - MicronOctal 11 - AdestoOctal	
0x480[15:0]	0x480[7:0]	Reserved	FLEXSPI_DUMMY_CYCLE_SEL				FLEXSPI_FEQ_SEL 000 - 100 MHz 001 - 133 MHz 010 - 166 MHz 011 - 200 MHz 100 - 80 MHz 101 - 20 MHz		
0x480[31:16]	0x480[23:16]	NOC_ID_REMAP_BYPASS	ROM_NO_LOG if blown, ROM will not log event to log buffer	SDP_DISABLE Disable USB serial download	FORCE_BT_FROM_FUSE Boot from programmed fuses, not Boot Mode Pins	FLEXSPI_HOLD_TIME_SEL 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		WDOG_TIMEOUT_SELECT 00 - 2.0s 01 - 1.5s 10 - 1.0s 11 - 0.5s	
0x490[15:0]	0x490[7:0]	USDHC_PWR_EN 0 - No power cycle 1 - Enabled via	EMMC_FAST_BT 0 - Regular 1 - Fast Boot	SDMMC_BUS_WIDTH 00 - 8-bit 01 - 4-bit 10 - 8-bit DDR (MMC 4.4) 11 - 4-bit DDR (MMC 4.4)	SD_SPEED: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104	EMMC_SPEED: 00 - Normal 01 - High		USDHC_VOL_SEL For Normal Boot Mode IO Voltage 0 - 3.3V 1 - 1.8V	USDHC_MFG_VOL_SEL For Mfg Mode IO Voltage 0 - 3.3V 1 - 1.8V
0x490[31:16]	0x490[23:16]	RECOVERY_SDMMC_BOOT_DIS 0 - Enable 1 - Disable	IMG_CNTN_SET1_OFFSET				USDHC_PAD_SION_EN 0 - Disable 1 - Enable	Reserved	USDHC_DLL_EN 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/eMMC
0x4A0[15:0]	0x4A0[7:0]	SD_CALI_STEP '00' - 1 TBD	USDHC_PWR_INTERVAL 00 - 20ms 01 - 10ms 10 - 5ms 11 - 2.5			USDHC_PWR_DELAY 0 - 5ms 1 - 2.5ms	USDHC_PWR_POLARITY 0 - Low 1 - High	USDHC_OVRD_PAD_SETTING_UP1	EMMC_FAST_BT_ACK 0 - Boot Ack Disabled 1 - Boot Ack Enabled
0x4A0[31:16]	0x4A0[23:16]	Reserved							
0x4B0[15:0]	0x4B0[7:0]	Reserved	NAND_GPMI_DDR_DLL_VAL (GPMI Read DDR DLL Target Value) 0000 - 7 0001 - 1 0111 - 0 1111 - 15					Reserved	NAND_CS_NUM (Nand Number Of Devices) 00 - 1 01 - 2 10 - 4 11 - Reserved
0x4B0[31:16]	0x4B0[23:16]	Reserved	FlexSPI NAND Busy Bit Offset Override			FlexSPI NAND CS Interval 00-100ns 01-200ns 10-400ns 11-50ns		FlexSPI NAND Column Address Width 00-12 01-13 10-14 11-15	

Full Line Address	Physical Address	7	6	5	4	3	2	1	0
0x470[15:0]	0x470[15:8]	BOOT_MODE_FUSES BootRom will retrieve boot mode from these fuses instead of BOOT_MODE pins if * BOOT_MODE_PINS=0x0 or * BT_FUSE_SEL blown				OVERRIDE_USDHC_BT_SEL 0 - Do not override 1 - Override	OVERRIDE_USDHC_BT_SEL_VAL 00 - uSDHC1 SD 01 - uSDHC1 eMMC 10 - uSDHC2 eMMC 11 - uSDHC3 SD		OVERRIDE_NAND_PG_PER_BLK 0 - Do not override 1 - Override
0x480[15:0]	0x480[15:8]	BT_LPB (Core/DDR/Bus) '00'/'01' - LPB Disable '10' - Div by2 '11' - Div by 4		BT_LPB_POLARITY (GPIO polarity)	ICACHE_DIS L1 I-Cache DISABLE	TZASC_EN	WDOG_EN '0' - Disabled '1' - Enabled	BT_FREQ_SEL (ARM/DDR) 0 - 800 / 800 MHz 1 - 400 / 400 MHz	DCACHE_DIS Disable L1 and L2 D-Cache
0x480[31:16]	0x480[31:24]	ECSPI_PORT_SEL 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3		ECSPI_ADDR_SEL 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)	ECSPI_CS_SEL(SPI only) 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		RECOVER_ECSPI_BOOT_EN '0' - Disabled '1' - Enabled		DCACHE_BYPASS_DIS
0x490[15:0]	0x490[15:8]	USDHC_DLL_SEL 0 - DLL Slave Mode for 1 - DLL Override Mode	SDMMC_DLL_DLY[6:0] Delay target for USDHC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						
0x490[31:16]	0x490[31:24]	USDHC_OVRD_PAD_SETTING_LOW8[7:0]							
0x4A0[15:0]	0x4A0[15:8]	BT_TOGGLE_MODE	NAND_FCB_SERCH_COUNT 00 - 2 01 - 2 10 - 4 11 - 8	NAND_TG_PREAMBLE_RD_LATENCY (Toggle Mode 33MHz Preamble Delay, Read Latency) '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111'-15 GPMICLK cycles.				NAND_RST_TIME
0x4A0[31:16]	0x4A0[31:24]	NAND_OVERRIDE_PAD_SETTING[7:0]							
0x4B0[15:0]	0x4B0[15:8]	NAND_READ_RETRY_SEQ_ID[3:0] 0000 - don't use read retry(RR) sequence embedded in ROM 0001 - Micron 20nm RR sequence 0010 - Toshiba A19nm RR sequence 0011 - Toshiba 19nm RR sequence 0100 - SanDisk 19nm RR sequence 0101 - SanDisk 1ynmRR sequence 0110 - Hynix 20nm A Die RR sequence 0111 - Hynix 26nm RR sequence 1000 - Hynix 20nm B Die RR sequence 1001 - Hynix 20nm C Die RR sequence Others - Reserved				NAND_ROW_ADDR_BYTES 00 - 3 01 - 2 10 - 4 11 - 5		Reserved	Reserved
0x4B0[31:16]	0x4B0[31:24]	RNG_TRIM[7:0]							

i.MX8M Plus Boot Mode

BOOT_MODE3 SW4 [1]	BOOT_MODE2 SW4 [2]	BOOT_MODE1 SW4 [3]	BOOT_MODE0 SW4 [4]	Boot Modes SW4 [1-4]
0	0	0	0	Boot From Internal Fuses
0	0	0	1	USB Serial Download
0	***0***	***1***	***0***	***USDHC3 (eMMC boot only, SD3 8-bit) Default***
0	0	1	1	USDHC2 (SD boot only, SD2)
0	1	0	0	NAND 8-bit single device 256 page
0	1	0	1	NAND 8-bit single device 512 page
0	1	1	0	QSPI 3B Read
0	1	1	1	QSPI Hyperflash 3.3V
1	0	0	0	ecSPI Boot
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Boot Switch



Caution:
BOOT_MODE0, BOOT_MODE1, BOOT_MODE2, BOOT_MODE3, JTAG_MOD and POR_B must be pulled to "111111" for i.MX8M Plus to enter Boundary Scan mode.

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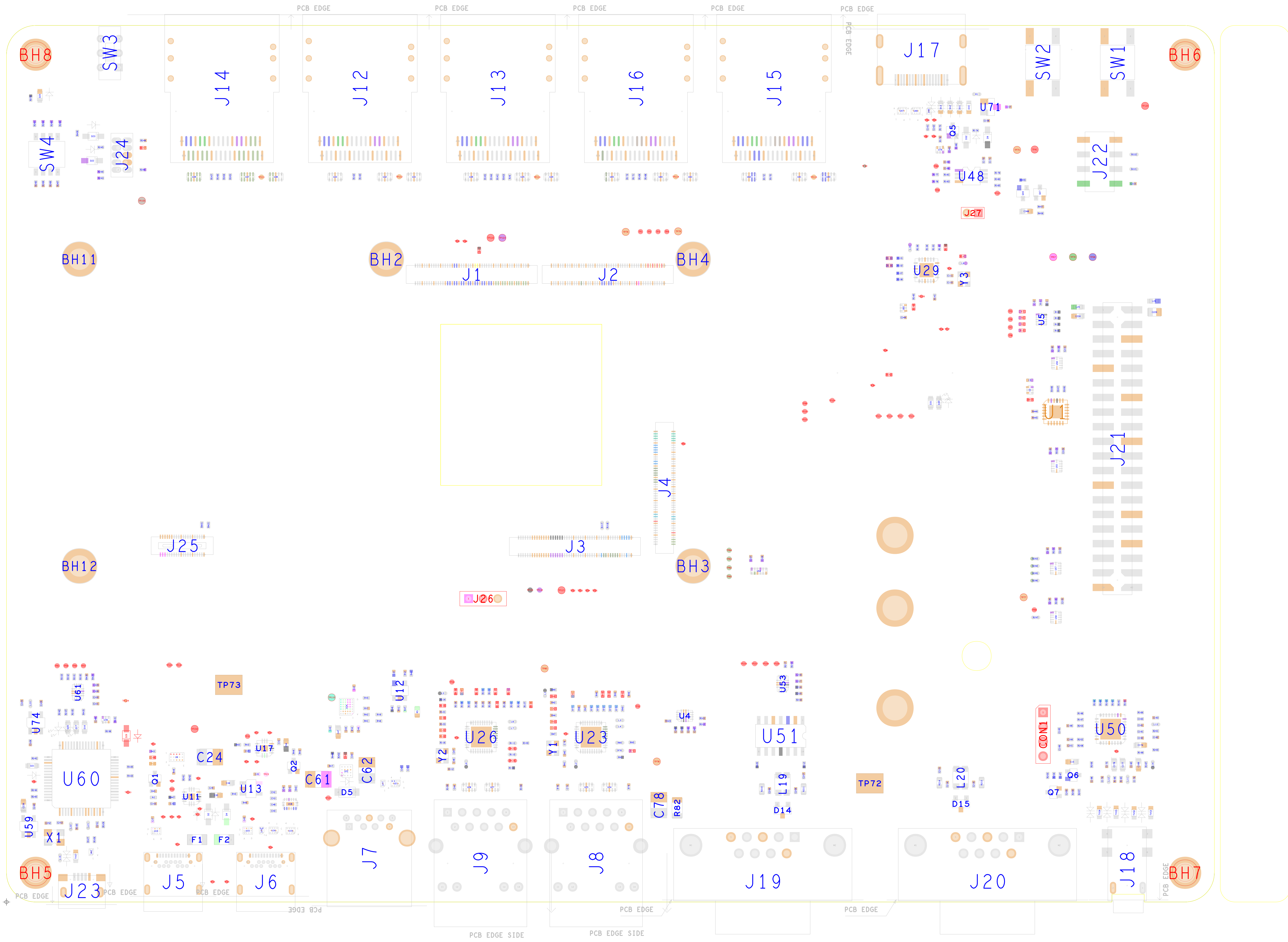
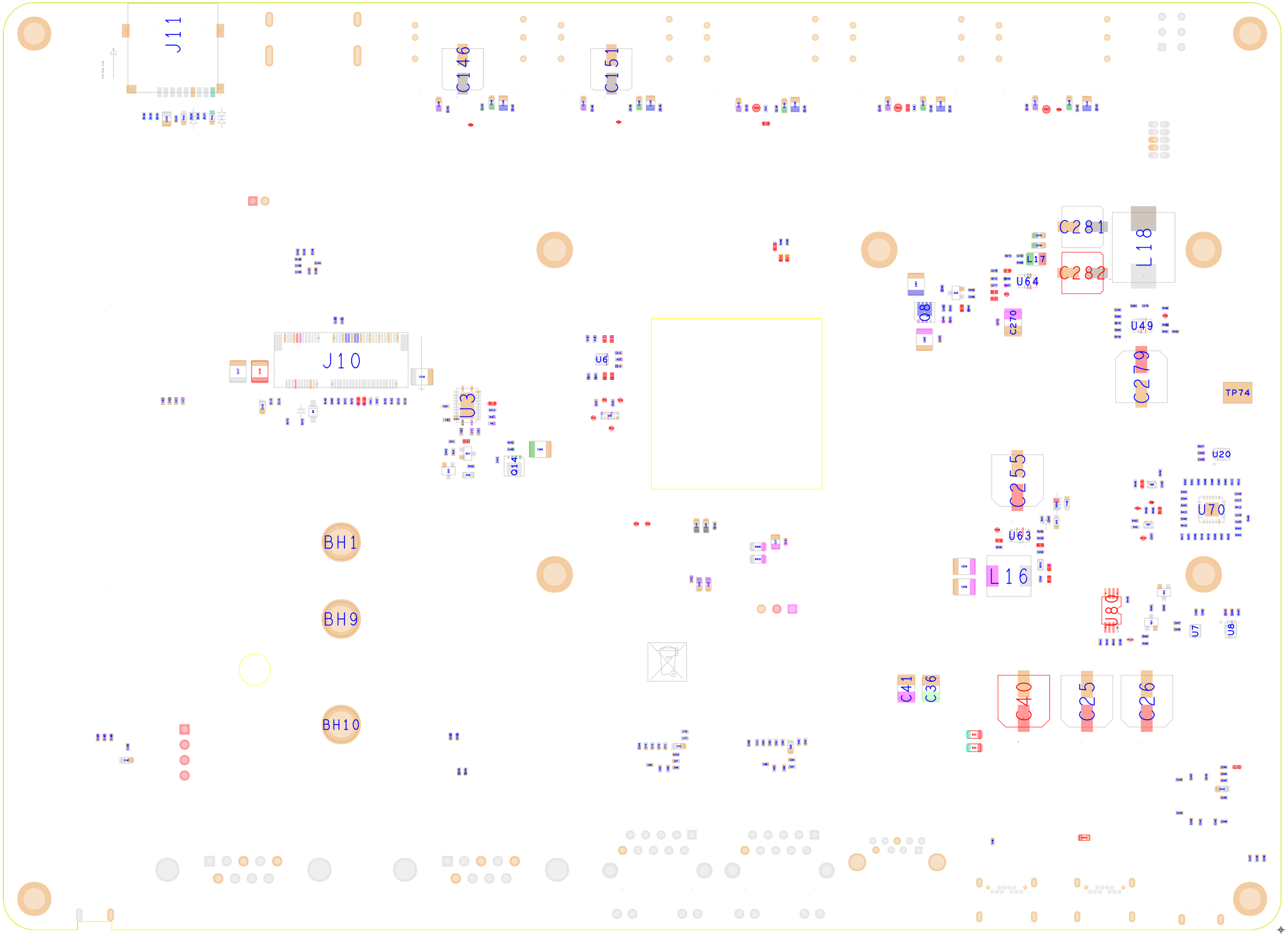
Designer: FL	Drawing Title:	8MPLUS-BB	
Drawn by: FL	Page Title:	BOOT_CFG	
Approved: <Approver>	Size A2	Document Number SCH-46370 PDF: SPF-46370	Rev B1
	Date: Thursday, May 13, 2021	Sheet 21 of 21	


PCB EDGE
BH8
SW3
J14
J12
J13
J16
J15
J17
SW2
SW1
BH6
U71
U48
J22
J27
SW4
J24
BH11
BH2
J1
J2
BH4
U29
Y3
U5
U1
J21
J4
BH12
J25
J3
BH3
J26
TP73
U61
U74
U12
U17
C24
U60
Q1
U11
U13
Q2
C61
C62
D5
U26
Y2
U23
Y1
U4
U53
U51
CON1
U50
TP72
L19
L20
D14
D15
Q6
Q7
C78
R82
U59
X1
F1
F2
BH5
J23
J5
J6
J7
J9
J8
J19
J20
J18
BH7
PCB EDGE SIDE


J11
C146
C151
J10
U3
U6
Q14
BH1
BH9
BH10
C281
C282
L18
L17
U64
Q8
C270
U49
C279
TP74
C255
U20
U70
U63
L16
U80
U7
U8
C41
C36
C40
C25
C26