UG10098

i.MX RT1180 Hardware Design Guide

Rev. 4.0 — 12 February 2026 **User guide**

Document information

Information	Content
Keywords	UG10098, i.MX RT1180 MCU, MIMXRT1180-EVK board, layout recommendations, design checklists, routing considerations, stack-up information, Ethernet, EtherCAT, Time Sensitive Networking (TSN)
Abstract	This document provides guidelines to help hardware engineers design and test their designs based on the i.MX RT1180 crossover MCU. It provides information about board layout recommendations and design checklists to ensure first-pass success and avoid board bring-up problems.

1 Introduction

The purpose of this document is to help hardware engineers design and test designs based on the i.MX RT1180 applications processor (Crossover MCU). It provides information about board layout recommendations and design checklists to ensure first-pass success and avoid board bring-up problems. This user guide is released along with the relevant device-specific hardware documentation such as data sheets, reference manuals, and application notes available on nxp.com.

i.MX RT1180 crossover MCU

The i.MX RT1180 Crossover MCU is a dual-core, real-time microcontroller featuring Arm Cortex M7 (CM7) and Cortex-M33 (CM33) cores. The CM7 core can operate at speeds of up to 800 MHz and the CM33 core can operate at speeds of up to 300 MHz with a 1.5 MB on-chip RAM.

The i.MX RT1180 includes an integrated Gbit/s Time Sensitive Networking (TSN) switch and an EtherCAT Device Controller to support multiple Industrial networking protocols (TSN, EtherCAT, Profinet, EtherNet/IP) bridging the communications between real-time Ethernet and Industry 4.0 systems.

The i.MX RT1180 integrates an advanced power management module with DC-DC and LDO regulators that reduce the complexity of external power supply and simplifies power sequencing. It also includes 1.5 MB on-chip RAM, various memory, and connectivity interfaces. ECC is built in for all internal TCMs, caches, and OCRAMs. The EdgeLock Enclave and Advance Profile enable advanced security.

2 Power supply

The i.MX RT1180 MCU integrates an advanced power management module with DC-DC and LDO regulators that reduce the complexity of external power supply. Users can use a discrete power supply or PMIC according to the application.

2.1 Power voltage specifications

For power supply voltage specifications, refer to the operating ranges table in the device data sheets listed in Section 10. See Table 1 and Table 2 for power supply decoupling recommendations.

Table 1. Processor supply capacitors when on-chip DC-DC regulators are used

Power rail	0.1 µF[1]	0.22 µF [1]	1 µF [1]	2.2 µF [1]	4.7 µF [1]	10 µF [1]	22 µF [1]	Notes
DCDC_IN_X	1				1		1	Place 0402 under balls M5 and M7. Place 0603 as close as possible to the processor.
DCDC_SENSE	1							Place under ball L8.
DCDC_1P8	1			1		1		Place 0402 under ball M4.
VDD_SOC_IN_X			2		3			Place 0402 under balls H8, H9, H10, J8, J10. Place 0603 as close as possible to the processor.
VDD_SOC_IN（Connect DCDC_LP through inductor）	1			1		1	1	Place close to the inductance.
VDDA_1P8_IN			1					Place under ball M12
VDD_AON_IN					1			Place under ball U14
VDD_AON_ANA					1			Place under ball P12
VDD_AON_DIG				1				Place under ball P11
VDD_BBSM_IN			1					Place under ball U12
VDD_BBSM_ANA				1				Place under ball R12
NVCC_AON				1				Place under ball F7
VDD_USB_1P8			1					Place under ball B17, isolate from 1V8 source with series ferrite bead (120 Ω @ 100 MHz)
VDD_USB_3P3			1					Place under ball G12, isolate from 3V3 source with series ferrite bead (120 Ω @ 100 MHz)
VDDA_ADC_1P8			1					Place under ball J13
VDDA_ADC_3P3			1					Place under ball J14
VDDA_1P0				1				Place under ball N11
NVCC_SD1				1				Place under ball C13
NVCC_SD2_X				1				Place under ball H12
NVCC_EMC1_X				1	1			Place 2.2 µF under balls J5 and J6

Table 1. Processor supply capacitors when on-chip DC-DC regulators are used*...continued*

Power rail	0.1 µF[1]	0.22 µF [1]	1 µF [1]	2.2 µF [1]	4.7 µF [1]	10 µF [1]	22 µF [1]	Notes
NVCC_EMC2_X				1	1			Place 2.2 µF under balls N6 and N7
NVCC_GPIO_AD_X				1	1			Place 2.2 µF under balls M11 and L12
NVCC_GPIO1_X				1				Place under ball D11
NVCC_GPIO2_X				1				Place under ball F9
NVCC_BBSM	1							Place under ball U11
ADC_VREFH[2]		1						Place under ball H16
USB1_VBUS			1					Place under ball D17
USB2_VBUS			1					Place under ball D16

[1] Capacitors of values 0.1, 0.22, 1, 2.2, and 4.7 µF have size 0402 (*40 mils long and 20 mils wide*), type X6S. Capacitor of value 22 µF has size 0603, type X6S.

[2] Avoid using the internal DCDC/LDO output for the ADC reference. Use a more accurate external voltage reference instead.

Table 2 lists the recommendation for processor supply capacitors when external PMIC or regulators are used and the on-chip DC-DC regulators are not used.

Table 2. Processor supply capacitors when external PMIC or regulators are used

Power rail	0.1 µF[1]	0.22 µF [1]	1 µF [1]	2.2 µF [1]	4.7 µF [1]	10 µF [1]	22 µF [1]	Notes
VDD_SOC_IN_X			2		3			Place 0402 under balls H8, H9, H10, J8, J10. Place 0603 as close as possible to the processor.
VDD_SOC_IN（Connect DCDC_LP through inductor）	1			1		1	1	Place close to inductance.
VDDA_1P8_IN			1					Place under ball M12
VDD_AON_IN					1			Place under ball U14
VDD_AON_ANA					1			Place under ball P12
VDD_AON_DIG					1			Place under ball P11
VDD_BBSM_IN			1					Place under ball U12
VDD_BBSM_ANA				1				Place under ball R12
NVCC_AON				1				Place under ball F7
VDD_USB_1P8			1					Place under ball B17, isolate from 1V8 source with series ferrite bead (120 Ω @ 100 MHz)
VDD_USB_3P3			1					Place under ball G12, isolate from 3V3 source with series ferrite bead (120 Ω @ 100 MHz)
VDDA_ADC_1P8			1					Place under ball J13
VDDA_ADC_3P3			1					Place under ball J14
VDDA_1P0				1				Place under ball N11
NVCC_SD1				1				Place under ball C13
NVCC_SD2_X				1				Place under ball H12
NVCC_EMC1_X				1	1			Place 2.2 µF under balls J5, J6
NVCC_EMC2_X				1	1			Place 2.2 µF under balls N6, N7
NVCC_GPIO_AD_X				1	1			Place 2.2 µF under balls M11, L12
NVCC_GPIO1_X				1				Place under ball D11
NVCC_GPIO2_X				1				Place under ball F9
NVCC_BBSM	1							Place under ball U11

Table 2. Processor supply capacitors when external PMIC or regulators are used*...continued*

Power rail	0.1 µF[1]	0.22 µF [1]	1 µF [1]	2.2 µF [1]	4.7 µF [1]	10 µF [1]	22 µF [1]	Notes
ADC_VREFH[2]		1						Place under ball H16
USB1_VBUS			1					Place under ball D17
USB2_VBUS			1					Place under ball D16

[1] Capacitors of value 0.1 µF, 0.22 µF, 1 µF, 2.2 µF, and 4.7 µF are size 0402 and the 22 µF capacitor has size 0805. Type X6S is used for automotive cluster and extended temperature range.
[2] Avoid using the internal DCDC/LDO output for the ADC reference. Use a more accurate external voltage reference instead.

Table 3. Power supply and BBSM domain signals

Item	Recommendation	Description
Power sequence	To guarantee a reliable operation of the device, comply with the power-up/power-down sequence guidelines (as described in the data sheet).	Any deviation from these sequences can result in these situations: • Excessive current during the power up phase • Prevention of the device from booting • Irreversible damage to the processor (worst-case scenario)
BBSM domain signals	Do not overload the coincell backup power rail VDD_BBSM_IN. These I/Os are associated with NVCC_BBSM (most inputs have on-chip pull resistors and do not require external resistors): • PMIC_STBY_REQ: configurable output • PMIC_ON_REQ: push-pull output • TEST_MODE: on-chip pulldown • POR: on-chip pullup • WAKEUP: This pin can wake up the SoC in the BBSM mode. WAKEUP cannot work as a GPIO • GPIO_BBSM_XX: on-chip pulldown	Concerning i.MX RT1180: • The chip internal LDO VDD_BBSM_ANA output current is 1 mA and must be tied together with NVCC_BBSM. • The GPIO_BBSM_XX pins can only function as tamper function if enabled, which means they cannot be used as general-purpose IO.
Power ripple	Maximum ripple voltage limitation.	The common limitation for the ripple noise is less than 5 % V (p-p) of the supply voltage average value. The related power rails affected are VDD_XXX, VDD_XXX_IN, VDDA_1P0, VDD_XXX_ANA, and VDD_XXX_DIG.
Supply currents	Maximum supply currents must comply with maximum supply currents in the data sheet.	Concerning i.MX RT1180: • The DCDC_DIG_X output current is 1000 mA and DCDC_1P8 output current is 150 mA.

2.2 Power sequence requirements

- For power supply sequencing requirements, refer to the section, 'Power supplies requirements and restrictions' of the *i.MX RT1180 Crossover Processors Data Sheet* (document IMXRT1180EC) see Section 10.

Figure 1 shows the power control logic of the MIMXRT1180-EVK board.

- It powers up BBSM first, then PMIC_ON_REQ is asserted to enable external DC-DC to power up other power domains.
- The **ON/OFF** button is used to switch PMIC_ON_REQ to control power modes.
- The **RESET** button and the WDOG output are used to reset the system power.

Note: *Figure 1 is applicable to i.MX RT1180 silicon.*

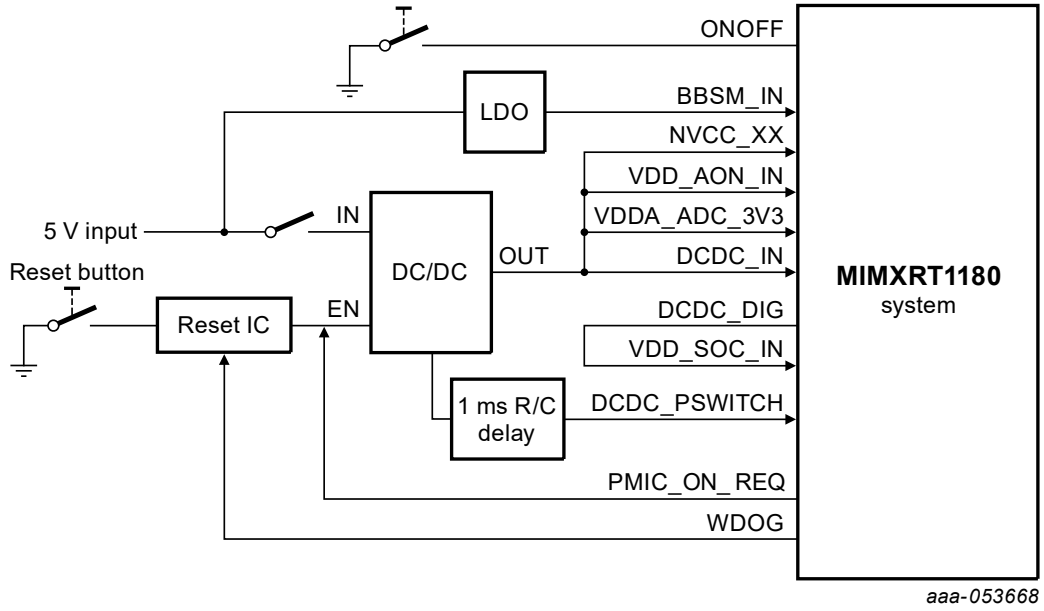


Figure 1. Power control diagram

Note:

- *There are few more power domains such as VDD_USB_1P8, VDD_USB_3P3, VDDA_ADC_1P8, VDDA_1P8_IN that are not depicted in the above figure. For details, refer to MIMXRT1180-EVK design schematic (Section 10).*
- *If a PMIC is used with i.MX RT1180 MCU in SNVS mode, ensure that the VDD_SOC_IN supply is switched off before the VDD_AON_DIG supply is off.*
- *As per errata 053252, if NVCC_xxx power up is ahead of VDD_SOC_IN or VDDA_1P8_IN, short pulses can occur on I/O during NVCC_xxx power ramp up. In some typical cases, the pulse is higher than 1.0 V. For customer applications impacted by this errata, the hardware workaround is to power VDDA_1P8_IN before NVCC_xxx.*

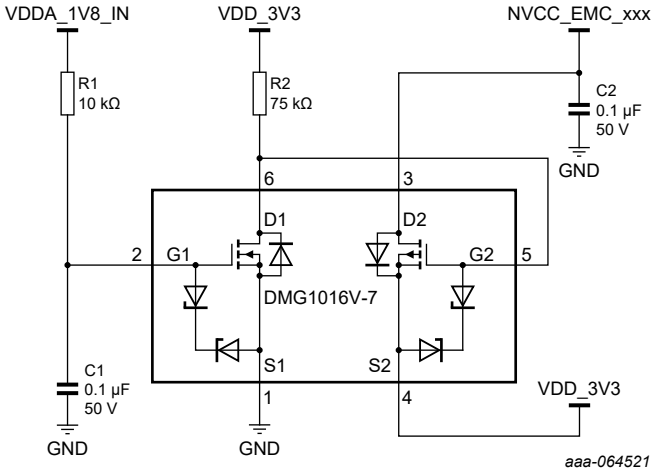


Figure 2. Hardware workaround circuit

2.3 On-chip DC-DC module

The internal DC-DC of the i.MX RT1180 MCU has two outputs:

- VDD_DIG: It is typically 0.7 V ~ 1.15 V and its switching frequency is about 1.5 MHz.
- VDD_1P8: It is the LDO output, which is typically 1.8 V.

The DC-DC requires external inductors and capacitors, as described in Figure 3. Pay attention to the below points:

- The recommended value for the external inductor is about 4.7 µH with the saturation current > 1.5 A and ESR < 0.1 Ω.
- The external bulk capacitor total is about 66 µF. It includes all the capacitors used on DCDC_DIG_X and VDD_SOC_IN.
- DCDC_PSWITCH must be delayed 1 ms after DCDC_IN to guarantee that DCDC_IN is stable before the DC-DC starts up.
- An RC delay circuit is recommended for providing the delay between DCDC_IN stable and DCDC_PSWITCH. The total RC delay must be 5 ms – 40 ms.
- DCDC_IN must reach a minimum 3.0 V within 0.3 x RC.
- To bypass the internal DC-DC, the signals DCDC_PSWITCH, and DCDC_MODE must be tied to the ground. Other signals such as DCDC_IN, DCDC_LP, and DCDC_SENSE can be floating.
- To avoid EMI issues, keep the DC-DC current loop as small as possible.

Figure 3 shows a sample DC-DC use case.

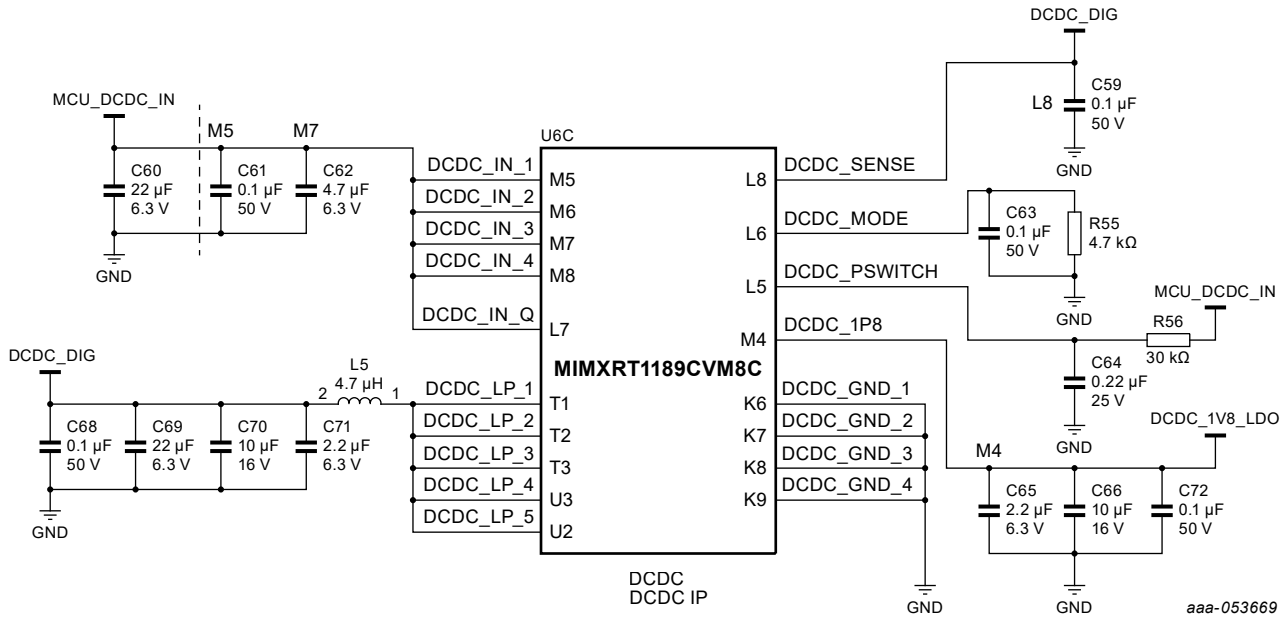


Figure 3. DC-DC use case

2.4 External PMIC

For certain use cases, especially automotive applications, if the internal DC-DC does not meet the SOC_IN current capability requirement, an external power supply (DC-DC) with higher than 1000 mA current capability must be used.

To implement the PMIC on i.MX RT1180 MCU, refer to *Using i.MX RT117x Processor with PF5020 PMIC for Auto Application* (document AN13213).

3 Clocks

The 32.768 kHz and 24 MHz oscillators are used for the MIMXRT1180-EVK schematic design. For the i.MX RT1180 MCU, it is necessary to use 24 MHz crystals for the hardware design.

See Table 4 for the clock configuration.

Table 4. Clock configurations

Signal name	Recommended connections	Description
RTC_XTALI/ RTC_XTALO	For the precision 32.768 kHz oscillator, connect a crystal between RTC_XTALI and RTC_XTALO. Choose a crystal with a maximum ESR (Equivalent Series Resistance) of 100 kΩ and follow the recommendation by the manufacturer for the loading capacitance. Do not use an external biasing resistor because the bias circuit is on the chip.	To achieve the exact oscillation frequency, the board capacitors must be reduced to account for the board and chip parasitics. The integrated oscillation amplifier is self-biasing, but relatively weak. Make sure to limit the parasitic leakage from RTC_XTALI and RTC_XTALO to either the power or the ground (>100 Ω). This debiases the amplifier and reduces the startup margin.
	For the external kHz source (if feeding an external clock into the device), RTC_ XTALI can be driven DC-coupled with RTC_XTALO floating or by a complementary signal.	If you want to feed an external low-frequency clock into RTC_ XTALI, the RTC_XTALO pin must remain unconnected or driven by a complementary signal. The voltage level of this forcing clock must not exceed the VDD_BBSM_ANA level and the frequency must be <100 kHz under the typical conditions.
	An on-chip loose-tolerance ring oscillator of approximately 32 kHz is available. If RTC_XTALI is tied to GND and RTC_XTALO is floating, the on-chip oscillator is engaged automatically.	The system can use the on-chip 32 kHz oscillator when a high-accuracy real-time clock is not required. The tolerance is ±25 %. The ring oscillator starts faster than the external crystal and is used until the external crystal reaches a stable oscillation. If no clock is detected at RTC_ XTALI at any time, the ring oscillator also starts automatically.
XTALI/XTALO	For the precision 24 MHz oscillator, connect a fundamental-mode crystal between XTALI and XTALO. A typical 80 Ω ESR crystal rated for a maximum drive level of 250 µW is acceptable. • Alternately, use a typical 50 Ω ESR crystal rated for a maximum drive level of 200 µW. • For the i.MX RT1180 24 MHz oscillator, the smaller the ESR, the better is the startup and power consumption. • To use the high-power mode, populate the 1 MΩ resistor between XTALI and XTALO. • Use a crystal with ESR < 100 Ω and CL <= 16 pF for startup .	The SDK software requires 24 MHz on XTALI/ XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, refer to section Bypass Configuration (24 MHz) from *i.MX RT1180 Reference Manual* (document *IMXRT1180RM*) See Section 10. For the bypass mode pin connection, the external bypass clock can be put in from the XTALI pin. At the same time, XTALO can be used as other functions. The voltage level of this forcing clock must not exceed the VDD_AON_ANA level. If this clock is used as a reference for the USB and Ethernet, there are strict frequency tolerance and jitter requirements. The ±50 ppm accuracy is required for the Ethernet while the ±100 ppm accuracy is required for the USB. For more details, see the Crystal Oscillator (XTALOSC) chapter in *i.MX RT1180 Reference Manual* (document *IMXRT1180 RM*) See Section 10.
CLK1_P/CLK1_ N	Internal use only	These pins are used for NXP internal testing. The CLK1_P and CLK1_N pair must be left floating.

4 Boot reset and miscellaneous

Table 5 shows the recommended guidelines for the boot, reset, and miscellaneous configurations, such as ON/OFF, TEST_MODE, and NC pins.

Table 5. Boot configuration

Item	Recommendation	Description
BOOT_CFG[15:0]	The BOOT_CFG signals are not wired out in the package. Follow the BOOT_CFG fuse setting in configuration.	For the correct boot configuration, see the 'System Boot' Chapter in the *i.MX RT1180 Processor Reference Manual*. [1]. ***Note:*** *Incorrect setting can result in an improper boot sequence.*
BOOT_MODE[2:0]	For logic 0: • Tie to GND through 100 kΩ external resistor. For logic 1: • Tie to the NVCC_AON power domain through a 1 kΩ external resistor.	BOOT_MODE2, BOOT_MODE1, and BOOT_MODE0 have on-chip pulldown devices with a nominal value of 35 kΩ. When the on-chip fuses determine the boot configuration, boot mode inputs can be disconnected.

[1] See Section 10

Table 6. Reset and miscellaneous recommendations

Item	Recommendation	Description
POR_B	The POR_B input (if used) must be immediately asserted at power up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. For further details and to ensure that all requirements are being met, see the Reference Manual[1].	For the correct boot configuration, see the '*System Boot*' Chapter *i.MX RT1180 Processor Reference Manual*. See Section 10.[1] ***Note:*** *Incorrect setting can result in an improper boot sequence.* POR_B signal has an internal 100 kΩ pull up to the BBSM domain. Pullup to NVCC_BBSM if you add an external pullup resistor. Otherwise, it causes other leakage during BBSM mode. Add the external reset IC to the circuit to guarantee POR_B is properly processed during power up/down, refer to the MIMXRT1180-EVK schematic design for details (see Section 10). ***Note:*** • *As the Low DCDC_IN detection threshold is 2.6 V, the reset threshold of the reset IC must be higher than 2.6 V. Then the whole chip is reset before the internal DC-DC module resets to ensure chip safety during power down.* • *For power-on reset, always ensure that the voltage on DCDC_PSWITCH PIN is below 0.5 V before power up.*
ON/OFF	For portable applications, the ON/OFF input can be connected to the ON/OFF SPST pushbutton. The on-chip debouncing is provided, and this input has an on-chip pullup. If not used, ON/OFF can remain not-connected. A 4.7 kΩ to 10 kΩ series resistor can be used when the current drain is critical.	A brief connection to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to GND generates an interrupt (intended to be a software-controllable power-down). Approximately 5 seconds (or more) to GND causes a forced OFF.

Table 6. Reset and miscellaneous recommendations*...continued*

Item	Recommendation	Description
TEST_MODE	The TEST_MODE input is internally connected to an on-chip pulldown device. This signal can be tied to the ground or left floating.	This input is reserved for the NXP manufacturing use.

[1] This device supports various peripherals for the boot ROM. Refer to *Section 12.2.1, 'Boot ROM pinmux for Serial Downloader and different boot peripherals*' in *i.MX RT1180 Processor Reference Manual* (document IMXRT1180RM) see Section 10.

5 ADC usage

i.MX RT1180 MCU has the 2x 16-bit dual-channel SAR ADC. To avoid these issues, refer to the below points for ADC-related circuit design:

- ADC power supply and reference
  The i.MX RT1180 MCU has two power supplies, namely VDDA_ADC_1P8 and VDDA_ADC_3P3 that supply power to the ADC. Refer to Table 1 and Table 2 for the decoupling capacitor placement. At the same time, ensure that the VDDA_ADC_1P8 supply is powered prior to the VDDA_ADC_3P3 supply as specified in the data sheet.
  i.MX RT1180 MCU VREFH can be supplied by the internal VREF output or an external LDO supply. In addition to these supplies, VDDA_ADC_1P8 is connected as the alternative reference option.
- Analog source impedance
  Refer to *Cookbook for SAR ADC Measurements, ADC measurements done properly* (document AN14373). The document describes the sampling circuit in detail and provides examples demonstrating the procedure to design external RC components of ADC. To use a suitable input impedance and filtering capacitor to sample correctly, follow the guidelines.

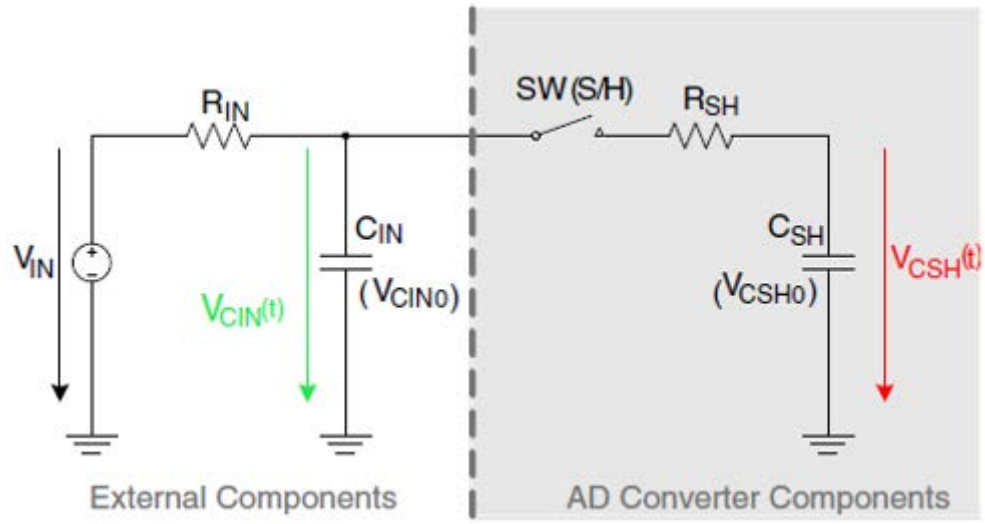


Figure 4. Equivalent sampling circuit

- ADC channel assignment
  The ADC1 module of the chip has 16 channels that are connected to the CH0A to CH7A and CH0B to CH7B. The ADC2 module of the chip has 14 channels that are connected to the CH0A to CH6A and CH0B to CH6B. Channels with suffix A are associated with the side-A converter while channels with suffix B are associated with the side-B converter in the ADC.
- ADC pin processing
  The PCB trace length for ADC pins must be as short as possible. In practical application design, consider the complete influence of parasitic parameters on PCB traces for ADC pins. Special care must be taken to minimize noise levels on the analog power and reference pins.
  The input filters connected to the ADC have a significant impact on the noise immunity of the analog parts. The type of the filters to be used depends on the input signal frequency. The location of the filter capacitors is also important.
  To avoid noise impact, it is recommended to have ADC input signals surrounded with the GND plane to avoid noise impact. To avoid ADC input signals powered prior to other power domains, ensure that the residual voltage of other power domains is less than 0.5 V.

6 Layout recommendations

The i.MX RT1180 MCU has many high-performance peripherals that require a robust board layout design. The subsections that follow provide the guidelines to avoid hardware issues.

6.1 Stack-up

A high-speed design requires a good stack-up to have the right impedance for the critical traces.

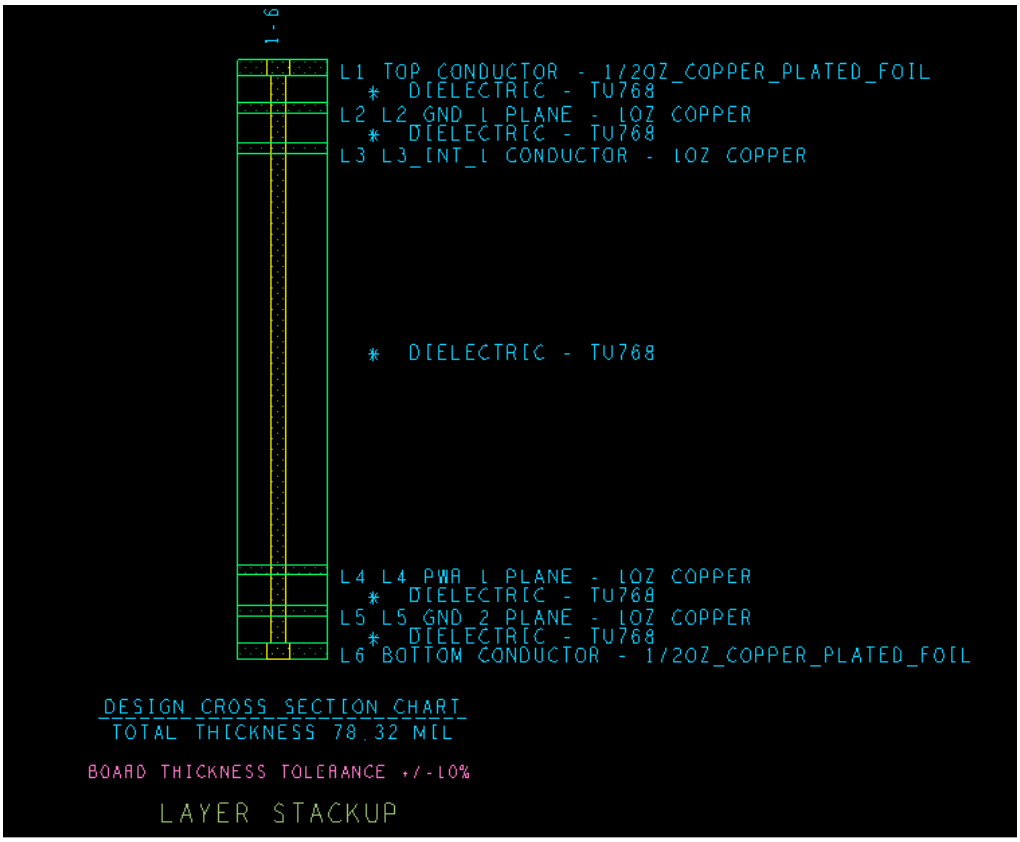
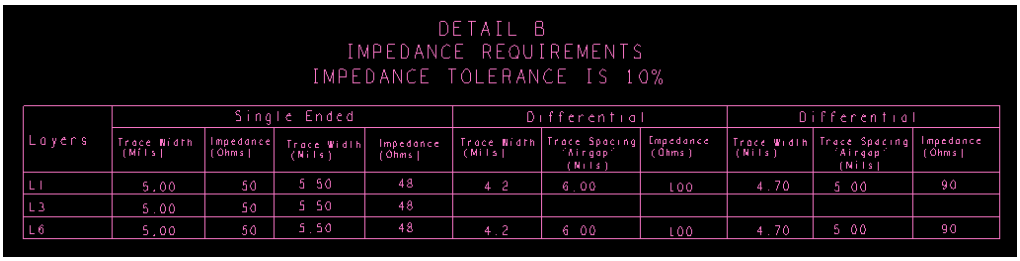


Figure 5. MIMXRT1180-EVK stackup

The constraints for the trace width depend on many factors. These factors are board stack-up and the associated dielectric and copper thickness, required impedance, and required current (for power traces). The stack-up also determines the constraints for routing and spacing. Follow the below guidelines when designing the stack-up and selecting the material for your board:

- The board stack-up is critical for the high-speed signal quality.
- Plan the impedance of the critical traces.
- The high-speed signals must have reference planes on adjacent layers to minimize crosstalk.
- The NXP reference design equals the Isola FR4.
- The NXP validation boards equal the Isola FR4.
- The recommended stack-up is six layers, with the layer stack shown in Figure 5. Figure 6 shows the MIMXRT1180-EVK PCB stack-up implementation.



DETAIL B
IMPEDANCE REQUIREMENTS
IMPEDANCE TOLERANCE IS 10%

Layers	Single Ended				Differential			Differential		
	Trace Width (Mils)	Impedance (Ohms)	Trace Width (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing "Airgap" (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing "Airgap" (Mils)	Impedance (Ohms)
L1	5.00	50	5.50	48	4.2	6.00	100	4.70	5.00	90
L3	5.00	50	5.50	48						
L6	5.00	50	5.50	48	4.2	6.00	100	4.70	5.00	90

Figure 6. MIMXRT1180-EVK board stack-up implementation

6.2 Placement of bulk and decoupling capacitors

Place small decoupling capacitors and larger bulk capacitors on the bottom side of the CPU. The 0402 decoupling capacitors and the 0603 bulk capacitors must be placed as close as possible to the power ball. Placing decoupling capacitors close to the power balls is critical to minimize inductance and ensure the high-speed transient current demand of the processor. The correct via size, trace width, and trace space are critical to preserve the adequate routing space. The recommended geometry is as follows:

- For the BGA constraint area:
  - The via type is 18/8 mils, the trace width is 4 mils, and the trace space is 3.79 mils.
- For the default area (except for the BGA):
  - The via type is 18/8 mils, the trace width is 5 mils, and the trace space is 7 mils.
  - The preferred BGA power-decoupling design layout is available at www.nxp.com.
  - Use the NXP design strategy for power and decoupling.

6.3 FlexSPI

FlexSPI is a flexible SPI host controller that supports two SPI channels and up to four external devices. Each channel supports Single/Dual/Quad/Octal mode data transfer (1/2/4/8 bidirectional data lines). FlexSPI is the most commonly used external memory.

For more information, refer to section '*FlexSPI parameters*' from the *i.MX RT1180 Data Sheet* (see Section 10). There are several sources for the internal sample clock for FlexSPI read data. These sources are listed below:

- Dummy read strobe generated by the FlexSPI controller and looped back internally:
  - (FlexSPIn_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by the FlexSPI controller and looped back through the DQS pad
  - (FlexSPIn_MCR0[RXCLKSRC] = 0x1)
- Read strobe provided by a memory device and input from a DQS pad
  - (FlexSPIn_MCR0[RXCLKSRC] = 0x3)

For QSPI flash without a DQS provided by the memory, the limiting SCK frequency is 60 MHz in the case of FlexSPIn_MCR0[RXCLKSRC] = 0x0. The limiting SCK frequency is 133 MHz in the case of FlexSPIn_MCR0[RXCLKSRC] = 0x1. The FlexSPI_DQS pin must be left floating in both these cases.

For the octal flash where a DQS signal is provided by the memory, you must use the option of FlexSPIn_MCR0[RXCLKSRC] = 0x3 that can achieve 166 MHz DDR R/W. In such case, the FlexSPI_DQS pin must be connected to the flash directly.

- HyperRAM/SDRAM selection limitation. The i.MX RT1180 ROM can only support the initialization of one-die HyperRAM/SDRAM device though the FlexSPI supports both one-die and dual-die devices. The dual-die device can work well in customer applications. Refer to *Section 4.1 SDRAM interface hardware rework* in *UM12021*. See Section 10.

6.4 SDRAM

The SDRAM interface (running at up to 200 MHz) is one of the critical interfaces for the chip routing. The controlled impedance for the single-ended traces must be 50 Ω. Ideally, the route all signals at the same length as the MIMXRT1180-EVK board. To route all signals at the same length (±50 mils), see the MIMXRT1180-EVK layout.

The SDRAM routing must be separated into two groups: data and address/control.

To separate all SDRAM signals into two groups, see the MIMXRT1180-EVK layout:

- SEMC_DQS signal line must be left floating.
- All data lines and DM[x]
- All address lines and control lines

MIMXRT1180-EVK board uses a 6-layer board design. Both routing groups refer to the GND plane for the impedance control. One group is routed at the top layer (the reference plane is the second layer), while the other group is routed at the bottom layer (the reference plane is the fifth layer).

Note: *By default, the SDRAM function is not enabled in the MIMXRT1180-EVK board because these signals are multiplexed with NETC pinmux. To enable SDRAM function, do the resistor switching between ENET and SDRAM signals. Refer to Section 4.1, 'SDRAM interface hardware rework' in UM12021.*

6.5 USB

Use these recommendations for the USB:

- Route the DP and DM differential pair first.
- Route the DP and DM signals on the top (or bottom) layer of the board.
- The trace width and spacing of the DP and DM signals must meet the differential impedance requirement of 90 Ω.
- Route the traces over the continuous planes (power and ground):
  - They must not pass over any power/GND plane slots or antietch.
  - When placing the connectors, make sure that the ground plane clearouts around each pin have ground continuity between all pins.
- Maintain the parallelism (skew-matched) between DP and DM, and match the overall differential length difference to fewer than 5 mils.
- Maintain the symmetric routing for each differential pair.
- Do not route the DP and DM traces under the oscillators or parallel to the clock traces (and/or data buses).
- Minimize the lengths of the high-speed signals that run parallel to the DP and DM pair.
- Keep the DP and DM traces as short as possible.
- Route the DP and DM signals with a minimum number of corners. Use 45-degree turns instead of 90-degree turns.
- Avoid layer changes (vias) on the DP and DM signals. Do not create stubs or branches.
- Provide the ground return vias within a 50 mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
- When the USB signals are not used, it is recommended to follow Section 8.

6.6 Ethernet

The i.MX RT1180 has one Ethernet controller that is a Gigabit Ethernet controller with support for AVB/TSN. For the RGMII port, the layout is critical and the guidelines are below.

- To ensure the correct RGMII function, the length of PCB trace must be less than 15 cm with a 5 pF loading to comply with the maximum 1 ns delay regulation, and the total trace loading (5 pF input loading included) must be within 15 pF.
- Clock and other high-speed traces must be as short as possible. Have a GND plane under these traces.
- RXC and TXC are high-speed (125 MHz) signals; keep a 20 mil space between clock and data signals.
- Match each RGMII TX and RX (RXC/RXD/RXCTL/RXDV) group trace length to within +/-50 mil.
- Route the RGMII traces at 50 Ω impedance and make sure to route those traces over an unbroken GND reference ground plane.
- For the RXC signal from the PHY, place R/C close to the PHY (fewer than 500 mils) and adjust the R/C value to tune the timing.
- Some PHY RST and INT signals need a 3V3 voltage even if the IO voltage is 1V8 (Realtek PHY).
- Multiple PHYs use the same SMI interface, pay attention to the pull-up resistors, do not use too strong pull-up.
- Only ETH2, ETH3, and ETH4 support RevMII mode.
- RMII/MII 10 Mbit/s PHY limitation is present due to the NETC MAC errata ERR051651. The 10 Mbit/s speed is restricted to PHYs that support octet alignment for preamble with minimum 1B. Refer to *Section 4.3, 'PHY compatibility evaluation report'* in UM12021 for the list of compatible PHYs validated by NXP.

6.7 EtherCAT

The i.MX RT1180 MCU has one EtherCAT peripheral controller that supports two MII/RMII 100 Mbit/s ports.

- EtherCAT and NETC use the same MDIO/MDC signals.
- The ECAT_RESET_OUT signal must be connected to both EtherCAT PHY's PHY_RST_B signals to prevent the PHYs from establishing a link while the eCAT IP is in reset status, or EtherCAT frames could be lost.
- The two PHY addresses must be continuous.
- For MII interface, all PHYs are connected to one EtherCAT Subordinate Controller (ESC) and the ESC itself must share a 25 MHz clock source. Therefore, a TX FIFO can be omitted. This can be achieved by sourcing the PHYs from an ESC clock output.
- Follow the *AN PHY Selection Guide. Requirements to Ethernet PHYs used for EtherCAT and EtherCAT G Ethernet PHY Examples*. (See Beckhoff website).

6.8 I3C

The i.MX RT1180 MCU has two I3C modules for connectivity and communication. Table 7 provides a comparison of I3C and I2C features.

Table 7. Comparison between I2C and I3C

Feature	I3C	I2C
SCL max frequency	12.5 MHz	1 MHz (FM+ mode)
IO topology	• SCL push-pull • SDA: open drain and push-pull	• SCL: open drain • SDA: open drain
Capacitive load per bus line	50 pF	• 400 pF for FM • 550 pF for FM+
Bus pull-up resistor	Integrated in the host controller	External pullup
Interrupt	In the band	Dedicated pin
Compatibility	Supports I2C target devices with 50 ns glitch filter	No support
Dynamic addressing	Yes	No
Ninth bit function	ACK or NACK address, Parity (write), and Bus control (read)	ACK or NACK
Bus functions	Common code commands (CCC)	Special address
Device feature support	3 mandatory registers BCR, DCR, LVR	No
Bus compliance	Yes, established as interoperability rules	No
Target reset	Unique pattern based	Hard-reset line
Target device clock stretching	Not allowed on I3C	Yes
Extended address (10 bit)	Not used on I3C	Optional
20 mA open drain driver	Not used on I3C	Supported in FM+ mode

Follow the below guidelines while designing I3C-related circuits:

- C_{load} (load capacitor) must be within 50 pF.
- SCL Clock Rise/Fall Time must be less than 60 ns.
- The total stub must be within 1.5 inch.
- To avoid reflection pulse, run an SI simulation.
- Remove external pullup resistor on SCL and SDA.
- Add 1 kΩ pull-up resistor from SDA to PUR pin besides exception.

It is also recommended that the I3C bus must only connect to a dedicated I3C device.

If the device uses a mixed mode (I2C+I3C), note the below requirements for the bus speed:

- Mixed Slow/Limited Bus: If the I2C device does not have a 50 ns IO Spike Filter, then the I3C bus max frequency is limited to 400 kHz in FM mode and 1 MHz in FM+ mode.
- Mixed Fast Bus: If the I2C device has 50 ns IO Spike Filter, then the I3C bus SCL High parameter `tIG_H_MIXED` is limited to 32 ns ~ 45 ns.

6.9 High-speed signal routing recommendations

The following list provides recommendations for routing the traces for high-speed signals.

Note: *The propagation delay and the impedance control must match to have a correct communication with the devices.*

- The high-speed signals (such as SDRAM, RMII, RGMII, USB, HyperFlash, SD card) must not cross gaps in the reference plane.
- Avoid creating slots, voids, and splits in the reference planes. To ensure that they do not create splits (space out vias), review the via voids.
- Provide ground return vias within a 100 mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
- A solid GND plane must be directly under the crystal-associated components and traces.
- To reduce crosstalk, clocks or strobes that are on the same layer must follow the below requirements:
  - At least 2.5× spacing from the adjacent traces
  - At least 2.5× height from the reference plane
- All synchronous modules must have the bus length matching and relative clock length control.
- For the SD module interfaces:
  - Match the data, clock, and CMD trace lengths (length delta depends on the bus rates).
  - Follow similar SDRAM rules for data, address, and control as for the SD module interfaces.
- To enable the i.MX RT1180 FlexSPI module to support QSPI flash, the FlexSPI_DQS pin must be kept floating to achieve high-speed access.

6.10 AC specifications for GPIO_AD or the GPIO_AON bank

Refer to Table 8 for AC specifications of the GPIO_AD/GPIO_AON bank.

Table 8. AC specifications for GPIO_AD/GPIO_AON bank

Serial no.	Characteristic	Condition	Maximum value	Unit
1	f_{max}[1][2]	Cload[1] = 15 pF	104	MHz
		Cload[1][2] = 30 pF	50	
		Cload [1][2]= 150 pF	10	

[1] DSE = 0/1, SRE = 0
[2] If the total Cload (Cap load) is larger than 30 pF, a 20 Ω or larger termination resistor is necessary. The resistor ensures that the Cload I/O drive is not larger than 30 pF.

7 Debugging and programming

This section provides the JTAG interface summary and recommendations for using the JTAG, SWD debug, and Serial Downloader I/O.

Note: *By default, the i.MX RT1180 silicon can use both SWD and JTAG modes using the Arm stitching sequence. The MIMXRT1180-EVK board can use the SWD or JTAG debug without any board modification.*

The MIMXRT1180-EVK also features a MCU-Link circuit, which makes it easier to debug without an external debugger.

Table 9. JTAG interface summary

JTAG signals	I/O type	On-chip termination	External termination
JTAG_TCK	Input	20–50 kΩ pull-down	Not required
JTAG_TMS	Input	20–50 kΩ pull-up	Not required; use 10 kΩ pull-up
JTAG_TDI	Input	20–50 kΩ pull-up	Not required; use 10 kΩ pull-up
JTAG_TDO	3-state output	None	Do not use pull-up or pull down
JTAG_TRSTB	Input	20–50 kΩ pull-up	For the JTAG_TRSTB pin, it is recommended to add a 4.7 kΩ external pulldown resistor for mass production. During the development state, this 4.7 kΩ resistor can be removed. To use other functions on this pin (such as GPIO, Timer), switch JTAG_TCK and JTAG_TMS first, and then switch the setting of JTAG_TRSTB.

Note:

For the on-chip termination values, refer to the i.MX RT1180 Crossover Processors Data Sheet (document IMXRT1180EC). See Section 10.

Table 10. JTAG recommendation

Signals	Recommendation	Description
JTAG_TDO	Do not add external pullup or pulldown resistors on JTAG_TDO.	See Table 9 for a summary of the JTAG interface. This I/O has an on-chip keeper circuit that avoids a floating condition.
JTAG signals other than JTAG_TDO	Ensure that the on-chip pullup/pulldown configuration is followed if external resistors are used with the JTAG signals (except for JTAG_TDO). For example, do not use an external pulldown on an input that has an on-chip pullup.	External resistors can be used with all JTAG signals except for JTAG_TDO, but they are not required. See Table 9 for a summary of the JTAG interface.

Table 11. SWD recommendation

Signals	Recommendation	Description
SWD_DIO	Same practice as JTAG_TMS	The SWD debug port is used by default on the MIMXRT1180-EVK board.
SWD_CLK	Same practice as JTAG_CLK	

The Serial Downloader mode of ROM provides a means to download a program image to the chip over a USB, UART, or LPSPI serial connection. In this mode, a host PC can communicate to the ROM bootloader using a serial download protocol. NXP ROM flashloader also uses these same serial connections. All boards must

make at least one of the Serial Downloader ports (USB1, LPUART1, or LPSPI1) available to use the NXP image and fuse programming enablement.

Table 12. Serial Downloader I/Os table

Signals	Recommendation	Description
USB1	These peripherals can be used as a Serial Downloader. Refer to Serial Boot (Serial Downloader) for more information. To disable all the Serial Downloader peripherals, use the DIS_SERIAL_DWNLD fuse. To disable separately each type of Serial Downloader peripheral, set the DIS_USB_HID_DWNLD, DIS_SPI_WDNLD, and DIS_UART_DWNLD variables.	The ROM polls for the LPUART1, LPSPI1, and USB1 activity circularly until the ROM gets 0x5A, 0xA6 from the LPUART RXD, SPI_SDI, or first HID report from the USB bus. When an active connection port is found, the ROM uses it for the PC downloading.
LPUART1		
LPSPI1		

8 Unused pins recommendations

Table 13 shows the recommended connections for unused analog interfaces.

Table 13. Recommended connections for unused analog interfaces

Module	Ball name	Recommendations if unused
32 kHz oscillator	RTC_XTALI, RTC_XTALO	Not connected If the external crystal is not connected, it is recommended that RTC_XTALI ties to GND.
ADC	ADC_VREFH	10 kΩ resistor to ground
	VDDA_ADC_1P8	10 kΩ resistor to ground
	VDDA_ADC_3P3	10 kΩ resistor to ground
CCM	CLK1_N, CLK1_P	Not connected
DAC	DAC_OUT	Not connected
DC-DC	DCDC_IN, DCDC_IN_Q, DCDC_DIG, DCDC_1V8	Not connected
	DCDC_SENSE, DCDC_LP, DCDC_LN	Not connected
	DCDC_PSWITCH, DC-DC_ MODE	To ground
USB	USB1_DN, USB1_DP, USB1_VBUS, USB2_DN, USB2_DP, USB2_VBUS	Not connected
	VDD_USB_1P8	Tie directly to power; capacitors are not required.
	VDD_USB_3P3	Tie directly to power; capacitors are not required.
SYS OSC	XTALI, XTALO	Not connected

Note: *Tie unused digital IOs to low level or configure these signals to pull down.*

9 Acronyms

Table 14 lists the acronyms used in this document.

Table 14. Acronyms

Acronym	Description
AVB	Audio Video Bridging
AON	Always on (domain)
ADC	Analog-to-Digital Converter
BBSM	Battery Backed Secure Module
CLK	Clock
EtherCAT	Ethernet for Control Automation Technology
EEPROM	Electrically Erasable Programmable Read-only Memory
Flex-SPI	Flexible Serial Peripheral Interface
GPIO	General-Purpose Input/Output
HID	Human Interface Device
I2C	Inter-Integrated Circuit
I3C	Improved inter-Integrated circuit
JTAG	Joint Test Action Group
LDO	Low-Dropout Regulator
LPI2C	Low-Power Inter-Integrated Circuit (I2C)
LPSPI	Low-Power Serial Peripheral Interface
MII	Media-Independent Interface
MCU	Microcontroller Unit
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuit
RGMII	Reduced Gigabit Media-Independent Interface
RMII	Reduced Media-Independent Interface
SDRAM	Synchronous Dynamic Random Access Memory
SEMC	Smart External Memory Controller
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver Transmitter
TSN	Time Sensitive Network
USB	Universal Serial Bus

10 References

For more information, refer to the following documents:

- *i.MX RT1180 Crossover Processors Data Sheet* (document IMXRT1180EC)
- *i.MX RT1180 Processor Reference Manual* (document IMXRT1180RM)
- *MIMXRT1180-EVK User Manual* (document UM12021)
- For *AN PHY Selection Guide. Requirements to Ethernet PHYs used for EtherCAT and EtherCAT G Ethernet PHY Examples*. (See Beckhoff website).
- For examples demonstrating the procedure to design external RC components of ADC, refer to the Application Note *Cookbook for SAR ADC Measurements, ADC measurements done properly* (document AN4373).
- To implement an external PMIC on i.MX RT1180 MCU, refer to the document *'Using i.MX RT117x Processor with PF5020 PMIC for Auto Application'* (document AN13213).

Additional documents and design resources are available on the URLs below:

- i.MX RT1180
- MIMXRT1180-EVK
- MIMXRT1180-EVK design file

Note: *Some of the documents listed above are NXP confidential. For access to these documents, consult your local Field Application Engineer (FAE).*

11 Revision history

Table 15 summarizes the revisions to this document.

Table 15. Revision history

Document ID	Release date	Description
UG10098 v.4.0	12 February 2026	Added a Note and an image Figure 2 in the topic, Section 2.2.
UG10098 v.3.0	16 July 2025	Added Section 6.10
UG10098 v.2.0	26 June 2025	First public release
UG10098 v.1.0	18 July 2024	Preliminary release

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