NPS7601

WLCSP parallelable 1.5 V to 5.5 V, 1.5 A, low Iq load switch with true reverse current blocking

Rev. 1 — 24 November 2025 Product data sheet

1. General description

The NPS7601 is a compact, single-channel, regulated forward-drop load switch with always-on, true reverse current blocking capabilities. It provides efficient switching between power rails, minimizing power loss and enabling precise load control.

The NPS7601 operates across an input voltage range of 1.5 V to 5.5 V, and supports up to 1.5 A of continuous current. An active-high enable (EN) input controls its operation, allowing for isolation of the load by blocking current in both directions when the pin is held low. When EN is asserted high and the input voltage exceeds the output, the NPS7601 turns on in a controlled manner, managing inrush current to prevent voltage droop on the power source.

To achieve fast-acting, true reverse current blocking with minimal transient reverse current, the device utilizes a regulated forward voltage scheme. This active control method overcomes the limitations of common IN-to-OUT voltage comparator-based solutions, which often require hundreds of milliamps before activation.

The NPS7601 is suitable for various applications, including:

- Power supply sequencing
- Power supply multiplexing
- Power supply OR-ing
- Parallel operation for high-current loads

NPS7601 is offered in a compact WLCSP4 (SOT8113) package and is qualified for operation over an ambient temperature range of -40 °C to 125 °C.

2. Features and benefits

- Input voltage range: 1.5 V to 5.5 V
- Maximum continuous current: 1.5 A
- Low quiescent current (I_Q): 600 nA (typ)
- Low shutdown current (I_{SD}): 120 nA (typ)
- Reverse leakage current: -220 nA (out of the IN pin)
- True reverse current blocking
  - $V_{IN} \geq 1.5$ V (with EN is HIGH and $V_{OUT} \geq V_{IN}$)
  - $V_{IN} = 0$ V (when $V_{OUT} \geq V_{IN}$)
- Controlled rise time at start-up
- Over-temperature protection
- Short-circuit protection
- SOT8113, 4-pin wafer-level chip-scale package
- Ambient temperature range (T_a): -40 °C to +125 °C

3. Applications

- Consumer electronics
- Wearables
- IoT devices
- Battery powered and battery backup systems
- USB powered devices

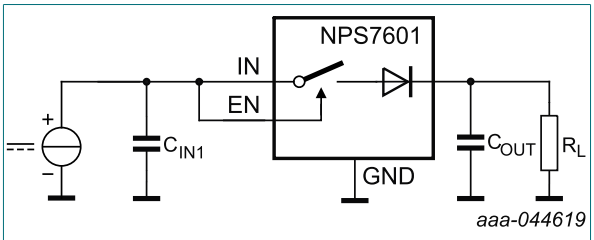


Fig. 1. Simplified application

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NPS7601UP	-40 °C to +125 °C	WLCSP4	plastic surface-mounted package; 4-pin	SOT8113

5. Marking

Table 2. Marking code

Type number	Marking code
NPS7601UP	sG

6. Functional diagram

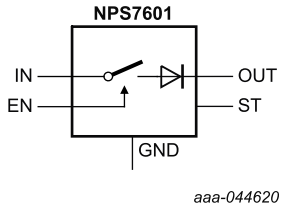


Fig. 2. Logic symbol

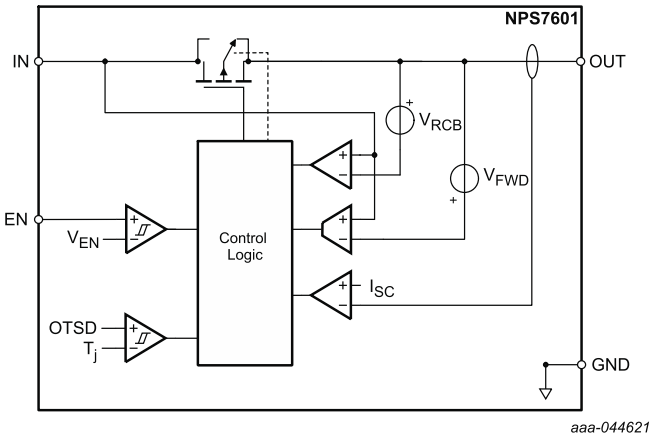


Fig. 3. Functional diagram

7. Pin configuration and description

7.1. Pin configuration

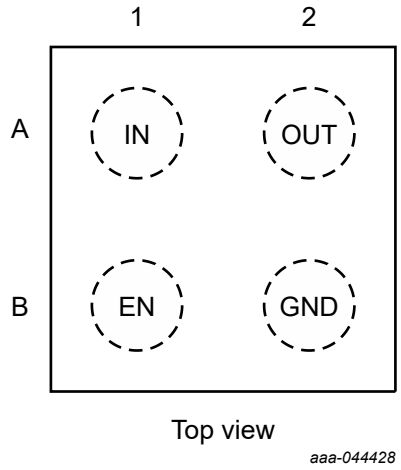


Fig. 4. Pin configuration SOT8113 (WLCSP4)

7.2. Pin description

Table 3. Pin description

Symbol	Pin	I/O	Description
IN	A1	I	Input connection of the load switch. Connect to a power supply. Bypass with a low ESR capacitance of at least 0.1 µF.
OUT	A2	O	Output connection of the load switch. Connect to the load. Bypass with a low ESR capacitance of at least 0.33 µF.
EN	B1	I	Active high enable input to the IC. Connect to IN to permanently enable the device. Connect to GND to disable. Connect EN to an I/O to control it. Do not leave this pin floating.
GND	B2	GND	Ground (0 V)

8. Specifications

8.1. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	input voltage		-0.3	6	V
V_{OUT}	output voltage		-0.3	6	V
V_{EN}	EN pin voltage		-0.3	6	V
I_{OUT}	continuous load current		internally limited		A
T_j	junction temperature		-40	150	°C
T_{stg}	storage temperature		-65	150	°C

8.2. ESD ratings

Table 5. ESD ratings

Symbol	Parameter	Conditions	Value	Unit
V_{ESD}	electrostatic discharge	HBM: ANSI/ESDA/JEDEC JS-001 class 2	±2000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C2a	±500	V

8.3. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	input voltage		1.5	5.5	V
V_{OUT}	output voltage		0	5.5	V
I_{OUT}	max continuous output current	>2.0 V input	-	1.5	A
		1.6 V to 1.9 V		0.5	A
		1.5 V		50	mA
$I_{OUT,SW}$	maximum pulsed switch current	≤120 ms, 2% duty-cycle, V_{IN} = 3.3 V/5.0 V	-	2	A
V_{EN}	EN Pin voltage		0	5.5	V

8.4. Recommended components

Table 7. Recommended components

Nominal component values, derating factors not included.

Symbol	Parameter		Min	Nom	Max	Unit
C_{IN}	capacitance on IN	[1]	0.1	1	-	µF
C_{OUT}	capacitance on OUT	[2][3]	0.33	0.47	-	µF

[1] An input capacitor is required for proper operation.
[2] An output capacitor is required for proper operation.
[3] See Section 10.8 for the detailed guidance on appropriately sizing the output capacitor.

8.5. Thermal information

Table 8. Thermal information

Thermal resistance according to JEDEC51-5 and -7

Symbol	Parameter	SOT8113	Unit
$R_{\Theta JA}$	junction-to-ambient thermal resistance	173	°C/W
Ψ_{JT}	junction-to-top characterization parameter	5	°C/W

8.6. Electrical characteristics

Table 9. Static characteristics

V_{IN} = 3.6 V, V_{EN} = 3.6 V, C_{OUT} = 0.33µF unless otherwise specified.

Symbol	Parameter	Conditions	T_a = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
Input						
$I_{IN,Q}$	input quiescent current	$V_{EN} = V_{IN}$	-	600	1100	nA
$I_{IN,SD}$	input shutdown current	EN = LO	-	120	430	nA
Pass FET						
V_{FWD}	forward voltage drop	V_{IN} = 1.5 V; I_O= 50 mA	-	21	50	mV
		V_{IN} = 3.6 V; I_O= 100 mA	-	29	52	mV
		V_{IN} = 3.6 V; I_O= 500 mA [2]	-	55	72	mV
		V_{IN} = 3.6 V; I_O= 1000 mA [2]	-	110	155	mV
		V_{IN} = 5.5 V; I_O= 100 mA	-	31	50	mV
Reverse current blocking						
V_{RCBA}	RCB activation voltage	$V_{OUT} - V_{IN}$	-	31	-	mV
V_{RCBD}	RCB deactivation voltage	$V_{IN} - V_{OUT}$	-	41	-	mV
$I_{IN,LKGE}$	leakage current into IN, enabled	V_{OUT} = 4 V [2]	-220	331	615	nA
		V_{OUT} = 5 V	-220	332	615	nA
$I_{OUT,LKGE}$	leakage current into OUT, enabled	V_{OUT} = 4 V [2]	-200	372	1200	nA
		V_{OUT} = 5 V	-200	449	1200	nA
$I_{IN,LKGD}$	leakage current into IN, disabled	V_{OUT} = 4 V; EN = LO [2]	-500	-	500	nA
		V_{OUT} = 5 V; EN = LO	-500	-	500	nA
Enable input						
$V_{EN,HI}$	enable high threshold		1.2	-	-	V
$V_{EN,LO}$	enable low threshold		-	-	0.4	V
$V_{EN,HYS}$	enable hysteresis		-	45	-	mV
$I_{EN,HI}$	enable input current	V_{EN} = 3.6 V	-	-	50	nA
Short-circuit protection						
I_{LIM}	over current limit	R_L = 100 mΩ	-	2.2	-	A
Over-temperature shutdown						
T_{OTSD}	over-temperature shut down	T_j rising [2]	170	175	-	°C
T_{OTHYS}	over-temperature hysteresis	T_j falling [2]	-	35	-	°C

[1] All typical values are measured at T_{amb} = 25 °C.
[2] *Not tested in production. Obtained by characterization.*

8.7. Dynamic characteristics

Table 10. Dynamic characteristics

V_{IN} = 3.6 V, C_{OUT}= 1 µF, R_L = open unless otherwise specified.

Symbol	Parameter	Conditions	T_a = 25 °C			Unit
			Min	Typ	Max	
$t_{ON,DLY}$	turn-on delay time	V_{EN} = LO to HI step to V_{OUT} = 10 %	-	660	-	µs
t_{RISE}	rise time	V_{OUT} = 10 % to V_{OUT} = 90%	-	100	-	µs
t_{RCB}	reverse current blocking time	V_{OUT} = V_{IN}-100 mV to V_{IN} +100mV step to I_{IN} <1 mA [1]	-	20	-	µs
t_{LIM}	current limit response time	OUT shorted with 100 mΩ to I_{OUT} within 10% of I_{LIM} [1]	-	35	-	µs

[1] *Not tested in production. Obtained by characterization.*

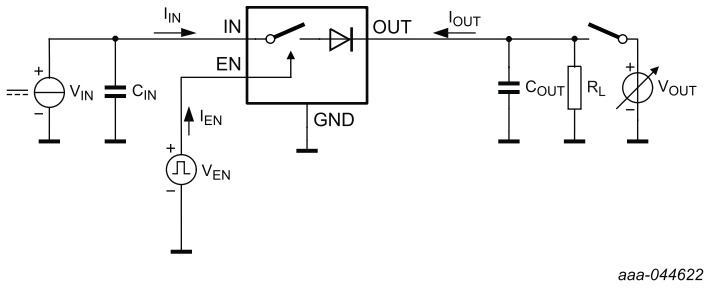


Fig. 5. Test circuit

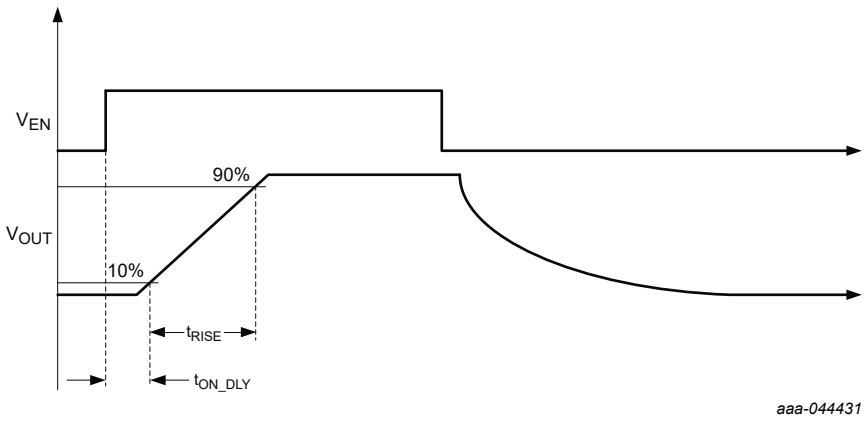
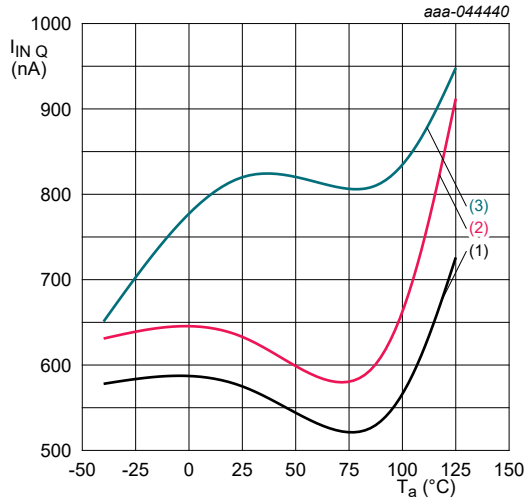


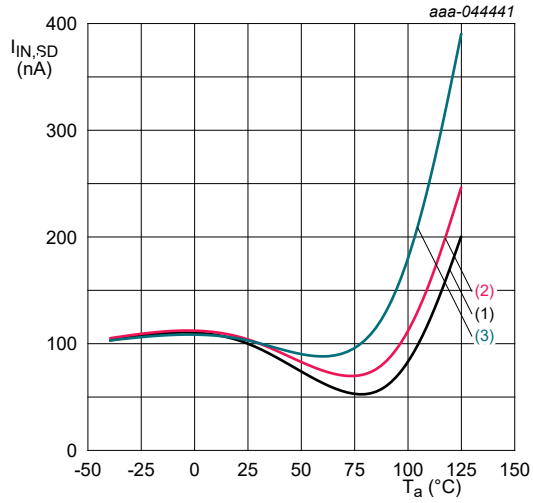
Fig. 6. Timing diagrams

8.8. Typical characteristics



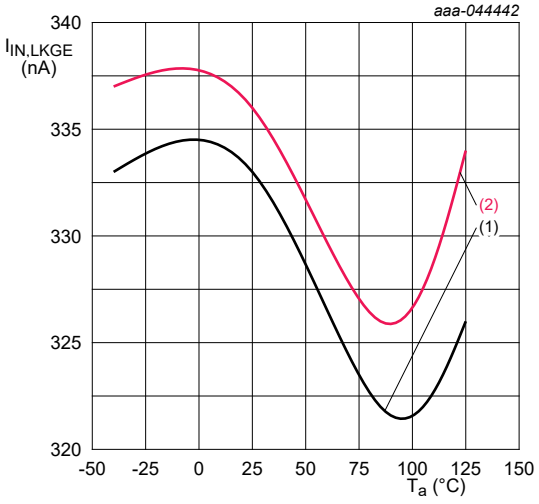
1) V_{IN} = 1.5 V
2) V_{IN} = 3.6 V
3) V_{IN} = 5.5 V

Fig. 7. Input quiescent current ($I_{IN,Q}$) versus ambient temperature



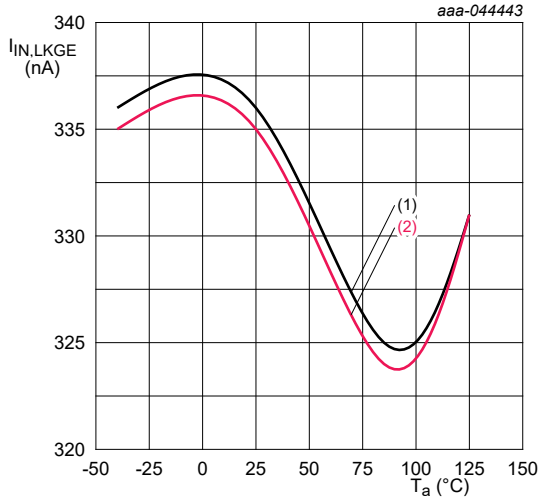
1) V_{IN} = 1.5 V
2) V_{IN} = 3.6 V
3) V_{IN} = 5.5 V

Fig. 8. Input shutdown current ($I_{IN,SD}$) versus ambient temperature



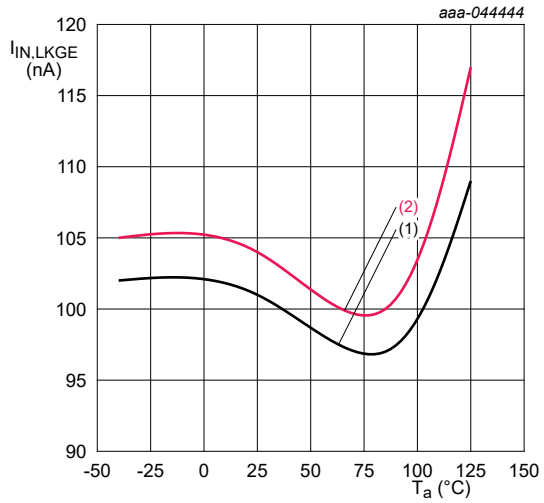
1) V_{IN} = 1.5 V
2) V_{IN} = 3.6 V

Fig. 9. Input leakage current, enabled, ($I_{IN,LKGE}$) ambient temperature at V_{OUT} = 4 V



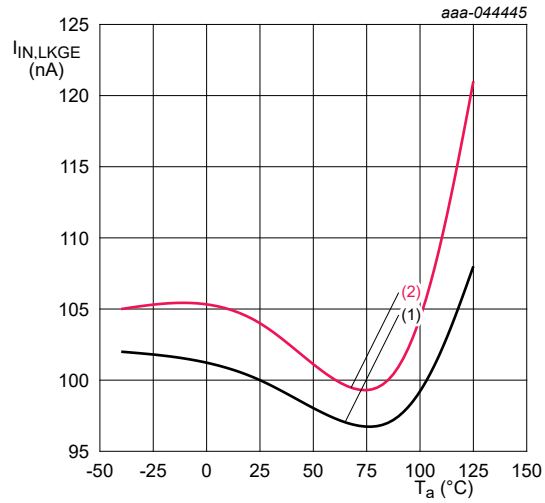
1) V_{IN} = 1.5 V
2) V_{IN} = 3.6 V

Fig. 10. Input leakage current, enabled, ($I_{IN,LKGE}$) versus ambient temperature at V_{OUT} = 5 V



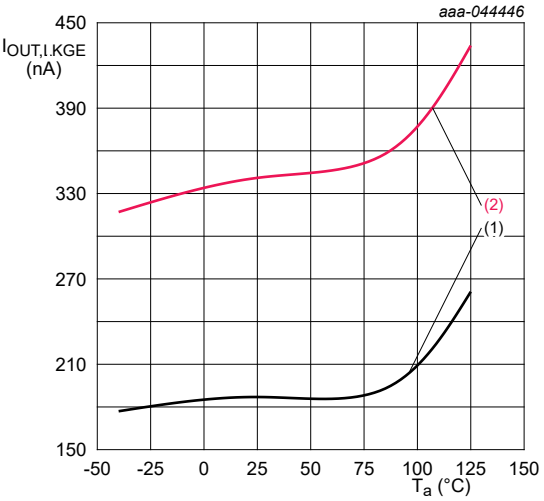
1) V_{IN} = 1.5 V
2) V_{IN} = 3.6 V

Fig. 11. Input leakage current, disabled, ($I_{IN,LKGD}$) versus ambient temperature at V_{OUT} = 4 V



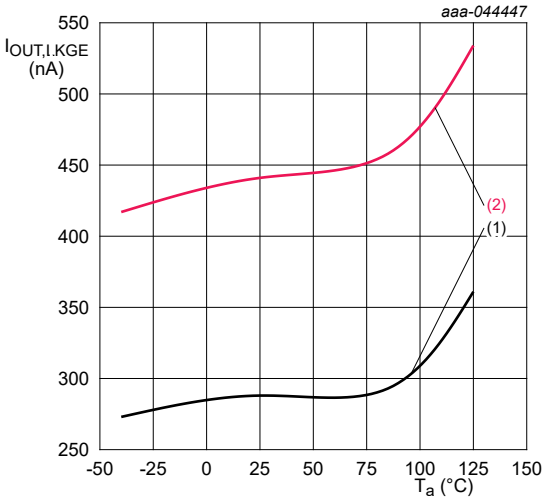
1) V_{IN} = 1.5 V
2) V_{IN} = 3.6 V

Fig. 12. Input leakage current, disabled, ($I_{IN,LKGD}$) versus ambient temperature at V_{OUT} = 5 V



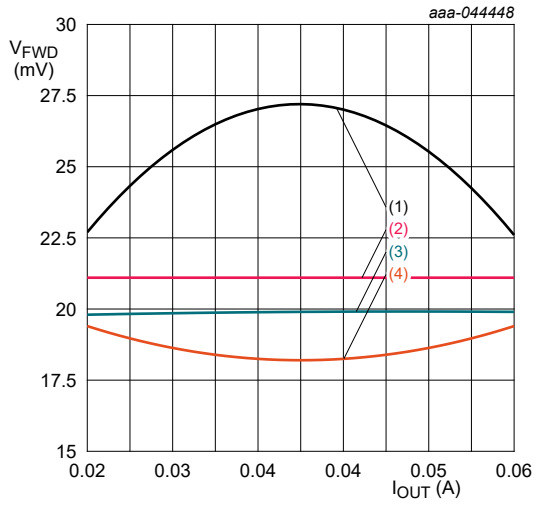
1) V_{IN} = 1.5 V
2) V_{IN} = 3.6 V

Fig. 13. Output leakage current, enabled, ($I_{OUT,LKGE}$) versus ambient temperature at V_{OUT} = 4 V



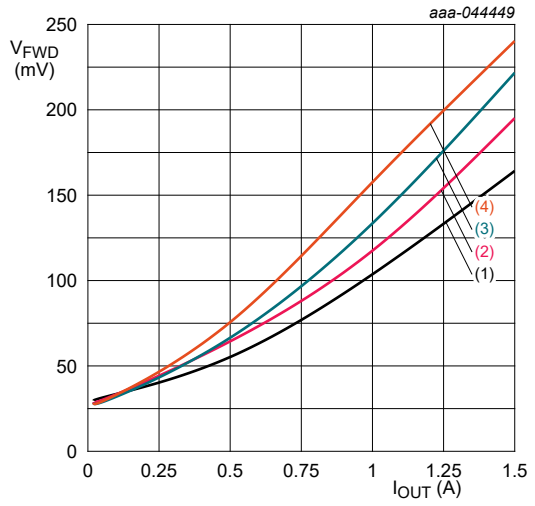
1) V_{IN} = 1.5 V
2) V_{IN} = 3.6 V

Fig. 14. Output leakage current, enabled, ($I_{OUT,LKGE}$) versus ambient temperature at V_{OUT} = 5 V



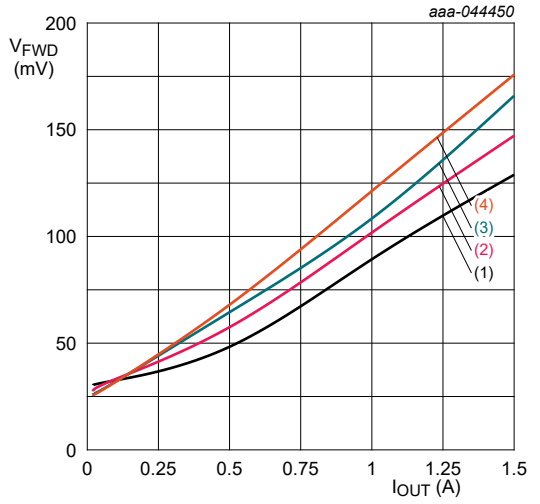
1) T_a = -40 °C
2) T_a = 25 °C
3) T_a = 85 °C
4) T_a = 125 °C

Fig. 15. Forward voltage drop versus load current at V_{IN} = 1.5 V



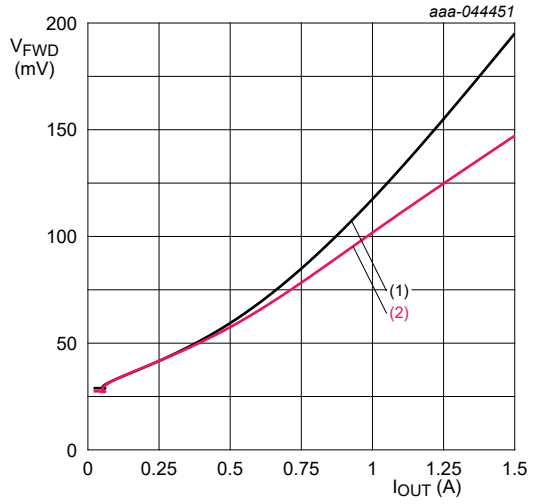
1) T_a = -40 °C
2) T_a = 25 °C
3) T_a = 85 °C
4) T_a = 125 °C

Fig. 16. Forward voltage drop versus load current at V_{IN} = 3.6 V



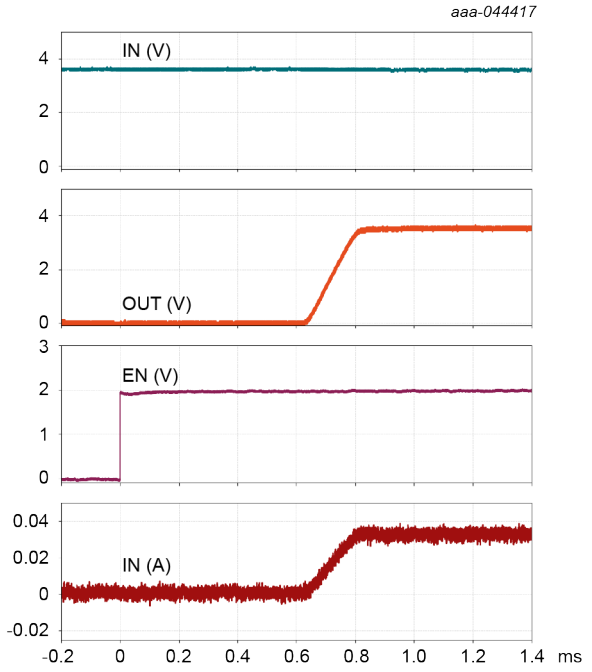
1) T_a = -40 °C
2) T_a = 25 °C
3) T_a = 85 °C
4) T_a = 125 °C

Fig. 17. Forward voltage drop versus load current at V_{IN} = 5 V



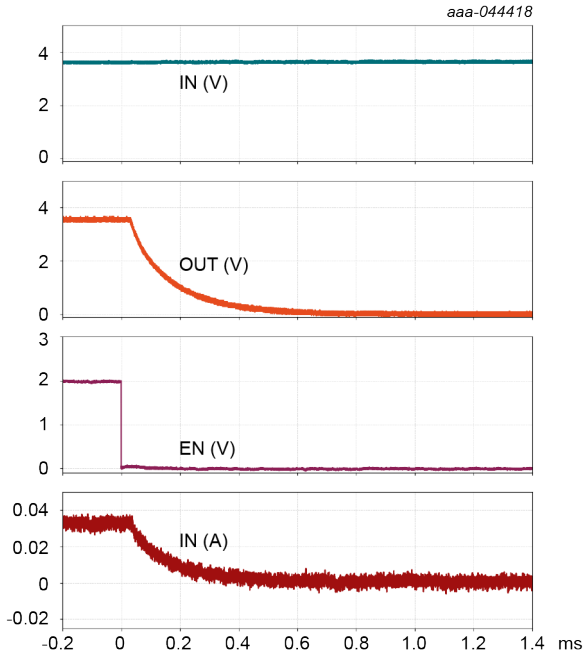
1) V_{IN} = 3.6 V
2) V_{IN} = 5.5 V

Fig. 18. Forward voltage drop versus load current at T_a = 25 °C



- R_L = 120 Ω
- V_{IN} = 3.6 V

Fig. 19. Start-up with enable



- R_L = 120 Ω
- V_{IN} = 3.6 V

Fig. 20. Shutdown with enable

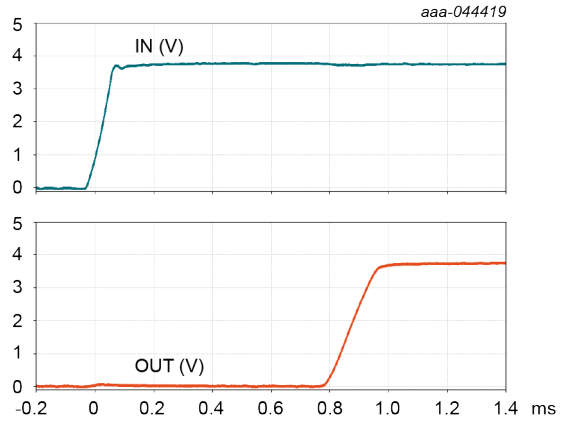


Fig. 21. Start-up with V_{IN} (V_{IN} ramp from 0 V to 3.6 V in 100 µs, EN tied to V_{IN}, R_L = 120 Ω)

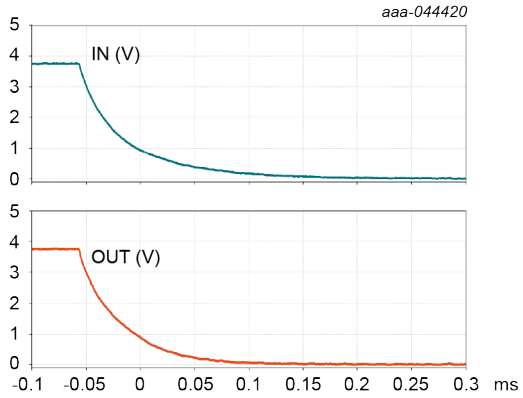
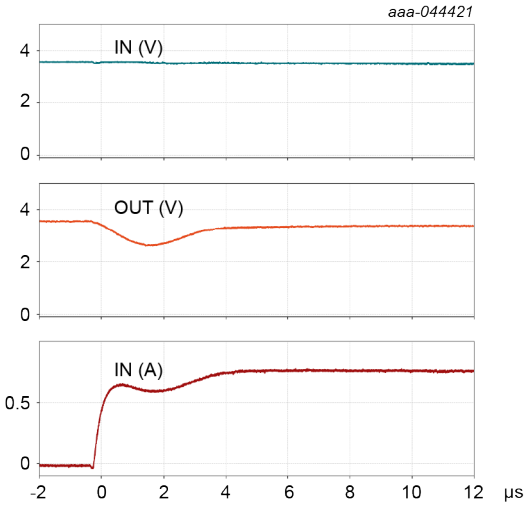
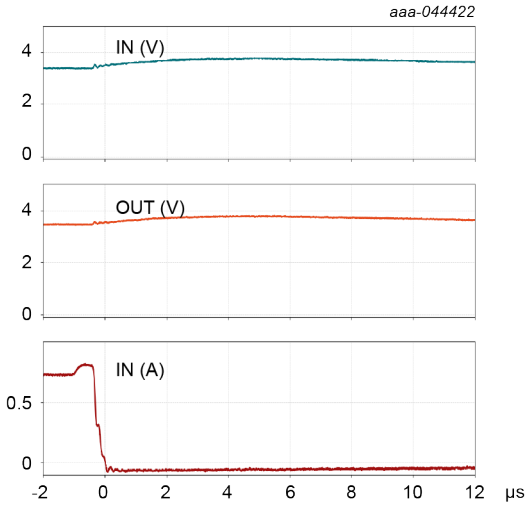


Fig. 22. Shutdown with V_{IN} (V_{IN} ramp from 3.6 V to 0 V in 100 µs, EN tied to V_{IN}, R_L = 120 Ω)



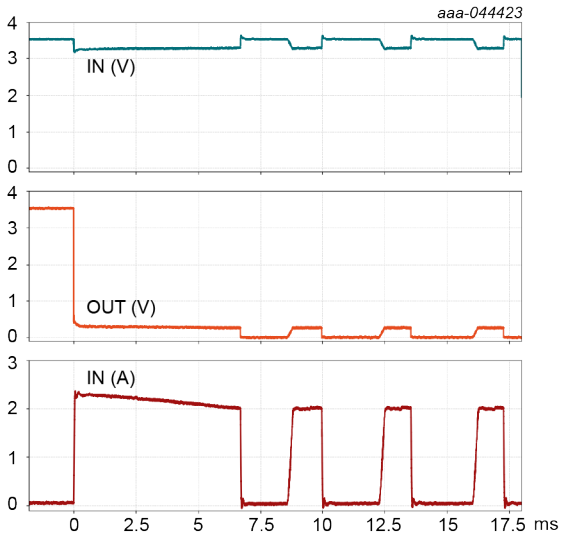
- V_{IN} = 3.6 V

Fig. 23. Load step response (I_{OUT} step from 0 A to 0.75 A)



- V_{IN} = 3.6 V

Fig. 24. Load step response (I_{OUT} step from 0.75 A to 0 A)



- V_{IN} = 3.6 V
- C_{IN} = 100 µF
- Output shorted with 0.1 Ω resistor

Fig. 25. Short circuit response

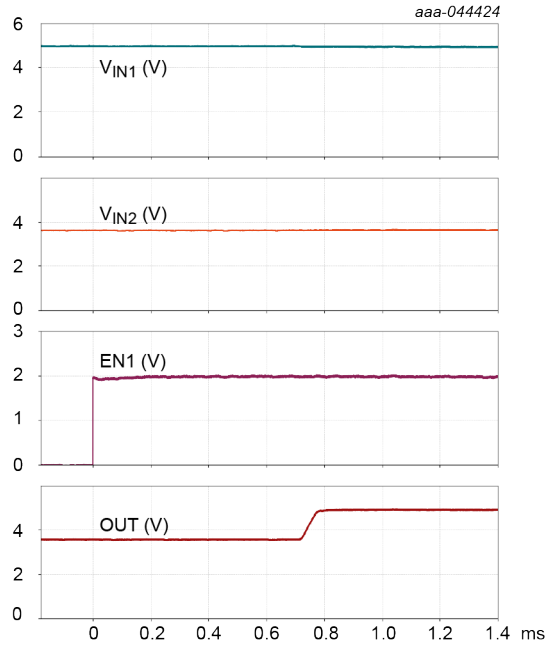


Fig. 26. OR-ing with enable (V_{IN1} = 5 V, V_{IN2} = 3.6 V; EN1 Low to High transition, EN2 tied to V_{IN2})

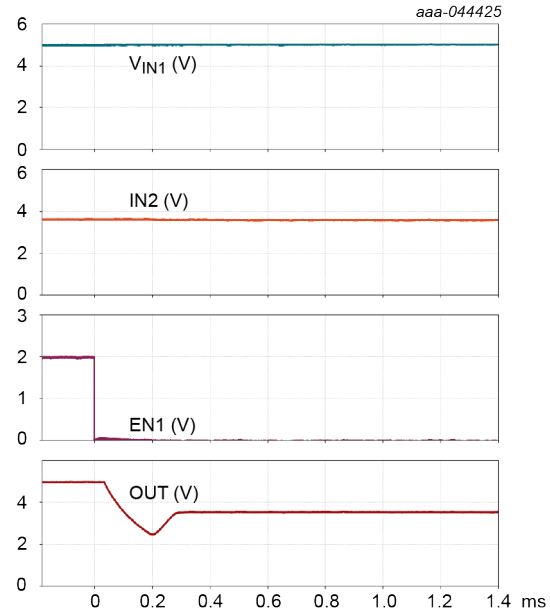


Fig. 27. OR-ing with enable (V_{IN1} = 5 V, V_{IN2} = 3.6 V; EN1 High to Low transition, EN2 tied to V_{IN2})

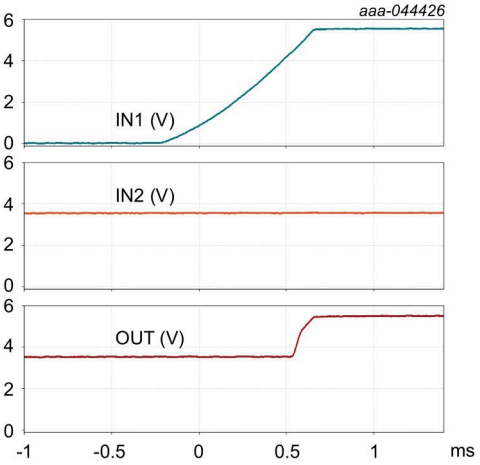


Fig. 28. OR-ing with V_{IN} (V_{IN1} = 0 V to 5 V in 1 ms, V_{IN2} = 3.6 V; EN1 tied to V_{IN1}, EN2 tied to V_{IN2})

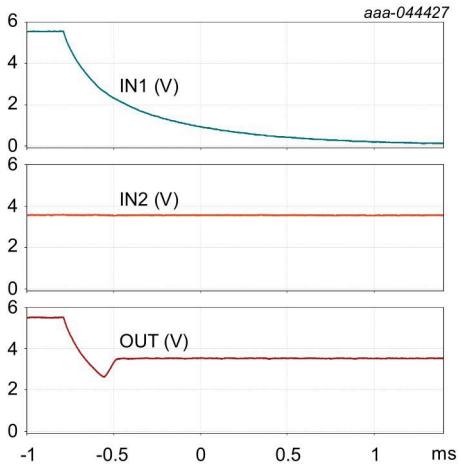


Fig. 29. OR-ing with V_{IN} (V_{IN1} = 5 V to 0 V in 1 ms, V_{IN2} = 3.6 V; EN1 tied to V_{IN1}, EN2 tied to V_{IN2})

9. Functional description

NPS7601 implements a regulated P-channel MOSFET to achieve a low forward voltage drop from its input to its output. This regulated control scheme is designed to overcome the limitations of traditional comparator-based reverse current blocking, which can allow hundreds of milliamps of reverse current to flow before activation.

The device integrates key protection features, including over-temperature protection and reverse current blocking. For enhanced safety, its reverse current blocking is always active, even when the input voltage (V_{IN}) is 0 V. During shutdown, the device has very low leakage currents, which minimizes power consumption to downstream modules during standby.

9.1. Startup

The device starts when the voltage at either IN or OUT pins reaches 1.5 V. Until then, there is insufficient voltage to power up the internal circuitry.

When V_{IN} exceeds 1.5 V, V_{OUT} < V_{IN}, and EN is low, the device enters Power-On-Reset (POR). In this situation, the switch is held OFF and the body diode is oriented such that the anode is at OUT and cathode is at IN. If EN pin goes high, the IC starts charging the output capacitor with an internally controlled slew rate. Once the capacitor is fully charged, the internal FET's gate is controlled by a transconductance amplifier to maintain a constant difference between V_{IN} and V_{OUT} to minimize the power loss. If EN is pulled low at any time, the FET is turned OFF.

9.2. Functional modes

Table 11 summarizes the various functional modes of NPS7601 and the status of the switch in each mode.

Table 11. Device functional modes (V_{IN} ≥ 1.5 V)

V_{IN}	Functional mode	EN pin	Power device state
V_{IN} ≥ 1.5 V	OFF	LOW	OFF: forward and reverse voltage blocking
	ON	HIGH	ON: forward conduction regulated V_{FWD}
	Reverse current blocking V_{OUT} > V_{IN}	X	OFF: reverse blocking
	Output short	HIGH	ON: forward conduction regulated I_{OUT}
	Thermal fault	HIGH	OFF: reverse blocking
V_{IN} = 0 V	OFF	X	OFF: reverse voltage blocking

The forward voltage drop of NPS7601 depends on the input voltage and load current. Fig. 30 shows the internal block diagram of the NPS7601 in forward regulation mode. Based on this figure, the drop seen between the IN and OUT pins (V_{FWD}) is given by the equation

$$V_{FWD} = I_{OUT} \times \left(R_{BP1} + R_{BP2}\right) + V_{FET}$$

where I_{OUT} is the load current, R_{BP1} and R_{BP2} are the bond pad impedances and V_{FET} is the voltage drop across the FET.

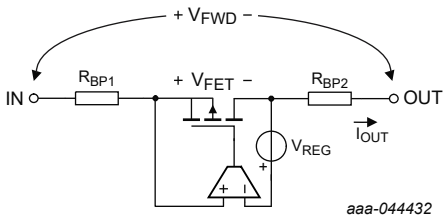


Fig. 30. NPS7601 regulation scheme

The voltage drop across the FET is regulated to V_{REG} until the load current increases to a point where

$$I_{OUT} = \frac{V_{REG}}{R_{ON}}$$

Where R_{ON} is the resistance of the FET.

The overall variation of the forward voltage incorporating all these effects is shown in Fig. 31.

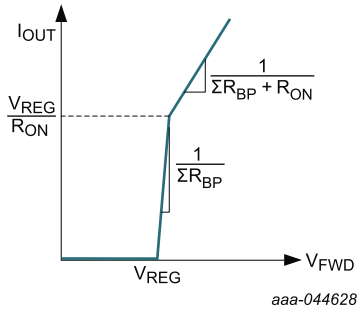


Fig. 31. NPS7601 I-V curve

9.3. Reverse current blocking

Reverse Current Blocking (RCB) protection is always active, regardless of the state of EN. This protects the power supply from having to sink currents.

Two scenarios can activate the reverse current blocking functional mode:

- Output voltage starts rising and exceeds the input voltage (eg: OR-ing with two different voltage levels)
- Input voltage starts falling and goes below the output voltage (eg: loss of input power)

In either case, NPS7601 tries to maintain the forward drop between V_{IN} and V_{OUT}. As the V_{IN}-V_{OUT} differential starts reducing, the transconductance amplifier modulates the gate of the FET to increase its resistance to maintain the $V_{IN} – V_{OUT}$ differential. Once $V_{IN} \leq V_{OUT}$, the transconductance amplifier turns off the pass transistor and prevents reverse currents. An internal comparator detects when $V_{IN} \leq V_{OUT} - V_{RCBA}$ and flips the body diode polarity to ensure that the diode remains reverse biased.

When V_{IN} starts rising (or V_{OUT} starts falling) and V_{IN} exceeds $V_{OUT} + V_{RCBD}$, the body diode polarity is flipped such that the anode is at IN and the pass FET starts conducting.

In case of an extremely fast transition from forward conduction to reverse bias, the comparator also acts to turn off the pass transistor before the transconductance amplifier has a chance to react.

9.4. Output overload and temperature protection

The NPS7601 is protected from output short-circuit and over-temperature conditions. When the output current exceeds I_{LIM}, NPS7601 limits the current through the device to I_{LIM}. It stays in this current regulation mode until the output overload condition disappears or the junction temperature of the part exceeds T_{OTSD}.

An example of this behavior is illustrated in a waveform diagram in Fig. 32.

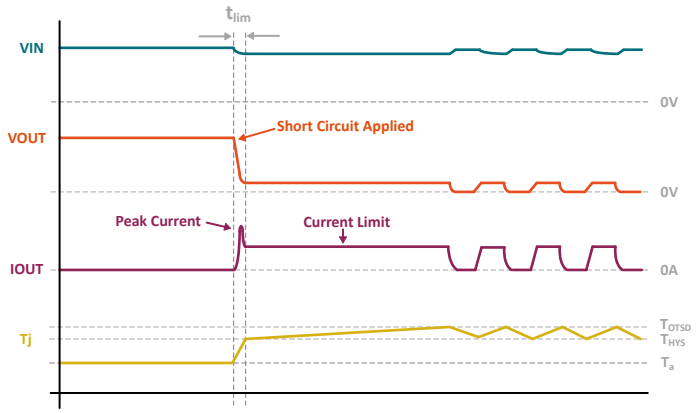


Fig. 32. NPS7601 current limiting and over-temperature shut down

Once an over-temperature condition is detected, NPS7601 turns off the pass transistor. When the NPS7601 cools down such that $T_j < T_{OTSD} - T_{HYS}$, the part attempts restart in an inrush-controlled manner.

10. Application information

The NPS7601 load switch is a versatile device suitable for high side power switching, protecting against reverse current conditions, OR-ing and simple power multiplexing. The following sections provide application examples to aid the design of products using NPS7601.

Please note that application implementation information in the following sections is not part of the Nexperia component specification. Nexperia's device users are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1. Power multiplexing and load switching

As NPS7601 has forward voltage blocking, it is possible to use a single device as a high side load switch with short-circuit protection or multiple devices for power multiplexing.

Fig. 33 depicts an application example that can be used to switch between a USB-PD source, a wall wart, and a Li-ion battery.

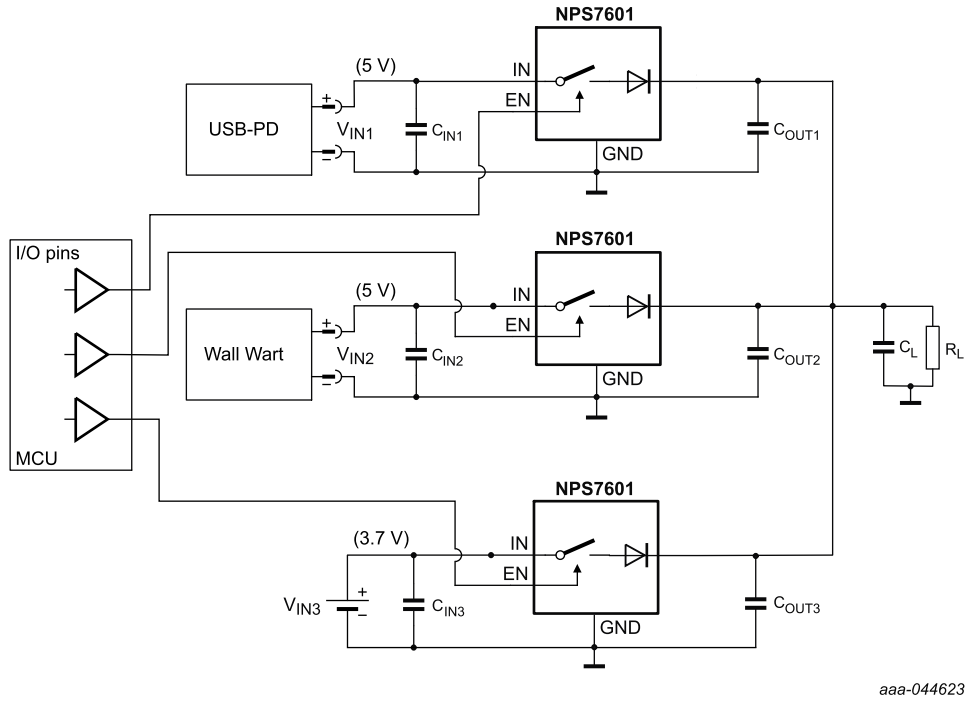


Fig. 33. Power multiplexing and load switching

10.2. Power sequencing

Using load switches for power sequencing helps control the order in which different parts of a system receive power. This process is crucial for preventing damage and malfunction in systems with multiple voltage rails or sensitive components, as it manages inrush current during startup.

The NPS7601 can manage this sequence without external control signals. A staggered power-up sequence is created by connecting the output of one NPS7601 (U1) to the enable pin of a second NPS7601 (U2). This ensures that the load connected to U1 is powered on before the load connected to U2.

As shown in the circuit diagram in Fig. 34, the first load switch turns on, and its output voltage becomes available after a turn-on delay ($t_{ON,DLY}$). Once this voltage rises above the enable threshold level ($V_{EN,HI}$), it triggers the second load switch to turn on.

For applications requiring a longer delay, an RC (resistor-capacitor) circuit can be added to increase the turn-on time.

The results of this power sequencing are shown in the waveform diagram in Fig. 35.

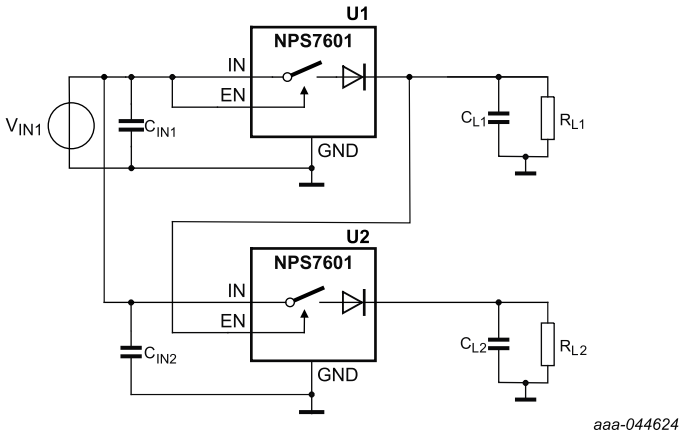


Fig. 34. Power sequencing diagram

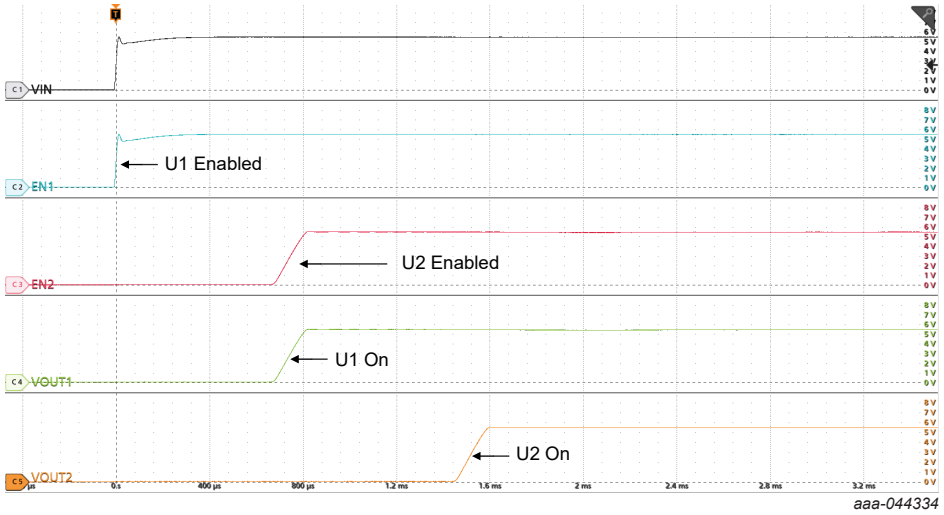


Fig. 35. Power sequencing results

10.3. n+1 OR-ing using load switches

There is no specific limitation to the number of NPS7601 load switches used for power OR-ing. The example below illustrates a common two power supply scenario with smooth transitions between supplies.

Some devices operate from a fixed power supply such as a standard 5 V USB port output in normal conditions but must quickly transition to a 1.5 V battery backup when the power supply is disabled or unplugged. Using two NPS7601 devices in a power OR-ing configuration, the downstream load remains uninterrupted when either the DC supply or the backup battery are disconnected.

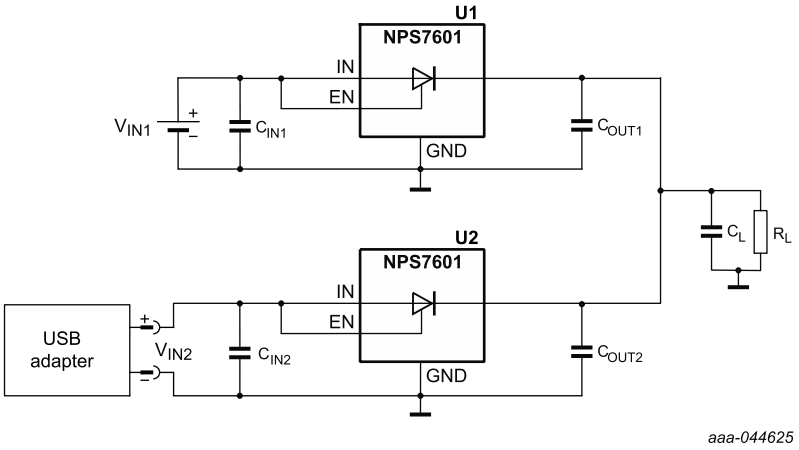


Fig. 36. OR-ing power supply and battery

The scope capture shows the output voltage (V_{OUT}) being initially powered by V_{IN1} at 5 V. When V_{IN1} is removed, V_{IN2} at 1.5 V powers V_{OUT}. When V_{IN1} is reconnected, V_{OUT} is once again powered by V_{IN1}.

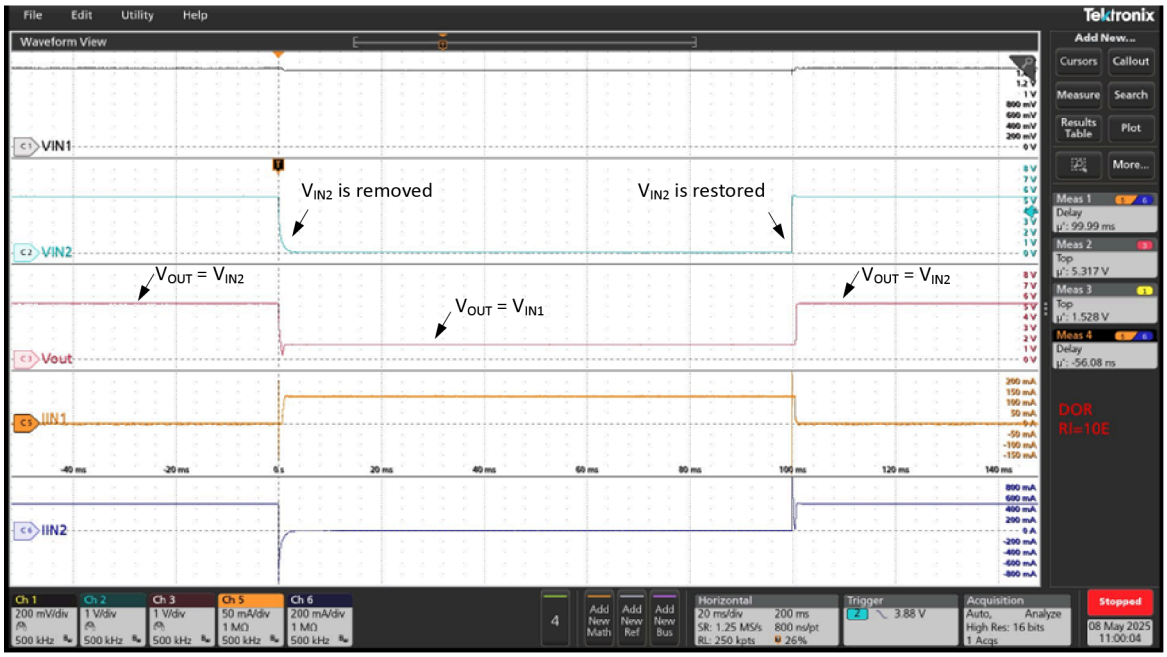


Fig. 37. Waveforms showing OR-ing behavior

10.4. n+1 OR-ing using NPS7601 and conventional diodes

When voltage drops and electrical losses of one of two power sources is not of concern, a combination of load switches and conventional diodes can be implemented as shown in Fig. 38. In this example the AC-DC adapter is the primary power source supplying 5 V to the system with three alkaline cells providing a 4.5 V backup. As stated in Section 8.6, consideration should be given to the V_F rating of the Schottky diode as well as worst case tolerances of the supply voltages to ensure seamless transitions.

A resistor, R_{PD}, connected to ground in the Schottky diode path is recommended to prevent diode reverse leakage during blocking conditions from charging C_{IN1} and raising V_{IN1}.

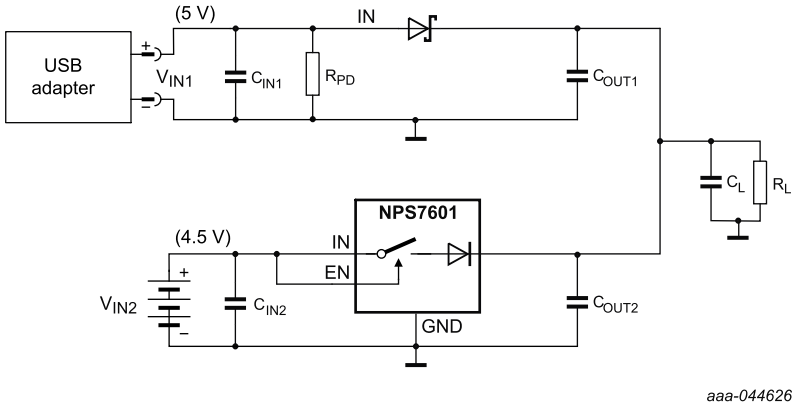


Fig. 38. OR-ing behavior with a combination of load switch and Schottky diodes

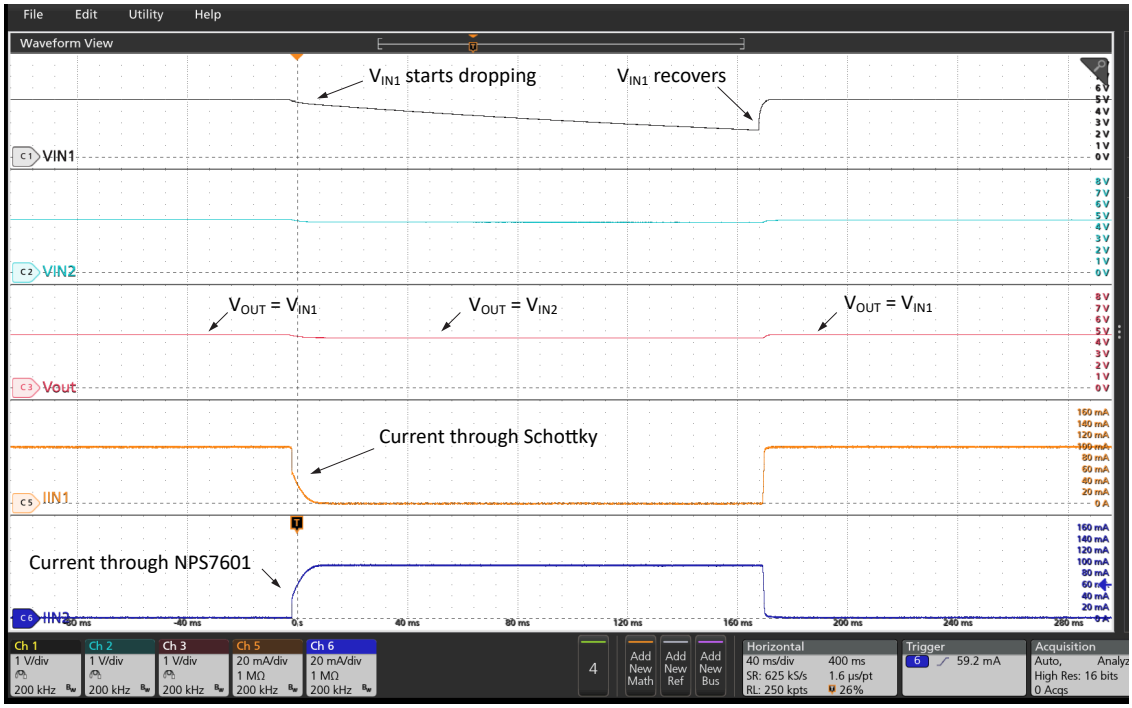


Fig. 39. Waveforms showing OR-ing behavior with a combination of load switch and Schottky diode (PMEG4010)

10.5. Paralleling NPS7601 for thermal and sustained high current considerations

As with using any power semiconductor component, thermal ratings must be observed to maintain device reliability (see Section 8.5). System thermal analysis should be performed to ensure the device junction temperature, T_J, remains below 125 °C under all operating conditions. If analysis shows that using a single NPS7601 can cause a thermal violation, two NPS7601s can be paralleled to share the load current and lower internal power dissipation as shown in Fig. 40. Fig. 41 shows two NPS7601s supporting a combined 2 A load current with 1 A current flowing in each NPS7601.

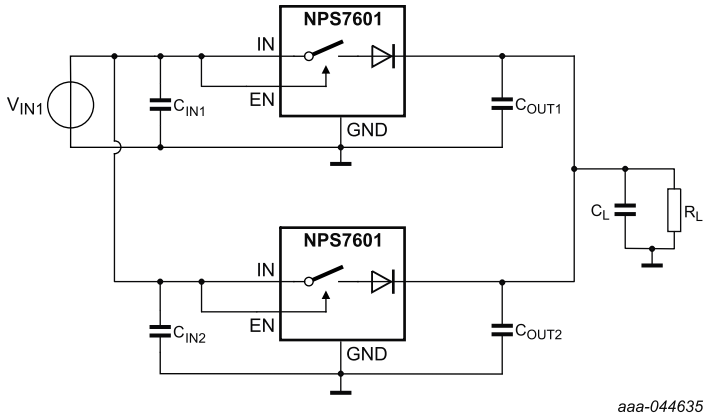


Fig. 40. Paralleling two NPS7601 load switch for high current

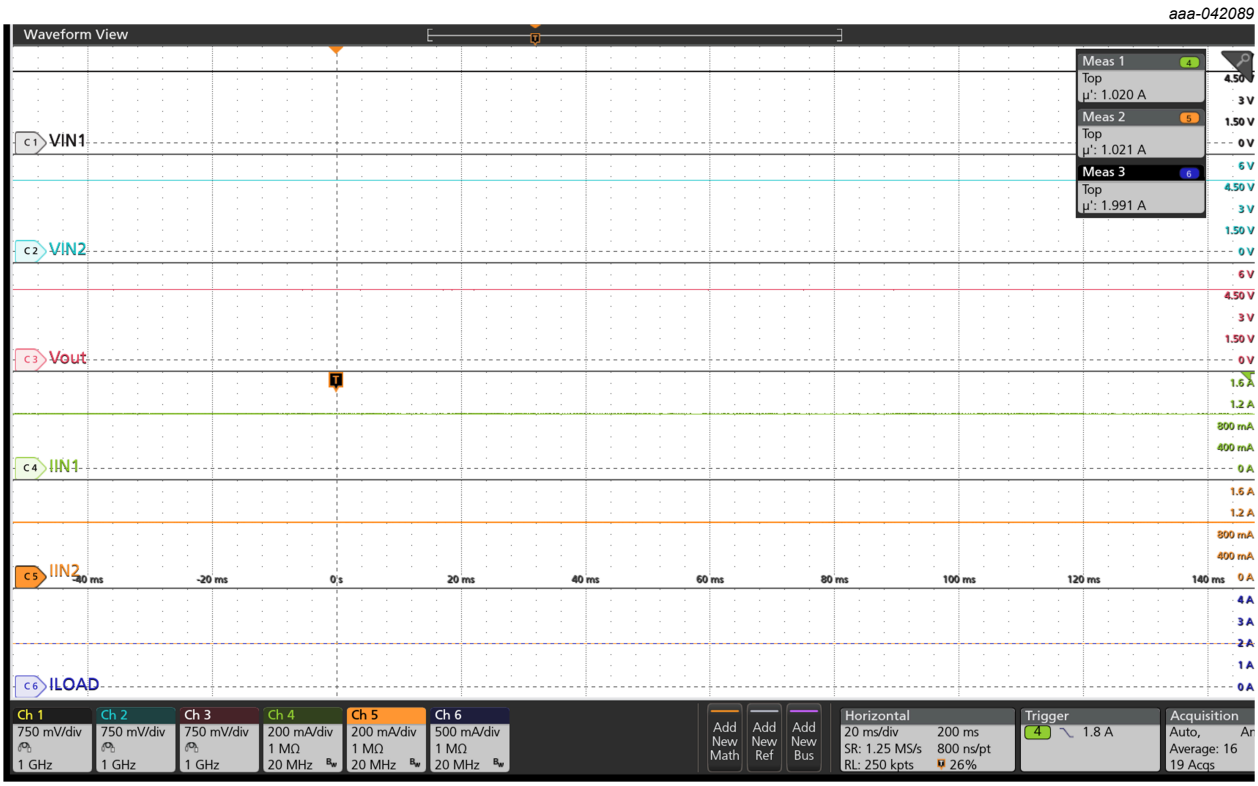


Fig. 41. Waveforms showing paralleling of two NPS7601s

10.6. Thermal characteristics and power dissipation

The junction temperature of a semiconductor device is determined by the internal power dissipation and its capacity to dissipate heat to the surrounding environment. The electronic equivalent is shown in Fig. 42.

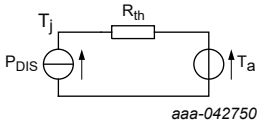


Fig. 42. Thermal diagram

From the diagram, the formula for calculating the junction temperature can be derived as follows:

$$T_j = P_{DIS} \times R_{th} + T_{amb}$$

Where T_j is the junction temperature, P_{DIS} is the power dissipation, R_{th} is the thermal resistance, and T_{amb} is the ambient temperature.

The internal power dissipation is given by:

$$P_{DIS} = I_{OUT} \times (V_{IN} - V_{OUT})$$

Where I_{OUT} is the output current, V_{IN} is the input voltage, and V_{OUT} is the output voltage.

It is a characteristic of semiconductor devices that power losses increase with rising temperatures. Operating the device above the specified maximum junction temperature of 125°C can lead to thermal runaway due to these increased losses, thereby reducing the device's lifespan or triggering thermal protection.

The aforementioned equations can be used to estimate the junction temperature for a given application. To verify the actual junction temperature, the specified Ψ_{JT} value can be used in conjunction with the measured top package temperature:

$$T_j = \Psi_{JT} \times P_{DIS} + T_{TOP}$$

where T_{TOP} is the top surface temperature of the package.

10.7. Power supply recommendations

NPS7601 is designed to operate with a V_{IN} range of 1.5 V to 5.5 V.

The V_{IN} power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps.

In most cases, using an input capacitance (C_{IN}) of 0.1 + 1 µF is sufficient to prevent the supply voltage from drooping. In other cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance is required on the input.

An effective capacitance of no less than 0.3 µF, after applying voltage and temperature derating factors, is required on the OUT pin to ensure the stability of the control loop Gm amplifier.

10.8. Output capacitance considerations

When selecting the output capacitor (C_{OUT}) for the NPS7601, consider inrush current, thermal performance, startup behavior, and system stability. Internal validation showed stable operation with output capacitance up to 1000 µF (1 mF).

Testing used hot-plug conditions at V_{IN} = 5.5 V, load current = 1.5 A, and C_{OUT} = 1 mF at an ambient temperature of 85 °C. The device completed over 1 million cycles with no degradation or abnormal behavior. This result confirms the robustness of the NPS7601 under high output capacitance.

The NPS7601 can support output capacitance above 1 mF. This allows flexibility for designs that require large bulk capacitance or load stabilization. However, the correct value of C_{OUT} depends on the system design and operating conditions. The designer must check inrush current, thermal limits, startup behavior, and stability before selecting a capacitor. While 1 mF is a validated safe value, higher values are acceptable at the designer's discretion.

10.9. PCB layout

For optimal performance, all PCB traces must be kept as short as possible.

To reduce the impact of parasitic inductance on device operation, place input and output capacitors as close to the device as possible.

Additionally, use wide traces for the V_{IN}, V_{OUT}, and GND connections to minimize parasitic resistance and inductive effects.

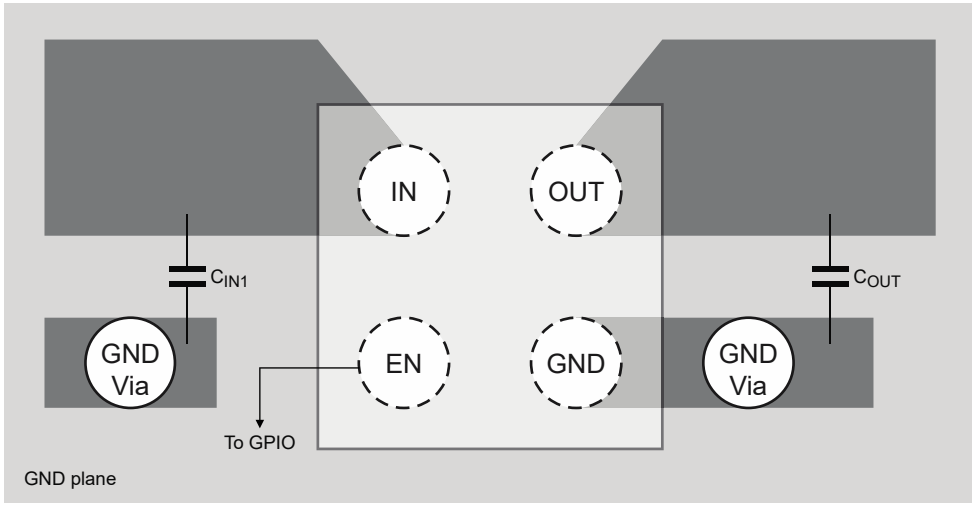
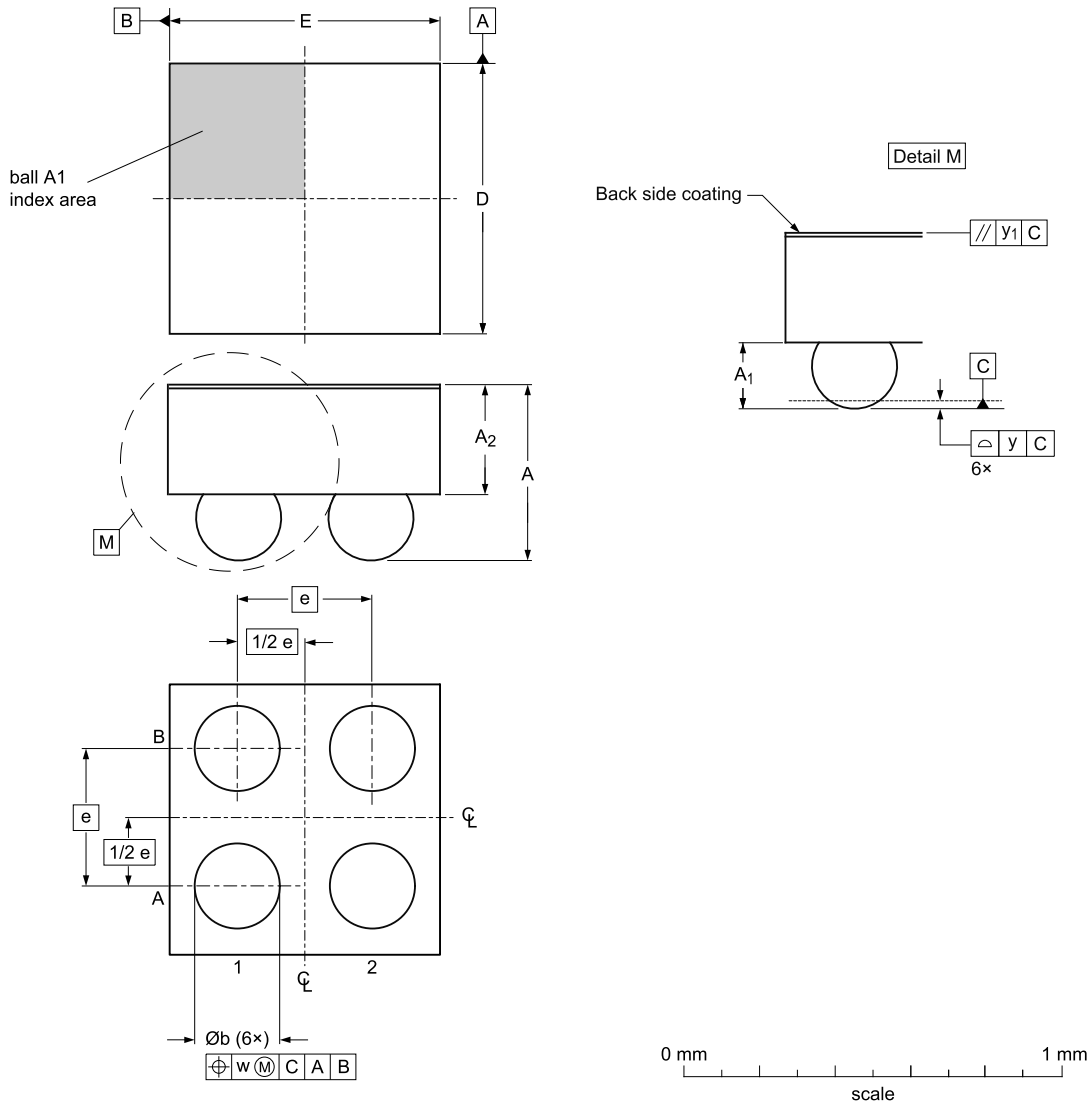


Fig. 43. PCB layout

11. Package outline

WLCSP4: wafer level chip-size package; 4 bumps **SOT8113**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	w	y	y_1
mm	max	0.465		0.290	0.245	0.745	0.745	0.35 BSC	0.015	0.05	0.06
	nom			0.265	0.225	0.715	0.715				
	min		0.145	0.240	0.205	0.685	0.685				

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8113						25-09-30

Fig. 44. Package outline WLCSP4 (SOT8113)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
ESR	Equivalent Series Resistance
FET	Field-Effect Transistor
HBM	Human Body Model
IEC	International Electrotechnical Commission
JEDEC	Joint Electron Device Engineering Council
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PMOS	P-channel Metal-Oxide Semiconductor

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NPS7601 v.1	20251124	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 24 November 2025