

NIS5020, NIS5021, NIS5820

+12 Volt Electronic Fuse

The NIS5x2x Series eFuse is a cost effective, resettable fuse which can greatly enhance the reliability of a hard drive or other circuit from both catastrophic and shutdown failures.

It is designed to buffer the load device from excessive input voltage which can damage sensitive circuits. It includes an overvoltage clamp circuit that limits the output voltage during transients but does not shut the unit down, thereby allowing the load circuit to continue its operation.

Features

- 14 mΩ and 24 mΩ Typical $R_{DS(on)}$ Options
- Tristate Enable
- Overcurrent Protection
- Thermally Protected
- Integrated Soft-Start Circuit
- Fast Response Overvoltage Clamp Circuit
- Internal Undervoltage Lockout Circuit
- Internal Charge Pump
- NIS5020 and NIS5820 in WDFN10 3x3
- NIS5021 in WDFN10 4x4
- Hot Pluggable
- ESD HBM Rating: 1.5 kV
- ESD CDM Rating: 1.0 kV
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Hard Drives
- Solid State Drives
- Servers
- Mother Boards
- Fan Drives



ON Semiconductor®

www.onsemi.com

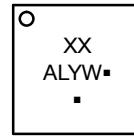
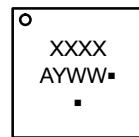


WDFN10 4x4
CASE 511DS



WDFN10 3x3
CASE 522AA

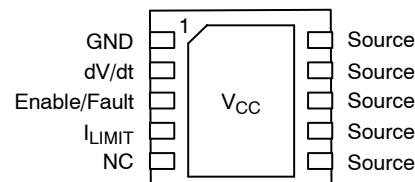
MARKING DIAGRAMS



XX = Specific Device Code
(2A = 5020, 2B = 5021,
2J = 5820)
A = Assembly Location
L = Wafer Lot
Y = Year
WW, W = Work Week
■ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



WDFN10

(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

NIS5020, NIS5021, NIS5820

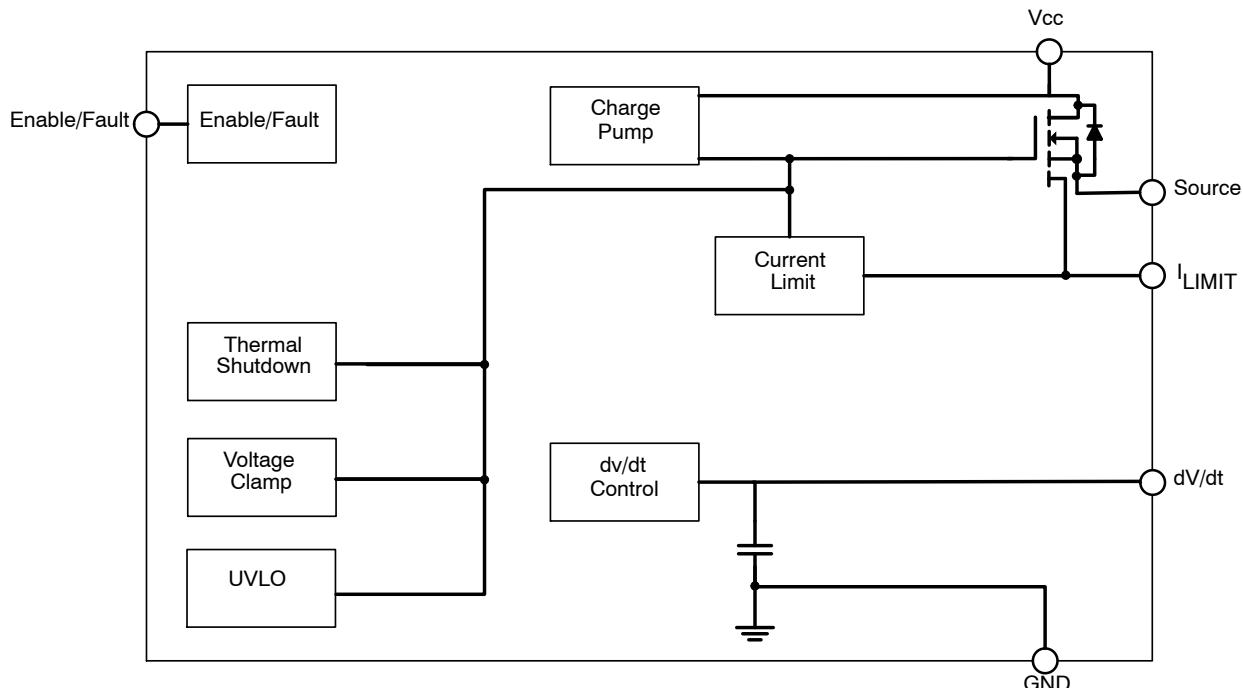


Figure 1. Block Diagram

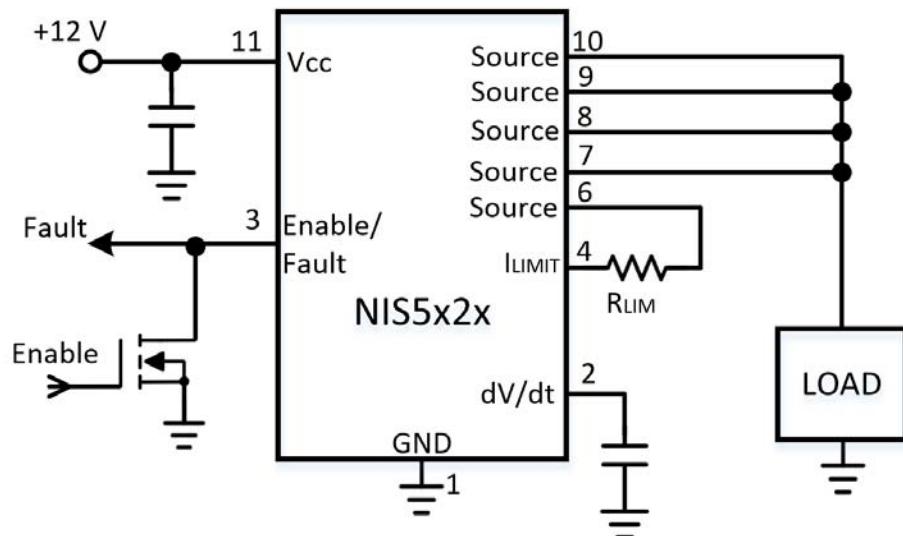


Figure 2. Application Circuit with Kelvin Current Sensing

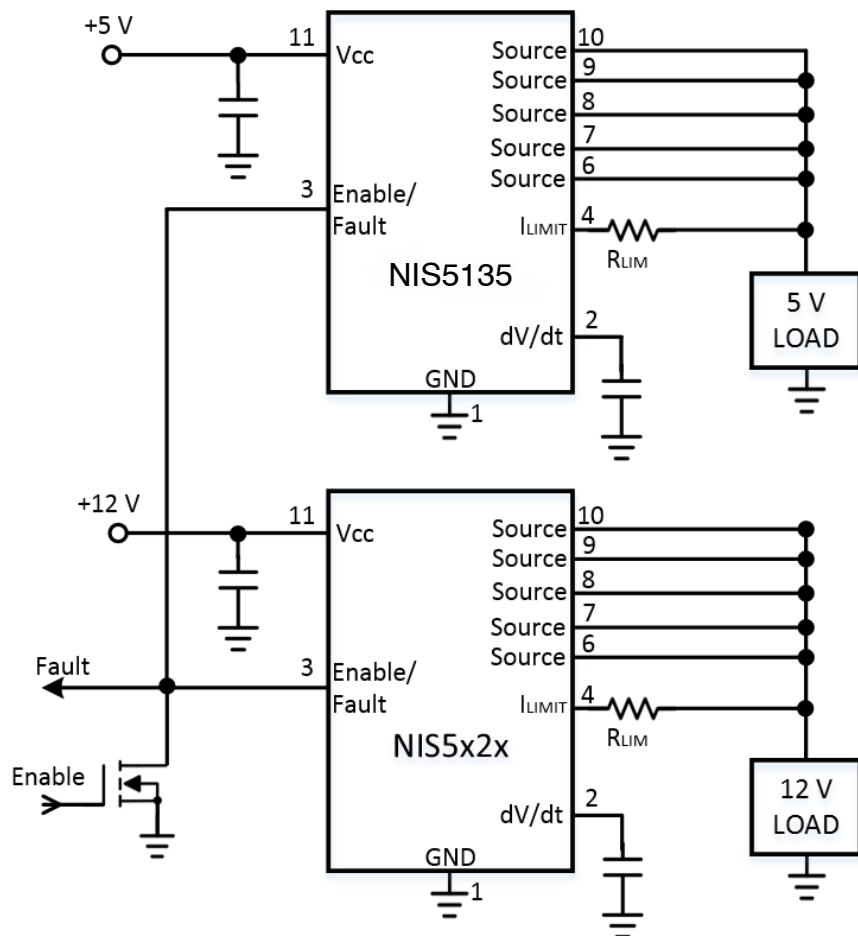


Figure 3. Common Thermal Shutdown between 12 V and 5 V Family Devices

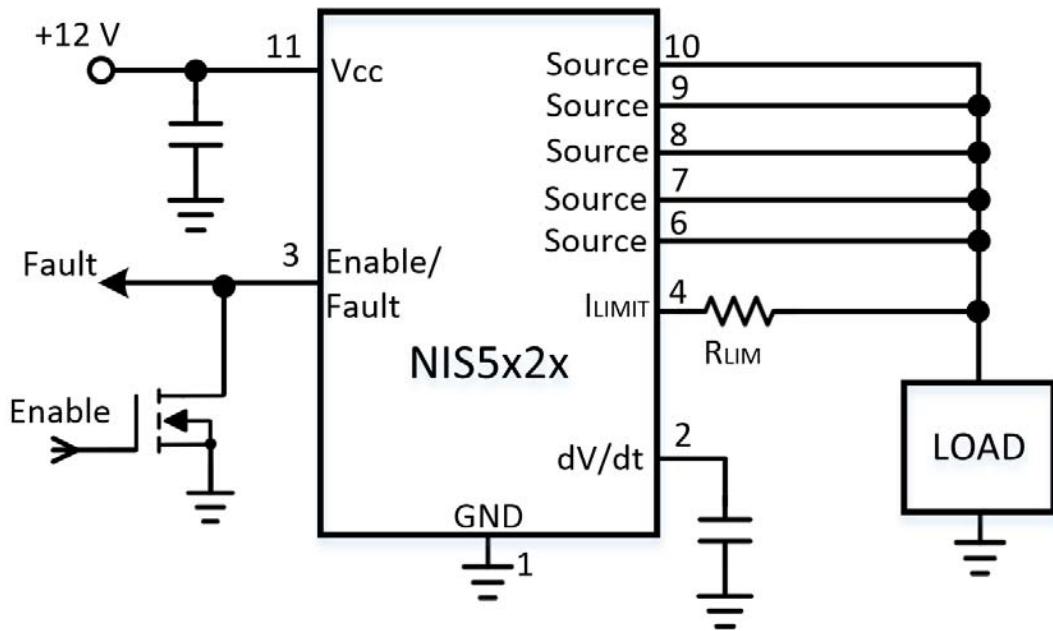


Figure 4. Application Circuit with Direct Current Sensing

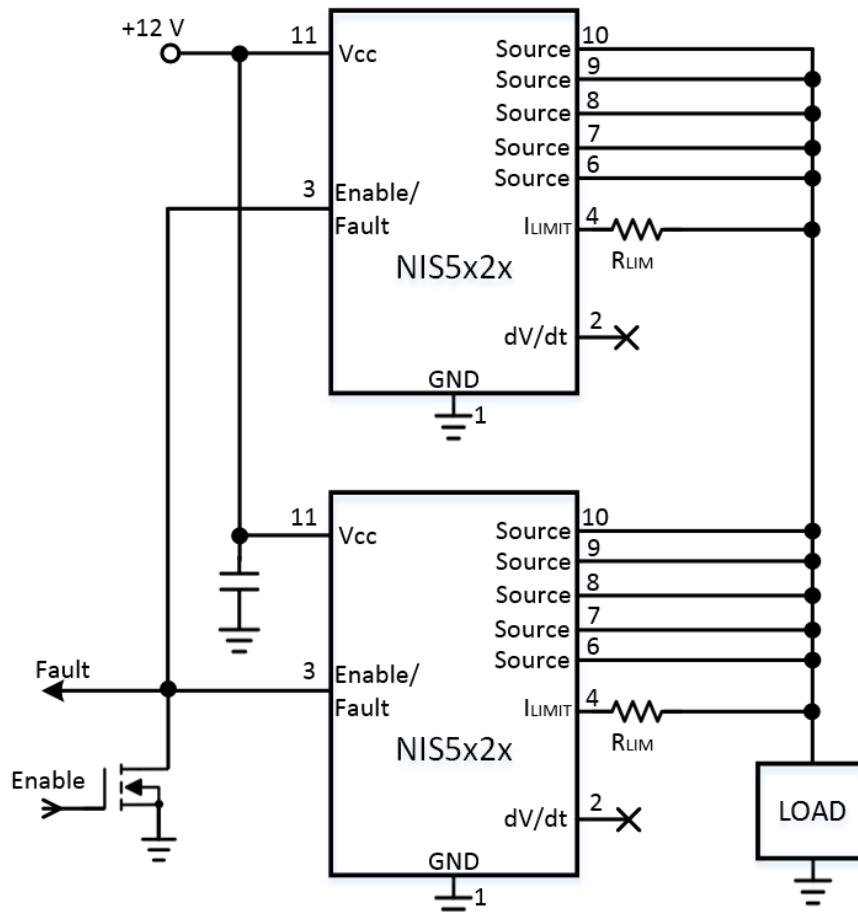


Figure 5. Paralleling eFuses

NIS5020, NIS5021, NIS5820

PIN FUNCTION DESCRIPTION

Pin No. DFN10	Pin Name	Description
1	GND	Negative input voltage to the device. This is used as the internal reference for the IC.
2	dV/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn on. It has an internal capacitor that allows it to ramp up over a period of 1 ms. An external capacitor can be added to this pin to increase the ramp time. If an additional time delay is not required, this pin should be left open.
3	Enable/ Fault	The enable/fault pin is a tri-state, bidirectional interface. It can be pulled to ground with an external open-drain or open collector device to shut down the eFuse. It can also be used as a status indicator; if the voltage level is intermediate (around 1.4V), the eFuse is in thermal shutdown. If the voltage level is high (around 3V) the eFuse is operating normally. Do not actively drive this pin to any voltage. Do not connect a capacitor to this pin.
4	I_{LIMIT}	A resistor between this pin and the source pin sets the overload and short circuit current limit levels
5	NC	No Connect. Leave this pin unconnected.
6-10	Source	Source of the internal power FET and the output terminal of the fuse
11 (Pad)	V_{CC}	Positive input voltage to the device. Connect a 1.0 μ F or greater capacitor from V_{CC} to GND as close as possible to the IC.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage, operating, steady-state (V_{CC} to GND) Transient (100 ms) (Note 1)	V_{CC}	-0.3 to +18	V
		-0.3 to +20	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Guaranteed by characterization only.

NIS5020, NIS5021, NIS5820

THERMAL RATINGS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction-to-Air, NIS5020 (4 layer High-K JEDEC JESD51-7 PCB, 100 mm ² , 2 oz. Cu)	θ_{JA}	50	°C/W
Thermal Resistance, Junction-to-Air, NIS5021 (4 layer High-K JEDEC JESD51-7 PCB, 100 mm ² , 2 oz. Cu)		40	
Thermal Characterization Parameter, Junction-to-Top (4 layer High-K JEDEC JESD51-7 PCB, 100 mm ² , 2 oz. Cu)	Ψ_{J-T}	2.6	°C/W
Thermal Characterization Parameter, Junction-to-Board (4 layer High-K JEDEC JESD51-7 PCB, 100 mm ² , 2 oz. Cu)	Ψ_{J-B}	11.7	°C/W
Total Continuous Power Dissipation, NIS5020 @ $T_A = 25^\circ\text{C}$ (4 layer High-K JEDEC JESD51-7 PCB, 100 mm ² , 2 oz. Cu) Derate above 25°C	P_{\max}	2.5 20	W mW/°C
Total Continuous Power Dissipation, NIS5021 @ $T_A = 25^\circ\text{C}$ (4 layer High-K JEDEC JESD51-7 PCB, 100 mm ² , 2 oz. Cu) Derate above 25°C	P_{\max}	3.1 25	W mW/°C
Operating Temperature Range	T_J	-40 to 150	°C
Non-operating Temperature Range	T_J	-55 to 150	°C
Lead Temperature, Soldering (10 Sec)	T_L	260	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: $V_{CC} = 12\text{ V}$, $C_L = 20\text{ }\mu\text{F}$, dV/dt pin open, $R_{LIM} = 24\text{ }\Omega$, $T_A = 25^\circ\text{C}$)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET					
Delay Time (enabling of chip to V_{OUT} rising to 10% of $V_{CC} = 12\text{ V}$, $C_{OUT} = 0\text{ }\mu\text{F}$)	T_{DLY}		200		μs
ON Resistance (Note 4)	NIS5020	R_{DSON}	11	14	18
	NIS5021		11	14	18
	NIS5820		19	24	30
ON Resistance $T_J = 140^\circ\text{C}$ (Note 5)	NIS5020	$R_{DSON@140C}$		22	
	NIS5021			22	
	NIS5820			37	
Continuous Current ($T_A = 25^\circ\text{C}$, 100 mm ² 1 oz. Cu per layer, one layer (Note 5))	NIS5020	I_D		6.6	
	NIS5021			6.9	
	NIS5820			5.0	
Continuous Current ($T_A = 25^\circ\text{C}$, 4 layer High-K JEDEC JESD51-7 PCB, >800 mm ² , 2 oz. Cu (Note 5))	NIS5020	I_D		10	
	NIS5021			11	
	NIS5820			8.0	
Off State Leakage ($V_{in} = 12\text{ V}$, $EN = 0$)	I_{OFF}			1	μA

THERMAL LATCH

Shutdown Temperature (Notes 2, 5)	T_{SD}	150	175	200	°C
Thermal Hysteresis (Decrease in die temperature for turn on, does not apply to latching parts)	T_{HYST}		45		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. eFuse is latched off until the En/Fault pin is pulled low and then released or a power on reset is applied to the device.
3. Does not include fan out of Enable/Fault function.
4. Pulse test: Pulse width 300 s, duty cycle 2%
5. Verified by design.

NIS5020, NIS5021, NIS5820

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: $V_{CC} = 12 \text{ V}$, $C_L = 20 \mu\text{F}$, dV/dt pin open, $R_{LIM} = 24 \Omega$, $T_A = 25^\circ\text{C}$)

Characteristics	Symbol	Min	Typ	Max	Unit
UNDER/OVERVOLTAGE PROTECTION					
V_{OUT} Maximum ($V_{CC} = 18 \text{ V}$)	$V_{out-clamp}$	13	14	15	V
Undervoltage Lockout (Turn on, Voltage Going High)	V_{UVLO}	7.8	8.5	9.2	V
UVLO Hysteresis	V_{Hyst}		0.8		V
KELVIN CURRENT LIMIT					
Overload/Trip Current, $R_{lim} = 75 \Omega$	NIS5020/ NIS5021	I_{TRIP}		7.6	A
Short Circuit/Holding Current $R_{lim} = 75 \Omega$		I_{HOLD}	1.8	3.4	A
Overload/Trip Current, $R_{lim} = 75 \Omega$	NIS5820	I_{TRIP}		5.3	A
Short Circuit/Holding Current $R_{lim} = 75 \Omega$		I_{HOLD}		2.0	A
SLEW RATE CONTROL					
Slew Rate (no capacitor on dV/dt pin)	SR	0.7	1.0	1.9	ms
ENABLE/FAULT					
Logic Level Low (Output Disabled)	V_{in-low}	0.35	0.58	0.81	V
Logic Level Mid (Thermal Fault, Output Disabled)	V_{in-mid}	0.82	1.4	1.95	V
Logic Level High (Output Enabled)	$V_{in-high}$	1.96	2.2	2.5	V
High State Maximum Voltage	V_{in-max}	2.51	3.3	5.0	V
Logic Low Sink Current ($V_{ENABLE} = 0 \text{ V}$)	I_{in-low}		-17	-25	μA
Logic High Leakage Current for External Switch ($V_{ENABLE} = 3.3 \text{ V}$)	$I_{in-leak}$			1.0	μA
Maximum Fanout for Fault Signal (Total number of chips that can be connected to this pin for simultaneous shutdown)	Fan			3.0	Units
TOTAL DEVICE					
Bias Current	I_{Bias}		650	800	μA
Operational ($I_{Load} = 0 \text{ A}$)					
Shutdown (EN = 0) (Note 3)			100	150	
Fault			110	200	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. eFuse is latched off until the En/Fault pin is pulled low and then released or a power on reset is applied to the device.
3. Does not include fan out of Enable/Fault function.
4. Pulse test: Pulse width 300 s, duty cycle 2%
5. Verified by design.

TYPICAL CHARACTERISTICS

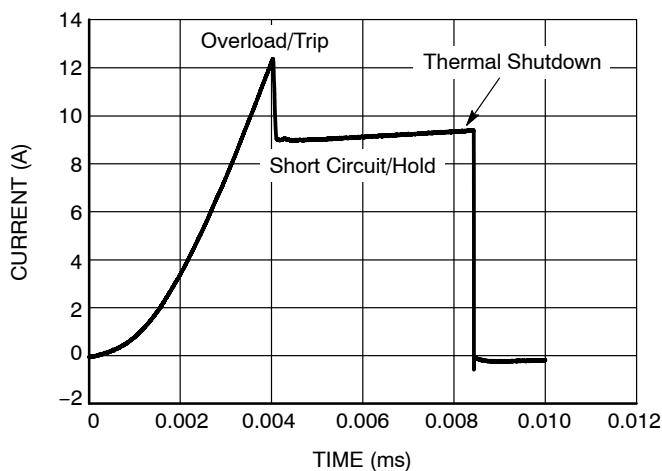


Figure 6. Slow Fault Current Limit Characteristic of NIS5020

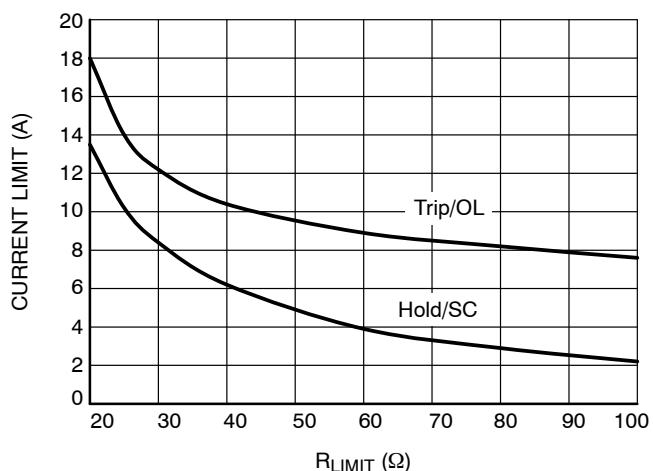


Figure 7. NIS5020/NIS5021 Current Limit vs. R_{LIMIT} for Kelvin Sensing

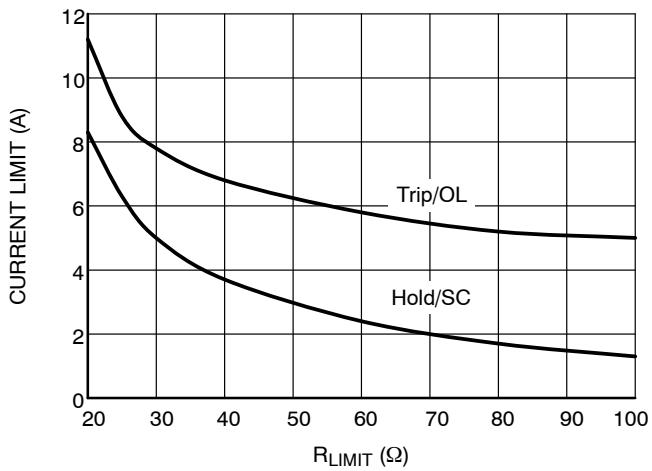


Figure 8. NIS5820 Current Limit vs. R_{LIMIT} for Kelvin Sensing

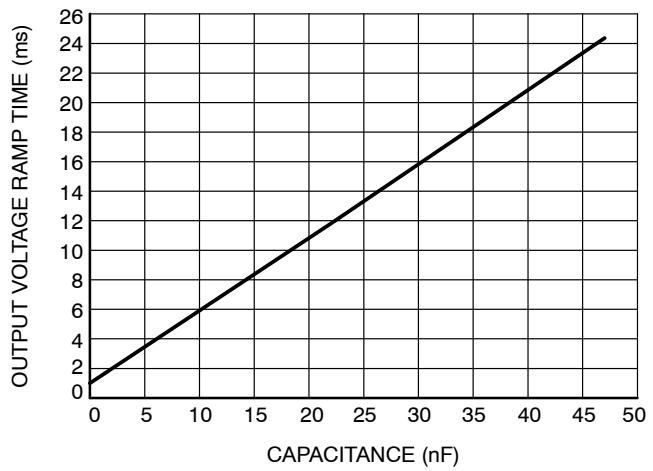


Figure 9. Output Voltage Ramp Time vs. dv/dt Capacitance

NIS5020, NIS5021, NIS5820

TYPICAL CHARACTERISTICS

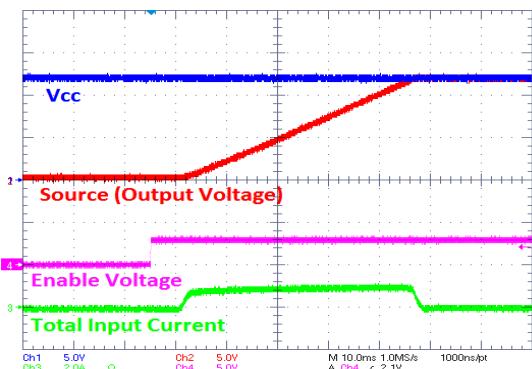


Figure 10. NIS5020 Slew Rate Control

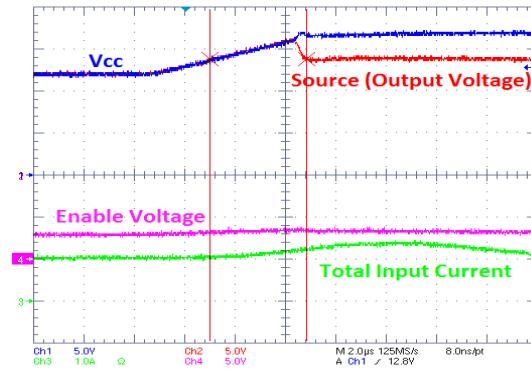


Figure 11. NIS5020 Overvoltage Clamp Operation

APPLICATIONS INFORMATION

Paralleling eFuses

If the output current capability required by an application is higher than the current which can be carried by a single eFuse, it is possible to parallel eFuses to achieve a higher current throughput. Up to four eFuses can be paralleled to achieve a higher current. All of the eFuses will have a common thermal shutdown. Refer to Figure 5 for the schematic connection of parallel eFuses. The VCC pins of every eFuse must be shorted together. The Source pins of each eFuse must be shorted together. Each eFuse should be configured either in Kelvin or Direct mode and have its individual current limiting resistor R_{LIM} connected between I_{LIMIT} and Source pins. The Enable pins of all the eFuses must be shorted together for common shutdown functionality and connected to an open-drain or open collector device in case it is desired to turn off all the eFuses at the same time. The dv/dt pins of eFuses must NOT be shorted together; they should be either left floating for a standard output ramp-up time or have individual dv/dt capacitor to ground.

Every eFuse will carry equal amount of current during normal operation and overcurrent events. If any of the eFuses goes to thermal shutdown first, it will pull down the Enable pin and make the other eFuses to shut down as well.

Basic Operation

This device is a self-protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output voltage, output current and die temperature.

On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits. The output voltage, which is controlled by an internal dV/dt circuit, will slew from 0 V to the rated output voltage in 1 ms. The device will remain on as long as the temperature does not exceed the 175°C limit that is programmed into the chip.

The internal current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the internally set current limit level. The input overvoltage clamp also does not shutdown the part, but will limit the output voltage in the event that the input exceeds the V_{CLAMP} level.

An internal charge pump provides bias for the gate voltage of the internal n-channel power FET and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage (V_{CC}) and ground.

Current Limit

The current limit circuit uses a SENSEFET along with a reference and amplifier to control the peak current in the device. The SENSEFET allows for a small fraction of the load current to be measured, which has the advantage of reducing the losses in the sense resistor.

The current limit circuit has two limiting values, one for short circuit events which are defined as the mode of

operation in which the gate is high and the FET is fully enhanced. The overload mode of operation occurs when the device is actively limiting the current and the gate is at an intermediate level. For a more detailed description of this circuit please refer to application note AND9441.

Connection of R_{LIMIT} current limit setting resistor can be made as shown in Figure 2 (Kelvin connection), or Figure 4 (Direct connection). Both connections result in a similar current limit thresholds and behavior. It is important to make sure that layout trace connecting R_{LIMIT} resistor to pins 4 and 6 is as short as possible. The shortest possible distance on a PCB must be used to connect pin 6 to R_{LIM} resistor before pin 6 is connected to a common load node.

Ovvoltge Clamp

The overvoltage clamp consists of an amplifier and reference. It monitors the output voltage and if the input voltage exceeds 14 V, the gate drive of the main FET is reduced to limit the output. This is intended to allow operation through transients while protecting the load. If an overvoltage condition exists for many seconds, the device may overheat due to the voltage drop across the FET combined with the load current. In this event, the thermal protection circuit would shut down the device. Refer to Figure 12 for typical overvoltage clamp behavior

Undervoltage Lockout

The undervoltage lockout circuit uses a comparator with hysteresis to monitor the input voltage. If the input voltage drops below the specified level, the output switch will be switched to a high impedance state.

Slew Rate Control

The dV/dt circuit brings the output voltage up under a linear, controlled rate regardless of the load impedance characteristics. An internal ramp generator creates a linear ramp, and a control circuit forces the output voltage to follow that ramp, scaled by a factor.

The default ramp time is approximately 1 ms. This pin includes an internal current source of approximately 1 μ A. Since the current level is very low, it is important to use a ceramic cap or other low leakage capacitor. Aluminum electrolytic capacitors are not recommended for this circuit. The ramp time from 10% to 90% of the nominal output voltage can be determined by the following equation:

$$C_{ext} = \left(\frac{t}{0.5E06} \right) - 1.4 \text{ nF}$$

Where: C is in Farads,
t is in Seconds

Anytime that the unit shuts down due to a fault, enable shutdown, or recycling of input power, the timing capacitor will be discharged and the output voltage will ramp from 0 at turn on. Refer to Figures 9 and 11 for slew rate control and typical Slew Rate behavior.

Enable/Fault

The Enable/Fault Pin is a multi-function, bidirectional pin that can control the output of the chip as well as send information to other devices regarding the state of the chip. When this pin is low, the output of the fuse will be turned off. When this pin is high the output of the fuse will be turned-on. If a thermal fault occurs, this pin will be pulled low to an intermediate level by an internal circuit. To use as a simple enable pin, an open drain or open collector device should be connected to this pin. Due to its tri-state operation, it should not be connected to any type of logic with an internal pull-up device. Do not connect external capacitor directly to this pin.

If the chip shuts down due to the die temperature reaching its thermal limit, this pin will be pulled down to an intermediate level. This signal can be monitored by an external circuit to communicate that a thermal shutdown has occurred. If this pin is tied to another device in this family, a thermal shutdown of one device will cause both devices to disable their outputs. Both devices will turn on once the fault is removed for the auto-retry devices.

Since this is a latching thermal device, the outputs will be enabled after the enable pin has been pulled to ground with an external switch and then allowed to go high or after the input power has been recycled.

Thermal Protection

The NIS5x2x Series includes an internal temperature sensing circuit that senses the temperature on the die of the power FET. If the temperature reaches 175°C, the device will shut down, and remove power from the load. Output power can be restored by either recycling the input power or toggling the enable pin. Power will automatically be reapplied to the load for auto-retry devices once the die temperature has been reduced by 45°C.

The thermal limit has been set high intentionally, to increase the trip time during high power transient events. It is not recommended to operate this device above 150°C for extended periods of time.

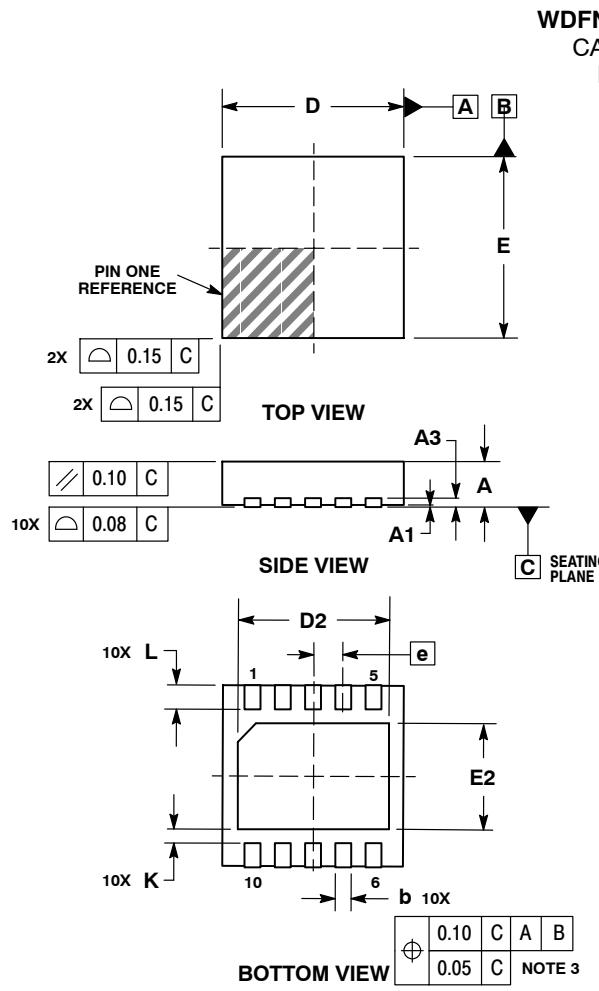
The similar devices from different voltage families can be configured together as shown in Figure 3 for a common thermal shutdown.

ORDERING INFORMATION

Device	Marking	Features	Package	Shipping [†]
NIS5020MT1TXG	5020	Latch	WDFN10-3x3	3000 / Tape & Reel
NIS5020MT2TXG	5020A	Auto-Retry	WDFN10-3x3	3000 / Tape & Reel
NIS5021MT1TXG	5021	Latch	WDFN10-4x4	3000 / Tape & Reel
NIS5021MT2TXG	5021A	Auto-Retry	WDFN10-4x4	3000 / Tape & Reel
NIS5820MT1TXG	5820	Latch	WDFN10-3x3	3000 / Tape & Reel
NIS5820MT2TXG	5820A	Auto-Retry	WDFN10-3x3	3000 / Tape & Reel

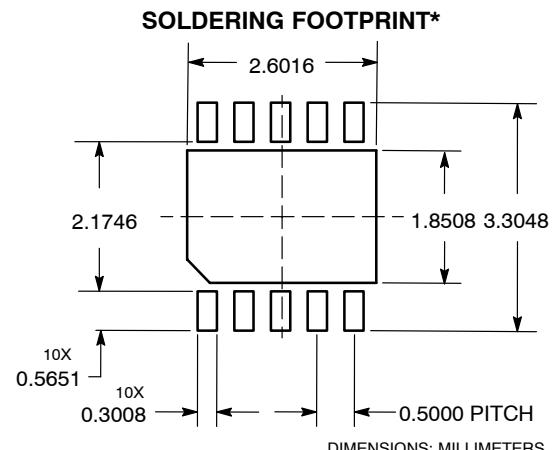
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS



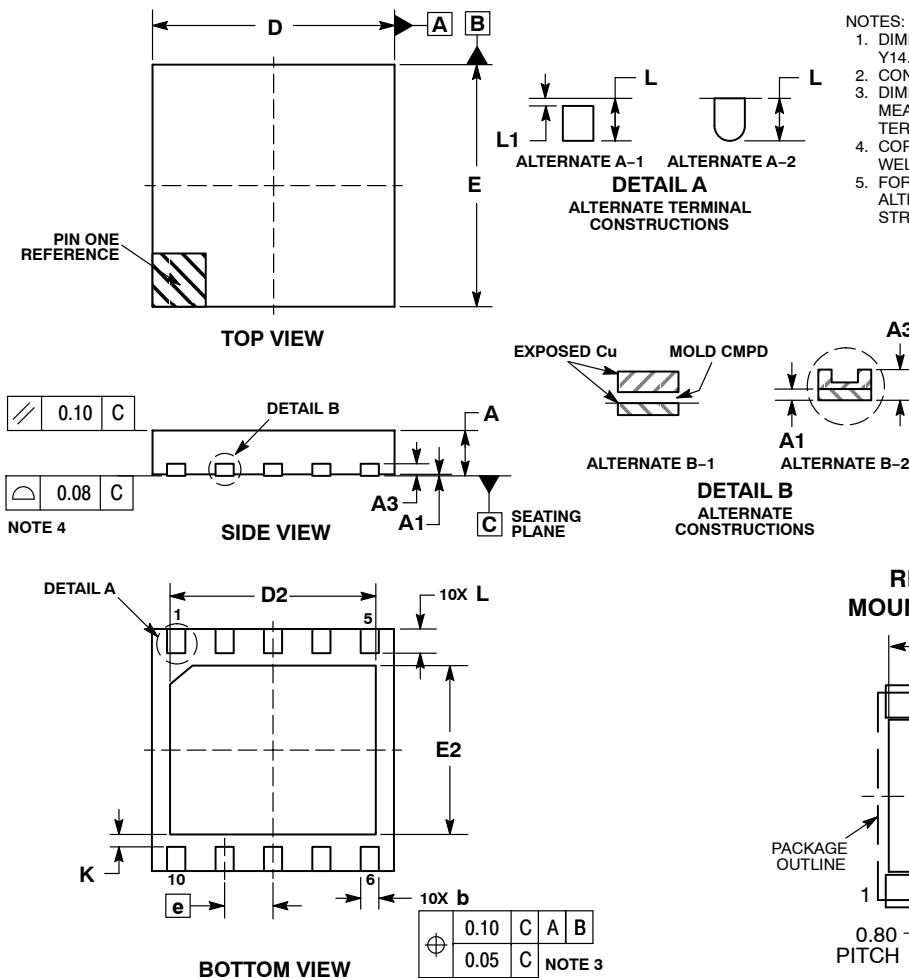
NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.03	0.05
A3	0.20	REF	
b	0.18	0.24	0.30
D	3.00	BSC	
D2	2.45	2.50	2.55
E	3.00	BSC	
E2	1.75	1.80	1.85
e	0.50	BSC	
K	0.19	TYP	
L	0.35	0.40	0.45



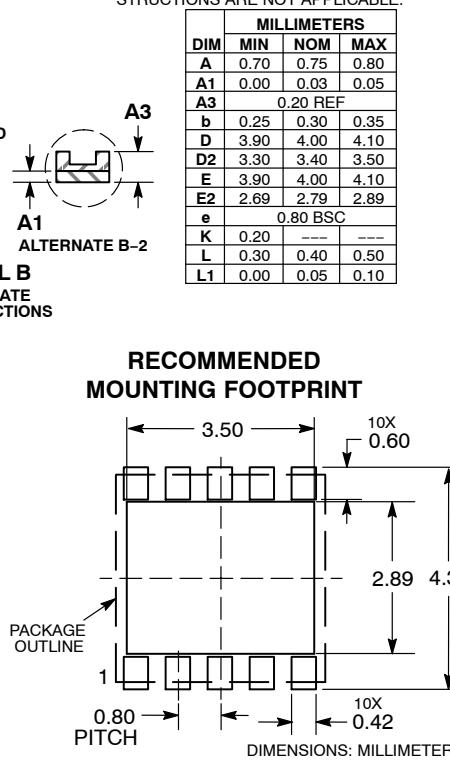
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

WDFN10 4x4, 0.8P
CASE 511DS
ISSUE O

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE B-1 AND DETAIL A ALTERNATE A-1 CONSTRUCTIONS ARE NOT APPLICABLE.



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor](#):

[NIS5021MT1TXG](#)