

# NFAP1060L3TT

## Advance Information Intelligent Power Module (IPM), 600 V, 10 A

The NFAP1060L3TT is a fully-integrated inverter power stage consisting of a high-voltage driver, six IGBT's and a thermistor, suitable for driving permanent magnet synchronous (PMSM) motors, brushless-DC (BLDC) motors and AC asynchronous motors. The IGBT's are configured in a 3-phase bridge with separate emitter connections for the lower legs for maximum flexibility in the choice of control algorithm. The power stage has a full range of protection functions including cross-conduction protection, external shutdown and under-voltage lockout functions. An internal comparator and reference connected to the over-current protection circuit allows the designer to set the over-current protection level.

### Features

- Three-phase 10A/600V IGBT Module with Integrated Drivers
- Compact 44 mm x 20.9 mm Single In-line Package
- Built-in Under Voltage Protection
- Cross-conduction Protection
- Adjustable Over-current Protection Level
- Integrated Bootstrap Diodes and Resistors
- Thermistor for Substrate Temperature Measurement
- UL1557 Certification (File number: E339285)

### Typical Applications

- Industrial Drives
- Industrial Pumps
- Industrial Fans
- Industrial Automation

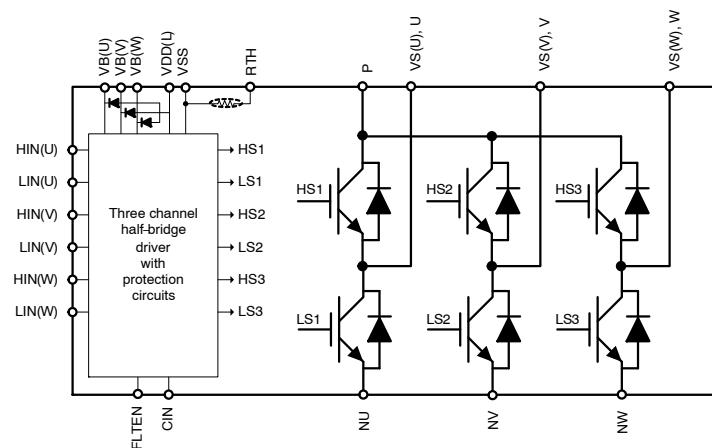


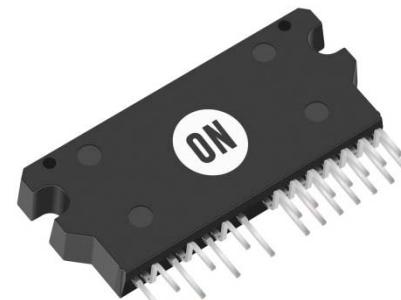
Figure 1. Functional Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.



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SIP29  
CASE 127FB

### MARKING DIAGRAM



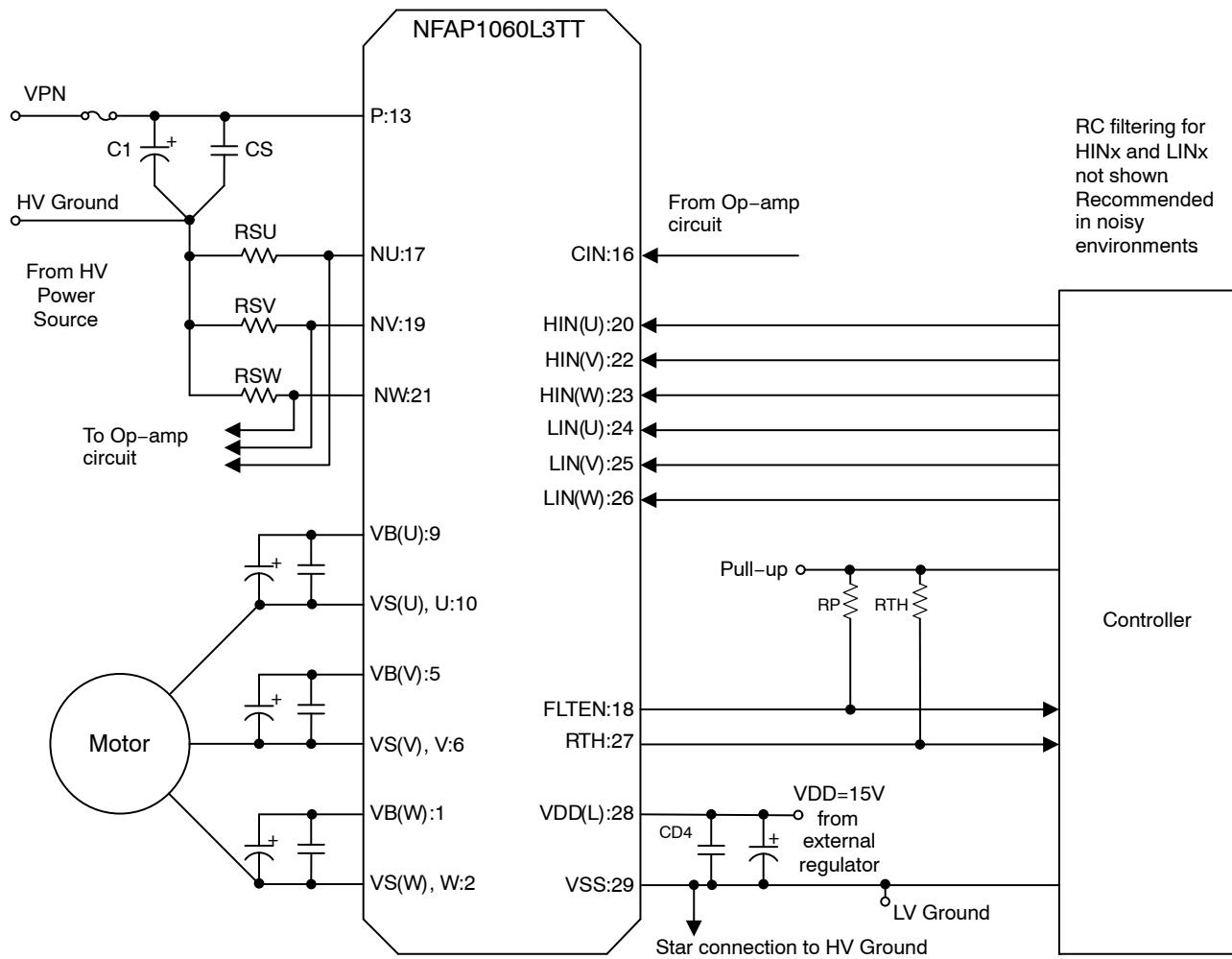
(Top View)

NFAP1060L3TT = Specific Device Code  
ZZZ = Assembly Input Ordering Code  
A = Assembly Site  
T = Test Site  
Y = Year Code  
W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
NFAP1060L3TT	SIP29 (Pb-Free)	120 / Box

**NFAP1060L3TT**



**Figure 2. Application Schematic**

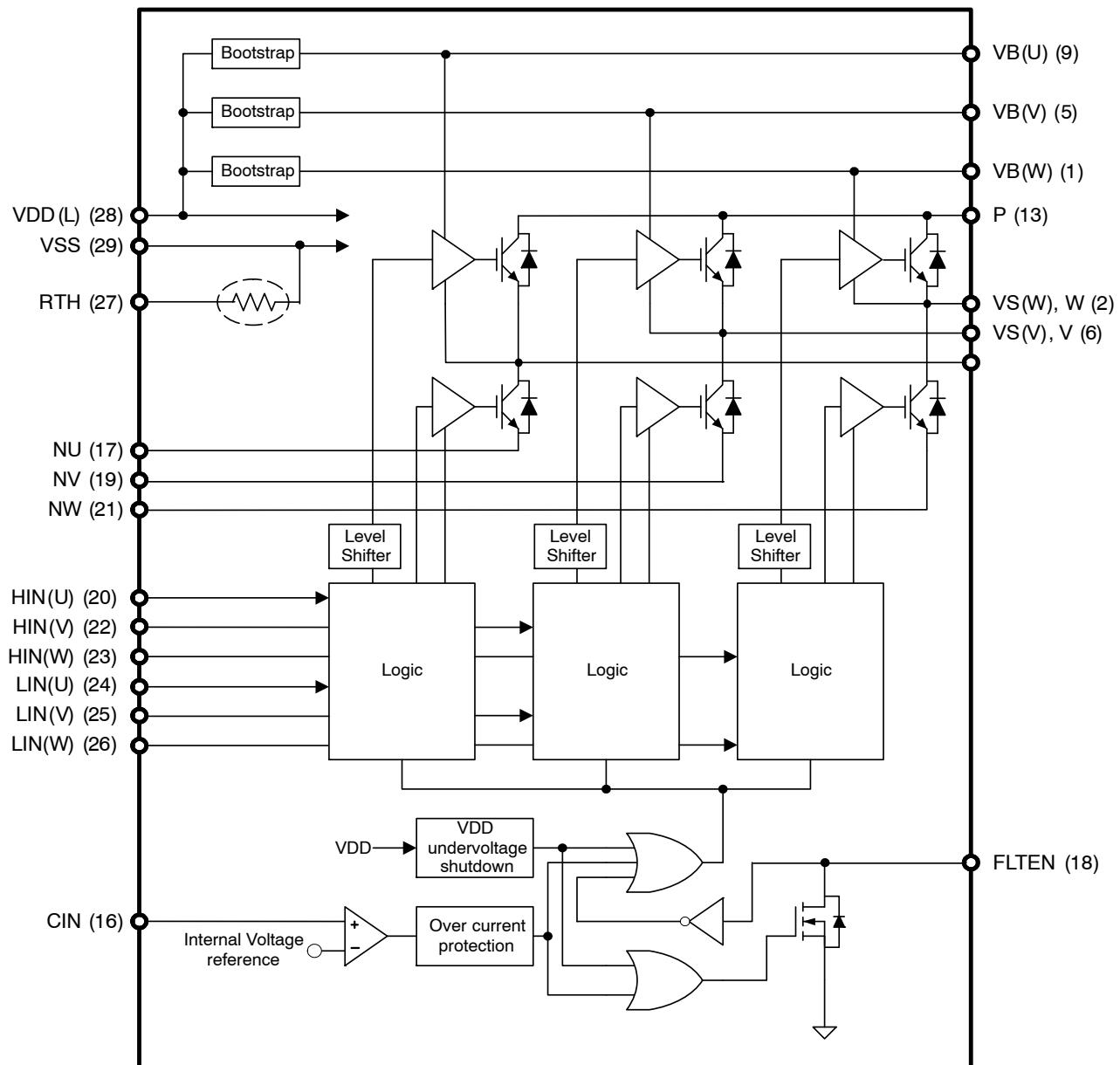


Figure 3. Simplified Block Diagram

**Table 1. PIN FUNCTION DESCRIPTION**

Pin	Name	Description
1	VB(W)	High-Side Bias Voltage for W phase IGBT Driving
2	VS(W), W	High-Side Bias Voltage GND for W phase IGBT Driving, Output for W Phase
5	VB(V)	High-Side Bias Voltage for V phase IGBT Driving
6	VS(V), V	High-Side Bias Voltage GND for V phase IGBT Driving, Output for V Phase
9	VB(U)	High-Side Bias Voltage for U phase IGBT Driving
10	VS(U), U	High-Side Bias Voltage GND for U phase IGBT Driving, Output for U Phase
13	P	Positive DC-Link Input
16	CIN	Input for Current Protection
17	NU	Negative DC-Link Input for U Phase
18	FLTEN	Fault Output, Enable Input
19	NV	Negative DC-Link Input for V Phase
20	HIN(U)	Signal Input for High-Side U Phase
21	NW	Negative DC-Link Input for W Phase
22	HIN(V)	Signal Input for High-Side V Phase
23	HIN(W)	Signal Input for High-Side W Phase
24	LIN(U)	Signal Input for Low-Side U Phase
25	LIN(V)	Signal Input for Low-Side V Phase
26	LIN(W)	Signal Input for Low-Side W Phase
27	RTH	Series Resister for Thermistor (Temperature Detection)
28	VDD(L)	Low-Side Bias Voltage for IC and IGBTs Driving
29	VSS	Low-Side Common Supply Ground

NOTE: Pins 3, 4, 7, 8, 11, 12, 14 and 15 are not present

**Table 2. ABSOLUTE MAXIMUM RATINGS** at  $T_c = 25^\circ\text{C}$  (Note 1)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	VPN	P-NU,NV,NW, VPN (surge) < 500 V (Note 2)	450	V
Collector – Emitter Voltage	Vces	P-U,V,W; U-NU; V-NV; W-NW	600	V
Each IGBT Collector Current	$\pm I_c$	P,U,V,W,NU,NV,NW terminal current	$\pm 10$	A
Each IGBT Collector Current (Peak)	$\pm I_{cp}$	$T_c = 25^\circ\text{C}$ , Under 1ms Pulse Width	20	A
Corrector Dissipation	Pc	$T_c = 25^\circ\text{C}$ , Per One Chip	19	W
High-Side Control Bias voltage	VBS	VB(U)-U, VB(V)-V, VB(W)-W (Note 3)	-0.3 to +20.0	V
Control Supply Voltage	VDD	VDD(L)-VSS	-0.3 to +20.0	V
Input Signal Voltage	VIN	HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W) – VSS	-0.3 to $V_{DD}$	V
FLTEN Terminal Voltage	VFLTEN	FLTEN-VSS	-0.3 to $V_{DD}$	V
Current Sensing Input Voltage	VCIN	CIN-VSS	-0.3 to +7.0	V
Operating Junction Temperature	Tj		150	$^\circ\text{C}$
Storage Temperature	Tstg		-40 to +125	$^\circ\text{C}$
Module Case Operation Temperature	Tc		-40 to +125	$^\circ\text{C}$
Tightening Torque	MT	Case mounting screws	0.9	Nm
Isolation Voltage	Viso	50 Hz sine wave AC 1 minute (Note 4)	2000	Vrms

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This surge voltage developed by the switching operation due to the wiring inductance between P and NU, NV, NW terminal.
3. VBS=VB(U)-U, VB(V)-V, VB(W)-W
4. Test conditions : AC2500V, 1 s

**Table 3. RECOMMENDED OPERATING RANGES**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	VPN	P-NU,NV,NW	0	280	450	V
High-Side Control Bias voltage	VBS	VB(U)-VS(U), VB(V)-VS(V), VB(W)-VS(W)	13.0	15	17.5	V
Control Supply Voltage	VDD	VDD(L)-VSS	14.0	15	16.5	V
ON-state Input Voltage	VIN(ON)	HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W) - VSS	3.0	-	5.0	V
OFF-state Input Voltage	VIN(OFF)		0	-	0.3	V
PWM Frequency	fPWM		1	-	20	kHz
Dead Time	DT	Turn-off to Turn-on (external)	0.5	-	-	μs
Allowable Input Pulse Width	PWIN	ON and OFF	1	-	-	μs
Tightening Torque		'M3' type screw	0.6	-	0.9	Nm

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 4. ELECTRICAL CHARACTERISTICS** at  $T_c = 25^\circ\text{C}$ ,  $V_{\text{BIAS}} (\text{VBS}, \text{VDD}) = 15 \text{ V}$  unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
<b>POWER OUTPUT SECTION</b>						
Collector-Emitter Leakage Current	$V_{\text{CE}}=600\text{V}$	$I_{\text{CES}}$	-	-	1	mA
Bootstrap Diode Reverse Current	$VR(\text{DB})=600\text{V}$	$I_{\text{R}(\text{DB})}$	-	-	1	mA
Collector-Emitter Saturation Voltage	$V_{\text{DD}}=\text{VBS}=15\text{V}$ , $\text{IN}=5\text{V}$ , $I_{\text{C}}=10\text{A}$ , $T_{\text{J}}=25^\circ\text{C}$	$V_{\text{CE}(\text{sat})}$	-	2.1	2.7	V
	$V_{\text{DD}}=\text{VBS}=15\text{V}$ , $\text{IN}=5\text{V}$ , $I_{\text{C}}=5\text{A}$ , $T_{\text{J}}=100^\circ\text{C}$		-	1.8	-	V
FWDi Forward Voltage	$\text{IN}=0\text{V}$ , $I_{\text{C}}=-10\text{A}$ , $T_{\text{J}}=25^\circ\text{C}$	$V_F$	-	2.2	2.8	V
	$\text{IN}=0\text{V}$ , $I_{\text{C}}=-5\text{A}$ , $T_{\text{J}}=100^\circ\text{C}$		-	1.7	-	V
Junction to Case Thermal Resistance	Inverter IGBT Part (per 1/6 Module)	$R_{\text{th}(\text{j}-\text{c})\text{Q}}$	-	-	6.3	°C/W
	Inverter FRD Part (per 1/6 Module)	$R_{\text{th}(\text{j}-\text{c})\text{F}}$	-	-	11.6	°C/W

**DRIVER SECTION**

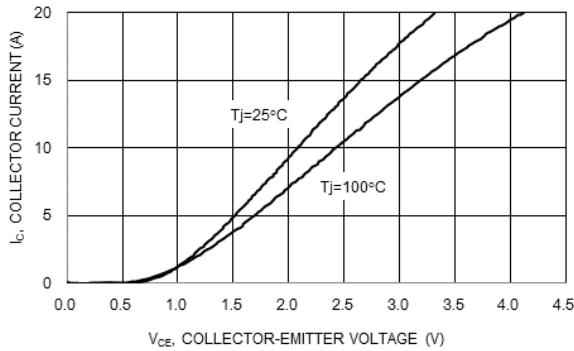
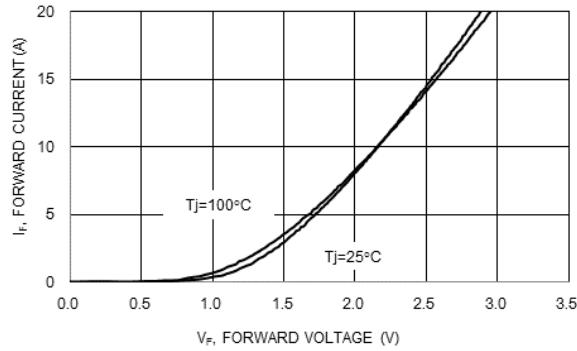
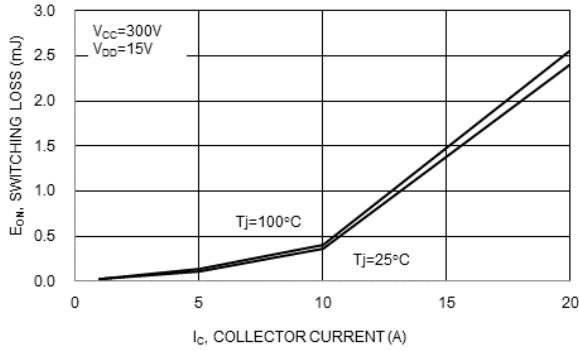
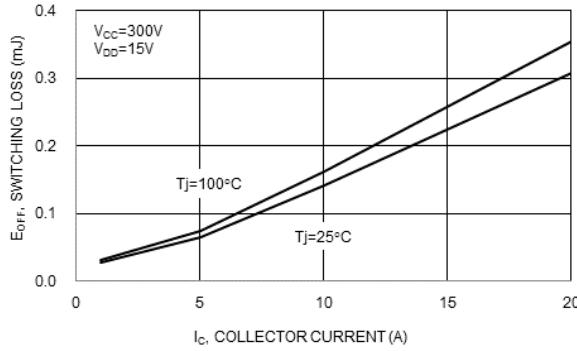
Quiescent VBS Supply Current	$\text{VBS}=15\text{V}$ , $\text{HIN}=0\text{V}$ , per driver	$I_{\text{QBS}}$	-	0.07	0.4	mA
Quiescent VDD Supply Current	$\text{VDD}(\text{L})=15\text{V}$ , $\text{HIN}=0\text{V}$ , $\text{VDD}(\text{L})-\text{VSS}$	$I_{\text{QDDL}}$	-	0.85	3.0	mA
ON Threshold voltage	$\text{HIN}(\text{U}), \text{HIN}(\text{V}), \text{HIN}(\text{W}), \text{LIN}(\text{U}),$ $\text{LIN}(\text{V}), \text{LIN}(\text{W}) - \text{VSS}$	$\text{VIN}(\text{ON})$	-	-	2.5	V
OFF Threshold voltage		$\text{VIN}(\text{OFF})$	0.8	-	-	V
Logic 1 Input Current	$\text{VIN} = +3.3 \text{ V}$	$I_{\text{IN}+}$	-	660	-	μA
Logic 0 Input Current	$\text{VIN} = 0 \text{ V}$	$I_{\text{IN}-}$	-	-	2	μA
FLTEN Terminal Sink Current	FAULT : ON / $\text{VFLTEN} = 0.1 \text{ V}$	$I_{\text{OSD}}$	-	2	-	mA
Fault-Output Pulse Width	$\text{FLTEN}-\text{VSS}$	$t_{\text{FOD}}$	20	-	-	μs
Enable Threshold	$\text{FLTEN}-\text{VSS}$	$V_{\text{EN}+}$	-	-	2.5	V
		$V_{\text{EN}-}$	0.8	-	-	V
Short Circuit Trip Level	$\text{CIN}-\text{VSS}$	$V_{\text{SC}(\text{ref})}$	0.44	0.49	0.54	V
High-Side Control Bias Voltage Under-Voltage Protection	Reset Level	$UV_{\text{BSR}}$	10.3	11.1	11.9	V
	Detection Level	$UV_{\text{BSD}}$	10.1	10.9	11.7	V
Supply Voltage Under-Voltage Protection	Reset Level	$UV_{\text{DDR}}$	10.3	11.1	11.7	V
	Detection Level	$UV_{\text{DDD}}$	10.1	10.9	11.5	V

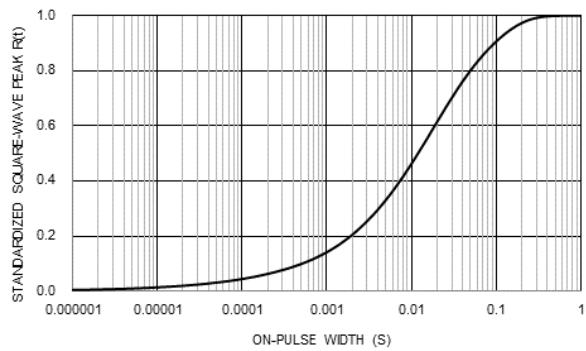
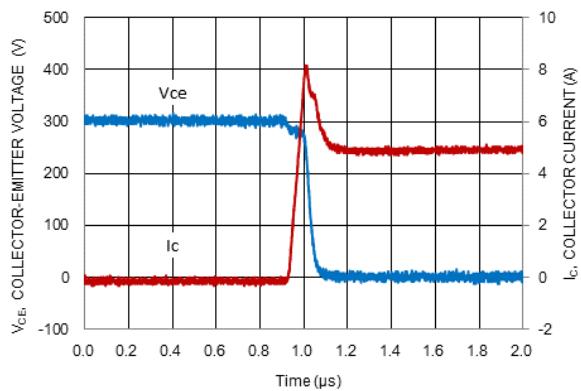
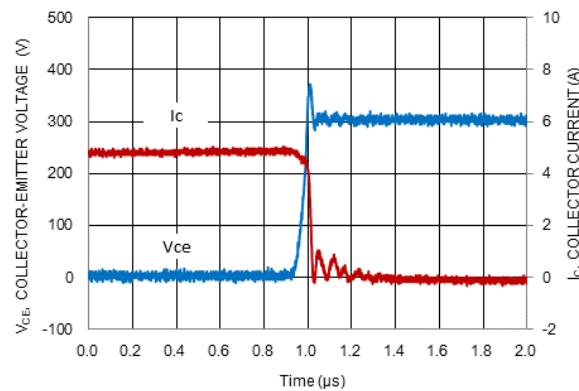
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Table 5. ELECTRICAL CHARACTERISTICS**

at  $T_c = 25^\circ\text{C}$ ,  $V_{\text{BIAS}} (\text{VBS, VDD}) = 15 \text{ V}$ ,  $V_{\text{CC}} = 300 \text{ V}$ ,  $L = 3.0 \text{ mH}$  unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
<b>SWITCHING CHARACTER</b>						
Switching Time	$I_C = 10 \text{ A}$ , $T_j = 25^\circ\text{C}$	$t_{\text{ON}}$	–	0.5	1.0	$\mu\text{s}$
		$t_{\text{OFF}}$	–	0.5	1.0	$\mu\text{s}$
Turn-on Switching Loss	$I_C = 5 \text{ A}$ , $T_j = 25^\circ\text{C}$	$E_{\text{ON}}$	–	114	–	$\mu\text{J}$
Turn-off Switching Loss		$E_{\text{OFF}}$	–	65	–	$\mu\text{J}$
Total Switching Loss		$E_{\text{TOT}}$	–	179	–	$\mu\text{J}$
Turn-on Switching Loss	$I_C = 5 \text{ A}$ , $T_j = 100^\circ\text{C}$	$E_{\text{ON}}$	–	136	–	$\mu\text{J}$
Turn-off Switching Loss		$E_{\text{OFF}}$	–	75	–	$\mu\text{J}$
Total Switching Loss		$E_{\text{TOT}}$	–	211	–	$\mu\text{J}$
Diode Reverse Recovery Energy	$I_C = 5 \text{ A}$ , $T_j = 100^\circ\text{C}$	$E_{\text{REC}}$	–	27	–	$\mu\text{J}$
Diode Reverse Recovery Time		$t_{\text{RR}}$	–	174	–	$\text{ns}$
Reverse Bias Safe Operating Area	$I_C = 20 \text{ A}$ , $V_{\text{CE}} = 450 \text{ V}$	RBSOA	Full Square			
Short Circuit Safe Operating Area	$V_{\text{CE}} = 400 \text{ V}$ , $T_j = 100^\circ\text{C}$	SCSOA	5	–	–	$\mu\text{s}$

**TYPICAL CHARACTERISTICS INV SECTION**

**Figure 4.  $V_{\text{CE}}$  vs.  $I_C$  for Different Temperatures ( $V_{\text{DD}} = 15 \text{ V}$ )**

**Figure 5.  $V_F$  vs.  $I_F$  for Different Temperatures**

**Figure 6.  $E_{\text{ON}}$  vs.  $I_C$  for Different Temperatures**

**Figure 7.  $E_{\text{OFF}}$  vs.  $I_C$  for Different Temperatures**

**TYPICAL CHARACTERISTICS INV SECTION****Figure 8. Thermal Impedance Plot****Figure 9. Turn-on Waveform**  
 $T_j = 100^\circ\text{C}$ ,  $V_{CC} = 300$  V**Figure 10. Turn-off Waveform**  
 $T_j = 100^\circ\text{C}$ ,  $V_{CC} = 300$  V

## APPLICATIONS INFORMATION

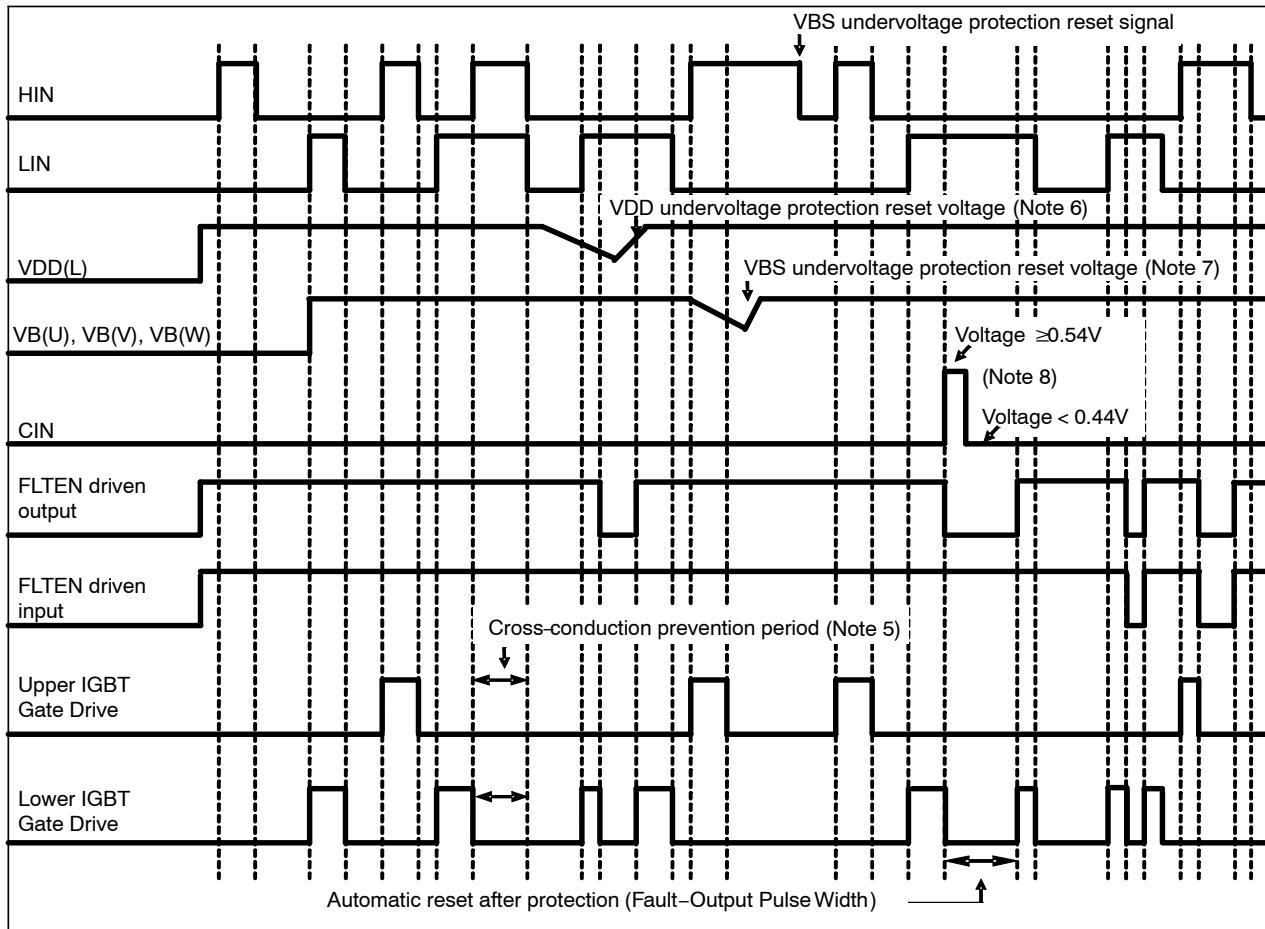


Figure 11. Input / Output Timing Chart

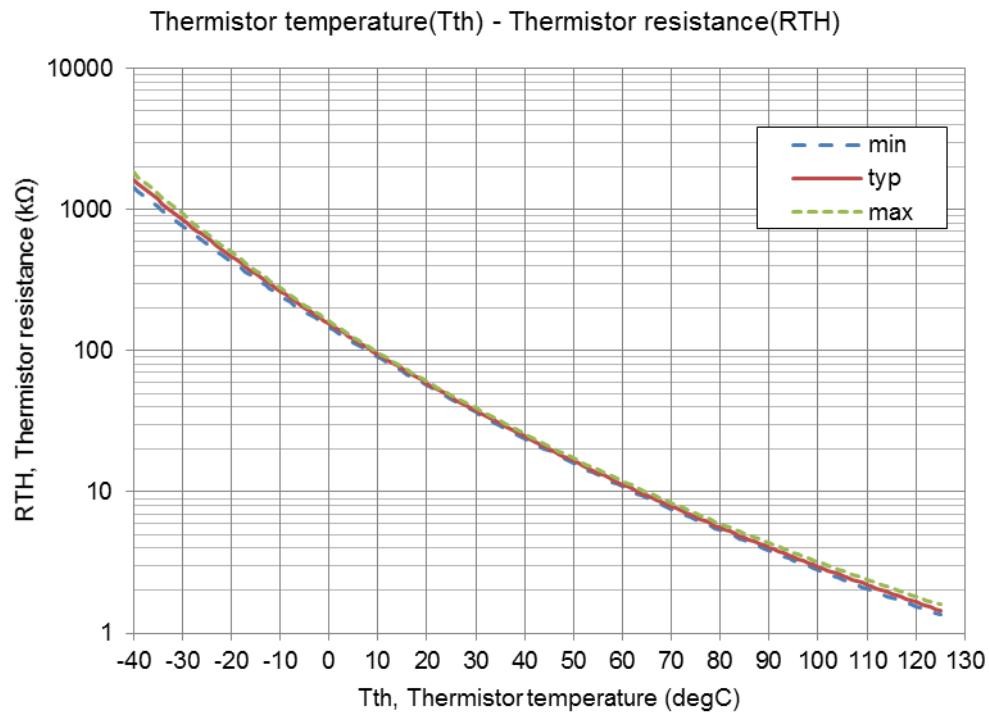
- This section of the timing diagram shows the effect of cross-conduction prevention.
- This section of the timing diagram shows that when the voltage on VDD(L) decreases sufficiently all gate output signals will go low, switching off all six IGBTs. When the voltage on VDD(L) rises sufficiently, normal operation will resume.
- This section shows that when the bootstrap voltage on VB(U) (VB(V), VB(W)) drops, the corresponding high side output U (V, W) is switched off. When the voltage on VB(U) (VB(V), VB(W)) rises sufficiently, normal operation will resume.
- This section shows that when the voltage on CIN exceeds the threshold, all IGBT's are turned off. Normal operation resumes later after the over-current condition is removed.

Table 6. INPUT / OUTPUT LOGIC TABLE

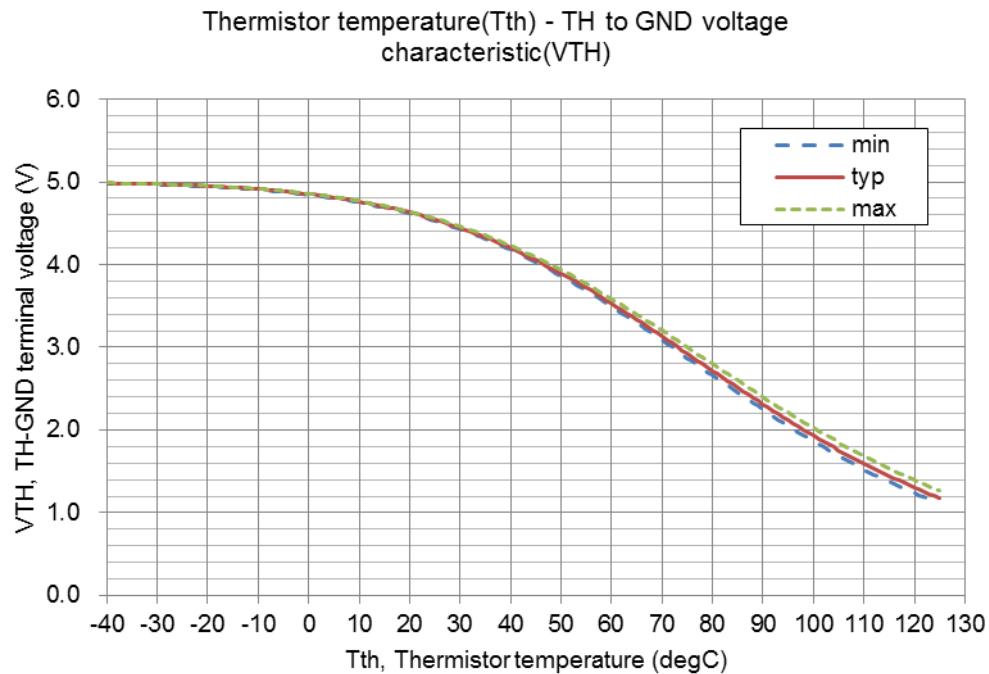
INPUT			OUTPUT			
HIN	LIN	ITRIP	High side IGBT	Low side IGBT	U,V,W	FAULT
H	L	L	ON	OFF	VP	OFF
L	H	L	OFF	ON	NU, NV, NW	OFF
L	L	L	OFF	OFF	High Impedance	OFF
H	H	L	OFF	OFF	High Impedance	OFF
X	X	H	OFF	OFF	High Impedance	ON

Table 7. THERMISTOR CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	$R_{25}$	$T_{th}=25^{\circ}\text{C}$	45.59	47	48.41	$\text{k}\Omega$
	$R_{125}$	$T_{th}=125^{\circ}\text{C}$	1.34	1.45	1.59	$\text{k}\Omega$
B-Constant (25 to 50°C)	B		3953	4021	4033	K
Temperature Range			-40		+125	$^{\circ}\text{C}$



**Figure 12. Thermistor Resistance vs. Thermistor Temperature**



**Figure 13. Thermistor Voltage vs. Thermistor Temperature**  
Conditions:  $RTH = 4.7 \text{ k}\Omega$ , pull-up voltage 5.0 V (see Figure 12)

**FLTEN Pin**

The FLTEN pin is connected to an open-drain FAULT output and an ENABLE input, it is required a pull-up resistor. If the pull-up voltage is 5 V, use a pull-up resistor with a value of 6.8 kΩ or higher. If the pull-up voltage is 15 V, use a pull-up resistor with a value of 20 kΩ or higher. The pulled up voltage in normal operation for the FLTEN pin should be above 2.5 V, noting that it is connected to an internal ENABLE input. The FAULT output is triggered if there is a VDD under-voltage or an overcurrent condition.

Driving the FLTEN terminal pin is used to enable or shut down the built-in driver. If the voltage on the FLTEN pin rises above the positive going ENABLE threshold, the output drivers are enabled. If the voltage on the FLTEN pin falls below the negative going ENABLE threshold, the drivers are disabled.

**Under-voltage Protection**

If VDD goes below the VDD supply under-voltage lockout falling threshold, the FAULT output is switched on. The FAULT output stays on until VDD rises above the VDD supply under-voltage lockout rising threshold. After VDD has risen above the threshold to enable normal operation, the driver waits to receive an input signal on the LIN input before enabling the driver for the HIN signal. The hysteresis is approximately 200 mV.

**Overcurrent Protection**

An over-current condition is detected if the voltage on the CIN pin is larger than the reference voltage. There is a blanking time of typically 350 ns to improve noise immunity. After a shutdown propagation delay of typically 0.9 μs, the FAULT output is switched on. The FAULT output is held on for 20 μs (minimum).

The over-current protection threshold should be set to be equal or lower to 2 times the module rated current (I<sub>o</sub>).

An additional fuse is recommended to protect against system level or abnormal over-current fault conditions.

**Capacitors on High Voltage and VDD Supplies**

Both the high voltage and VDD supplies require an electrolytic capacitor and an additional high frequency capacitor. The recommended value of the high frequency capacitor is between 100 nF and 10 μF.

**Minimum Input Pulse Width**

When input pulse width is less than 1 μs, an output may not react to the pulse. (Both ON signal and OFF signal)

**Calculation of Bootstrap Capacitor Value**

The bootstrap capacitor value C<sub>B</sub> is calculated using the following approach. The following parameters influence the choice of bootstrap capacitor:

- VBS: Bootstrap power supply.  
15 V is recommended.
- QG: Total gate charge of IGBT at VBS = 15 V.  
17 nC
- UVLO: Falling threshold for UVLO.  
Specified as 12 V.
- IDMAX: High-side drive power dissipation.  
Specified as 0.4 mA
- TONMAX: Maximum ON pulse width of high side IGBT.

**Capacitance Calculation Formula:**

$$CB = (QG + IDMAX * TONMAX) / (VBS - UVLO)$$

The relationship between TONMAX and C<sub>B</sub> becomes as follows. C<sub>B</sub> is recommended to be approximately 3 times the value calculated above. The recommended value of C<sub>B</sub> is in the range of 1 to 47 μF, however, the value needs to be verified prior to production. When not using the bootstrap circuit, each high side driver power supply requires an external independent power supply.

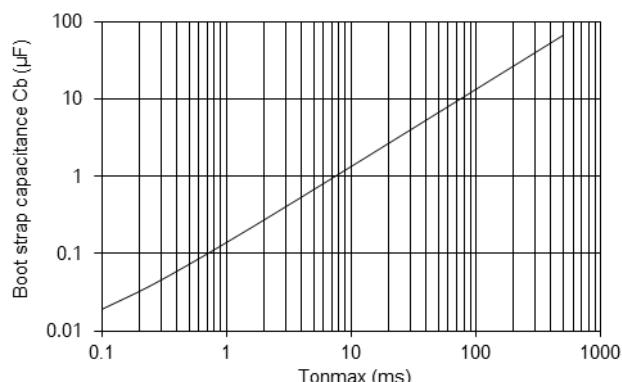


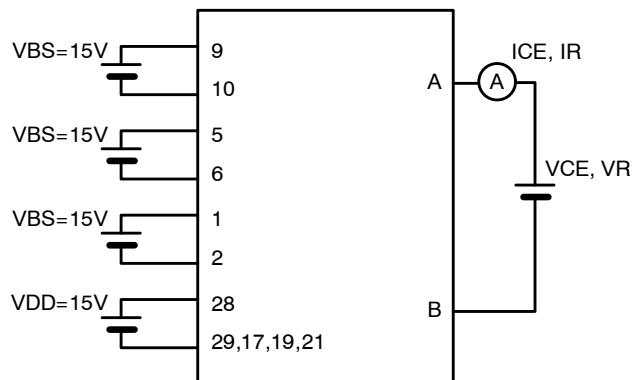
Figure 14. Bootstrap Capacitance vs. Tonmax

**TEST CIRCUITS**
**I<sub>ces</sub>, I<sub>R</sub>(DB)**

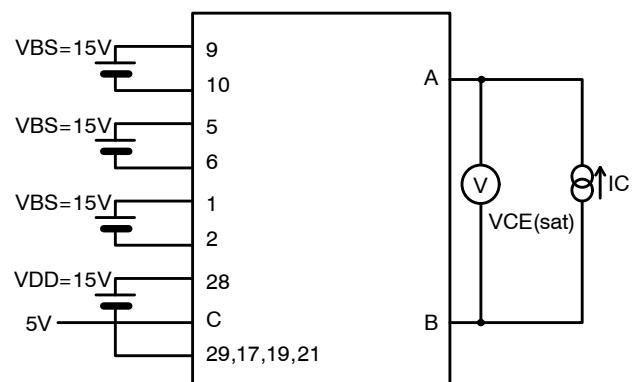
	U <sub>+</sub>	V <sub>+</sub>	W <sub>+</sub>	U <sub>-</sub>	V <sub>-</sub>	W <sub>-</sub>
A	13	13	13	10	6	2
B	10	6	2	17	19	21

U<sub>+</sub>,V<sub>+</sub>,W<sub>+</sub> : High side phase  
U<sub>-</sub>,V<sub>-</sub>,W<sub>-</sub> : Low side phase

	U(DB)	V(DB)	W(DB)
A	9	5	1
B	29	29	29


**Figure 15. Test Circuit for I<sub>CE</sub>**
**V<sub>CE</sub>(sat) (Test by pulse)**

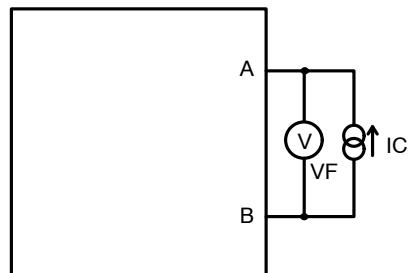
	U <sub>+</sub>	V <sub>+</sub>	W <sub>+</sub>	U <sub>-</sub>	V <sub>-</sub>	W <sub>-</sub>
A	13	13	13	10	6	2
B	10	6	2	17	19	21
C	20	22	23	24	25	26


**Figure 16. Test Circuit for V<sub>CE</sub>(SAT)**
**V<sub>F</sub> (Test by pulse)**

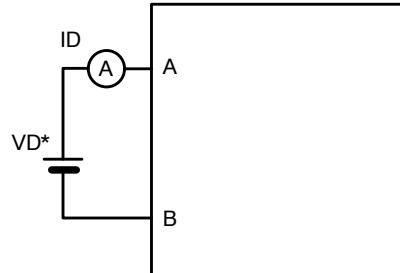
	U <sub>+</sub>	V <sub>+</sub>	W <sub>+</sub>	U <sub>-</sub>	V <sub>-</sub>	W <sub>-</sub>
A	13	13	13	10	6	2
B	10	6	2	17	19	21

	U(DB)	V(DB)	W(DB)
A	9	5	1
B	28	28	28


**Figure 17. Test Circuit for V<sub>F</sub>**
**I<sub>QBS</sub>, I<sub>QDDL</sub>**

	VBS U <sub>+</sub>	VBS V <sub>+</sub>	VBS W <sub>+</sub>	V <sub>DD</sub>
A	9	5	1	28
B	10	6	2	29


**Figure 18. Test Circuit for I<sub>D</sub>**

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**SWITCHING TIME** (The circuit is a representative example of the lower side U phase.)

	U+	V+	W+	U-	V-	W-
A	13	13	13	13	13	13
B	17	19	21	17	19	21
C	10	6	2	13	13	13
D	17	19	21	10	6	2
E	20	22	23	24	25	26

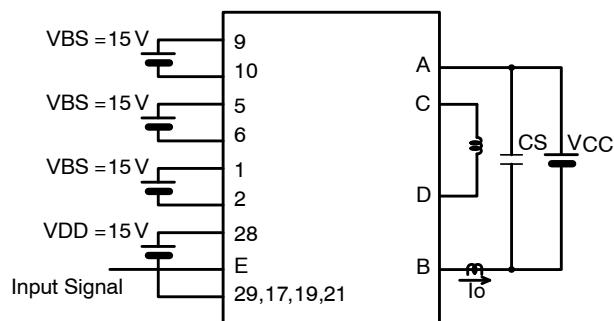
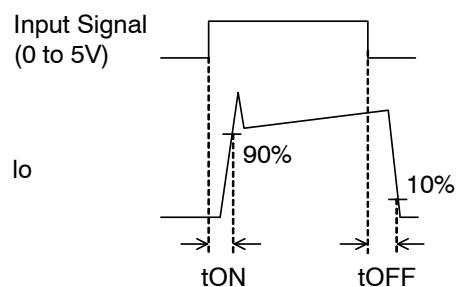


Figure 19. Test Circuit for Switching Time



# NFAP1060L3TT

## PACKAGE DIMENSIONS

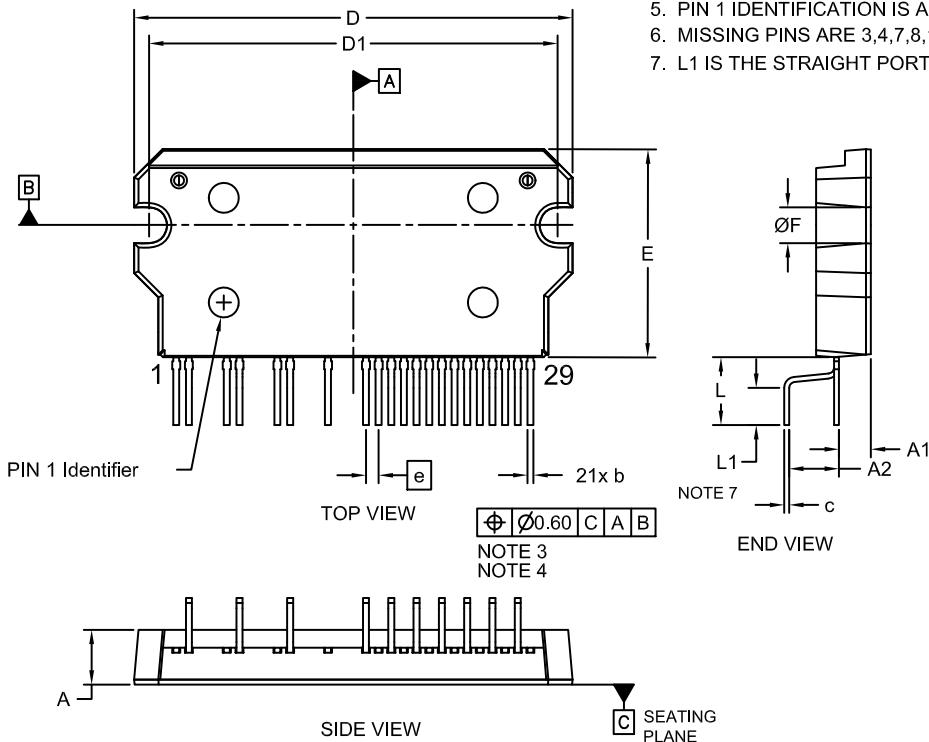
### SIP29, 44.0x20.9 FP-1

CASE 127FB

ISSUE O

#### NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b and c APPLY TO THE PLATED LEADS AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP.
4. POSITION OF THE LEAD IS DETERMINED AT THE ROOT OF THE LEAD WHERE IT EXITS THE PACKAGE BODY.
5. PIN 1 IDENTIFICATION IS A MIRRORED SURFACE INDENT.
6. MISSING PINS ARE 3,4,7,8,11,12,14 AND 15.
7. L1 IS THE STRAIGHT PORTION OF THE LEAD AFTER THE BEND.



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