

Intelligent Power Module (IPM)

Inverter, 1200 V, 25 A

NFAM2512L7B

General Description

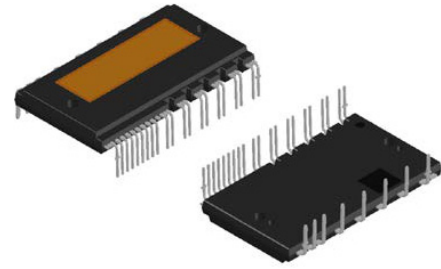
NFAM2512L7B is an advanced IPM module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC and PMSM motors. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts, over-current shutdown, thermal monitoring of drive IC, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

Features

- 1200 V 25 A 3-Phase FS7 IGBT Inverter, Including Control ICs for Gate Drive and Protections
- Very Low Thermal Resistance Using Al₂O₃ DBC Substrate
- Active Logic Interface
- Built-in Under-voltage Protection (UVP)
- Built-In Bootstrap Diodes/Resistors
- Separate Low-side IGBT Emitter Connections for Individual Current Sensing of Each Phase
- Temperature Sensor (TSU Output by LVIC)
- UL Certification: E209204
- This is a Pb-Free Device

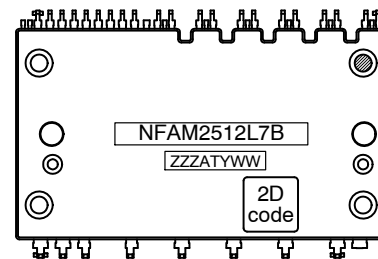
Typical Application

- Industrial Drives
- Industrial Pumps
- Industrial Fans
- Industrial Automation



CASE MODGX
DIP39, 54.5x31.0 EP-2

MARKING DIAGRAM



NFAM2512L7B = Specific Device Code
 ZZZ = Assembly Lot Code
 A = Assembly Location
 T = Test Location
 Y = Year
 WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping [†] (Qty / Packing)
NFAM2512L7B	DIP39, 31.0x54.5 (Pb-Free)	90 / BOX

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PIN CONFIGURATION

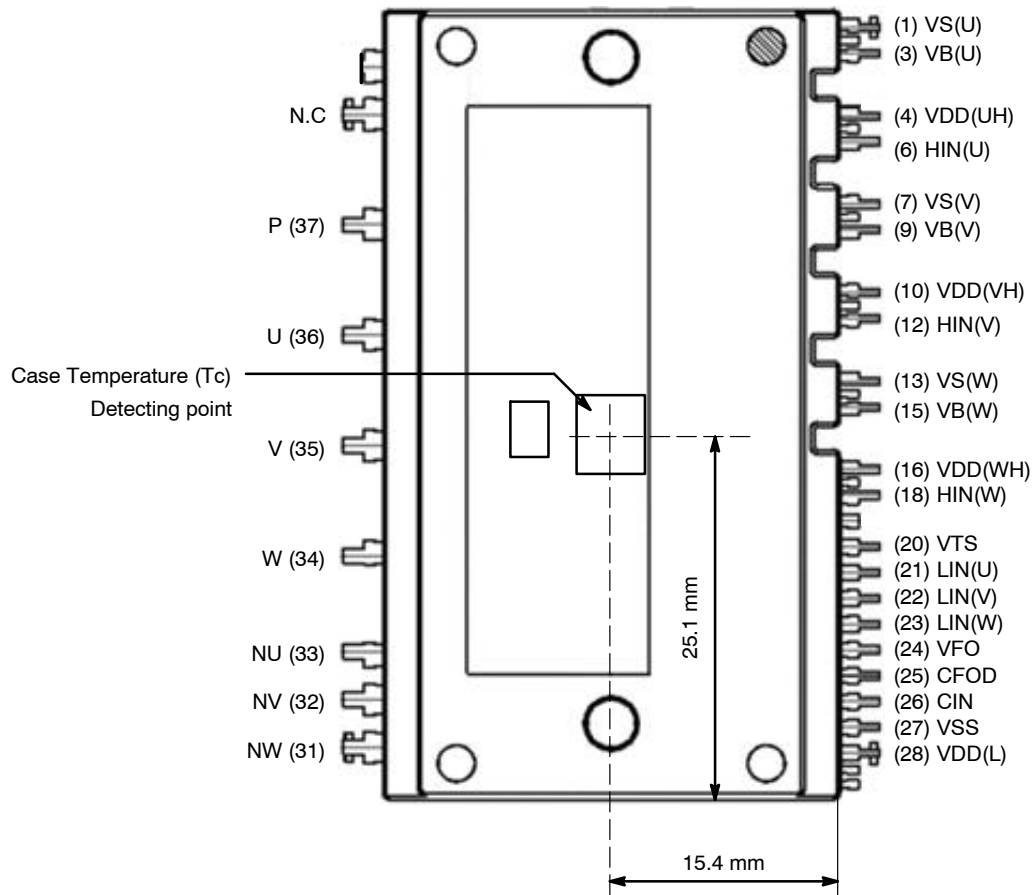


Figure 1. Pin Configuration – Top View

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PIN DESCRIPTION

Pin Number	Name	Description
1	VS(U)	High-Side Bias Voltage Ground for U-Phase IGBT Driving
(2)	–	Dummy
3	VB(U)	High-Side Bias Voltage for U-Phase IGBT Driving
4	VDD(UH)	High-Side Bias Voltage for U-Phase IC
(5)	–	Dummy
6	HIN(U)	Signal Input for High-Side U-Phase
7	VS(V)	High-Side Bias Voltage Ground for V-Phase IGBT Driving
(8)	–	Dummy
9	VB(V)	High-Side Bias Voltage for V-Phase IGBT Driving
10	VDD(VH)	High-Side Bias Voltage for V-Phase IC
(11)	–	Dummy
12	HIN(V)	Signal Input for High-Side V-Phase
13	VS(W)	High-Side Bias Voltage Ground for W-Phase IGBT Driving
(14)	–	Dummy
15	VB(W)	High-Side Bias Voltage for W-Phase IGBT Driving
16	VDD(WH)	High-Side Bias Voltage for W-Phase IC
(17)	–	Dummy
18	HIN(W)	Signal Input for High-Side W-Phase
(19)	–	Dummy
20	VTs	Output for LVIC Temperature Sensing Voltage
21	LIN(U)	Signal Input for Low-Side U-Phase
22	LIN(V)	Signal Input for Low-Side V-Phase
23	LIN(W)	Signal Input for Low-Side W-Phase
24	VFO	Fault Output
25	CFOD	Capacitor for Fault Output Duration Selection
26	CIN	Input for Over Current Protection
27	VSS	Low-Side Common Supply Ground
28	VDD(L)	Low-Side Bias Voltage for IC and IGBTs Driving
(29)	–	Dummy
(30)	–	Dummy
31	NW	Negative DC-Link Input for W Phase
32	NV	Negative DC-Link Input for V-Phase
33	NU	Negative DC-Link Input for U-Phase
34	W	Output for W-Phase
35	V	Output for V-Phase
36	U	Output for U-Phase
37	P	Positive DC-Link Input
38	N.C	No Connection
(39)	–	Dummy

*Pins of () are the dummy for internal connection. These pins should be no connection.

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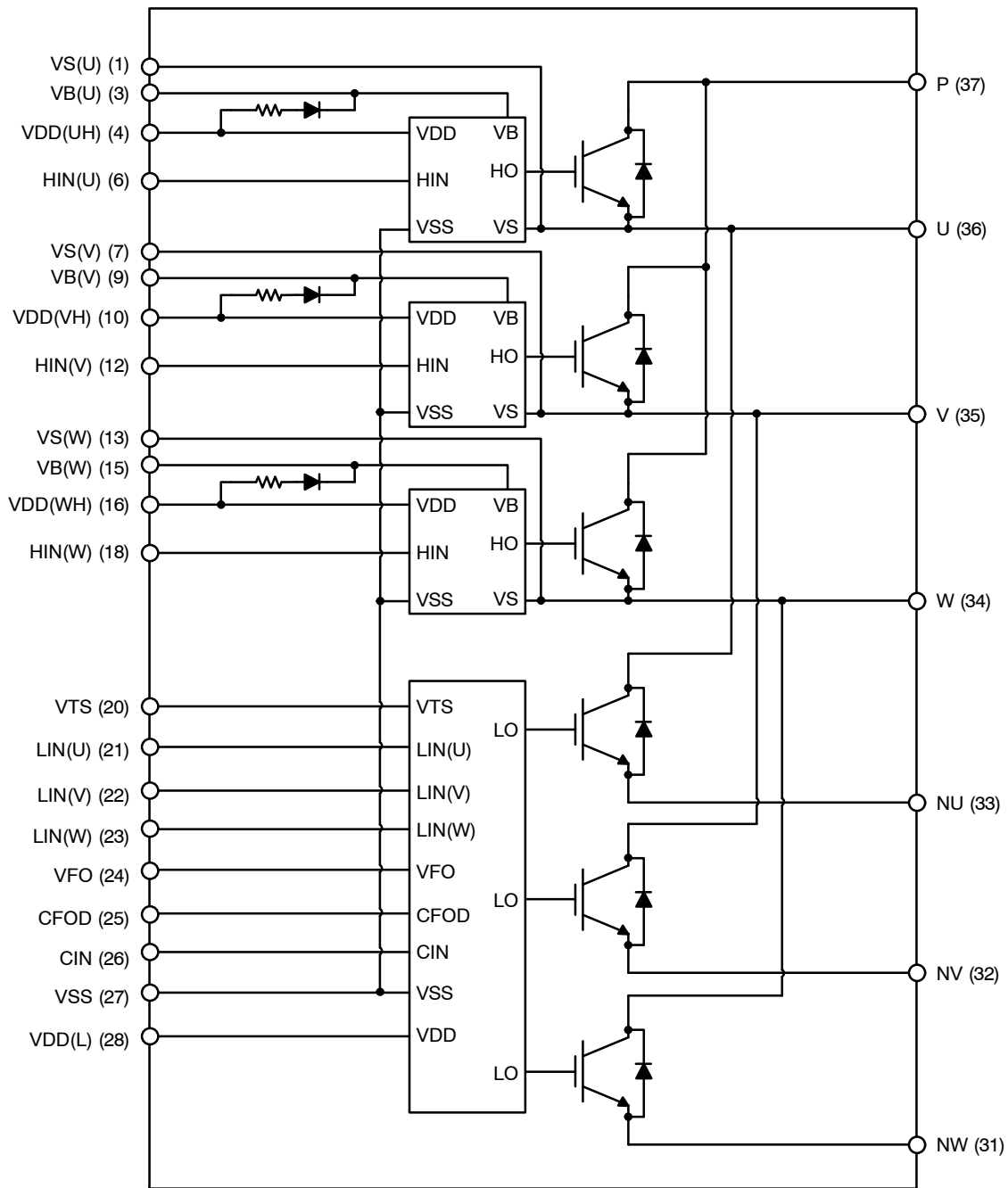


Figure 2. Equivalent Block Diagram

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ABSOLUTE MAXIMUM RATINGS (VDD = 15 V and Tj = 25°C unless otherwise noted)

Symbol	Description	Conditions	Ratings	Unit
INVERTER PART				
VPN	Supply Voltage	Applied between P – NU, NV, NW	900	V
VPN(surge)	Supply Voltage (Surge)	Applied between P – NU, NV, NW (Note 1)	1000	V
Vces	Collector – Emitter Voltage		1200	V
VRRM	Maximum Repetitive Reverse Voltage		1200	V
±Ic	Each IGBT Collector Current		25	A
±Icp	Each IGBT Collector Current (Peak)	Tc = 25°C, Tj ≤ 150°C, under 1 ms Pulse Width	50	A
Pc	Collector Dissipation	Tc = 25°C per One Chip (Note 2)	156	W
Tj	Operating Junction Temperature		–40~150	°C

CONTROL PART

VDD	Control Supply Voltage	Applied between VDD(H), VDD(L) – VSS	20	V
VBS	High-Side Control Bias Voltage	Applied between VB(U) – VS(U), VB(V) – VS(V), VB(W) – VS(W)	20	V
VIN	Input Signal Voltage	Applied between HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W) – VSS	–0.3~VDD + 0.3	V
VFO	Fault Output Supply Voltage	Applied between VFO – VSS	–0.3~VDD + 0.3	V
IFO	Fault Output Current	Sink Current at VFO pin	2	mA
VCIN	Current Sensing Input Voltage	Applied between CIN – VSS	–0.3~VDD + 0.3	V

TOTAL SYSTEM

VPN(PROT)	Self-Protection Supply Voltage Limit (Short Circuit Protection Capability)	VDD = VBS = 13.5~16.5 V, Tj = 150°C, Non-repetitive, <2 μs	800	V
Tc	Case Operation Temperature	See Figure 1	–40~125	°C
Tstg	Storage Temperature		–40~125	°C
Viso	Isolation Voltage	60 Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat Sink Plate	2500	V _{rms}

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surge voltage developed by the switching operation due to the wiring inductance between P and NU, NV, NW terminal.
2. Calculation value considered to design factor.

THERMAL RESISTANCE

Symbol	Description	Conditions	Min	Typ	Max	Unit
Rth(j–c)Q	Junction to Case Thermal Resistance (Note 3)	Inverter IGBT part (per 1/6 module)	–	–	0.8	°C/W
Rth(j–c)F		Inverter FRD part (per 1/6 module)	–	–	1.2	°C/W

3. For the measurement point of case temperature (Tc), please refer to Figure 1.

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ELECTRICAL CHARACTERISTICS (VDD = 15 V and Tj = 25°C unless otherwise noted)

Symbol		Parameter	Test Conditions		Min	Typ	Max	Unit
INVERTER PART								
Ices		Collector – Emitter Leakage Current	Tj = 25°C, VCE = VCES	–	–	1	mA	
			Tj = 150°C, VCE = VCES	–	–	10	mA	
VCE(sat)		Collector – Emitter Saturation Voltage	VDD = VBS = 15 V, Ic = 20 A, Tj = 25°C	–	1.50	1.90	V	
			VDD = VBS = 15 V, Ic = 20 A, Tj = 150°C	–	1.75	–	V	
VF		FWDi Forward Voltage	VIN = 0 V, IF = 20 A, Tj = 25°C	–	1.70	2.10	V	
			VIN = 0 V, IF = 20 A, Tj = 150°C	–	1.65	–	V	
HS	ton	High Side Switching Times	VPN = 600 V, VDD = 15 V, Ic = 20 A Tj = 25°C, Inductive Load Switching See Figure 3, 24, 25 (Note 4)	1.00	1.35	1.90	μs	
	tc(on)			–	0.16	0.55	μs	
	toff			–	1.55	2.00	μs	
	tc(off)			–	0.21	0.30	μs	
	trr			–	0.23	–	μs	
LS	ton	Low Side Switching Times		1.00	1.44	1.90	μs	
	tc(on)			–	0.21	0.55	μs	
	toff			–	1.60	2.00	μs	
	tc(off)			–	0.21	0.30	μs	
	trr			–	0.25	–	μs	
CONTROL PART								
IQDDH		Quiescent VDD Supply Current	VDD(UH, VH, WH) = 15 V, HIN(U,V,W) = 0 V	VDD(UH) – VSS VDD(VH) – VSS VDD(WH) – VSS	–	–	0.3	mA
IQDDL			VDD(L) = 15 V, LIN(U, V, W) = 0 V	VDD(L) – VSS	–	–	2.0	mA
IPDDH		Operating VDD Supply Current	VDD(UH, VH, WH) = 15 V, fPWM = 20 kHz, duty = 50%, applied to one PWM Signal Input for High-Side	VDD(UH) – VSS VDD(VH) – VSS VDD(WH) – VSS	–	–	0.4	mA
IPDDL			VDD(L) = 15 V, fPWM = 20 kHz, duty = 50%, applied to one PWM Signal Input for Low-Side	VDD(L) – VSS	–	–	5.0	mA
IQBS		Quiescent VBS Supply Current	VBS(U, V, W) = 15 V, HIN(U, V, W) = 0 V	VB(U) – VS(U), VB(V) – VS(V), VB(W) – VS(W)	–	–	0.3	mA
IPBS		Operating VBS Supply Current	VDD(UH,VH,WH) = VBS(U, V, W) = 15 V, fPWM = 20 kHz, duty = 50%, applied to one PWM Signal Input for High-Side	VB(U) – VS(U), VB(V) – VS(V), VB(W) – VS(W)	–	–	3.5	mA
VIN(ON)		ON Threshold Voltage	HIN(U, V, W) – VSS, LIN(U, V, W) – VSS		–	–	2.6	V
VIN(OFF)		OFF Threshold Voltage			0.8	–	–	V
VCIN(ref)		Over Current Trip Level	VDD = 15 V	CIN – VSS	0.46	0.48	0.50	V
UVDDD		Supply Circuit Under-Voltage Protection	Detection Level		10.3	–	12.5	V
UVDDR			Reset Level		10.8	–	13.0	V
UVBSD		Supply Circuit Under-Voltage Protection	Detection Level		10.0	–	12.0	V
UVBSR			Reset Level		10.5	–	12.5	V
VTS		Voltage Output for LVIC Temperature Sensing Unit	VTS–VSS = 5.1 kΩ, Temp. = 25°C (Note 5)		1.12	1.25	1.38	mV
VFOH		Fault Output Voltage	VDD(L) = 0 V, CIN = 0 V, VFO Circuit: 10 kΩ to 5 V Pull-up		4.9	–	–	V
VFOL			VDD(L) = 0 V, CIN = 1 V, VFO Circuit: 10 kΩ to 5 V Pull-up		–	–	0.95	V
tFOD		Fault-Out Pulse Width	CFOD = 22 nF (Note 6)		1.6	2.4	–	ms

ELECTRICAL CHARACTERISTICS (VDD = 15 V and Tj = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BOOTSTRAP PART						
VF	Bootstrap Diode Forward Current	If = 0.1 A (See Figure 6)	2.1	2.5	2.9	V
RBOOT	Built-in Limiting Resistance		12.5	15.5	18.5	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at Tj = Ta = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

Values based on design and/or characterization.

- ton and toff include the propagation delay of the internal drive IC. tc(on) and tc(off) are the switching times of IGBT under the given gate*driving condition internally. For the detailed information, please see Figure 3.
- TLVIC is the temperature of LVIC itself. VTS is only for sensing temperature of LVIC and cannot shutdown IGBTs automatically. The relationship between VTS voltage output and LVIC temperature is described in Figure 4. It is recommended to add 5.1 kΩ pull down resistor between VTS and VSS (Signal Ground) as described in Figure 5 for linear output characteristics at low temperature. Refer to the application note for usage of VTS.
- The fault-out pulse width tFOD depends on the capacitance value of CFOD according to the following approximate equation:

$$tFOD = 0.11 \times 10^6 \times CFOD \text{ (s)}$$

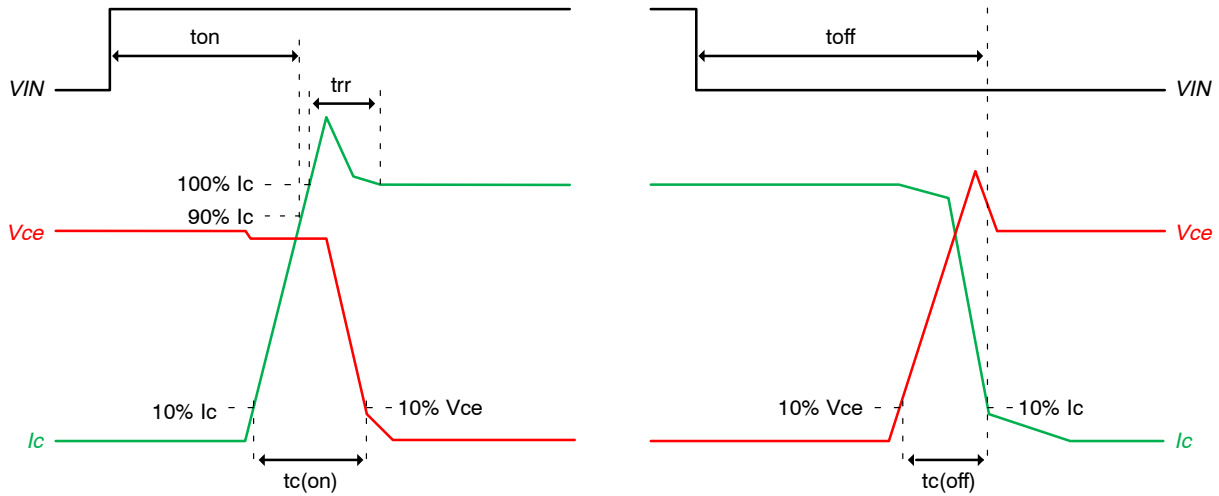


Figure 3. Switching Time Definition

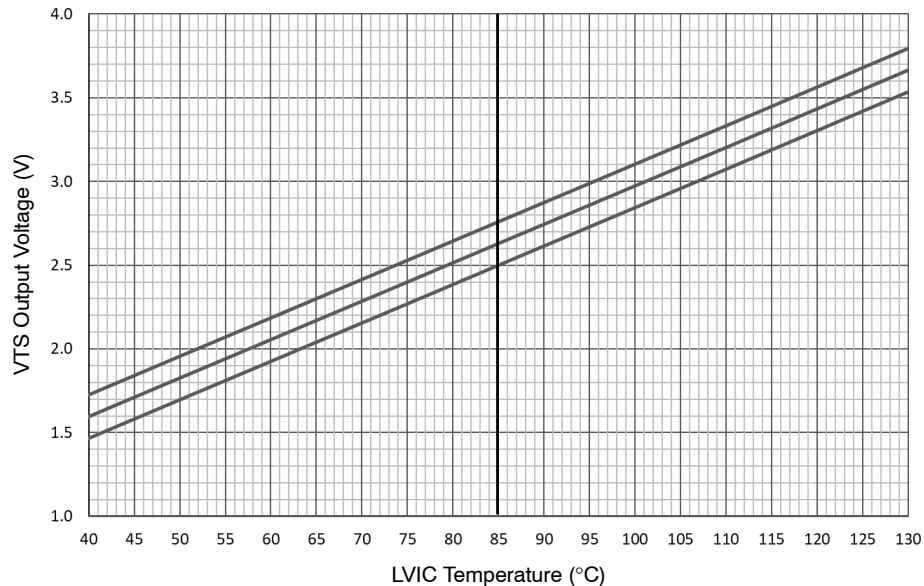


Figure 4. Temperature of LVIC vs. VTS Characteristics

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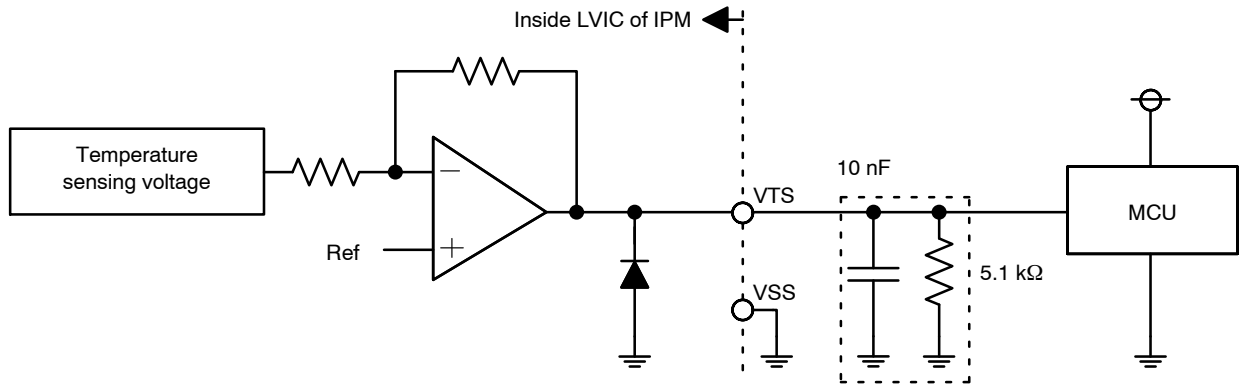


Figure 5. Internal Block Diagram and Interface Circuit of VTS

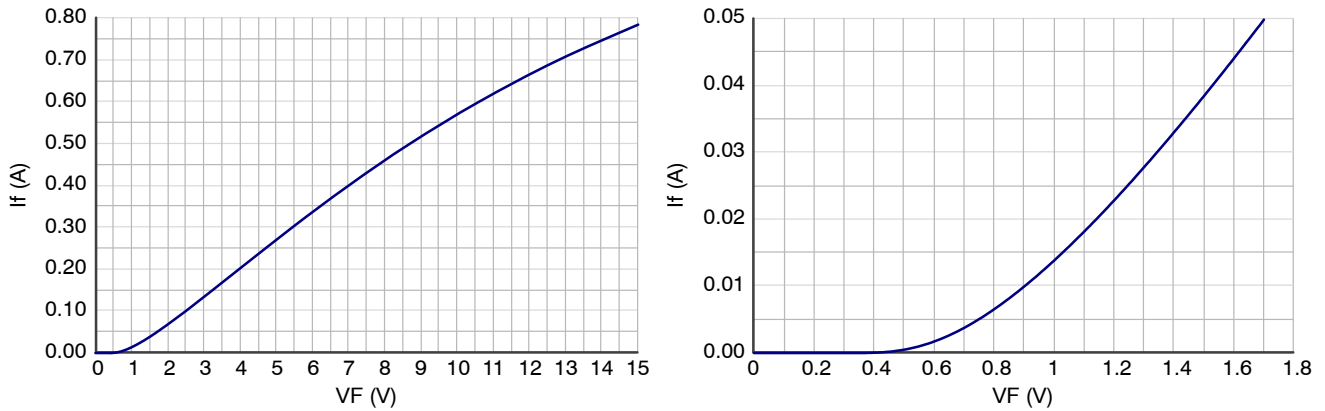


Figure 6. Characteristics of Bootstrap Diode/Resistor (Right Figure is Enlarged Figure)

RECOMMENDED OPERATING CONDITIONS

Symbol	Description	Conditions	Value			Unit	
			Min	Typ	Max		
VPN	Supply Voltage	Applied between P – NU, NV, NW	–	600	800	V	
VDD	Control Supply Voltage	Applied between VDD(H) – VSS, VDD(L) – VSS	13.5	15	16.5	V	
VBS	High–Side Bias Voltage	Applied between VB(U) – VS(U), VB(V) – VS(V), VB(W) – VS(W)	13.0	15	18.5	V	
dVDD / dt, dVBS / dt	Control Supply Variation		–1	–	1	V/μs	
Tdead	Blanking Time for Preventing Arm – Short	For Each Input Signal	1.5	–	–	μs	
fPWM	PWM Input Signal	–40°C ≤ Tc ≤ 125°C, –40°C ≤ Tj ≤ 150°C	1	–	20	kHz	
Io	Allowable r.m.s. Current	VPN = 600 V, VDD = VBS = 15 V, P.F. = 0.8, Tc ≤ 125°C, Tj ≤ 150°C (Note 7)	fPWM = 5 kHz	–	–	24.7	A rms
		fPWM = 15 kHz	–	–	14.3	A rms	
PWIN(ON)	Minimum Input Pulse Width	VDD = VBS = 15 V, Wiring Inductance between NU, V, W and DC Link N < 10 nH (Note 8)	1.0	–	–	μs	
PWIN(OFF)			2.0	–	–		
Package Mounting Torque		M3 Type Screw	0.6	0.7	0.9	Nm	

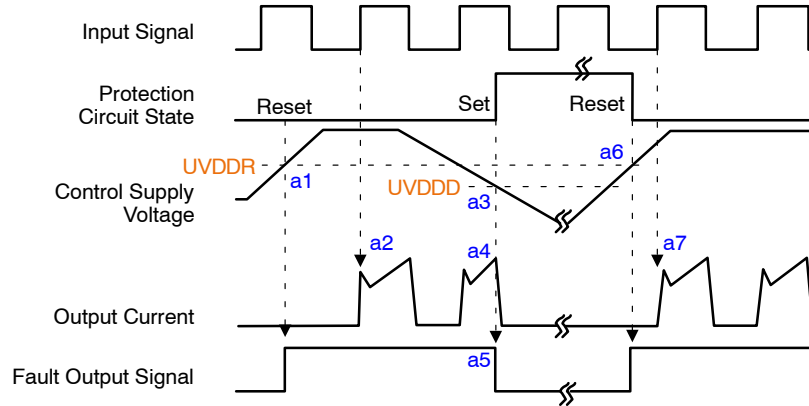
Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Flatness tolerance of the heatsink should be within –5 μm to +10 μm.

7. Allowable output current value is the reference data for the safe operation of this product. This may be different from the actual application and operating condition.

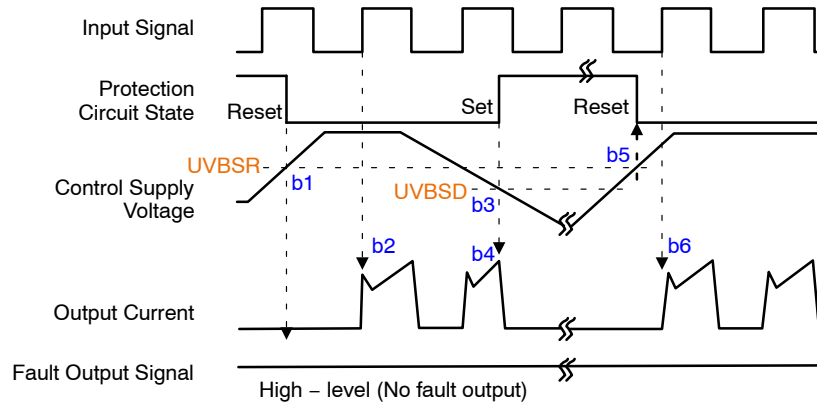
8. Product might not make response if input pulse width is less than the recommended value.

Time Charts of Protective Function



- a1: Control supply voltage rises: After the voltage rises UVDDR, the circuits start to operate when next input is applied.
- a2: Normal operation: IGBT ON and carrying current.
- a3: Under voltage detection (UVDDD).
- a4: IGBT OFF in spite of control input condition.
- a5: Fault output operation starts with a fixed pulse width.
- a6: Under voltage reset (UVDDR).
- a7: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

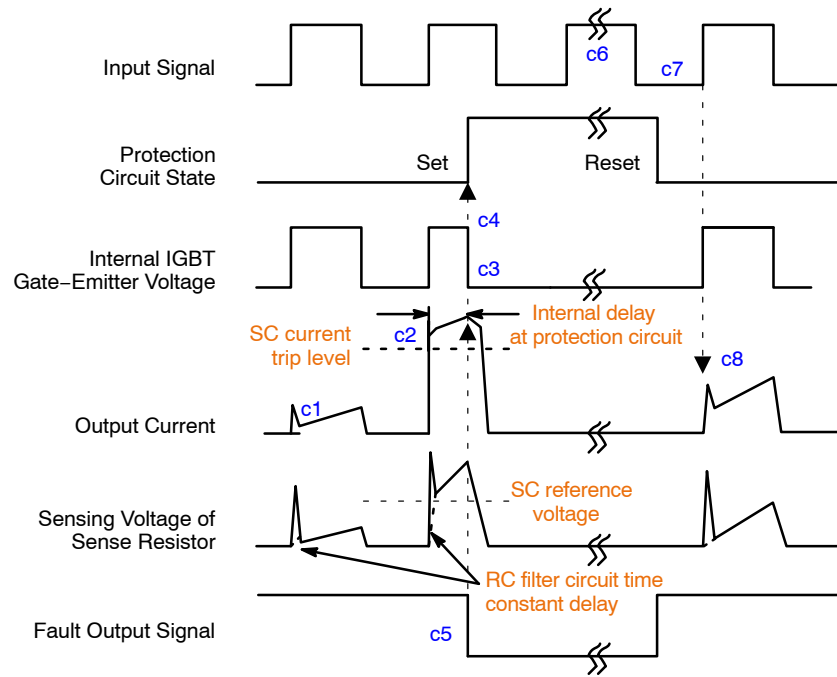
Figure 7. Under-Voltage Protection (Low-Side)



- b1: Control supply voltage rises: After the voltage reaches UVBSR, the circuits start to operate when next input is applied.
- b2: Normal operation: IGBT ON and carrying current.
- b3: Under voltage detection (UVBSD).
- b4: IGBT OFF in spite of control input condition, but there is no fault output signal.
- b5: Under voltage reset (UVBSR).
- b6: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

Figure 8. Under-Voltage Protection (High-Side)

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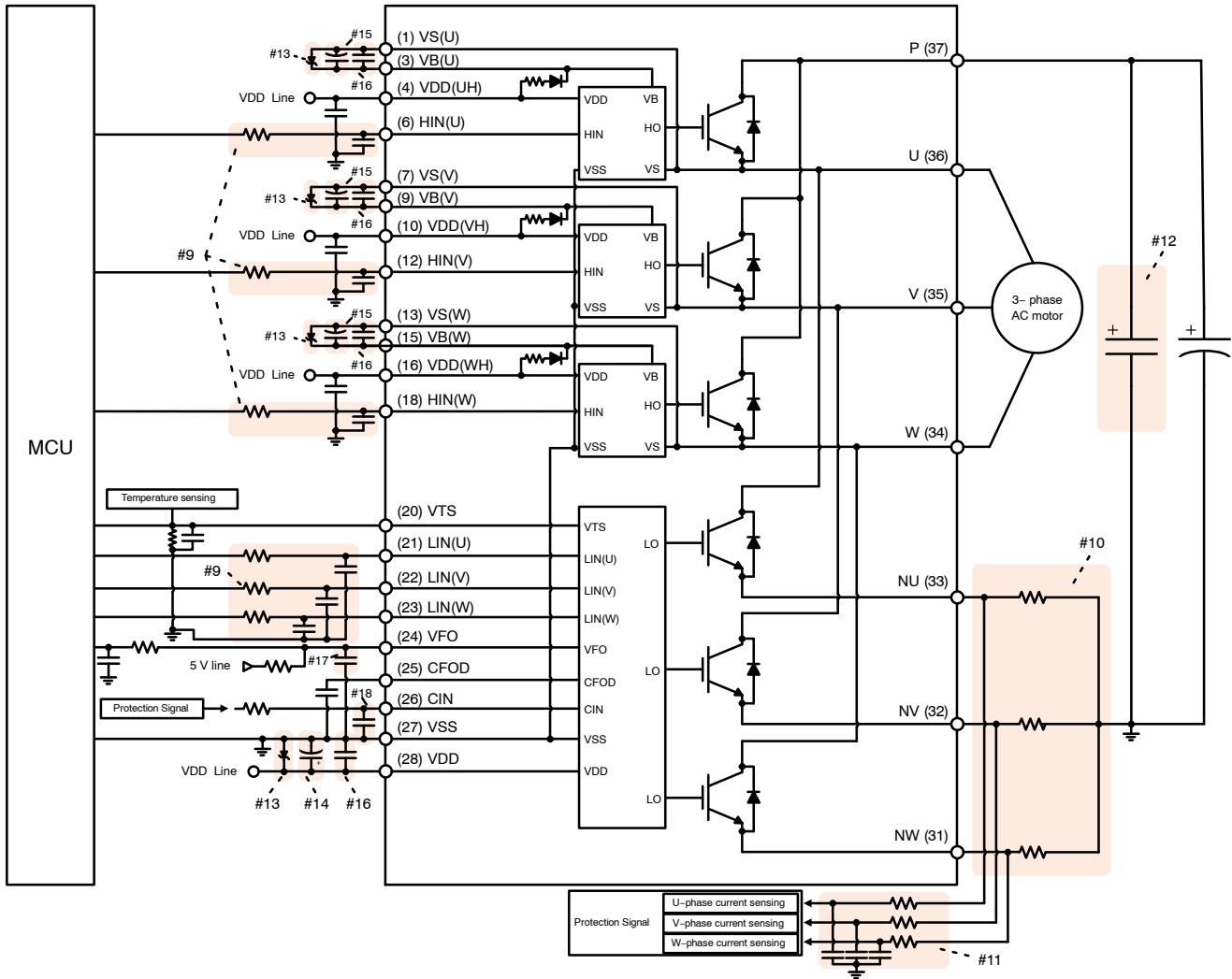
(with the external sense resistance and RC filter connection)

- c1: Normal operation: IGBT ON and carrying current.
- c2: Short circuit current detection (SC trigger).
- c3: All low-side IGBT's gate are hard interrupted.
- c4: All low-side IGBTs turn OFF.
- c5: Fault output operation starts with a fixed pulse width.
- c6: Input HIGH: IGBT ON state, but during the active period of fault output the IGBT doesn't turn ON.
- c7: Fault output operation finishes, but IGBT doesn't turn on until triggering next signal from LOW to HIGH.
- c8: Normal operation: IGBT ON and carrying current.

Figure 9. Short-Circuit Current Protection (Low-Side Operation Only)

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TYPICAL APPLICATION CIRCUIT



To avoid malfunction, the wiring of each input should be as short as possible (less than 2–3 cm). Each capacitor should be mounted as close to the pins of the product as possible. VFO output is open-drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes IFO up to 1 mA. Please refer to Figure 5.

NOTE:

9. Input signal is active-HIGH type. There is a 5 kΩ resistor inside the IC to pull-down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. RC time constant should be selected in the range 50~150 ns. (Recommended R = 100 Ω, C = 1 nF)
10. Each wiring pattern inductance should be minimized (Recommend less than 10 nH). Use the shunt resistor of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring should be connected to the terminal of the shunt resistor as close as possible.
11. In the short-circuit protection circuit, please select the RC time constant in the range 1.5~2 μs. Do enough evaluation on the real system because short-circuit protection time may vary wiring pattern layout and value of the RC time constant.
12. To prevent surge destruction, the wiring between the snubber capacitor and the P & GND pins should be as short as possible. The use of a high-frequency non-inductive capacitor of around 0.1~0.22 μF between the P & GND pins is recommended.
13. The zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (Recommended zener diode is 22 V / 1 W, which has the lower zener impedance characteristic than about 15 Ω).
14. VDD electrolytic capacitor is recommended around 7 times larger than VBS electrolytic bootstrap capacitor.
15. Please choose the VBS electrolytic bootstrap capacitor with good temperature characteristic.
16. 0.1~0.2 μF R-category ceramic capacitors with good temperature and frequency characteristics is recommended.
17. Fault out pulse width can be adjusted by capacitor connected to the CFOD terminal.
18. To prevent protection function errors, CIN capacitor should be placed as close to CIN and VSS pins as possible.

Figure 10. Typical Application Circuit

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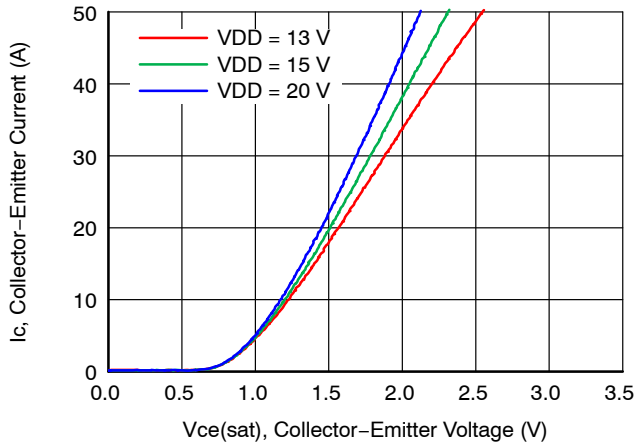


Figure 11. Collector-Emitter Saturation Voltage

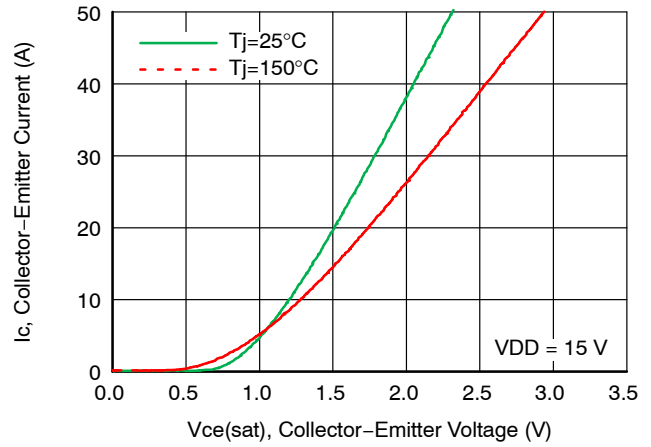


Figure 12. Collector-Emitter Saturation Voltage

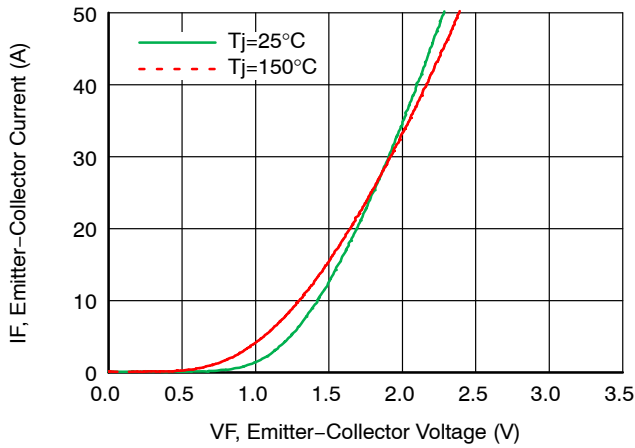


Figure 13. Collector-Emitter Forward Voltage

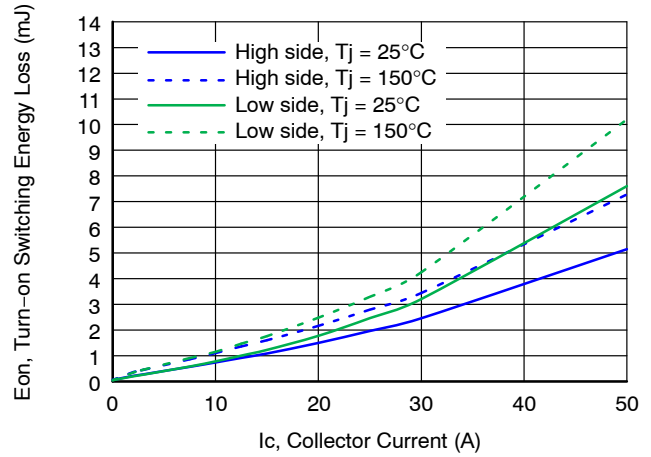


Figure 14. Typ. Turn-on Switching Energy Loss

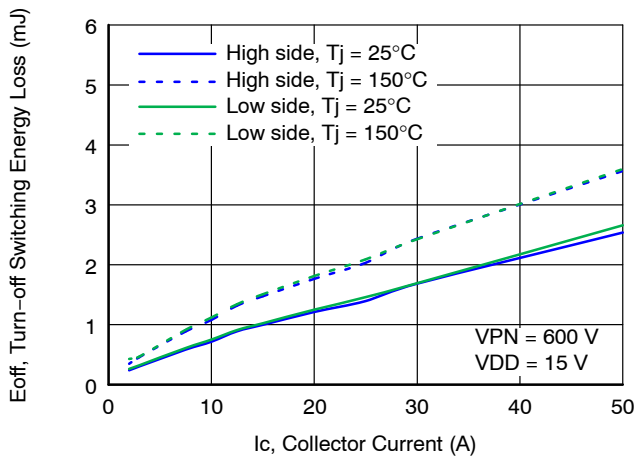


Figure 15. Typ. Turn-off Switching Energy Loss

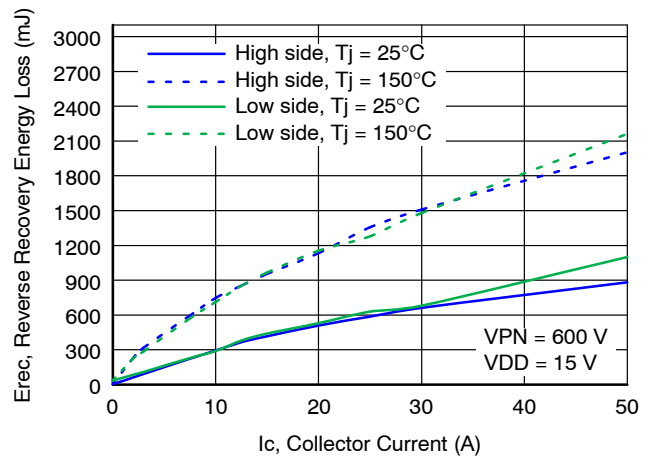


Figure 16. Typ. Reverse Recovery Energy Loss

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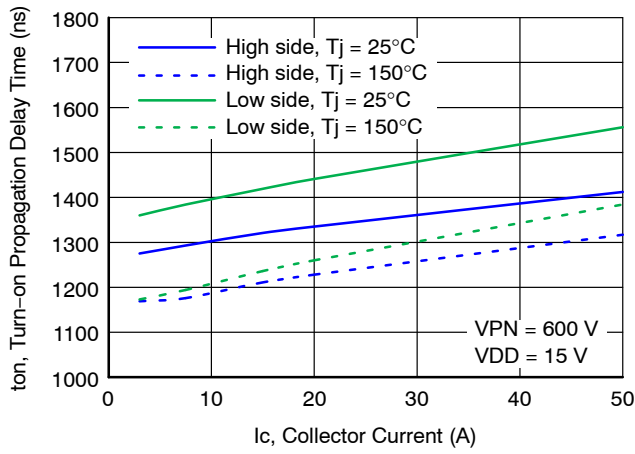


Figure 17. Turn-on Propagation Delay Time

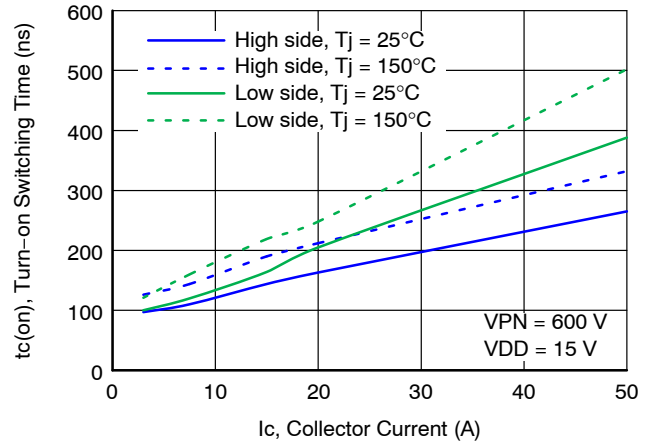


Figure 18. Typ. Turn-on Switching Time

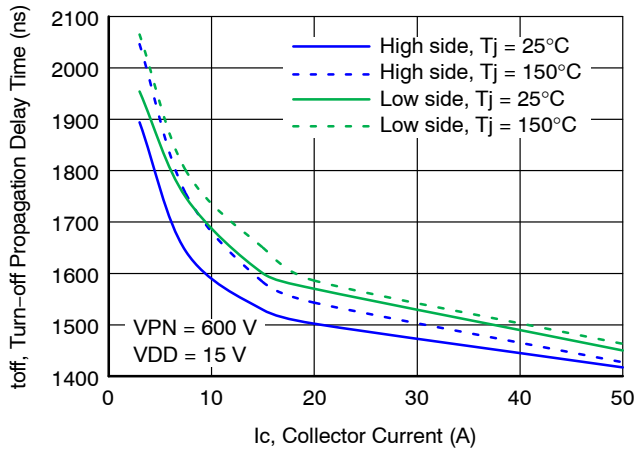


Figure 19. Turn-off Propagation Delay Time

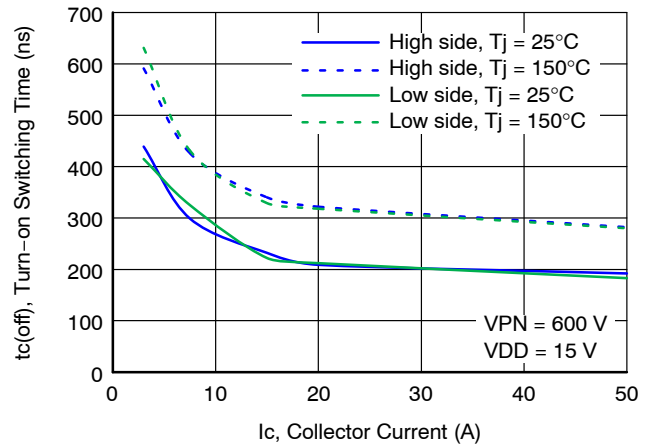


Figure 20. Typ. Turn-off Switching Time

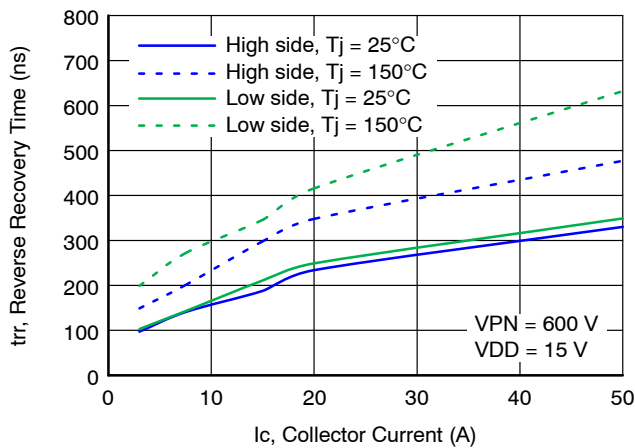


Figure 21. Typ. Reverse Recovery Time

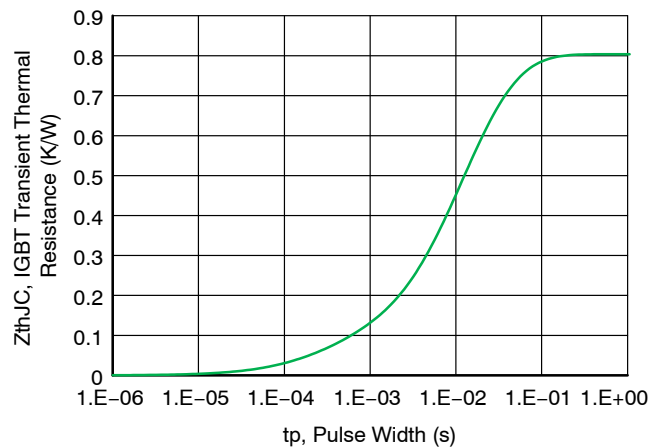


Figure 22. IGBT Transient Thermal Resistance

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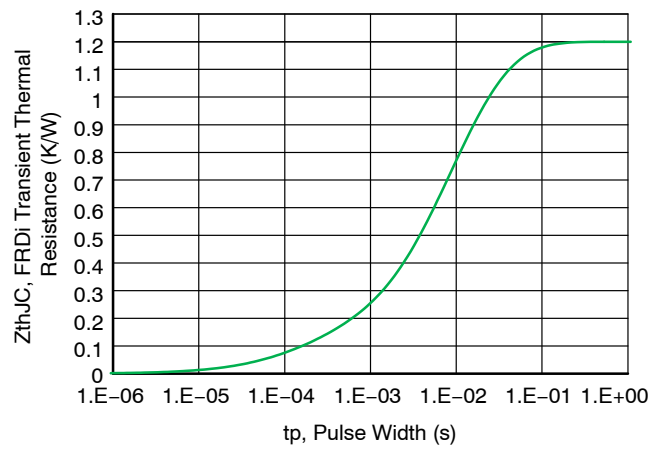


Figure 23. FRDi Transient Thermal Resistance

TURN-ON/OFF SWITCHING WAVEFORM

(Switching condition: VDC = 600 V, VDD = 15 V, Tj = 25°C, Ic = 20 A)

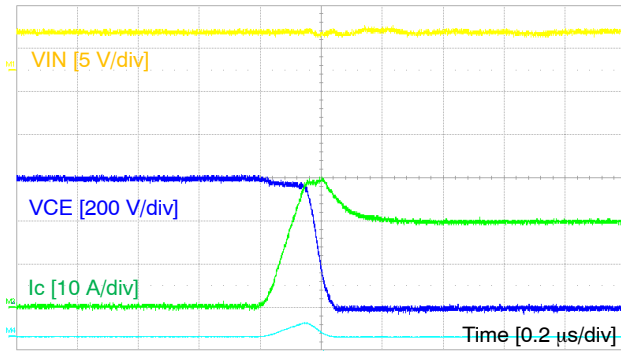


Figure 24. Turn-on Switching Waveform

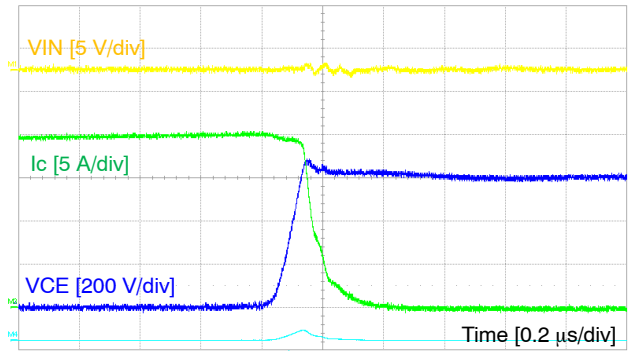


Figure 25. Turn-of Switching Waveform

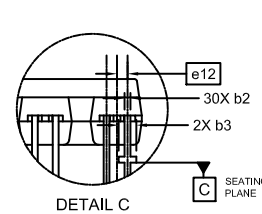
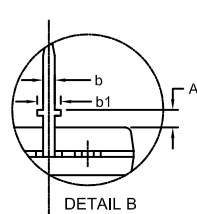
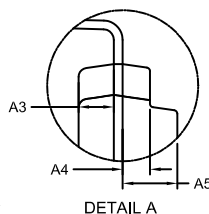
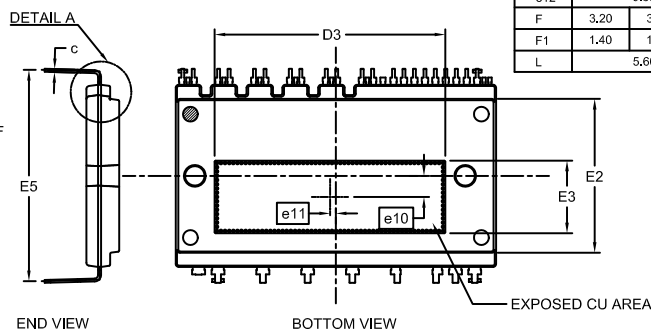
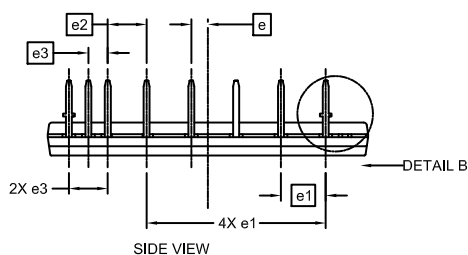
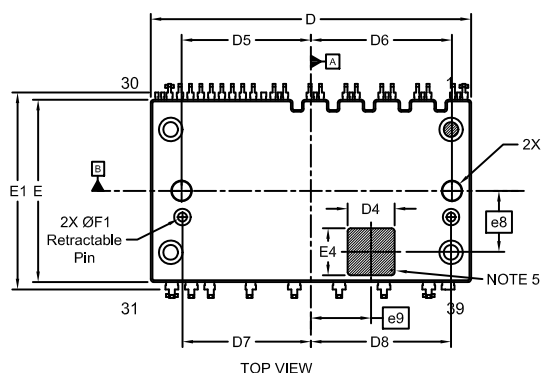
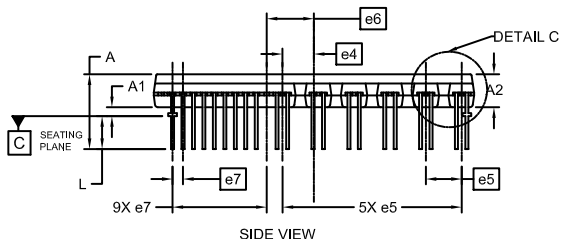
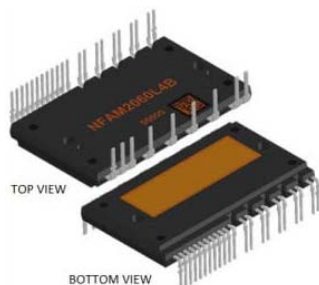
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



DIP39, 54.5x31.0 EP-2 CASE MODGX ISSUE O

DATE 02 APR 2019



DIM	MILLIMETERS			DIM	MILLIMETERS		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	12,20	12,7	13,2	E	30,90	31,00	31,10
A1	1,00	1,50	2,00	E1	33,50 REF		
A2	5,50	5,60	5,70	E2	26,14 REF		
A3	2,00 REF			E3	12,35 REF		
A4	1,55 REF			E4	8,00 REF		
A5	3,10 REF			E5	35,40	35,90	36,40
b	0,90	1,00	1,10	e	2,81 REF		
b1	1,90	2,00	2,10	e1	7,62 BSC		
b2	0,40	0,50	0,60	e2	6,60 BSC		
b3	1,40	1,50	1,60	e3	3,30 BSC		
c	0,50 REF			e4	5,35 REF		
D	54,40	54,50	54,60	e5	6,10 BSC		
D3	39,25 REF			e6	8,02 REF		
D4	8,00 REF			e7	1,78 BSC		
D5	22,00 REF			e8	10,35 REF		
D6	24,00 REF			e9	10,25 REF		
D7	21,85 REF			e10	3,60 REF		
D8	23,85 REF			e11	1,00 REF		
				e12	0,89 BSC		
				F	3,20	3,30	3,40
				F1	1,40	1,50	1,60
				L	5,60 REF		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b and c APPLY TO THE PLATED LEADS AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP.
4. POSITION OF THE LEAD IS DETERMINED AT THE BASE OF THE LEAD WHERE IT EXITS THE PACKAGE BODY.
5. AREA FOR 2D BAR CODE.
6. SHORTENED/CUT PINS ARE 2,5,8,11,14,17,19,29, 30 AND 39.

GENERIC MARKING DIAGRAM*

XXXXXXXXXXXXXXXXXX
ZZZATYWW

XXXXX = Specific Device Code
ZZZ = Assembly Lot Code
AT = Assembly & Test Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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