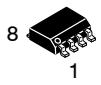
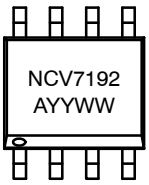
Bridge Signal Conditioning Interface with Analog or SENT Output

NCV7192



SOIC-8 NB
CASE 751-07

MARKING DIAGRAM



A = Assembly Site
YYWW = Assembly Start Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

The NCV7192 is a Signal Conditioning Interface with Analog or SENT output, capable for Automotive Safety Applications. The IC receives a differential signal from the external sensing element, conditions gain and offset with a configurable amplification stage, compensates for sensor nonlinearity and temperature dependency, and delivers the result as digital SENT or ratiometric analog output signal. A separate measurement channel linearizes and measures the resistance of an external NTC to capture a medium temperature and communicate it over the SENT interface. The integrated EEPROM is programmable over the output pin for storage of configuration settings and compensation coefficients, as well as free format customer payload data. The NCV7192 includes failure diagnostics and internal protections against shorts, overvoltage, and reverse voltage to support Safety Applications.

Features

- Resistive Bridge Impedance: 1 to 25 kΩ
- Differential Input Range ($S_{IN\_FSS} + S_{IN\_PO}$): From 2 mVpk/Vbdr to 125 mVpk/Vbdr
- Integrated DSP to Compensate Bridge and Temperature Non-Linearity Using Polynomes
- Calibration Interface over OUTX Pin
- Low-noise Amplification Stage with Programmable Gain/Offset
- Temperature Measurement with Bridge Impedance or Internal Junction Diode
- Medium Temperature Measurement with External NTC
- SENT Output According to the Standard SAE J2716 (April 2016)
- Analog Output Buffer Driven by a 14-bit DAC with Programmable Clip Levels
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

Safety Mechanisms

- Sensor Connectivity Error Detection
- Bridge Signal Measurement BIST
- Temperature Measurement BIST
- DSP BIST
- Analog Output Connectivity Error Detection
- SENT Connectivity Error Detection

Typical Applications

- Pressure Sensors With Piezo-resistive Bridge
- Force/torque Sensors With Resistive Strain-gauge

Public Data Sheet

Interested in what you see? If you would like more detailed information, please request the full version of our data sheet.

Request Full Data Sheet

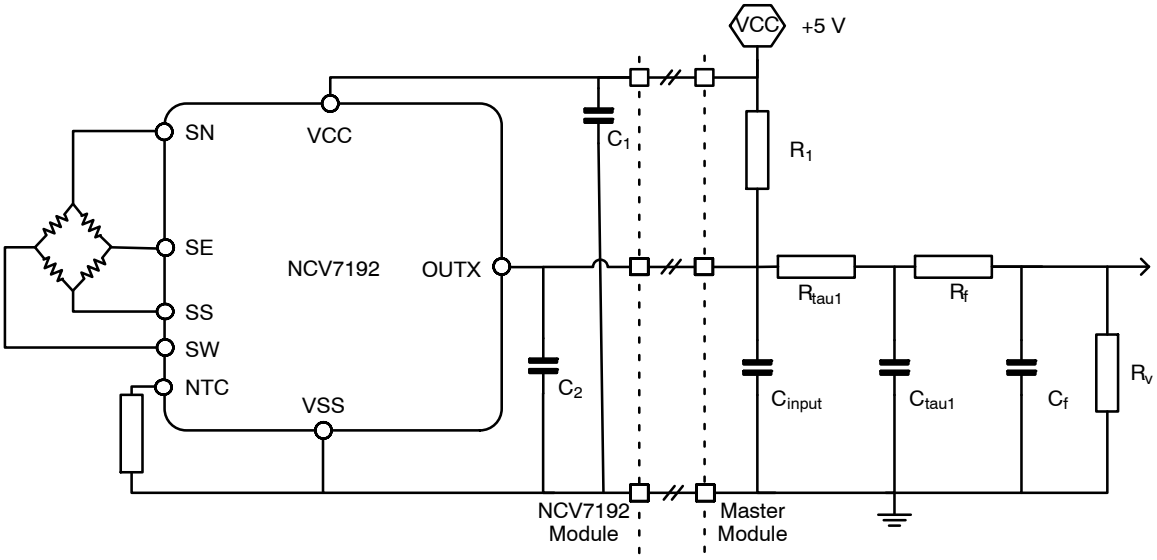


Figure 1. Application Diagram for SENT Application

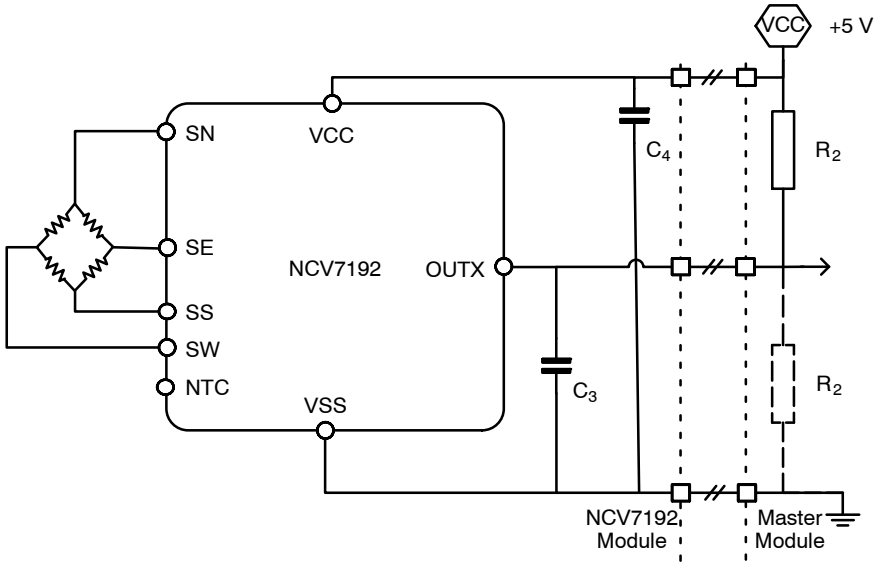


Figure 2. Application Diagram for Analog Output Application

ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Min	Max	Unit
VCC Supply Voltage Range	V_{CCAM}	−30	30	V
OUTX Pin Voltage Range	V_{OUTXAM}	−30	30	V
Sensor Pins SE, SW Voltage Range	V_{SESWAM}	−18	18	V
Sensor SN Abs Max Rating	V_{SNAM}	−18	18	V
Sensor in Pin SS Voltage Range	V_{SSAM}	−3.6	3.6	V
Pin NTC Voltage Range	V_{NTCAM}	−3.6	3.6	V
Storage Temperature for Packaged Devices	T_{st}	−55	150	°C
Junction Temperature under Bias	T_J	−40	165	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. It is not implied that more than one of these ratings can be applied simultaneously

RECOMMENDED OPERATING CONDITIONS (Note 2)

Rating	Symbol	Min	Max	Unit
VCC Operating Range	VCC	4.5	5.5	V
VCC Operating Range for SENT Parametrical Performance	VCC_{SENT}	4.85	5.15	V
Junction Temperature under Bias	T_J	−40	165	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
2. It is not implied that more than one of these ratings can be applied simultaneously

APPLICATION CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Bridge Impedance	R_{BR}	1	–	25	kΩ
Ratio of Zero Signal Offset (S_{IN_PO}) and Sensor Full Scale Span (S_{IN_FSS})	S_{OSFS}	−2	–	2	–
Maximum Differential Input Range ($S_{IN\ FSS}$ + $S_{IN\ PO}$)	S_{IN}	−125	–	125	mV/Vbdr
NTC Impedance Range for Pull-up Resistor 1	$RNTC_{RPU1}$	57	–	20900	Ω
NTC Impedance Range for Pull-up Resistor 2	$RNTC_{RPU2}$	570	–	209000	Ω

ELECTRICAL CHARACTERISTICS (Valid only under recommended operating conditions; unless otherwise specified)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
VCC Current Consumption (No Output Load, No Sensing or NTC Element Attached, 10 ms after Start-up, Gain Stage 1 ≥ 1)		I_{VCC}	–	5	7	mA
SUPPLY VOLTAGE MONITOR						
VCC Reset Release Threshold, Supply Rising	(Note 3)	VCC_{PORH}	–	–	4.4	V
VCC Reset Enable Threshold, Supply Falling	(Note 3)	VCC_{PORL}	–	–	3.6	V
VCC Overvoltage Programmable Threshold Range		VCC_{OV}	5	–	6	V
VCC Undervoltage Programmable Threshold Range		VCC_{UV}	4	–	5	V
BRIDGE SIGNAL						
Bridge Drive Voltage V(SN) − V(SS) for a Typical 3 kΩ Bridge		V_{bdr}	–	3	–	V
Bridge Signal Differential Input Voltage Range Corresponding to Maximum ADC Input with Analog Signal Gain 1		PM_{ADCIN}	−200	–	200	mV
Programmable Range of Typical Analog Signal Gain		PM_{GA}	1/2	–	30	V/V
Maximum Programmable Full Signal Path Gain Towards the Analog Output Channel, Digital Coefficient Gain 1	(Note 3) Full Scale Output Range Min = 0.5 Max = 4.5 V	PM_{FPA}	–	600	–	V/V
Maximum Programmable Full Signal Path Gain Towards the SENT Bridge Signal Channel, Digital Coefficient Gain 1	(Note 3)	PM_{FPS}	–	613	–	kLSB/V
TEMPERATURE MEASUREMENT						
Junction Temperature Measurement (tint) Residual Error	Temperature Range −40 °C to +135 °C, R_{BR} > 2.5 kΩ	TM_{ACC_A}	−3.5	–	3.5	K
Junction Temperature Measurement (tint) Residual Error	Temperature Range −40 °C to +150 °C, R_{BR} > 2.5 kΩ	TM_{ACC_AH}	−5	–	5	K
Bridge Temperature Measurement Residual Error After Trim and Calibration	(Notes 3, 4)	TM_{ACC_BR}	−3	–	3	K

ELECTRICAL CHARACTERISTICS (Valid only under recommended operating conditions; unless otherwise specified) (continued)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
TEMPERATURE MEASUREMENT						
Allowed Bridge Resistance for Temperature Measurement	(Notes 3, 4)	TM_{R_BR}	1.2	–	9.5	kΩ
SENT OUTPUT DRIVER						
SENT Low State Voltage		V_{SENT_VOL}	–	–	0.5	V
SENT High State Voltage		V_{SENT_VOH}	4.1	–	–	V
SENT Fall Time	(Notes 7, 8)	T_{SFALL}	–	–	6.5	μs
SENT Rise Time	(Notes 7, 8)	T_{SRISE}	–	–	18	μs
SENT Edge to Edge Jitter	(Note 8)	DT_{SJIT}	–	0.1	–	μs
First Falling Edge of the First SENT Frame after Power-up		$OUTX_{S\_PUP}$	–	–	1.1	ms
SENT Clock Variation Versus Nominal Tick Time		T_{SCLK}	−20	0	+20	%
ANALOG OUTPUT DRIVER						
Analog Output Voltage Range	R_2 Typ = 4.7 kΩ VCC Typ = 5 V	$OUTX_{A\_RNG\_4p7K}$	0.2	–	4.8	V
Failure Band Low	R_2 Typ = 4.7 kΩ VCC Typ = 5 V	$OUTX_{A\_FBL\_4p7K}$	–	–	0.15	V
Failure Band High	R_2 Typ = 4.7 kΩ VCC Typ = 5 V	$OUTX_{A\_FBH\_4p7K}$	4.85	–	–	V
Output Ratio-metricity Error	(Notes 3, 5)	$OUTX_{A\_RME}$	−0.5	–	0.5	%
OUTX leakage in high-impedance state at 125 °C T_J	(Note 3)	$OUTX_{A\_LC125}$	−0.5		0.5	μA
Time from Power-up till Start of the Analog Output Driver	(Note 3)	$OUTX_{A\_PUP}$	–	–	1.2	ms
Analog Output Step Response Time (Digital Filter Disabled, Input Step to 90% of Output)	(Note 3) Total cap on OUTX Max = 240 nF	$OUTX_{A\_STR}$	–	–	0.5	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Designed to be met in stated voltage and temperature operating ranges, and characterized, though not parametrically tested in production.
4. For typical sensors – application specific and over limited temperature range.
5. After the device is fully calibrated in the intended application.

$$OUTX_{RME} = \frac{\frac{OUTX_{VCC}}{VCC}}{\frac{OUTX_{VCC=5V}}{5\ V}} - 1 \qquad \text{(eq. 1)}$$

6. Formula:
7. Specified from VTH = 3.8 V to VTL = 1.1 V on SENT output wire, ISUP ≤ 20 mA.
8. For 3 μs nominal clock tick including clock accuracy. For higher clock tick times these values can be increased proportionally.

DETAILED OPERATING DESCRIPTION

Basic Operation

The NCV7192 provides an excitation voltage to the resistive bridge and measures the differential output. Each individual bridge sensor presents its own errors and non-idealities that need to be compensated through a calibration process. Sensor offset, sensitivity and non-linearity, as well as the temperature dependency of each of these parameters can be compensated.

After device start-up, configuration settings and compensation coefficients are loaded from the EEPROM into shadow registers. Bridge output voltage and temperature measurements are periodically captured and processed in the DSP to compensate the sensor output with a high degree of accuracy. The amplified and compensated signal is made available at the selected output.

In calibration mode, bidirectional communication with the IC is possible to allow configuring the device and its measurement channels with appropriate gain and offset settings. Raw bridge signal and temperature measurement data are made available for calculation of compensation coefficients. The chosen settings and coefficients can be stored in the EEPROM.

The nominal supply voltage for the NCV7192 is 5 V, but the IC is protected against overvoltage and reverse battery connection, and the analog and digital outputs are protected against shorts to the battery or to ground.

One of two output stages can be selected to communicate the acquired measurements: a 5 V analog output proportional to bridge signal and ratiometric to the supply voltage or a digital output according to the SENT protocol (SAE J2716 Apr 2016).

Supply Voltage Monitor

The NCV7192 monitors the VCC supply to detect when it goes outside of the specified normal operating conditions. Both the undervoltage (VCC_{UV}) as well as the overvoltage (VCC_{OV}) thresholds have a programmable range that can be set in the associated EEPROM configuration bits. When the VCC goes outside of these programmed thresholds, the analog output driver will be either switched off or drive the OUTX voltage to one of the failure bands. The SENT driver will continue to operate but communicate this condition with a diagnostic fail flag.

Parametric performance of the device is not guaranteed outside of the nominal operating range.

Bridge Signal Measurement

The bridge is driven with a nominal 3 V excitation voltage. The analog front end measures the differential signal from the bridge. The input signal is applied to a low-noise amplification stage with typical gain settings indicated in the associated table. Once amplified, the signal must remain within the input range of the ADC (PM_{ADCIN}). To center the amplified input signal on the ADC input range, an offset of maximum $\pm 2xPM_{ADCIN}$ can be added to the amplified signal in $4xPM_{ADCIN}$ / PM_{TRBIT} increments.

Table 1.

Gain Setting	Max Sensitivity (mV/V)
0	125
1	114
2	105
…	…
23	17
24	16
…	…
47	2.1

After coarse offset and gain are applied to the differential input signal, the remaining offset and nonlinearity of the bridge signal as well as it's temperature behavior can be compensated for in the digital DSP.

The DSP uses the raw signal values (DP) and temperature (DT) measurements from their respective ADC's (see Temperature Measurement section on different temperature sources) and executes the following compensation:

$$P_a = A_a + B_a (DP - P_0T_0) + C_a (DP - P_0T_0) (DP - P1T_0) + D_a (DP - P_0T_0) (DP - P_1T_0) (DP - P_2T_0)$$

$$P_b = A_b + B_b (DP - P_0T_1) + C_b (DP - P_0T_1) (DP - P_1T_1) + D_b (DP - P_0T_1) (DP - P_1T_1) (DP - P_2T_1)$$

$$P_c = A_c + B_c (DP - P_0T_2) + C_c (DP - P_0T_2) (DP - P_1T_2) + D_c (DP - P_0T_2) (DP - P_1T_2) (DP - P_2T_2)$$

$$D_{OUT} = P_a + P_b (DT - DT_0) + P_c (DT - DT_0) (DT - DT_1)$$

In which:

- $P_{0...2}T_{0...2}$ are ADC readings at the different test points
- $A_{a..c} - D_{a..c}$ are coefficients that can be calculated during end-of-line calibration
- $DT_{0...2}$ are the digital readings at temperatures T0, T1 and T2 respectively
- D_{OUT} is the digital output word for bridge signal P and temperature T

The bridge signal and temperature measurements and coefficients can be programmed over the calibration interface and stored in the EEPROM.

The sensor pins are monitored to detect connectivity failures between the NCV7192 and the bridge sensor element. For SN, SE, SS and SW, short to VSS, short to SN and disconnection of the pin will result in a diagnostic error, as well as a short to an adjacent SN/SE/SS/SW pin.

Temperature Measurement

The NCV7192 can measure either the internal junction temperature or the bridge resistance for compensation of

temperature dependency of the bridge signal measurement. Selection of the appropriate temperature source is stored in the EEPROM during EOL calibration.

Readings from the selected temperature sensor are digitized and stored in a register where it is periodically updated.

The NCV7192 can measure medium temperature through an external NTC thermistor of choice. The thermistor is measured in a ratio with a factory trimmed, temperature-corrected reference resistor. After conversion to the digital domain, the ratio can be linearized with an in EEPROM programmable look-up table.

The SENT scale offset and SENT scale gain parameter allows to match the temperature values to the SENT temperature characteristic and calibrate out NTC unit-specific variation in the production line.

The NTC pin is monitored when it's measurement is enabled. An open or short to ground is detected and reported as a diagnostic error on the SENT driver.

The NTC temperature processing flags a failure if the measured ratio of the NTC and pull-up resistor goes outside of the range covered by the programmed LUT.

SENT Output Driver

The SENT output serializes bridge signal, temperature and diagnostic information in a digital waveform using the SENT protocol. The waveform is buffered by a driver and presented to the OUTX pin that is loaded with an external pull up.

The SENT output transmits according to the standard SAE J2716 (April 2016) protocol. The tick time for the SENT protocol is programmable with settings between 3 µs and 16 µs. The available tick time settings are 3, 4, 6, 10, 12 and 16 µs.

A pause pulse can be activated to achieve a full transmission frame length of 198 ticks for the high-speed option, 282 ticks for all other options.

The selectable options for fast channel data frames are P (high speed), P/P_{inv}, P/−. P/T, P/S. The checksum is a 4-bit CRC of the Data nibbles, implemented according to J2716 Section 5.4.2.2.

The slow channel data can transmit diagnostics, SENT revision, sensor type and configuration/ manufacturer codes as well as each of the temperature sources through an 8-bit message ID and 12 bit data field.

Analog Output Driver

The analog output consists of a 14-bit ratiometric D/A converter, a low-pass filter and a 5 V rail-to-rail output amplifier. Either a pull-up or a pull-down resistor is connected to the output. In analog output mode, only the bridge data is available.

The analog output driver is protected against shorts to VCC or VSS. Even a short of the VCC or OUTX pin to a high-voltage battery terminal (within the defined absolute maximum ratings) will not lead to immediate destruction and the device will return to normal operation after removal of the short. In absence of VCC, VSS or OUTX connection or when a reverse polarity is applied to the supply terminals, the driver is switched off and the output pin is high impedance. The voltage level at the OUTX terminal is in this case determined by the connected pull-up or pull-down resistor. Upon removal of the associated malfunction, the driver will resume normal operation.

If any of the internal diagnostic errors fail, the analog output driver is either driven to the high or low fail band. Internal diagnostics can be disabled in EEPROM configuration bits, though their disabling may affect the safety metrics.

Calibration Mode

The calibration interface enables read and write commands to the memory and allows to read back digitized measurement results to allow configuring the device for the intended application and calibrating the compensation coefficients for the particular bridge instance. The interface works as UART half duplex mode over the OUTX pin after the device is configured to Calibration Mode.

The NCV7192 can be brought in Calibration Mode by elevating the VCC supply voltage above the threshold VCC_{CM} and sending Key-code CCM over the OUTX pin after T_{CMWAIT} and before T_{CM} period after POR.

ORDERING INFORMATION

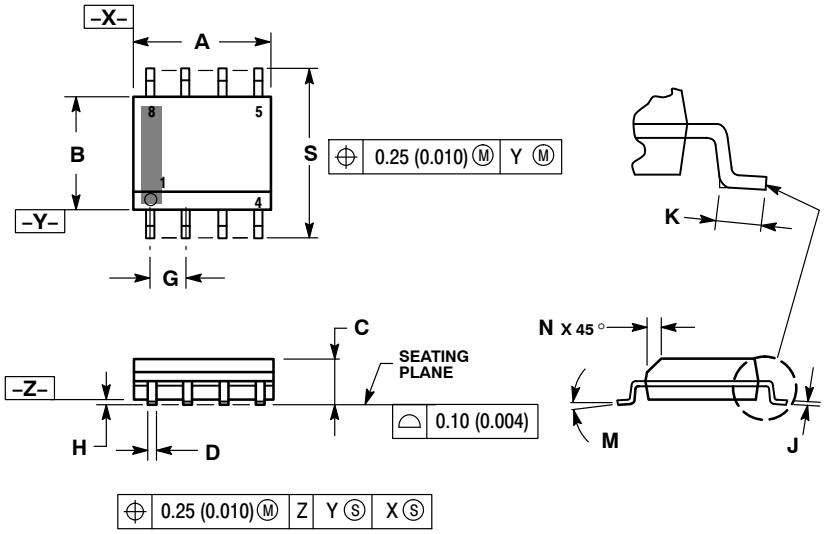
Device	Package	Shipping†
NCV7192D0R2G	SOIC8	3000 / Tape & Reel
NCV7192C1	Bare Die	Wafer Sale

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

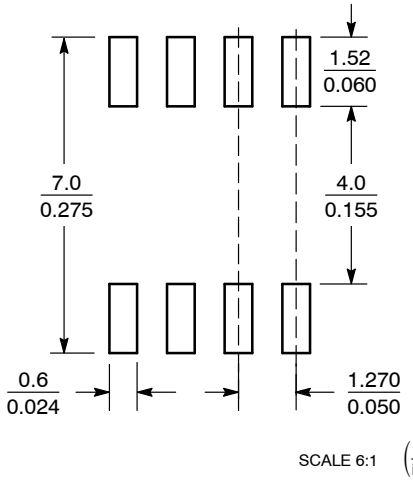
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

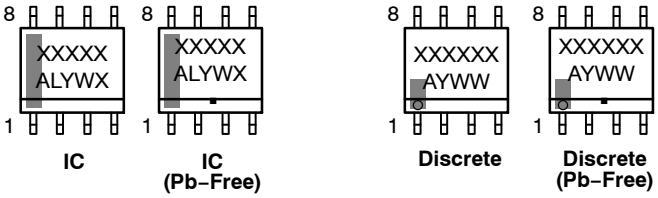
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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