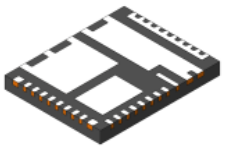
Integrated Driver and MOSFET with Integrated Current Monitor

NCP303345



PQFN24 4x5, 0.5P
CASE 483BV

NCP303345 is a smart power stage with a current sense driver, high side and low side MOSFETs for high current, high frequency DC-DC buck power conversion applications. The NCP303345 provides an output signal (IMON), which reports the real-time module current. NCP303345 operates in a wide input voltage and frequency range. NCP303345 is a high end DrMOS designed to work in computing power applications.

NCP303345 of each phase can be operated at its best current balance and thermal conditions. Flexibility of phase re-assignment and phase adding/shedding will be considered. As a result, the VR system situation will be better monitored, properly responded.

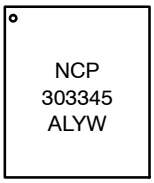
Features

- 3 V – 24 V Input Voltage
- 45 A Continuous Output Current
- 80 A Peak Current Protection
- Individual TMON Reporting, Individual Current Input Gain Adjustment
- High Accuracy IMON Output
- 5 V, 3.3 V PWM Compatibility
- Ultra Low Quiescent Current
- Fault Reporting(OTP, OCP)
- BOOT-SW Undervoltage Protection
- Driver Readiness Reporting
- Supports Intel® IMVP9.1/2/3

Applications

- Desktop & Notebook Microprocessors
- Graphic Cards
- Routers and Switches

MARKING DIAGRAM



NCP303345 = Specific Device Code
A = Assembly Location
L = Wafer Lot
YW = Year, Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NCP303345MNTWG	PQFN24	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

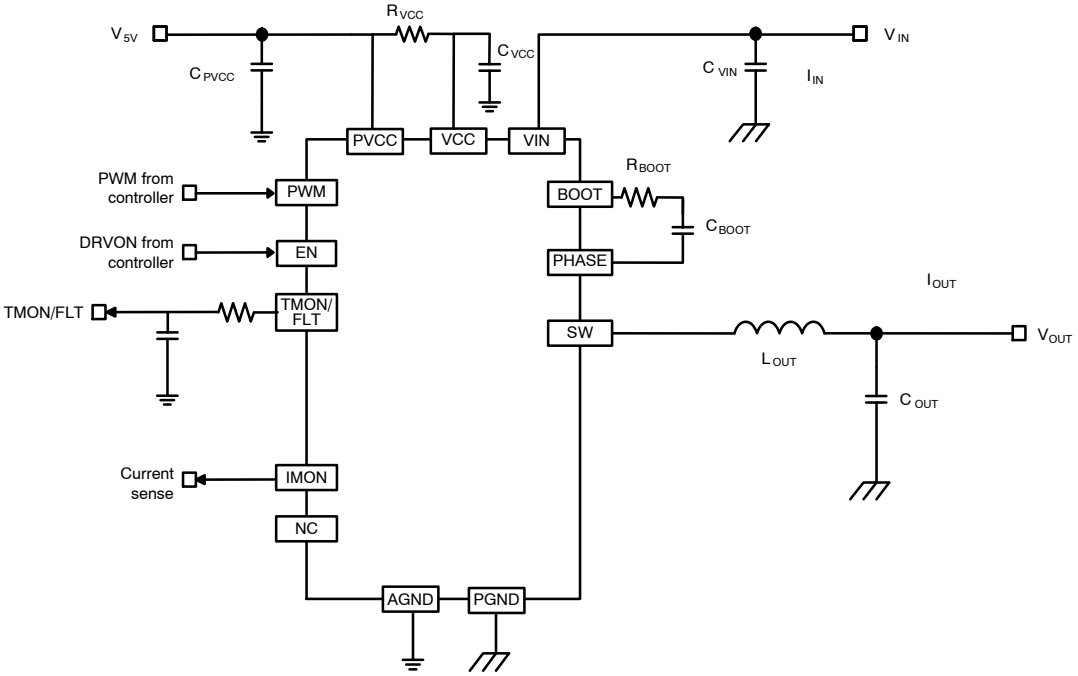


Figure 1. Application Schematic

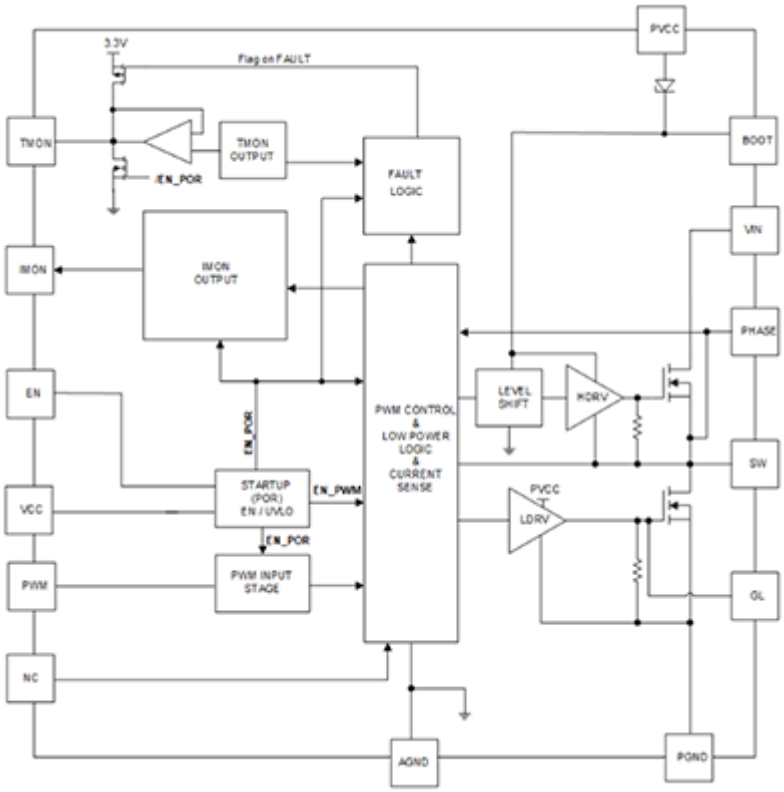


Figure 2. Block Diagram

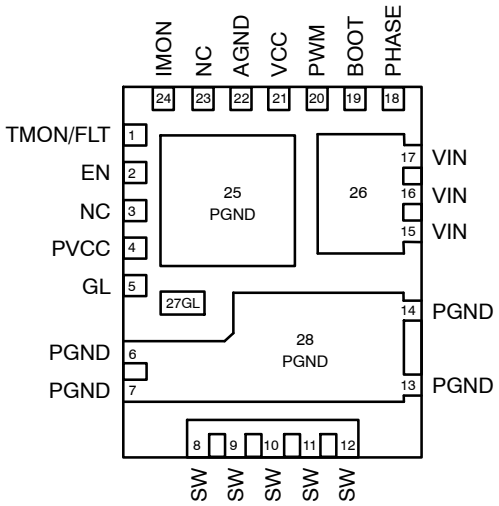


Figure 3. Pin Connections

PIN LIST AND DESCRIPTIONS

Pin No.	Symbol	Description
1	TMON/FLT	Temperature monitor; when VCC<POR, TMON output FET will be pulled down;pulled high in faults of over temperature and positive over current
2	EN	EN=Low disables most blocks; EN=high enables all blocks
3	NC	Leave floating or tie to GND
4	PVCC	Power supply for LS gate drivers
5, 27	GL	Low side gate
6–7, 13–14, 25, 28	PGND	Power ground for LS FET power stage
8–12	SW	Switch node
15–17, 26	VIN	Power stage high voltage input (HS FET drain)
18	PHASE	Phase node connection for boot capacitor
19	BOOT	Supply for high-side FET gate driver
20	PWM	PWM input to the drive IC
21	VCC	Power supply for analog control and boost circuit
22	AGND	Analog ground
23	NC	Not connected
24	IMON	Current monitoring

ABSOLUTE MAXIMUM RATINGS (Electrical Information − all signals referenced to PGND unless noted otherwise)

Symbol	Parameter		Min	Max	Unit
VCC	Supply Voltage	Referenced to AGND	−0.3	6	V
PVCC	Drive Voltage	Referenced to AGND	−0.3	6	V
VEN	Enable / Disable	Referenced to AGND	−0.3	VCC + 0.3	V
VPWM	PWM Signal Input	Referenced to AGND	−0.3	VCC + 0.3	V
VGL	Low Gate Test Pin	Referenced to AGND	−0.3	VCC + 0.3	V
VIMON	Current Monitor Output	Referenced to AGND	−0.3	VCC + 0.3	V
$VTMON_{/FLT}$	Thermal Monitor	Referenced to AGND	−0.3	VCC + 0.3	V
VIn	Power Input	Referenced to PGND, AGND	−0.3	30	V
Vin_{-Phase}	Vin−PHASE	Differential Vin−Phase	−0.3	30	V
		Differential Vin−Phase AC < 5 ns	−9	35	
Vphase	Phase	Referenced to PGND (DC Only)	−0.3	30	V
		Referenced to PGND, AC < 5 ns	−12	35	
VSW	Switch Node Input	Referenced to PGND (DC Only)	−0.3	30	V
		Referenced to PGND, AC < 5 ns	−7	35	
VBOOT	Bootstrap Supply	Referenced to PGND	−0.3	35	V
		Referenced to PGND, AC < 5 ns	−9	40	
VBOOT-PHASE	Boot to PHASE Voltage	DC Only	−0.3	6	V
		Referenced to PHASE, AC < 5 ns	−	9	
TJ	Maximum Junction Temperature		−	150	°C
ESD	Electrostatic Discharge Protection	Human Body Model,	2000	−	V
		Charged Device Model	500	−	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL INFORMATION

Symbol	Rating	Value	Unit
$\theta_{J\text{-Lead}}$	Thermal Resistance (Note 1)	1.10	°C/W
$\theta_{J\text{-CaseTop}}$		14.5	°C/W
$\theta_{J\text{-Ambient}}$		14.4	°C/W
TA	Operating Ambient Temperature Range	−40 to +125	°C
TSTG	Maximum Storage Temperature Range	−55 to +150	°C
MSL	Moisture Sensitivity Level	1	

1. Mounted on 4S2P test board with 0 LFM at T_A = 25 °C

RECOMMENDED OPERATING CONDITIONS

Pin Name	Parameter	Conditions	Min	Typ	Max	Unit
VCC, PVCC	Supply Voltage Range		4.5	5.0	5.5	V
VIN	Conversion Voltage		3	19	24 (Note 2)	V
	Continuous Output Current (Note 3)	F_{SW} = 800 kHz, V_{IN} = 19 V, V_{OUT} = 1.0 V, T_A = 25 °C	–	–	40	A
		F_{SW} = 300 kHz, V_{IN} = 19 V, V_{OUT} = 1.0 V, T_A = 25 °C	–	–	45	A
	Junction Temperature		–40	–	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Operating at high VIN can create excessive AC voltage overshoots on the SW-to-GND and BOOT-to-GND nodes during MOSFET switching transient. For reliable operation, SW to GND and BOOT to GND must remain at or below the Absolute Maximum Ratings in the table above.
3. Mounted on **onsemi** evaluation board. See page 19 for board details.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 V, V_{IN} = 19 V, V_{EN} = 5.0 V, C_{VCC} = 1.0 μF unless specified otherwise) Min/Max values are valid for the temperature range –40 °C ≤ T_J ≤ 125 °C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
BASIC OPERATION						
$I_{Q\_ENL\_VCC}$	Disabled Current	I_Q = V_{CC} + P_{VCC}, EN = 0 V	–	5	10	μA
$I_{Q\_VCC\_1MHz}$	Enable current in operation	I_Q = I_{VCC} + I_{PVCC}, F_{SW} = 1000 kHz, PWM = H/L, D = 0.1	0	33	40	mA
$V_{CC\_UVLO\_R}$	V_{CC} UVLO Threshold	VCC and PVCC rising	3.9	4.2	4.5	V
$V_{CC\_UVLO\_F}$	V_{CC} UVLO Threshold	VCC and PVCC rising	3.6	3.9	4.1	V
T_{D_POR}	Delay from POR to Driver Ready	VCC POR rising to TMON going from pulled low to TMON open drain (Limited by OTP fuse read). EN = High	50	80	200	μs
EN INPUT						
V_{EN_HIGH}	Enable Upper Threshold		2.0	–	V_{CC}	V
V_{EN_LOW}	EN Low Voltage Level	VCC = PVCC = 5 V, PWM disabled	0	–	0.65	V
T_{D_EN}	Enable Delay Time	PWM = LO, Delay Between EN from LO to HI to GL from LO to HIGH	1	15	30	μs
T_{D_DIS}	Disable Delay Time	PWM = LO, Delay Between EN from HI to LO to GL from HI to LO	1	15	45	ns
R_{EN_1}	EN Input Resistance 1	EN = High, VCC = PVCC = 0 V	–	13	–	MΩ
T_{PD_TMON}	Delay for TMON LOW → active	V_{CC} = V_{CCD} = 0 V, TMON FET gate pulled high by EN, measure from EN above 2.5 V to TMON falling	0.2	2.0	7.0	μs
R_{TMON_PD}	TMON Pull Down FET On Resistance	V_{CC} < POR, EN = High	2	4	8	Ω
PWM INPUT						
V_{IH_PWM}	Input High Voltage		2.7	–	–	V
V_{MID_PWM}	Input MID-State Voltage		1.2	–	2.3	V
V_{IL_PWM}	Input Low Voltage		0	–	0.8	V
T_{DEADON}	Non-overlap Delay, Leading Edge	GL ≤ 0.5 V to SW > 1.2 V. PWM Transition 0 → 1	–	10	–	ns
$T_{DEADOFF}$	Non-overlap Delay, Trailing Edge	SW ≤ 1.2 V to GL ≥ 0.5 V, PWM Transition 1 → 0	–	6	–	ns
$T_{PD\_SWR\_PWM}$	PWM Propagation Delay, Rising	PWM Going HIGH to GL Going LOW, VIH_PWM to 90% GL	–	30	–	ns

ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 5.0 V, V_{IN} = 19 V, V_{EN} = 5.0 V, C_{VCC} = 1.0 μF unless specified otherwise) Min/Max values are valid for the temperature range −40 °C ≤ T_J ≤ 125 °C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
PWM INPUT						
$T_{PD\_SWF\_PWM}$	PWM Propagation Delay, Falling	PWM Going LOW to GH Going LOW, VIL_PWM to 90% GH	–	30	–	ns
$T_{EX\_ZL\_PWM}$	Exiting PWM Mid-state Propagation Delay, Mid-to-Low	PWM from MID going LOW to 10% GL Rising	–	20	–	ns
$T_{EX\_ZH\_PWM}$	Exiting PWM Mid-state Propagation Delay, Mid-to-High	PWM from MID to HI to 10% SW Rising	–	25	–	ns
$T_{ENT\_ZH\_PWM}$	PWM High to Mid-State hold Off Time	PWM Going Mid to HS Going Off	–	40	–	ns
$T_{ENT\_ZL\_PWM}$	PWM Low to Mid-State hold Off Time	PWM Going Mid to LS Going Off	–	50	–	ns
$T_{MIN\_PWM\_HIGH}$	HS minimal turn on time	Forced PWM HI Pulse Required for GH to Charge from 0 to BOOT-SW	–	20	–	ns
$T_{D\_ENT\_LP\_PWM}$	Ultra Light Load Power State Entry Delay	PWM = tri-state or Low	50	75	120	μs
$T_{EX\_LP\_PWM}$	Lower Power Mode Exit Delay	PWM = tri-state to high to SW> 10% V_{IN}	–	25	–	ns
$T_{MIN\_PWM\_LOW}$	LS minimal turn on time	Forced PWM LOW Pulse Required for GL to Charge from 0 to PVCC	–	25	–	ns
IMON						
T_{D_IMON}	IMON Delay		–	50	–	ns
V_{IMON}	Dynamic range at IMON pin		1	1.3	2.5	V
IMON ACCURACY (T_J = 25 °C to 85 °C) (Note 4)						
I_{MON_OS}	Current Offset			±5		μA
I_{MON_GAIN}	IMON Gain	I_{OUT} = −10 A to 40 A		5		μA/A
A_{IMON_GAIN}	$V_{IMON} = I_{OUT} \times 5 \times 10^{-6} \times R_{IMON}$, R_{IMON} = 1 kΩ	I_{OUT} = −10 A to 40 A		±5		%
		I_{OUT} = 10 A to 35 A		±3		
TMON						
V_{TMON_25C}	Thermal Monitor Voltage	$T_A = T_J$ = 25 °C	0.755	0.800	0.845	V
V_{TMON_125C}		$T_A = T_J$ = 125 °C	1.57	1.60	1.63	V
V_{TMON_SLOPE}	TMON Slope		7.75	8.00	8.25	mV/°C
I_{SOURCE_TMON}	TMON Source Current	25 °C	1000	2900	4200	μA
I_{SINK_TMON}	TMON Sink Current	25 °C	36	42	51	μA
V_{OUT_TMON}	TMON Output Voltage Low	I_{TMON} = 4.4 mA (sink), $T_A = T_J$ = 125 °C, V_{CC} = 4.5 V	10	35	100	mV
		I_{TMON} = 4.4 mA (sink), $T_A = T_J$ = 30 °C, V_{CC} = 4.5 V	10	20	50	
OVER-TEMPERATURE PROTECTION FAULT						
	Over-Temperature Protection	Driver IC Temperature	–	150	–	°C
	OTW Hysteresis	Driver IC Temperature	–	18	–	°C
FAULT FLAG OUTPUT VOLTAGE/CURRENT						
V_{TMON_FAULT}	Fault Report Voltage for OTP or POCP	OTP or POCP for 8 consecutive cycles	3.0	3.3	3.4	V
LOW-SIDE DRIVER						
R_{SOURCE_GL}	Output Impedance, Sourcing	Source Current = 100 mA	0.5	1.02	1.7	Ω

ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 5.0 V, V_{IN} = 19 V, V_{EN} = 5.0 V, C_{VCC} = 1.0 μF unless specified otherwise) Min/Max values are valid for the temperature range −40 °C ≤ T_J ≤ 125 °C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
LOW-SIDE DRIVER						
R_{SINK_GL}	Output Impedance, Sinking	Sink Current = 100 mA	0.2	0.4	0.7	Ω
R_{PD_GL}	GL Pull Down Resistance	GL to PGND, V_{CC} = PGND	75	500	800	kΩ
BOOTSTRAP DIODE						
VF	Forward Voltage	Forward Bias Current = 2 mA	0.1	0.4	0.6	V
PRE OVER VOLTAGE PROTECTION						
V_{TH_PREOVP}	PreOVP Threshold	Voltage present on SW when EN goes high	3.05	3.25	3.45	V
HS CYCLE-BY-CYCLE POSITIVE OVER-CURRENT PROTECTION (POCP) (T_J = 25 °C to 85 °C)						
I_{LIM}	Peak Over-Current Limit		75	80	–	A
I_{LIM_HYS}	POCP Hysteresis		–	10	–	A
N_{POCP_LATCH}	POCP Latch Count	Consecutive cycles in High-Side current limit	–	8	–	
NEGATIVE OVER-CURRENT PROTECTION (NOCP) (T_J = 25 °C to 85 °C)						
I_{NOCP_LOW}	NOCP Trip LOW Level		−35	−30	−25	A

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Imon performance is guaranteed by independent ATE testing of Low-side slope and offset

Table 1. TRUTH TABLE

State	EN	PWM	HS FET	LS FET	TMON/FLT	IMON Status
Chip Disabled	L	X	OFF	OFF	Pulled down	Off
Chip Enabled	H	H	ON	OFF	Measured	Measured
Chip Enabled	H	Mid	OFF	ZCD	Measured	Measured
Chip Enabled	H	L	OFF	ON	Measured	Measured
POCP Latched	H	X	OFF	OFF	3.3 V	Measured
NOCP Latched	H	X	Follows PWM	Truncated	Measured	Measured
OTP activated and non-Latched	H	X	OFF	OFF	3.3 V	Measured

MOSFET TYPICAL PERFORMANCE CHARACTERISTICS

(Tests at T_A = 25 °C unless otherwise specified)

High Side

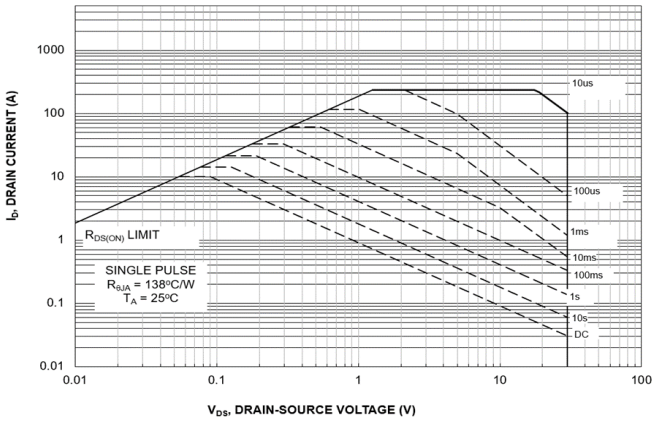


Figure 4. Unclamped Inductive Switching Capability

Low Side

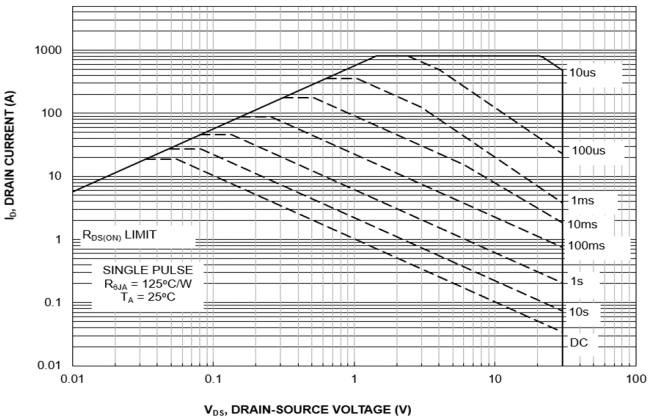


Figure 5. Unclamped Inductive Switching Capability

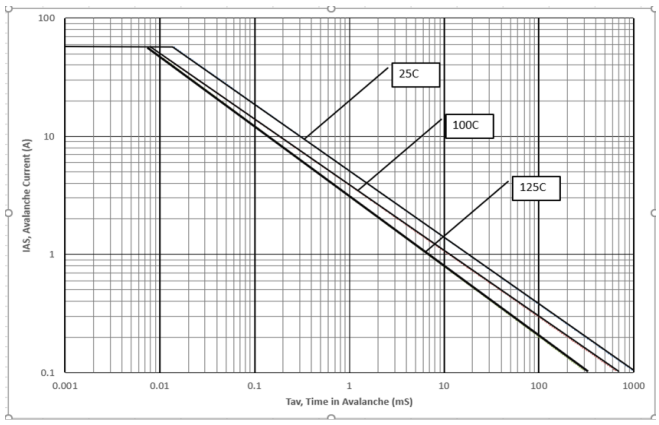


Figure 6. Forward Bias Safe Operating Area

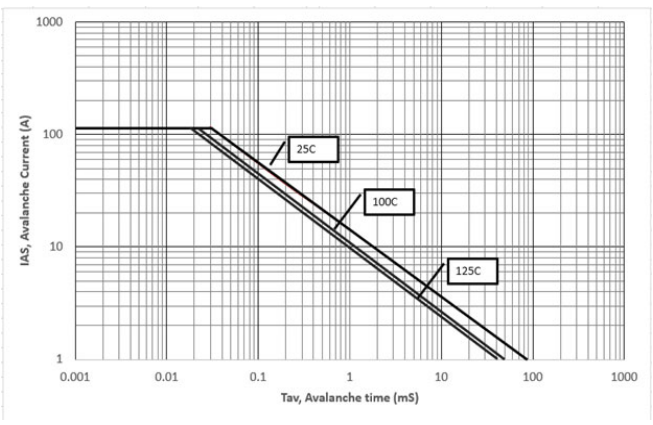


Figure 7. Forward Bias Safe Operating Area

TYPICAL PERFORMANCE CHARACTERISTICS

(Tests at T_A = 25 °C, Frequency = 500 kHz, V_{CC} = 5 V, V_{IN} = 19 V, and V_O = 1 V unless otherwise specified)

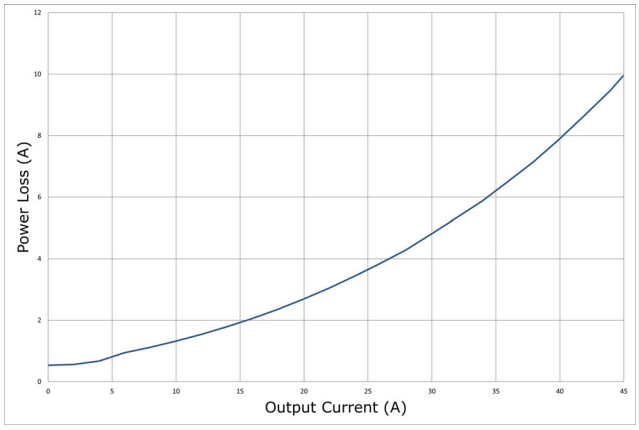


Figure 8. Power Loss vs. Output Current

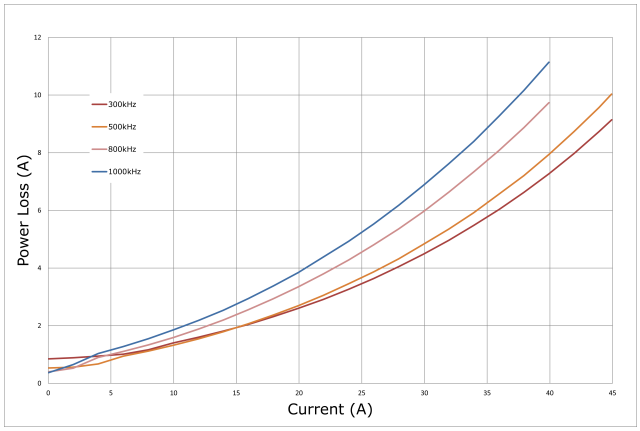


Figure 9. Power Loss vs. Switching Frequency

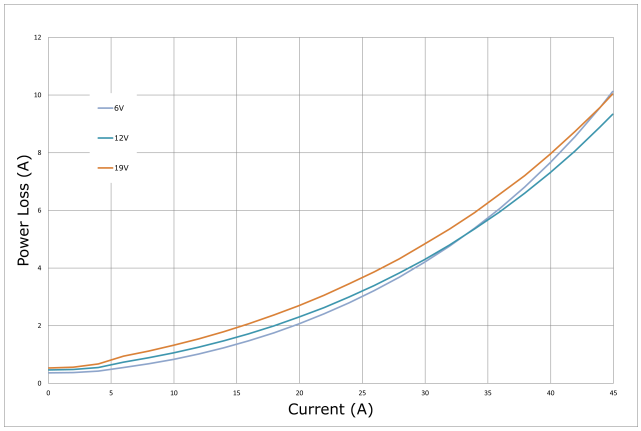


Figure 10. Power Loss vs. Input Voltage

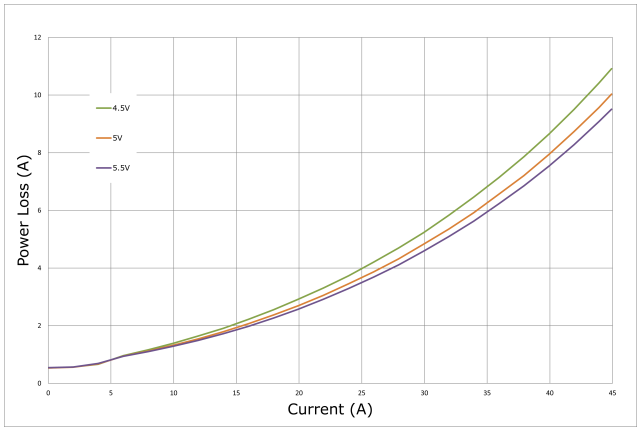


Figure 11. Power Loss vs. Driver Voltage

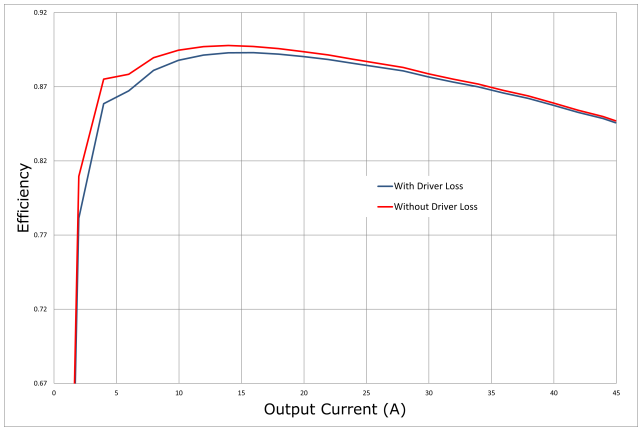


Figure 12. Efficiency vs. Output Load

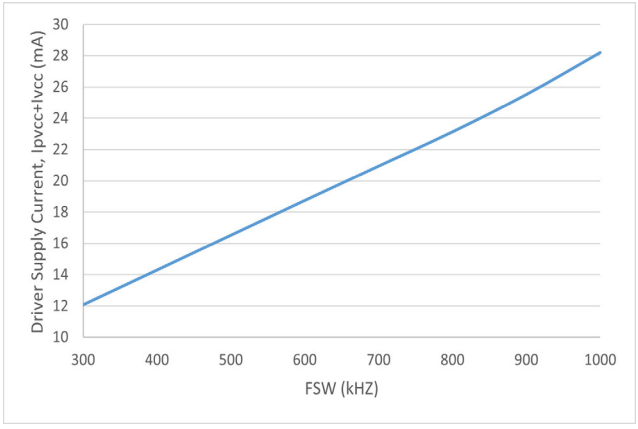


Figure 13. Driver Current vs. Switching Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Tests at T_A = 25 °C, Frequency = 500 kHz, V_{CC} = 5 V, V_{IN} = 19 V, and V_O = 1 V unless otherwise specified)

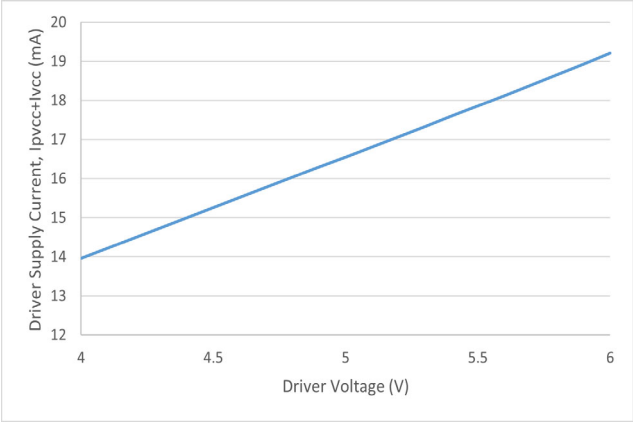


Figure 14. Driver Current vs. Driver Voltage

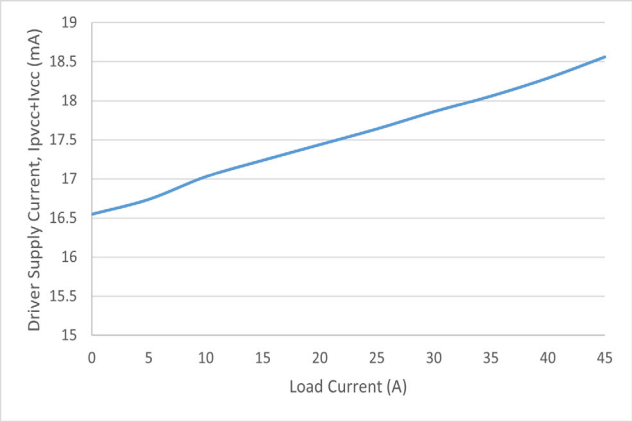


Figure 15. Driver Current vs. Output Current

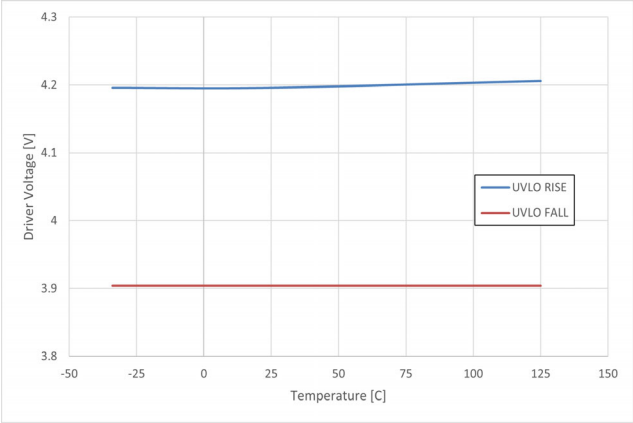


Figure 16. UVLO Threshold vs. Temperature

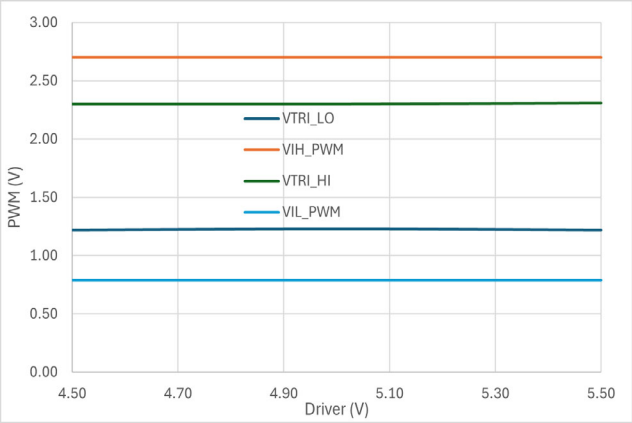


Figure 17. PWM Threshold vs. Driver Voltage

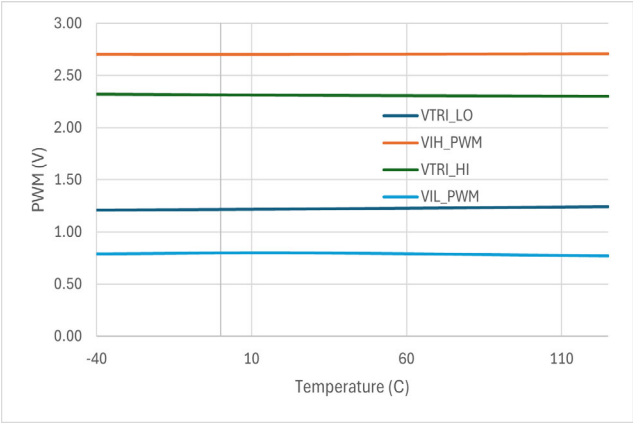


Figure 18. PWM Threshold vs. Temperature

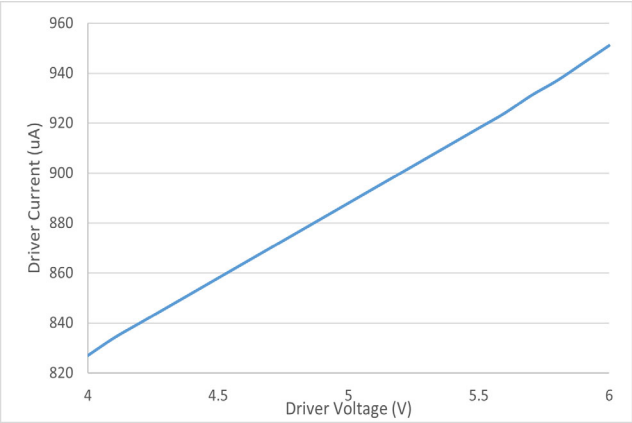


Figure 19. Quiescent Current vs. Driver Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Tests at T_A = 25 °C, Frequency = 500 kHz, V_{CC} = 5 V, V_{IN} = 19 V, and V_O = 1 V unless otherwise specified)

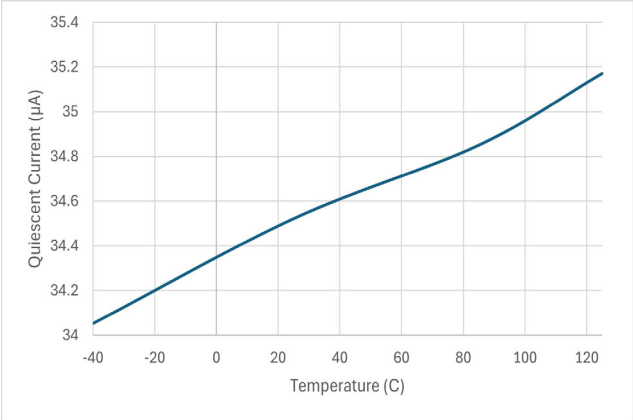


Figure 20. Quiescent Current vs. Temperature

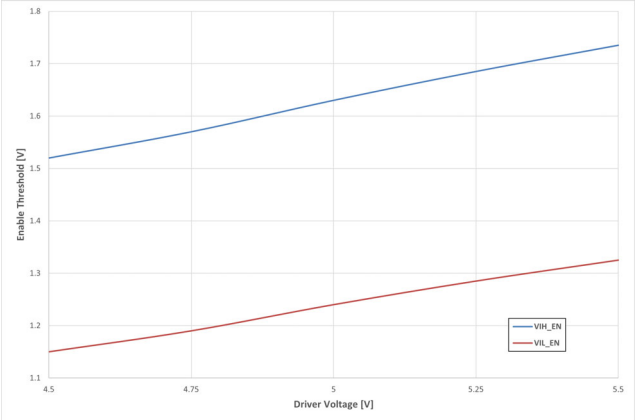


Figure 21. EN Threshold vs. Driver Voltage

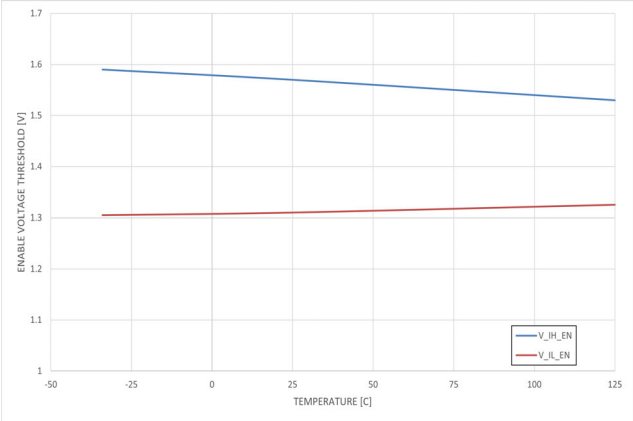


Figure 22. EN Threshold vs. Temperature

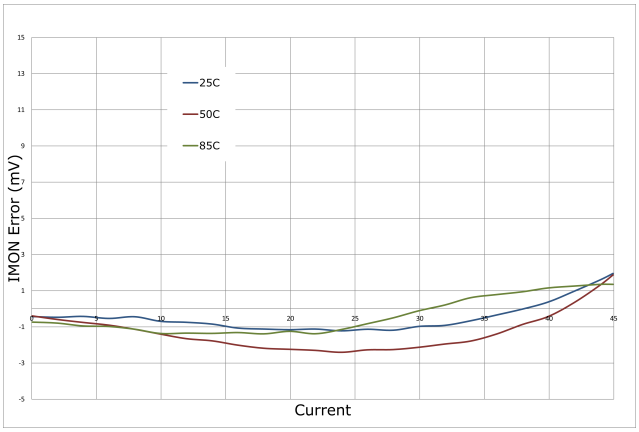


Figure 23. I_{MON} Accuracy vs. Temperature

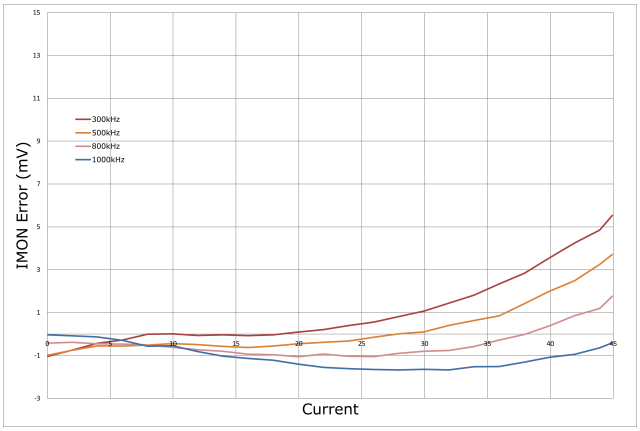


Figure 24. I_{MON} Accuracy vs. Switching Frequency

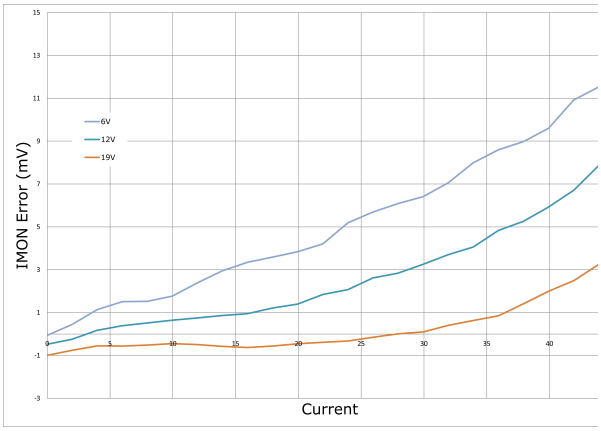


Figure 25. I_{MON} Accuracy vs. Input Voltage

FUNCTIONAL DESCRIPTION

The NCP303345 integrates the MOSFET drivers, high−side MOSFET and low−side MOSFET into a single package optimized for use in a synchronous buck converter topology. The NCP303345 supports numerous other functions such as current sense (IMON), Zero Current Detection (ZCD), thermal monitoring (TMON), under-voltage lock-out (UVLO), and over current protection (OCP). A PWM input signal is required to properly drive the high-side and the low-side MOSFETs. The part is capable of driving frequency up to 1 MHz

Power Sequence

NCP303345 requires four (4) input signals to conduct normal switching operation: VIN, VCC/PVCC, PWM, and EN. All combinations of power sequences are available.

The EN pin can be directly tied to the PWM controller for other purposes. Or the EN pin can be tied to the VCC rail with an external pull-up resistor and it will maintain HIGH once the VCC rail turns on.

EN and UVLO

The NCP303345 is enabled by both EN pin input signal and VCC UVLO. Table 2 summarizes the enable and disable logics. With EN low and VCC UVLO, NCP303345 is fully shut down. If VCC is ready but EN is low, it goes into sleep mode with very low quiescent current, where only critical circuitry is alive. The part will also be in calibration and read fuses/program itself during this state.

NCP303345 needs T_{D_POR} time to go from fully shutdown mode to power ready mode. The time is T_{D_EN} to go from enable high to driver ready.

The pin has an internal pulldown resistance to force a disabled state when it is left undriven.

Table 2. UVLO AND DRIVER STATE

VCC UVLO	EN	Driver State
0	X	Full driver shutdown (GH, GL = 0), requires T_{D_POR} for start-up
1	0	Partial driver shutdown (GH, GL = 0), requires T_{D_EN} for startup
1	1	Enabled (GH/GL follow PWM)
X	Open/0	Disabled (GH, GL = 0)

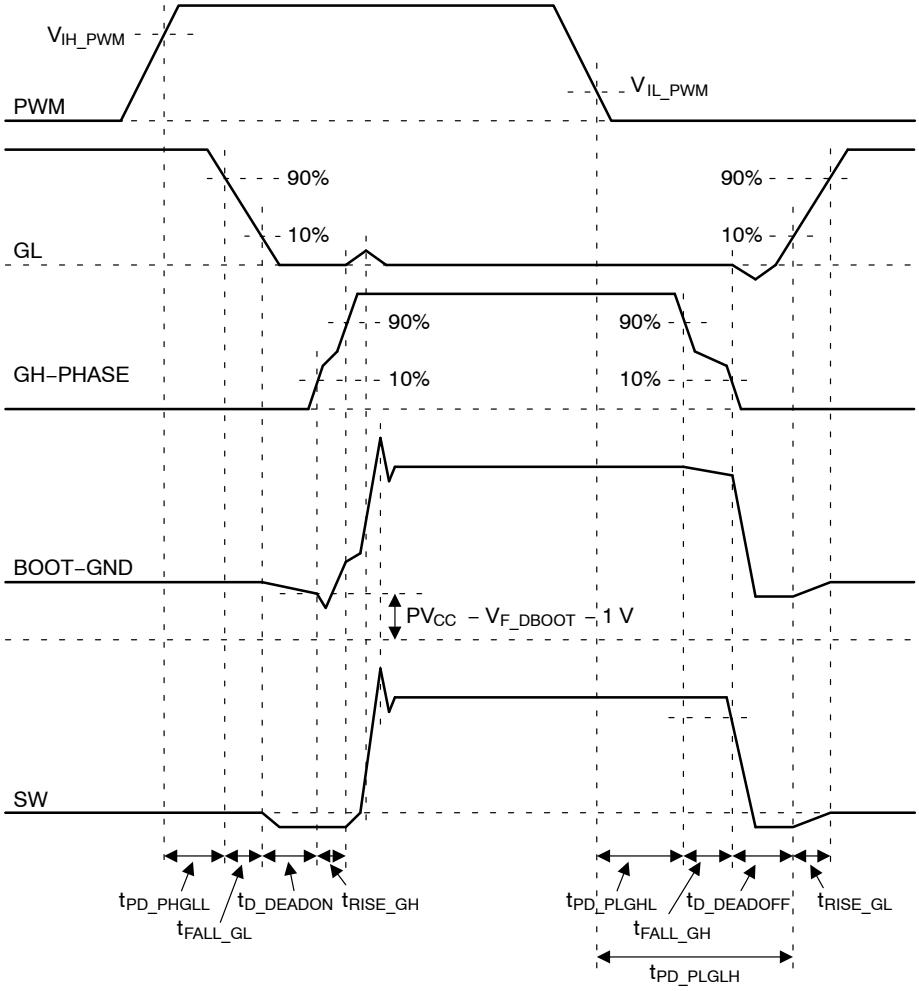
Zero Current Detect (ZCD)

At light load conditions, the inductor current can be negative due to the inductor current ripple. The zero current detection (ZCD) function in the NCP303345 can prevent negative current during these light load conditions and thus leads to higher efficiency. When ZCD is active, the NCP303345 will monitor the voltage at the SW pins when PWM exits the high state. There is a blanking timer that delays when this monitoring starts. As the inductor current falls towards zero, the voltage on the SW pins will become less negative. When the voltage on the SW pin reaches the ZCD threshold, the LS FET is turned off. Positive current can still flow through the body diode of the LS FET, but the body diode will block any current in the negative direction.

PWM

The PWM input is a tri-state logic interface. The tri-state gate drive has both logic HIGH and LOW levels, as well as a MID state for ZCD operation. When the PWM input signal enters and remains within the MID-State window for a defined hold-off time ($T_{ENT\_Zx\_PWM}$), the high side FET is turned off and low side FET goes into ZCD mode. This feature enables power stage diode emulation in light load operation and phase shedding depending on the controller feature set.

It is standard to have selection resistors on the PWM line to set features in the controller. These resistors should be accounted for in setting the drive strength of the PWM driver stage for MID-State operation.



t_{PD_PHGLL} = PWM HI to GL LO, V_{IH_PWM} to 90% GL
t_{FALL_GL} = 90% GL to 10% GL
t_{D_DEADON} = LS Off to HS On Dead Time, 10% GL to $V_{BOOT-GND} \le PV_{CC} - V_{F\_DBOOT} - 1$ V or BOOT-GND dip start point
t_{RISE_GH} = 10% GH to 90% GH, $V_{BOOT-GND} \le PV_{CC} - V_{F\_DBOOT} - 1$ V or BOOT-GND dip start point to GL bounce start point
t_{PD_PLGHL} = PWM LO to GH LO, V_{IL_PWM} to 90% GH or BOOT-GND decrease start point, $t_{PD\_PLGLH} - t_{D\_DEADOFF} - t_{FALL\_GH}$
t_{FALL_GH} = 90% GH to 10% GH, BOOT-GND decrease start point to 90% V_{SW} or GL dip start point
$t_{D\_DEADOFF}$ = HS Off to LS On Dead Time, 90% V_{SW} or GL dip start point to 10% GL
t_{RISE_GL} = 10% GL to 90% GL
t_{PD_PLGLH} = PWM LO to GL HI, V_{IL_PWM} to 10% GL

Figure 26. PWM Timing Diagram

High-Side Driver

The high-side driver (HDRV) is designed to drive a floating N-channel MOSFET (Q1). The bias voltage for the high-side driver is developed by a bootstrap supply circuit, consisting of the internal diode and external bootstrap capacitor (CBOOT). During startup, the SW node is held at PGND, allowing CBOOT to charge to PVCC through the internal bootstrap diode.

When the PWM input goes HIGH, HDRV begins to charge the gate of the high-side MOSFET (internal GH pin). During this transition, the charge is removed from the CBOOT and delivered to the gate of Q1. As Q1 turns on, PH rises to VIN, forcing the BOOT pin to VIN + VBOOT, which provides sufficient VGS enhancement for Q1. To complete the switching cycle, Q1 is turned off by pulling HDRV to PH. CBOOT is then recharged to VCC when the SW falls to PGND. HDRV output is in phase with the PWM input. The high-side gate is held LOW when the driver is disabled by a resistor to PH.

Low-Side Driver

The low-side driver (LDRV) is designed to drive the gate-source of a ground referenced low RDS(ON) N-channel MOSFET (Q2). The bias for LDRV is internally connected between VCC and PGND. When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the driver is disabled, LDRV is held LOW, by a resistor to GND.

Dead-Times

The driver IC design ensures minimum MOSFET dead times, while eliminating potential shoot-through (cross-conduction) currents. To ensure optimal module efficiency, body diode conduction times must be reduced to the low nano-second range during CCM and DCM operation. Delay circuitry is added to prevent gate overlap during both the low-side MOSFET off to high-side MOSFET on transition and the high-side MOSFET off to low-side MOSFET on transition.

Current Monitor (IMON)

The DrMOS current monitor accurately senses MOSFET currents. The currents are summed together to replicate the output filter inductor current. The signal is reported from the DrMOS module in the form of a 5 μA/A current signal. The IMON current will create proportional voltage drop to the R_{IMON} resistor terminated to an external voltage reference and differentially sensed by an external analog / digital PWM controller.

Consideration must be taken in order to maintain a voltage within the IMON dynamic range.

The motivation for the IMON feature is to replace the industry standard output filter DCR sensing, or output current sense using an external precision resistor. Both techniques are lossy and lead to reduced system efficiency. Inductor DCR sensing is also notoriously inaccurate for low value DCR inductors.

Over-Temperature Protection (OTP)

An over-temperature event is considered catastrophic in nature. OTP raises fault flag HIGH once TMON exceeds 150 °C temperature. The driver will shut off both LS and HS FETs when OTP is reached. The device will remain in this state until the temperature falls below OTP-hysteresis. At that point the fault will be cleared and the part will enter normal operation.

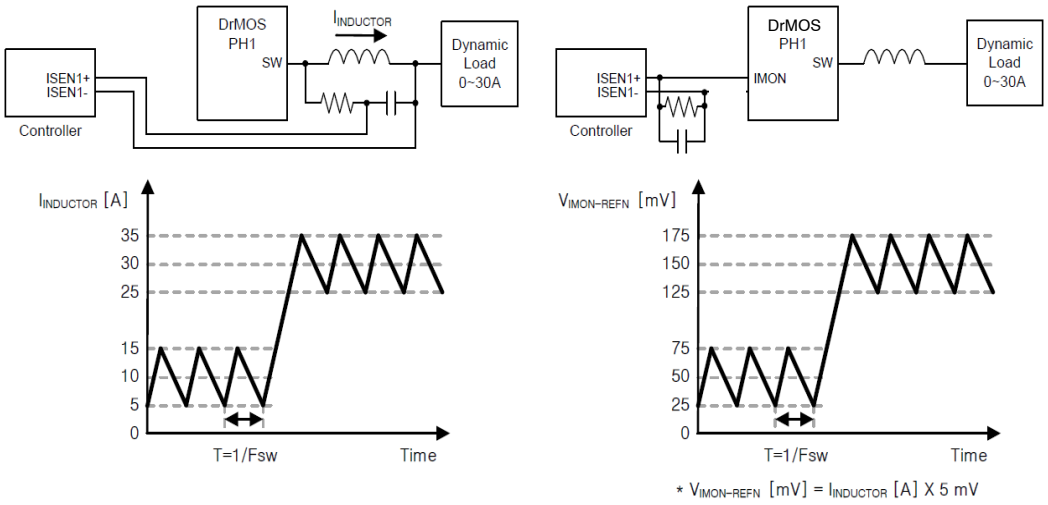


Figure 27. DrMOS with Inductor DCR Sensing vs. DrMOS with IMON

Temperature Monitor / Fault Flag (TMON / FLT)

The TMON/FLT pin on NCP303345 is a thermal monitor output in normal operation (TMON). The TMON pin output is a Proportional to Absolute Temperature (PTAT) voltage sourced signal referenced to AGND when no module FAULT is present. It will typically output 0.8 V at 25 °C with 8 mV/°C typical slope. Before power is ready (EN = 0), the pin has a strong pulldown resistance.

TMON/FLT pins from multiple DrMOS modules (used in multi-phase topologies) can be tied together to share a common thermal bus. Operating with this configuration will force the thermal bus signal to report the highest voltage output TMON signal to the controller (highest temperature). The TMON output has a low output impedance when sourcing current and a high output impedance when sinking current.

The TMON signal reported from the module pin is a buffered version of an internal TMON signal. Configuring the DrMOS module to share a common thermal bus will still permit each module to safely monitor its own temperature since the internal TMON signal is unaffected by the common thermal bus configuration.

The TMON/FLT pin is also used for fault reporting (FLT): over-current (POCP) and over-temperature (OTP) protection. The DrMOS will pull the TMON pin to 3.3 V for either POCP or an OTP event.

The TMON voltage has a slope defined as following equation.

$$\frac{V_{TMON}\,[V]}{T_J\,[°C]} = \frac{1.8\ V - 0.6\ V}{150\ °C - 0\ °C} = 8\ [mV/°C] \qquad \text{(eq. 1)}$$

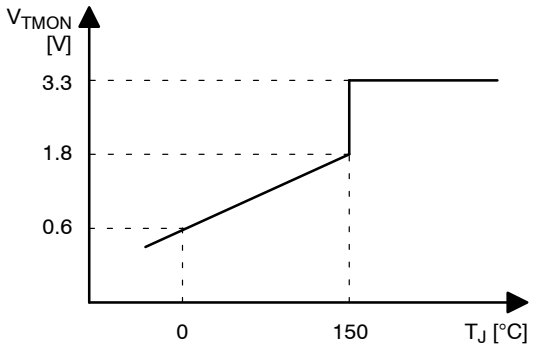


Figure 28. DrMOS T_J vs. V_{TMON}

Peak Over-Current Protection (POCP)

The NCP303345 has cycle-by-cycle over current protection. If current exceeds the POCP threshold, HS FET is gated off regardless of PWM command. HS FET cannot be gated on again until the current is less than the POCP threshold with a hysteresis. Fault flag will be pulled HIGH after eight consecutive cycle-by-cycle POCPs are detected. Both FETs are OFF after eight consecutive POCP counts. The fault flag will only clear with a toggle of EN, or a cycling of VCC.

Negative Over-Current Protection (NOCP)

The NCP303345 can detect large negative inductor current and protect the low side MOSFET. Once this negative current threshold is detected the driver module takes control and truncates LS on-time pulse (LS FET is gated off regardless of PWM command). The driver will stay in this state until one of two things happen 1) The timer expires in which case if the PWM pin is commanding the driver to turn on LS, the driver will respond and NOCP will again be monitored 2) PWM commands HS on in which case the driver will immediately turn on HS regardless of the Timer.

Low Power States

The NCP303345 complies with the required low power states needed to support the Intel IMVP9.1/2/3 specification. There are two lower power states available. Light load which occurs when the ZCD count exceeds eight and then there is ultralight load. That occurs when PWM is held at LOW or MID for greater than $T_{D\_ENT\_LP\_PWM}$.

APPLICATION INFORMATION

Decoupling Capacitor for PVCC and VCC

For the supply input (PVCC and VCC pin), local decoupling capacitors are required to supply the peak driving current and to reduce noise during switching operation. Use at least 0.68~2.2 μF / 0402~0603 / X5R~X7R multi-layer ceramic capacitors for the power rail. Keep these capacitors close to the PVCC and VCC pin and AGND copper planes. If either needs to be located on the bottom side of the board, put through-hole vias on each pad of the decoupling capacitor to connect the capacitor pad on bottom with the pins on top.

The supply voltage range on PVCC and VCC is 4.5 V~5.5 V, typically 5 V for normal applications.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}). A bootstrap capacitor of 0.1~0.22 μF / 0402~0603 / X5R~X7R is usually appropriate for most switching applications. A series bootstrap resistor may be needed for specific applications to lower high-side MOSFET switching speed. The boot resistor is required when the DrMOS is switching above 15 V V_{IN}; when it is effective at controlling V_{SW} overshoot. R_{BOOT} value from 0.5 to 6 Ω is typically recommended to reduce excessive voltage spike and ringing on the SW node. A higher R_{BOOT} value can cause lower efficiency due to high switching loss of high-side MOSFET.

Do not add a capacitor or resistor between the BOOT pin and GND.

It is recommended to add a PCB place holder for a small size 1 nF~1 μF capacitor close to the IMON external reference and AGND to reduce switching noise injection.

It is also recommended to add a small 10~47 pF capacitor in parallel with the IMON resistor from IMON to the external reference. This capacitor can help reduce switching noise coupling onto the IMON signal. The place of the IMON resistor and cap should be close to the controller, not the DrMOS to improve the sensing accuracy.

TMON (Output) / FAULT (Output)

It is recommended to put a 470 pF capacitor near the controller to help with noise. Total capacitance on TMON should not exceed 1 nF. That includes any capacitor components, or trace capacitance.

PCB LAYOUT GUIDELINE

All of the high-current paths; such as VIN, SW, VOUT, and GND coppers; should be short and wide for low parasitic inductance and resistance. This helps achieve a more stable and evenly distributed current flow, along with enhanced heat radiation and system performance.

Input ceramic bypass capacitors must be close to the VIN and PGND pins. This reduces the high-current power loop inductance and the input current ripple induced by the power MOSFET switching operation.

An output inductor should be located close to the NCP303345 to minimize the power loss due to the SW copper trace. Care should also be taken so the inductor dissipation does not heat the DrMOS.

Power MOSFETs used in the output stage are effective at minimizing ringing due to fast switching. In most cases, no RC snubber on SW node is required. If a snubber is used, it should be placed close to the SW and PGND pins. The resistor and capacitor of the snubber must be sized properly to not generate excessive heating due to high power dissipation.

Decoupling capacitor on VCC and BOOT capacitor should be placed as close as possible to the VCC~AGND and BOOT~PHASE pin pairs to ensure clean and stable power supply. Their routing traces should be wide and short to minimize parasitic PCB resistance and inductance.

The board layout should include a placeholder for small-value series boot resistor on BOOT~PHASE. The boot-loop size, including series R_{BOOT} and C_{BOOT}, should be as small as possible.

A boot resistor may be required and it is effective to control the high-side MOSFET turn-on slew rate and SW voltage overshoot. R_{BOOT} can improve noise operating margin in synchronous buck designs that may have noise issues due to ground bounce or high positive and negative V_{SW} ringing. Inserting a boot resistance lowers the DrMOS module efficiency. Efficiency versus switching noise must be considered. R_{BOOT} values from 0 Ω to 4.0 Ω are typically effective in reducing V_{SW} overshoot.

The VIN and PGND pins handle large current transients with frequency components greater than 100 MHz. If possible, these pins should be connected directly to the VIN and board GND planes. The use of thermal relief traces in series with these pins is not recommended since this adds extra parasitic inductance to the power path. This added inductance in series with either the VIN or PGND pin degrades system noise immunity by increasing positive and negative V_{SW} ringing.

PGND pad and pins should be connected to the GND copper plane with multiple vias for stable grounding. Poor grounding can create a noisy and transient offset voltage level between PGND and AGND. This could lead to faulty operation of gate driver and MOSFETs.

Ringing at the BOOT pin is most effectively controlled by close placement of the boot capacitor. Do not add any additional capacitors between BOOT to PGND. This may lead to excess current flow through the BOOT diode, causing high power dissipation.

Put multiple vias on the VIN and VOUT copper areas to interconnect top, inner, and bottom layers to evenly distribute current flow and heat conduction. Do not put too many vias on the SW copper to avoid extra parasitic inductance and noise on the switching waveform. As long as efficiency and thermal performance are acceptable, place only one SW node copper on the top layer and put no vias on the SW copper to minimize switch node parasitic noise. Vias should be relatively large and of reasonably low inductance. Critical high-frequency components; such as R_{BOOT}, C_{BOOT}, RC snubber, and bypass capacitors; should be located as close to the respective DrMOS module pins as possible on the top layer of the PCB. If this is not feasible, they can be placed on the board bottom side and their pins connected from bottom to top through a network of low-inductance vias.

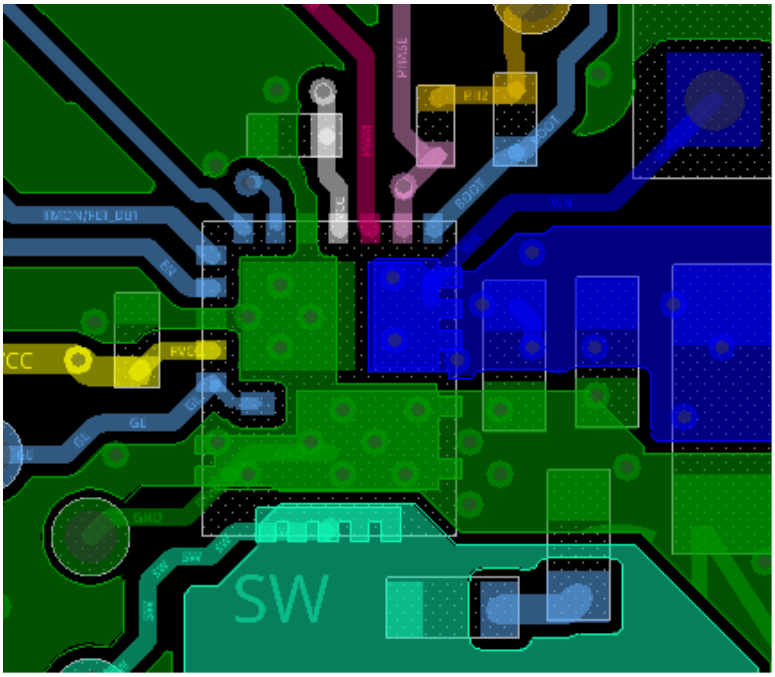


Figure 29. Layout Example − Top View

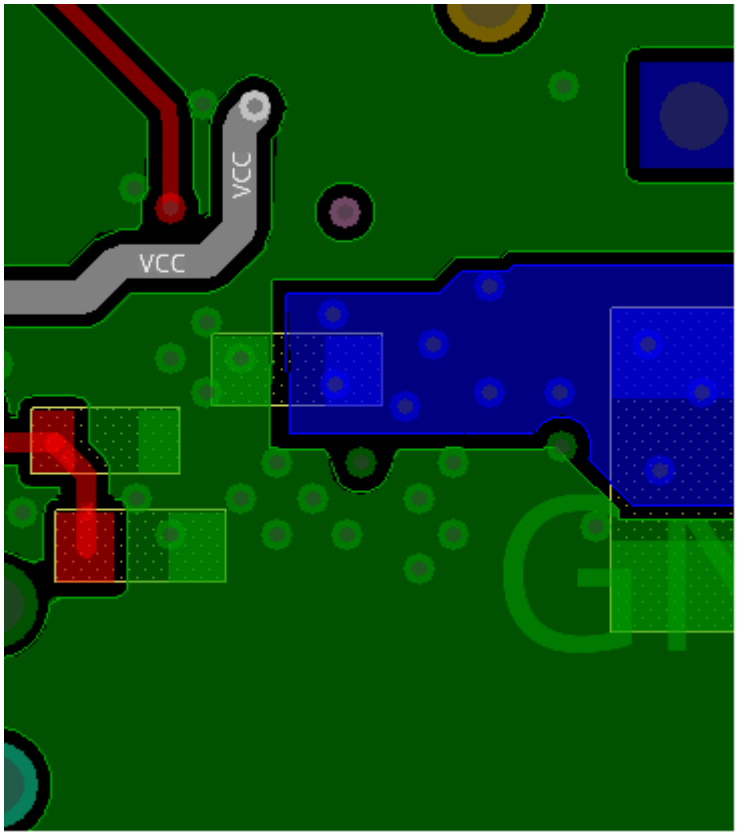


Figure 30. Layout Example − Bottom Layer

EVALUATION BOARD INFORMATION

The NCP303345 evaluation board (EVB) is 70 mm x 70 mm with 6 total layers. All layers have a 2 oz. copper finish.

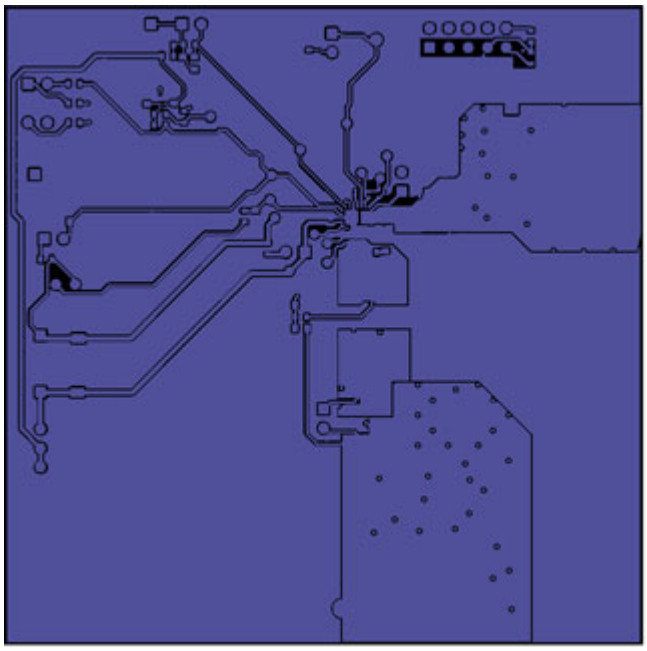


Figure 31. EVB Top Layer

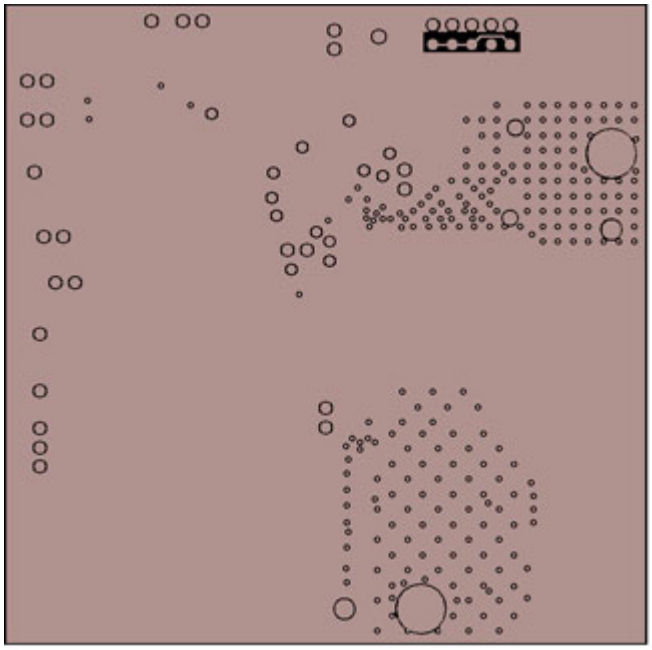


Figure 32. EVB Inner Layer 1

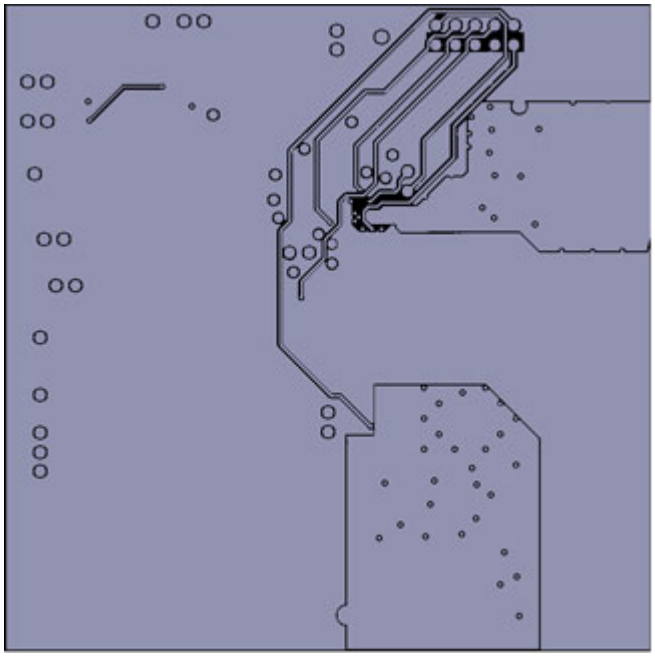


Figure 33. EVB Inner Layer 2

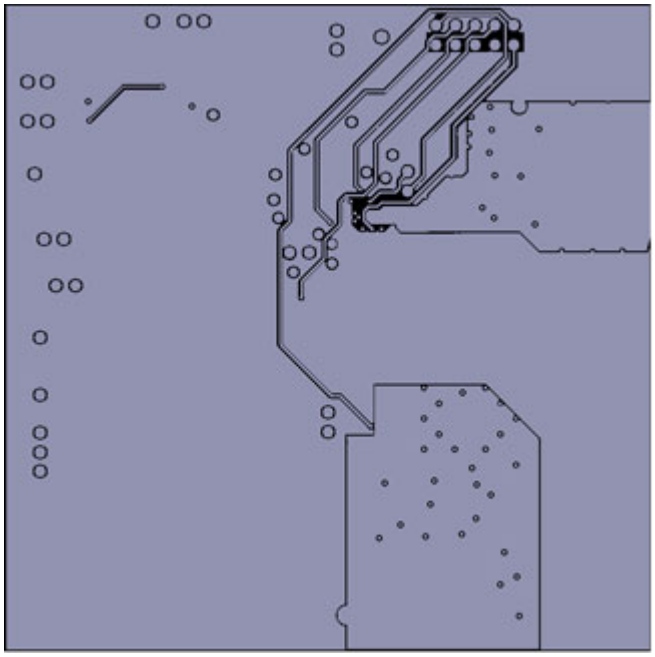


Figure 34. EVB Inner Layer 3

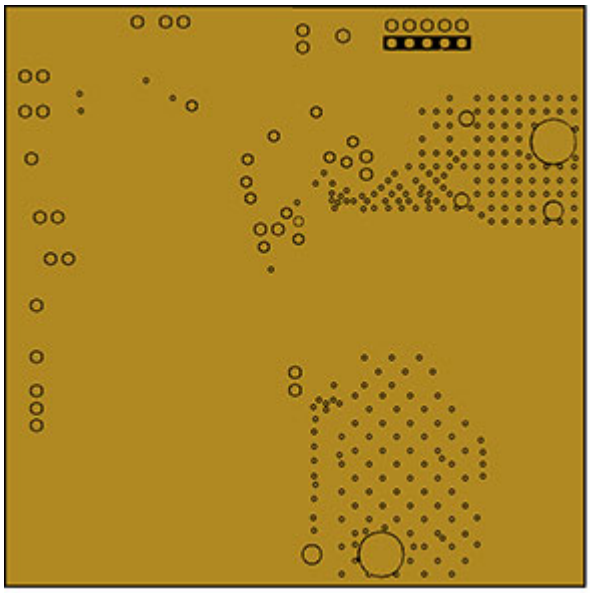


Figure 35. EVB Inner Layer 4

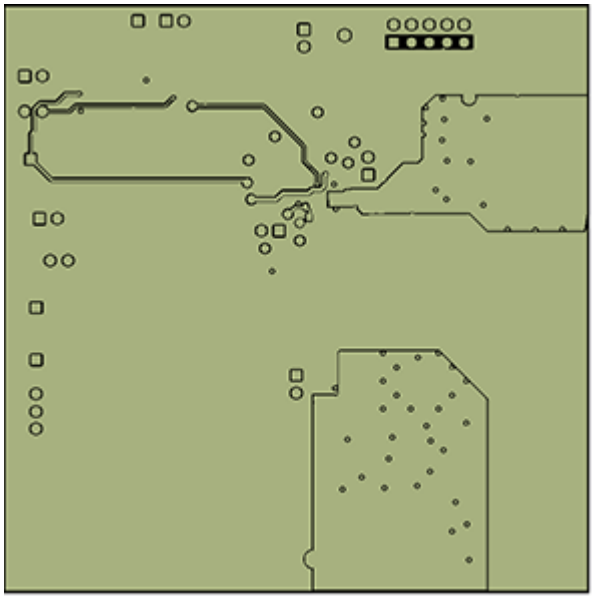


Figure 36. EVB Bottom Layer

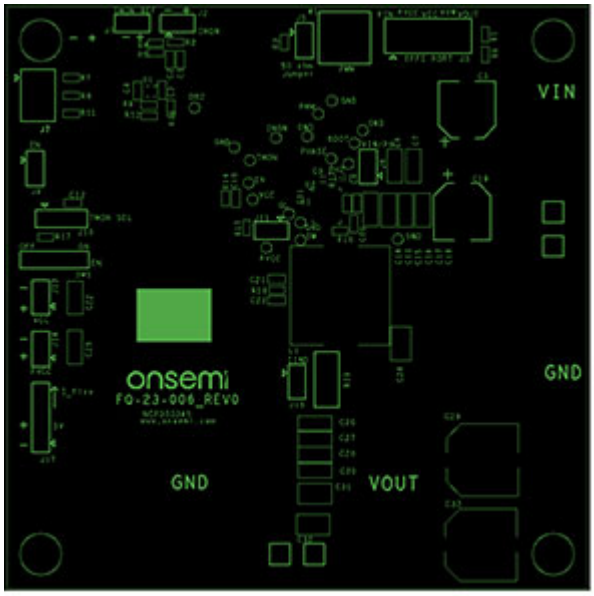


Figure 37. EVB Silkscreen Top

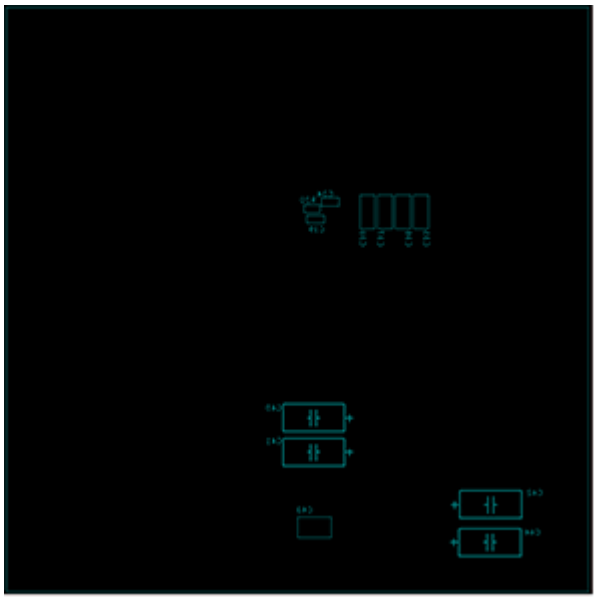
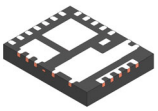


Figure 38. EVB Bottom Layer 3

REVISION HISTORY

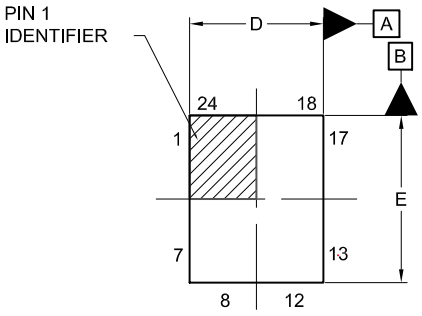
Revision	Description of Changes	Date
0	Initial document release.	11/10/2025
1	Corrected marking diagram coding.	2/5/2026
2	Removed recommendation for peak output current.	4/6/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

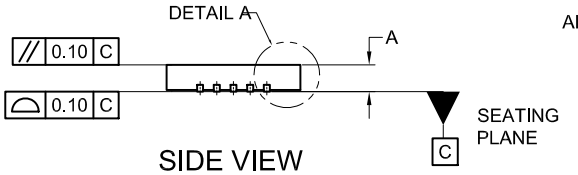


PQFN24 4.00x5.00x0.75, 0.50P
CASE 483BV
ISSUE C

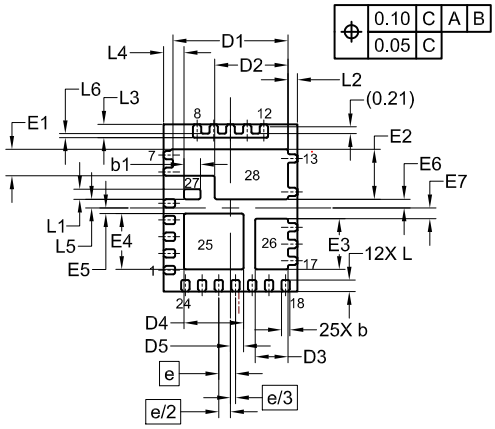
DATE 09 DEC 2024



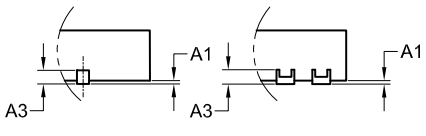
TOP VIEW



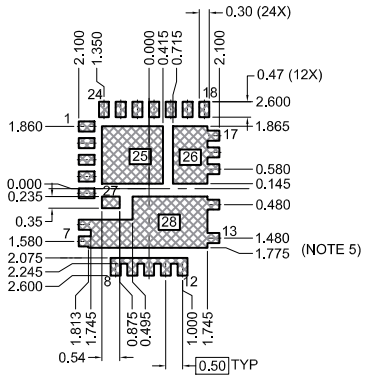
SIDE VIEW



BOTTOM VIEW



DETAIL A
ALTERNATE CONSTRUCTIONS



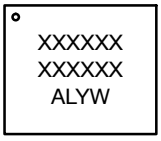
RECOMMENDED
MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES: UNLESS OTHERWISE SPECIFIED
1) THIS PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-220.
2) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DO NOT EXCEED 0.10 MM
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) DIMENSIONING AND TOLERANCING PER ASME Y14.5-2018.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.025	0.05
A3	0.15	0.20	0.25
b	0.20	0.25	0.30
b1	0.44	0.49	0.54
D	3.90	4.00	4.10
D1	3.34	3.44	3.54
D2	2.09	2.19	2.29
D3	0.88	0.98	1.08
D4	1.68	1.78	1.88
D5	0.34	0.39	0.44
E	4.90	5.00	5.10
E1	0.69	0.79	0.89
E2	1.39	1.49	1.59
E3	1.42	1.52	1.62
E4	1.57	1.67	1.77
E5	0.12	0.17	0.22
E6	0.21	0.26	0.31
E7	0.27	0.32	0.37
e	0.50 BSC		
e/2	0.35 BSC		
e/3	0.15 BSC		
L	0.29	0.34	0.39
L1	0.25	0.30	0.35
L2	0.23	0.28	0.33
L3	0.35	0.40	0.45
L4	0.56	0.61	0.66
L5	0.21	0.26	0.31
L6	0.07	0.12	0.17

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Assembly Lot Trace Code
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**PQFN24 4.00x5.00x0.75, 0.50P**		**PAGE 1 OF 1**

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