High-Voltage Switcher with Linearly Regulated Output

NCP10970

The NCP10970 includes a high−voltage switcher, linear regulator and a dedicated comparator circuitry. The switcher is suitable for building output voltage up to 16 V (adjustable by resistor divider on FB pin) protected against short−circuit. Dedicated internal circuitry prevents continuous conduction mode (CCM) operation improves the surge robustness, efficiency and EMI. In no−load/light−load conditions, the part enters skip cycle operation and ensures low standby power consumption.

A proprietary technique ensures high efficiency in the down−conversion process from output switcher voltage rail to raw sub voltage rail supplying a linear regulator.

A dedicated comparator circuitry provides a means to instruct the control section that an over−temperature point has been reached. The comparator input is biased by a precise constant current source and output is an open−drain type.

To ensure the very low no−load standby power, the device is equipped with a very effective standby mode with a low wake−up time for return to the normal operation mode.

Features

- Built−in 670 V, 18 Ω $R_{DS(on)}$ Lateral MOSFET
- High−voltage Start−up Current Source
- Fixed−frequency DCM Current−mode Control Scheme
- End of Demagnetization Detection Ensures DCM Operation only
- Short−circuit Protected Switcher Output with Auto−recovery Function
- 4 ms Soft Start
- Internal Linear Regulator with Short−circuit Protected Output
- Internal Comparator with Open Drain Output
- Internal Thermal Shutdown
- 16−pin SO Package with Creepage Distance
- These are Pb−Free Devices

Typical Applications

- Power Management for Smart Lighting Application
- Power Management for White Goods, IoT Application, etc.

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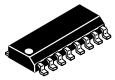
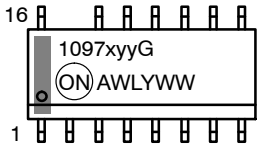


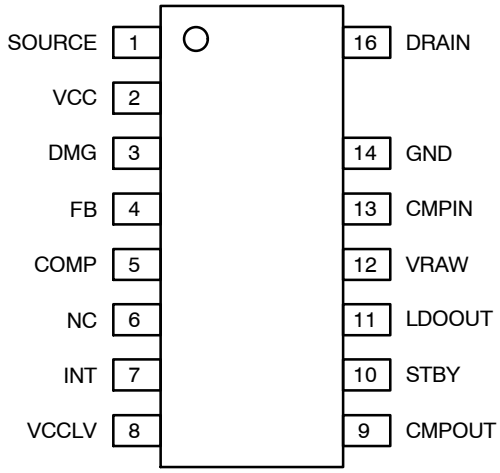
SOIC−16 NB, LESS PIN 15
CASE 752AC

MARKING DIAGRAM



1097xyy = Specific Device Code
(x = 0, yy = A1, B1)
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 22 of this data sheet.

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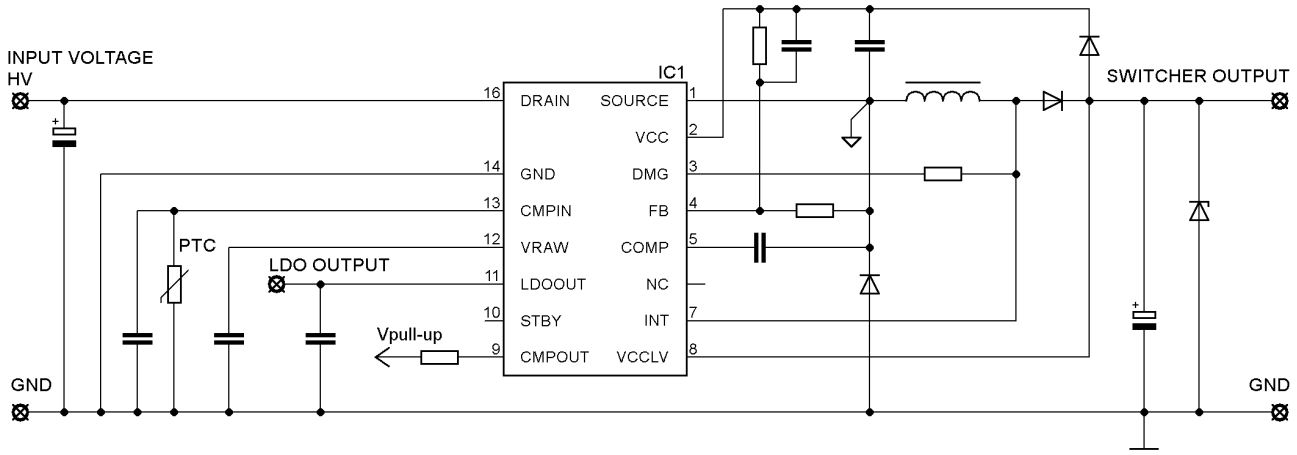


Figure 1. Application Schematic

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	SOURCE	The switcher ground	This pin is connected to the buck source/inductor junction and grounds the switcher circuitry. The dissipated heat of the transistor is conducted out through this pin.
2	VCC	Supplies the switcher section	The switcher V_{CC} voltage up to 20 V.
3	DMG	Demagnetization detection	This pin monitors the inductor magnetic activity.
4	FB	Feedback pin	This pin senses the output voltage through a resistive divider.
5	COMP	Loop compensation	The error amplifier output is available on this pin. The network connected between this pin and ground adjusts the control loop bandwidth.
6	NC	Not connected pin	Not connected pin for better isolation between high voltage and low voltage pins.
7	INT	The intermediate buck point	This is the input to generate the raw dc voltage.
8	VCCLV	Supplies the low−voltage section	The V_{CCLV} voltage biases the MOSFET driver, Comparator and LDO circuitry.
9	CMPOUT	Comparator output	Open−drain output pin of internal comparator. This pin is pulled low when the CMPIN passes above 1 V.
10	STBY	Standby pin	This pin affects the speed of comparator and IC consumption. Standby mode (grounded pin) − slow comparator. Active mode (> 3 V on pin) − fast comparator.
11	LDOOUT	LDO output	A short−circuit protected 3.3 V or 5 V rail.
12	VRAW	The intermediate bus rail	This is the raw voltage driving the LDO.
13	CMPIN	Comparator input	Input of the internal comparator, internally biased by a 120 μA current source.
14	GND	The ground of low−voltage section	−
15	−	−	Creepage distance.
16	DRAIN	Drain connection	The connection to the lateral MOSFET drain.

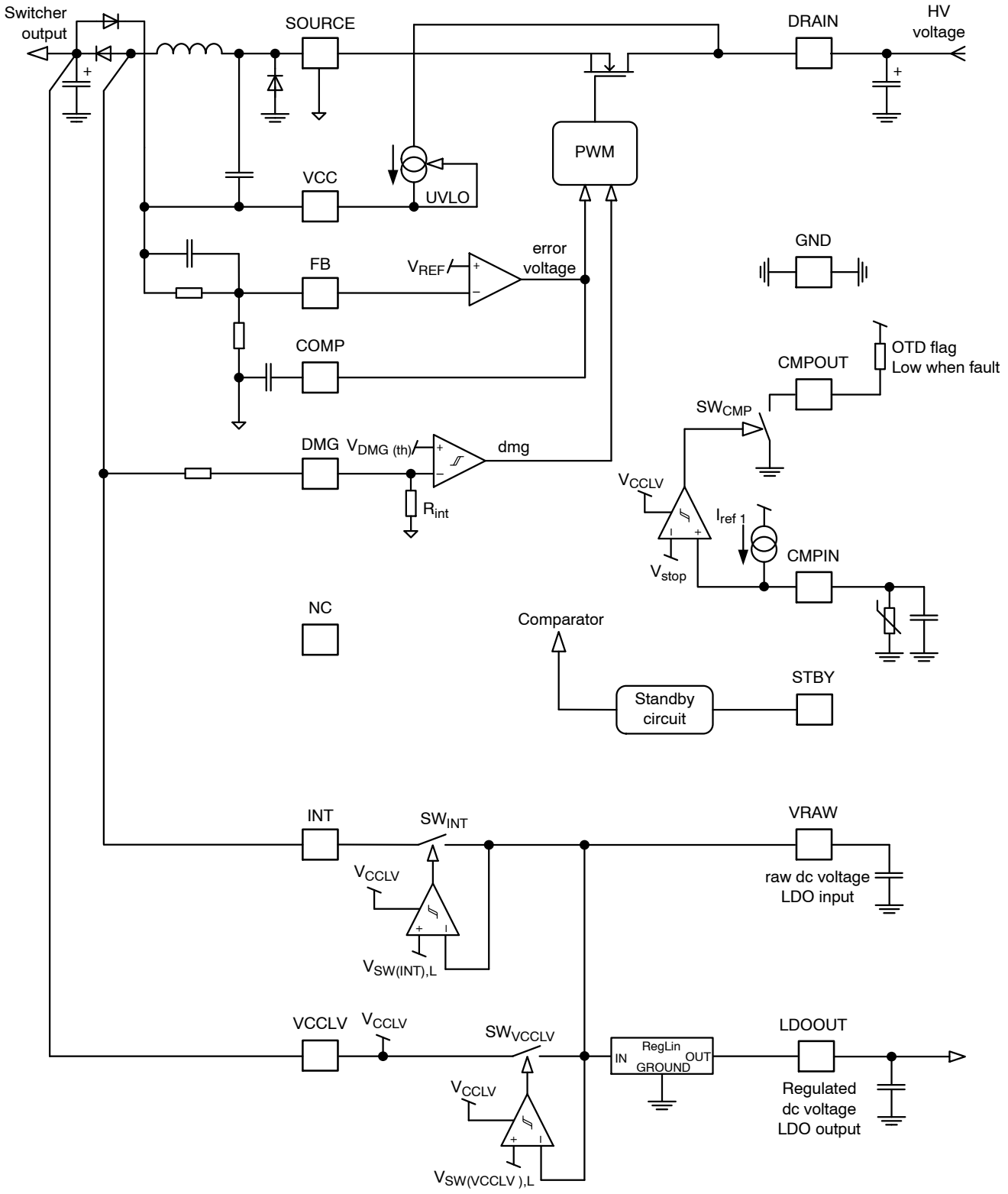


Figure 2. Simplified Block Diagram

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
SWITCHER PINS – VOLTAGE ON PINS RELATED TO SOURCE PIN			
BV_{DSS}	Drain voltage	−0.3 to 670	V
V_{CC}	Power Supply voltage pin, continuous voltage	−0.3 to 20	V
V_{FB}, V_{COMP}, V_{DMG}	Voltage on FB, COMP and DMG pins	−0.3 to 10	V
$I_{DMG,clamp}$	Maximum current of clamped DMG pin (voltage on pin is clamped to −0.7 V / 10 V)	−2 / 3	mA
LOW VOLTAGE PINS – VOLTAGE ON PINS RELATED TO GND PIN			
V_{CCLV}, V_{INT}	Power Supply voltage pins, continuous voltage	−0.3 to 20	V
V_{CMPIN}, V_{LDOOUT}, V_{STBY}	Voltage on CMPIN, STBY and LDOOUT pins, continuous voltage	−0.3 to 5.5	V
V_{CMPOUT}, V_{RAW}	Voltage on CMPOUT, VRAW pins, continuous voltage	−0.3 to V_{CC} + 0.3	V
COMMON PARAMETERS			
$T_{J,max}$	Maximum Junction Temperature	150	°C
$T_{storage}$	Storage Temperature Range	−60 to +150	°C
ESD_{HBM}	ESD Capability, Human Body Model	2	kV
ESD_{CDM}	ESD Capability, Charged−Device Model	1	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and is tested by the following methods:
   - ESD Human Body Model tested per JEDEC Standard JESD22−A114F
   - ESD Charged−Device Model tested per JEDEC Standard JESD22−C101F
   - Latch−up protection and exceeds 100 mA per JEDEC standard JESD78

THERMAL CHARACTERISTICS

Symbol	Rating	Value	Unit
$R_{\theta J-ASW}$	Thermal Resistance Junction−to−Air − switcher section only	150	°C/W
$R_{\theta J-ALV}$	Thermal Resistance Junction−to−Air − low−voltage section only	150	°C/W

ELECTRICAL CHARACTERISTICS – HIGH−VOLTAGE SWITCHER

(V_{CC} = V_{CCLV} = 12 V unless otherwise noted, for typical values T_J = 25°C, for min/max values T_J = −40°C to 125°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY SECTION AND V_{CC} MANAGEMENT						
$V_{CC(on)}$	V_{CC} increasing level at which the switcher starts operation		8.4	9.0	9.5	V
$V_{CC(min)}$	V_{CC} decreasing level at which the HV current source restarts		7.0	7.4	7.8	V
$V_{CC(off)}$	V_{CC} decreasing level at which the switcher stops operation (UVLO)		6.7	7.0	7.2	V
I_{CC1}	Internal IC consumption	f_{SW} = 65 kHz	−	1	−	mA
I_{CCskip}	Internal IC consumption	V_{COMP} = 0 V (No switching MOSFET)	−	340	−	μA
POWER SWITCH CIRCUIT						
$R_{DS(on)}$	Power Switch Circuit on−state resistance	I_D = 50 mA, T_J = 25°C I_D = 50 mA, T_J = 125°C	− −	18 33	23 38	Ω
BV_{DSS}	Power Switch Circuit & Startup breakdown voltage	$I_{D(off)}$ = 120 μA, T_J = 25°C Figure 9 shows the temp. dependency	670	−	−	V
$I_{DSS(off)}$	Power Switch & Startup off−state leakage current	T_J = 125 °C, V_{DS} = 670 V T_J = 125 °C, V_{DS} = 400 V	− −	5 2	− −	μA
t_r	Turn−on time (90% − 10%)	R_L = 50 Ω, V_{DS} set for I_{drain} = 0.7 x I_{PK}	−	35	−	ns

ELECTRICAL CHARACTERISTICS – HIGH–VOLTAGE SWITCHER (continued)
(V_{CC} = V_{CCLV} = 12 V unless otherwise noted, for typical values T_J = 25°C, for min/max values T_J = −40°C to 125°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
POWER SWITCH CIRCUIT						
t_f	Turn−off time (10% – 90%)		–	10	–	ns
$t_{on(min)}$	Minimum on time		–	300	–	ns
INTERNAL START−UP CURRENT SOURCE						
I_{start1}	High−voltage current source	V_{CC} = $V_{CC(on)}$ − 200 mV	4	8	12	mA
I_{start2}	High−voltage current source	V_{CC} = 0 V	–	0.4	–	mA
$V_{CC(th)}$	V_{CC} transient level for I_{start1} to I_{start2} toggling point		–	1.3	–	V
$V_{HV(min)}$	Minimum startup voltage	V_{CC} = $V_{CC(on)}$ − 200 mV	–	–	22	V
CURRENT COMPARATOR						
I_{PK}	Maximum internal current setpoint (Note 2)	T_J = 25°C	325	350	375	mA
$I_{PK(SW)}$	Final switch current with a primary slope of 320 mA/μs	f_{sw} = 65 kHz	–	370	–	mA
t_{SS}	Soft−start duration		–	4	–	ms
t_{prop}	Propagation delay from current detection to drain OFF state		–	70	–	ns
t_{LEB}	Leading Edge Blanking Duration		–	130	–	ns
INTERNAL OSCILLATOR						
f_{OSC}	Oscillation frequency (Note 3)	T_J = 25°C	59	65	71	kHz
D_{max}	Maximum duty ratio		62	66	72	%
DEMAGNETIZATION DETECTION BLOCK						
$V_{DMG(th)}$	Input threshold	Voltage is decreasing	15	50	85	mV
$V_{DMG(th,H)}$	Hysteresis	Voltage is increasing	–	25	–	mV
t_{dem}	Demag propagation delay		–	70	–	ns
t_{blank}	Blanking time after turn off the switcher transistor	Step from negative voltage value (equal to −1 mA) to positive voltage 1 V	0.5	1.0	–	μs
R_{int}	DMG pin internal resistance		–	40	–	kΩ
C_{int}	DMG pin internal capacitance	Guaranteed by design	–	10	–	pF
ERROR AMPLIFIER SECTION						
V_{REF}	Error amplifier reference voltage		3.2	3.3	3.4	V
I_{FB}	Input Bias Current	V_{FB} = 3.3 V	–	1	–	μA
G_M	Transconductance		–	2	–	mS
I_{OTAlim}	OTA maximum current capability	V_{FB} > V_{OTAen}	–	±150	–	μA
V_{OTAen}	FB voltage to disable OTA		0.7	1.3	1.7	V
COMPENSATION SECTION						
$I_{COMPfault}$	COMP current for which fault is detected		–	−40	–	μA
$I_{COMP100\%}$	COMP current for which internal current set−point is 100% (I_{PK})		–	−44	–	μA
$I_{COMPfreeze}$	COMP current for which internal current setpoint is I_{Freeze}		–	−80	–	μA
$I_{COMPskip}$	The COMP pin current level to enter skip mode		–	−120	–	μA
$V_{COMP(REF)}$	Equivalent pull−up voltage in linear regulation range	Guaranteed by design	–	2.7	–	V

ELECTRICAL CHARACTERISTICS – HIGH−VOLTAGE SWITCHER (continued)

(V_{CC} = V_{CCLV} = 12 V unless otherwise noted, for typical values T_J = 25°C, for min/max values T_J = −40°C to 125°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
COMPENSATION SECTION						
$R_{COMP(up)}$	Equivalent feedback resistor in linear regulation range	Guaranteed by design	–	17.7	–	kΩ
I_{Freeze}	Internal minimum current setpoint	$I_{COMP} < I_{COMPFreeze}$	–	110	–	mA
PROTECTIONS						
t_{SCP}	Fault validation before error flag is asserted	$I_{COMP} > I_{COMPfault}$	35	48	–	ms
$t_{recovery}$	OFF phase in fault mode		–	400	–	ms
V_{OVP}	V_{CC} voltage at which the switcher stops pulsing		17.0	18.0	18.8	V
t_{OVP}	Filter of V_{CC} OVP comparator		–	80	–	μs
TEMPERATURE MANAGEMENT						
TSD	Temperature shutdown	Guaranteed by design	150	160	–	°C
TSD_{HYST}	Hysteresis in shutdown	Guaranteed by design	–	20	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. There is no compensation ramp in this switcher as CCM operation is prevented by the demagnetization detector.
3. Oscillator frequency is measured with grounded DMG pin. The frequency f_{OSC} doesn't have to be observed in application due to active Demagnetization Detection Block.

ELECTRICAL CHARACTERISTICS – LOW VOLTAGE SECTION

(V_{CC} = V_{CCLV} = 12 V unless otherwise noted, for typical values T_J = 25°C, for min/max values T_J = −40°C to 125°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY SECTION						
$V_{CCLV(on)}$	V_{CCLV} increasing level for activation the internal switches SW_{INT} and SW_{VCCLV}		–	8.4	–	V
$V_{CCLV(Hyst)}$	V_{CCLV} hysteresis for deactivation		–	4.7	–	V
I_{CCLV1}	Internal IC consumption in standby (grounded pin STBY)	Low voltage section is biased, no switching of internal MOSFETs SW_{INT} and SW_{VCCLV}, no I_{ref1}	–	270	360	μA
I_{CCLV4}	Internal IC consumption in active mode (pin STBY in High state)	Low voltage section is biased, no switching of internal MOSFETs SW_{INT} and SW_{VCCLV}, no I_{ref1}	–	350	–	μA
RAW VOLTAGE GENERTION						
$R_{DS(on),INT}$	$R_{DS(on)}$ of internal MOSFET SW_{INT}	I_{DS} = 200 mA, T_J = 25°C I_{DS} = 200 mA, T_J = 125°C	– –	5 –	7 10	Ω
$R_{DS(on),VCCLV}$	$R_{DS(on)}$ of internal MOSFET SW_{VCCLV}	I_{DS} = 50 mA, T_J = 25°C I_{DS} = 50 mA, T_J = 125°C	– –	15 –	20 30	Ω
$V_{SW(VCCLV),L}$	Voltage for turn−on the switch SW_{VCCLV} · A version (3.3 V) · B version (5 V)	voltage is decreasing, T_J = 25°C	 3.56 5.25	 3.60 5.30	 3.64 5.35	V
$V_{SW(VCCLV),H}$	Voltage for turn−off the switch SW_{VCCLV} · A version (3.3 V) · B version (5 V)	voltage is increasing	 – –	 3.65 5.35	 – –	V
$V_{SW(INT),L}$	Voltage for turn−on the switch SW_{INT} · A version (3.3 V) · B version (5 V)	voltage is decreasing	 – –	 3.80 5.50	 – –	V
$V_{SW(INT),H}$	Voltage for turn−off the switch SW_{INT} · A version (3.3 V) · B version (5 V)	voltage is increasing	 – –	 3.85 5.55	 – –	V
$t_{del(SW)}$	Propagation delay of switches INT and VCCLV	voltage is decreasing/increasing	–	1.5	–	μs

ELECTRICAL CHARACTERISTICS – LOW VOLTAGE SECTION (continued)
(V_{CC} = V_{CCLV} = 12 V unless otherwise noted, for typical values T_J = 25°C, for min/max values T_J = −40°C to 125°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
LOW DROPOUT REGULATOR (Input capacitances C_{RAW} = 22 μF, Output capacitances C_{OUT} = 10 μF)						
$I_{LDOOUT(max)}$	Output current capability (Note 4)		–	100	–	mA
I_{CL}	Maximum limitation of output current	Figure 27 shows the temp. dependency	130	260	420	mA
V_{LDOOUT}	Output voltage accuracy · A version (3.3 V) · B version (5 V)	I_{OUT} = 1.0 mA, T_J = 25°C (Note 5)	 3.267 4.95	 3.300 5.00	 3.333 5.05	V
V_{DO}	Dropout voltage · A version (3.3 V) · B version (5 V)	I_{OUT} = 100 mA	–	150	250	mV
Reg_{LINE}	Line regulation	A version: 3.6 V < V_{IN} < 4 V, I_{OUT} = 1 mA B version: 5.4 V < V_{IN} < 6 V, I_{OUT} = 1 mA	–	–	10	mV
Reg_{LOAD}	Load regulation	I_{OUT} = 1.0 to 60 mA I_{OUT} = 1.0 to 100 mA	– –	5 9	15 20	mV
$Tran_{LOAD}$	Load transient response	I_{OUT} = 3.0 to 30 mA, t_{rise} = t_{fall} = 1 μs I_{OUT} = 50 to 100 mA, t_{rise} = t_{fall} = 1 μs	– –	35 40	– –	mV
PSRR	Power Supply Rejection Ratio	V_{IN} = 3.7 V for A version V_{IN} = 5.5 V for B version $V_{IN(pk-pk)}$ = 0.1 V, f = 1 kHz, I_{OUT} = 60 mA (Guaranteed by design) Figure 31 shows the freq. dependency	60	–	–	dB
V_{NOISE}	Output noise	I_{OUT} = 60 mA, f = 100 Hz to 100 kHz Figure 32 shows the freq. dependency	–	300	–	μV_{rms}
COMPARATOR						
$V_{CMP(on)}$	V_{CCLV} increasing level for activation the comparator		–	4.4	–	V
$V_{CMP(Hyst)}$	V_{CCLV} hysteresis for deactivation		–	0.6	–	V
V_{stop}	Voltage above which the COMPOUT pin is pulled down		0.95	1	1.06	V
$V_{restart}$	Voltage below which the COMPOUT pin is in high impedance state		0.75	0.8	0.85	V
I_{ref1}	Current source biasing the CMPIN pin		114	120	126	μA
R_{drain}	Internal MOSFET $R_{DS(on)}$		–	10	20	Ω
I_{CMPOUT}	Current capability of internal MOSFET – current flowing into COMPOUT pin	Guaranteed by design	10	–	–	mA
t_{del1}	Debouncing time constant on the comparator output from High to Low		–	0	–	μs
t_{del2}	Debouncing time constant on the comparator output from Low to High		–	0	–	μs
t_{del}	Comparator propagation delay – active mode – standby mode	Step 0.5 V to 1.2 V	 – –	 60 220	 105 –	ns
TEMPERATURE SHUTDOWN						
$TSD_{(LV)}$	Temperature shutdown	Guaranteed by design	150	160	–	°C
$TSD_{(LV)HYST}$	Hysteresis in shutdown	Guaranteed by design	–	20	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The accuracy of output voltage is guaranteed up to output current value specified by $I_{LDOOUT(max)}$. For higher output current value, the accuracy can be improved by using a higher capacitances C_{RAW}/C_{OUT}.
5. The output voltage V_{LDOOUT} of LDO is guaranteed for 25°C only. The temperature dependency graph shows the temperature dependency for −40°C to 125°C.

TYPICAL CHARACTERISTICS – HIGH VOLTAGE SWITCHER

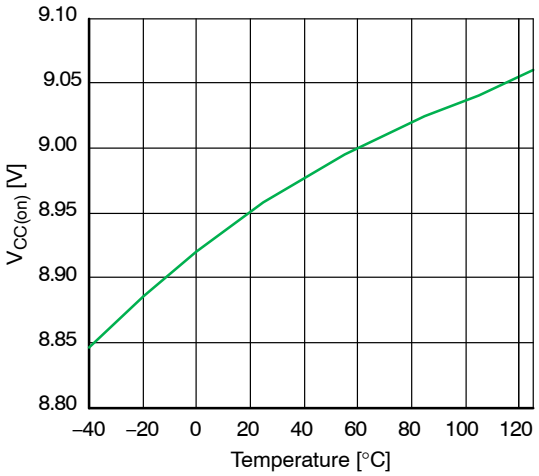


Figure 3. $V_{CC(on)}$ vs. Temperature

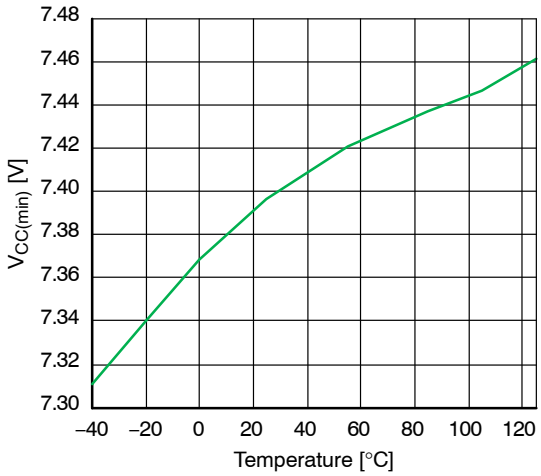


Figure 4. $V_{CC(min)}$ vs. Temperature

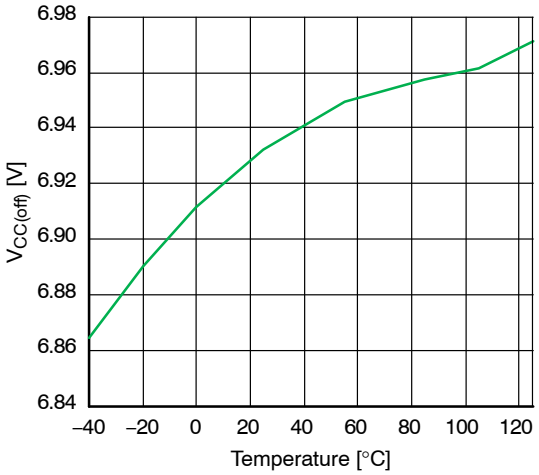


Figure 5. $V_{CC(off)}$ vs. Temperature

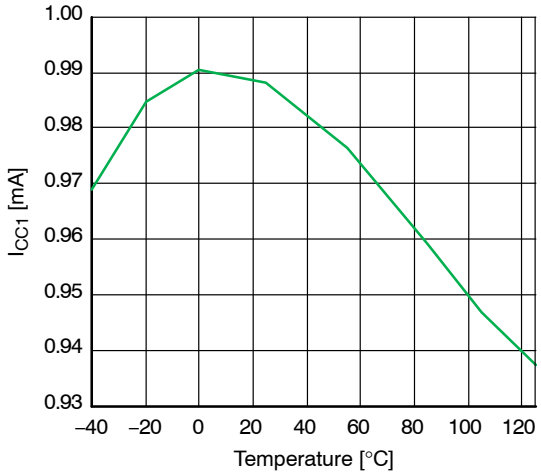


Figure 6. I_{CC1} vs. Temperature

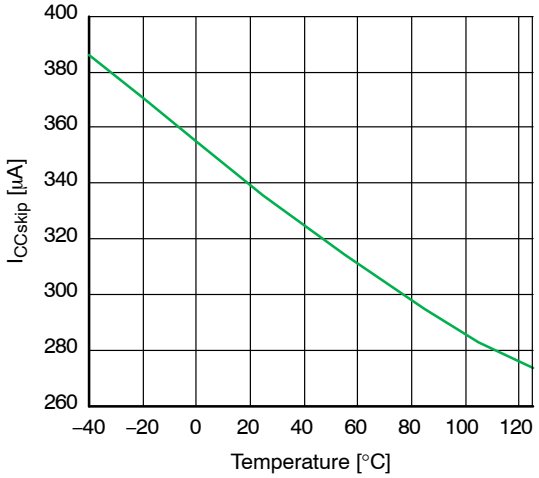


Figure 7. I_{CCskip} vs. Temperature

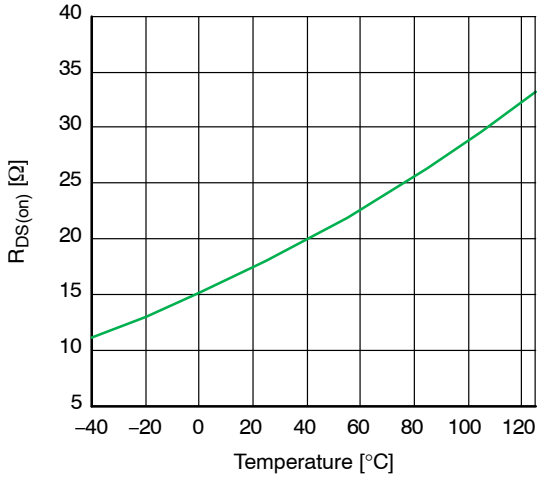


Figure 8. $R_{DS(on)}$ vs. Temperature

TYPICAL CHARACTERISTICS – HIGH VOLTAGE SWITCHER

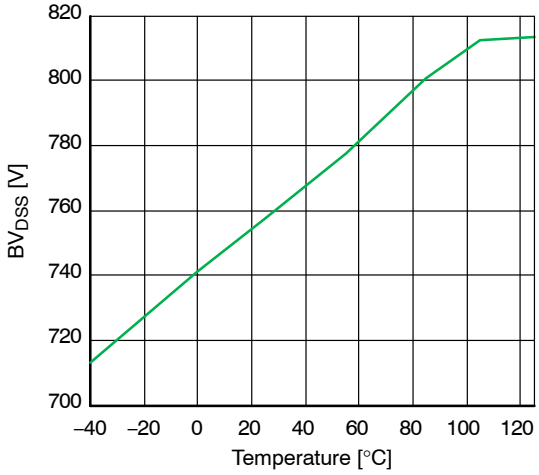


Figure 9. Breakdown voltage vs. Temperature

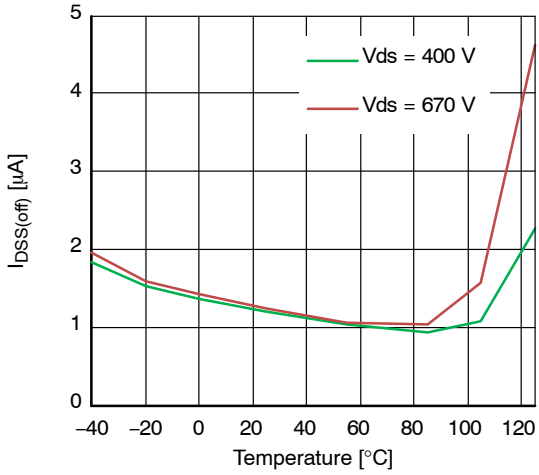


Figure 10. $I_{DSS(off)}$ vs. Temperature

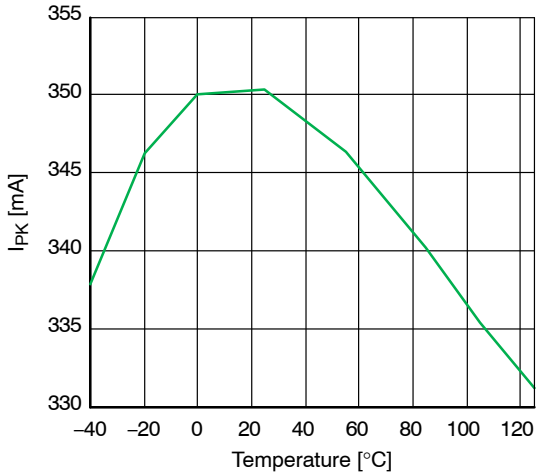


Figure 11. I_{PK} vs. Temperature

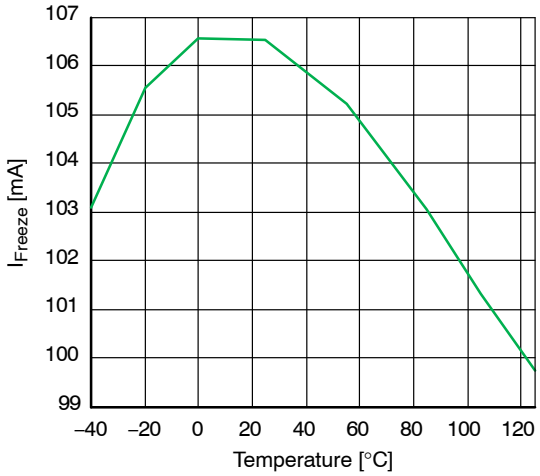


Figure 12. I_{Freeze} vs. Temperature

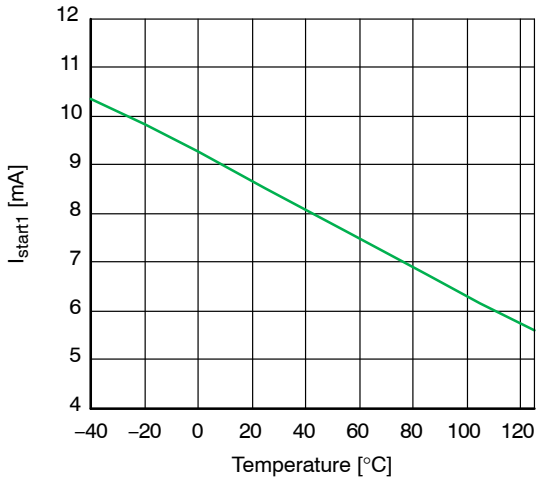


Figure 13. I_{start1} vs. Temperature

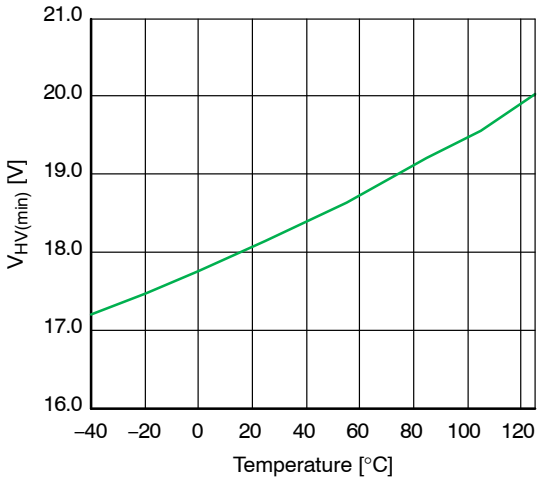


Figure 14. $V_{HV(min)}$ vs. Temperature

TYPICAL CHARACTERISTICS – LOW VOLTAGE SECTION

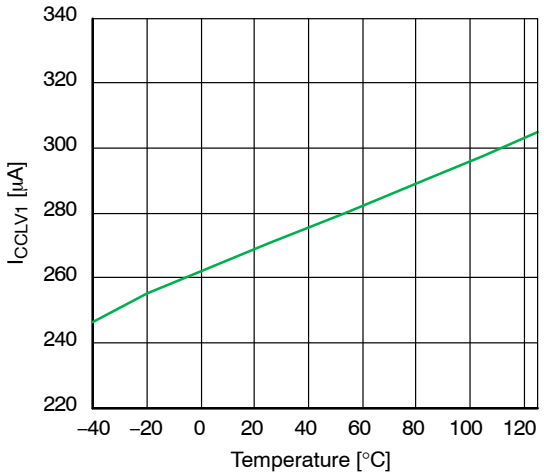


Figure 15. I_{CCLV1} vs. Temperature

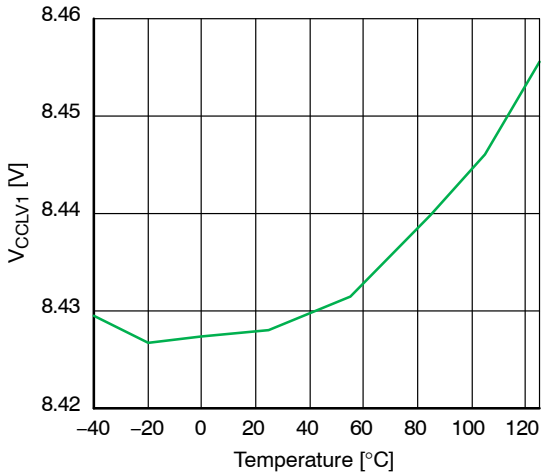


Figure 16. $V_{CCLV(on)}$ vs. Temperature

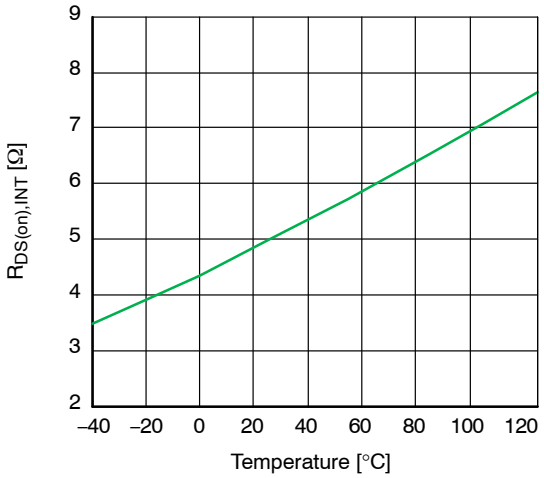


Figure 17. $R_{DS(on),INT}$ vs. Temperature

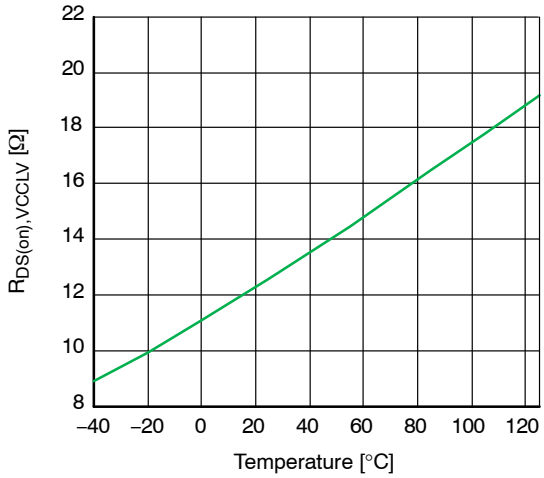


Figure 18. $R_{DS(on),VCCLV}$ vs. Temperature

TYPICAL CHARACTERISTICS – RAW VOLTAGE GENERATION FOR A1 VERSION (3.3 V OUTPUT)

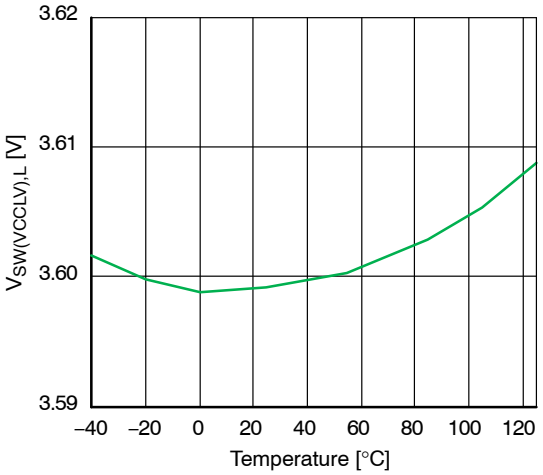


Figure 19. $V_{SW(VCCLV),L}$ vs. Temperature

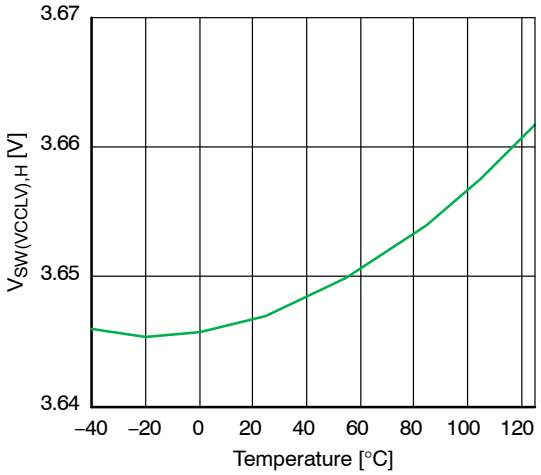


Figure 20. $V_{SW(VCCLV),H}$ vs. Temperature

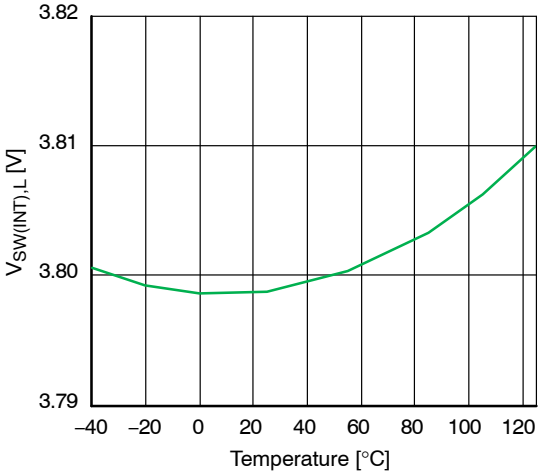


Figure 21. $V_{SW(INT),L}$ vs. Temperature

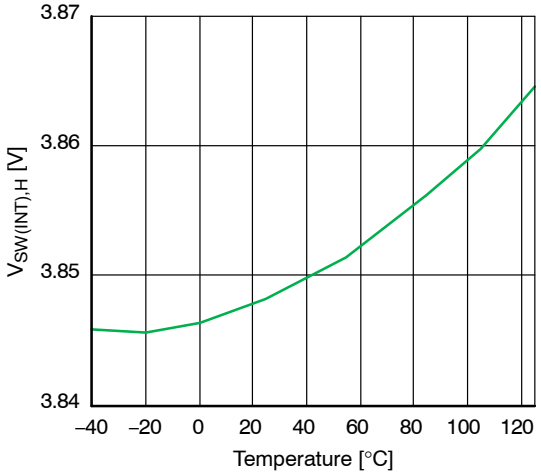


Figure 22. $V_{SW(INT),H}$ vs. Temperature

TYPICAL CHARACTERISTICS – RAW VOLTAGE GENERATION FOR B1 VERSION (5 V OUTPUT)

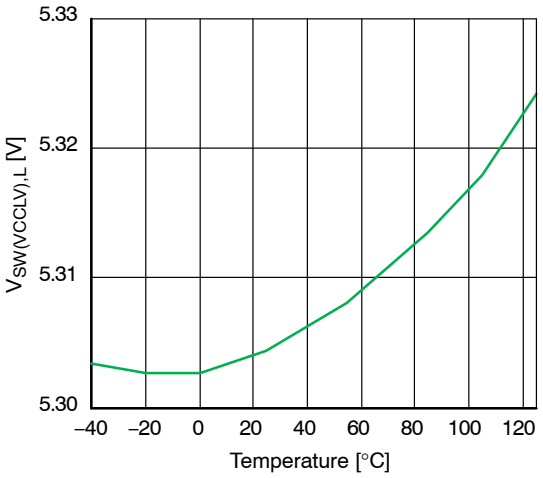


Figure 23. $V_{SW(VCCLV),L}$ vs. Temperature

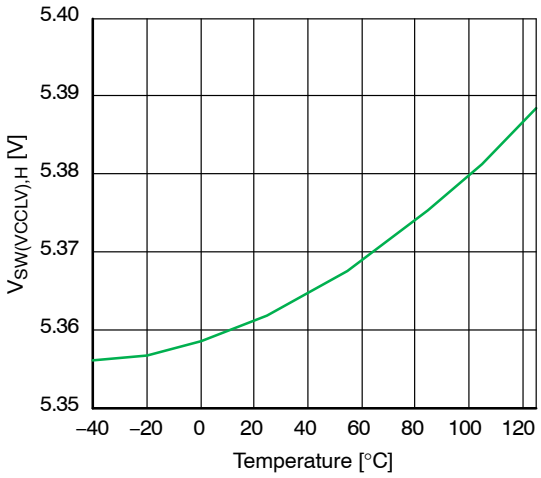


Figure 24. $V_{SW(VCCLV),H}$ vs. Temperature

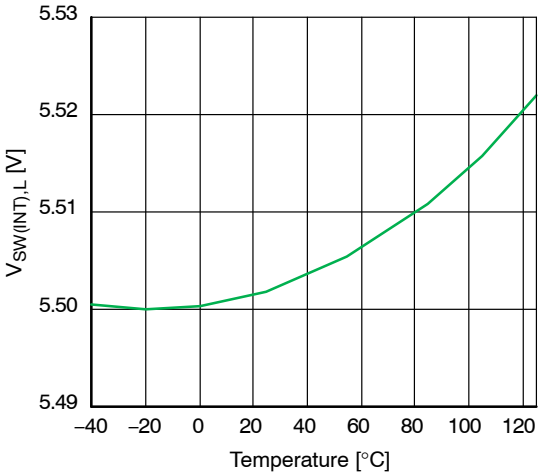


Figure 25. $V_{SW(INT),L}$ vs. Temperature

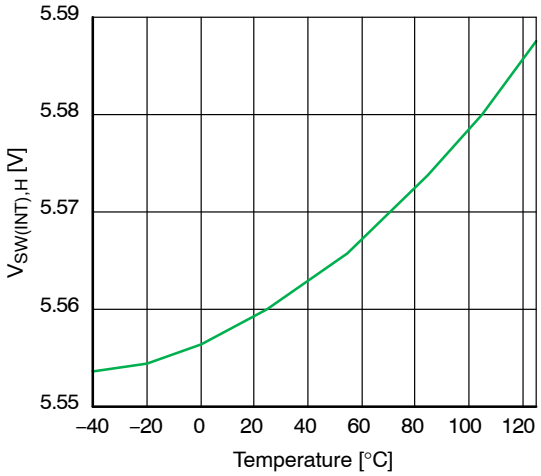


Figure 26. $V_{SW(INT),H}$ vs. Temperature

TYPICAL CHARACTERISTICS – LOW DROPOUT REGULATOR

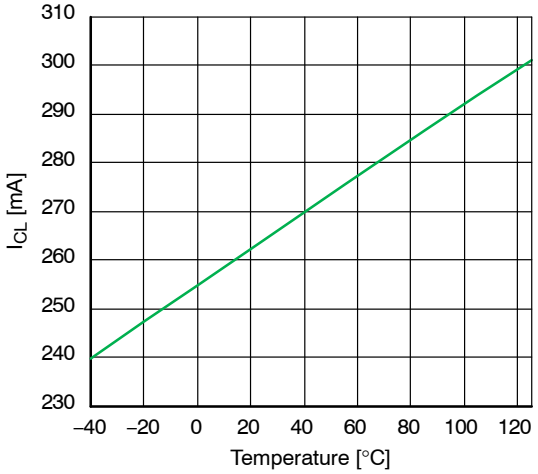


Figure 27. I_{CL} vs. Temperature

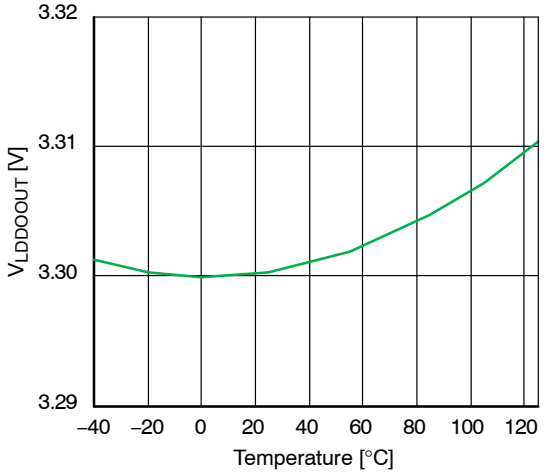


Figure 28. V_{LDOOUT} vs. Temperature (A Version)

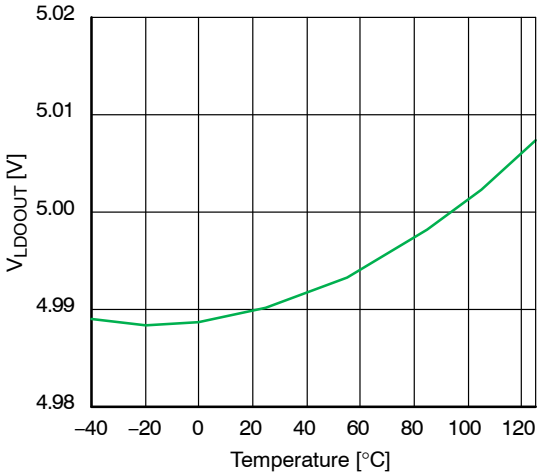


Figure 29. V_{LDOOUT} vs. Temperature (B Version)

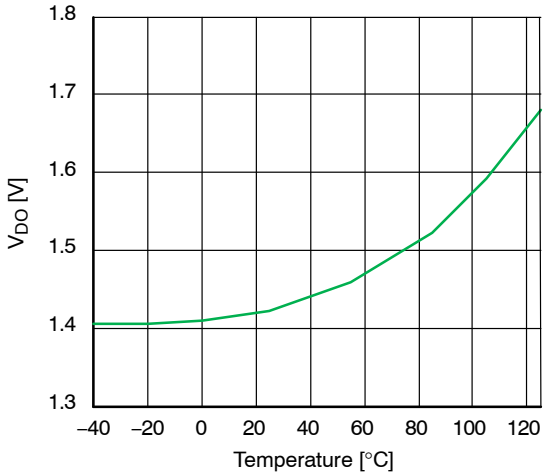


Figure 30. V_{DO} vs. Temperature

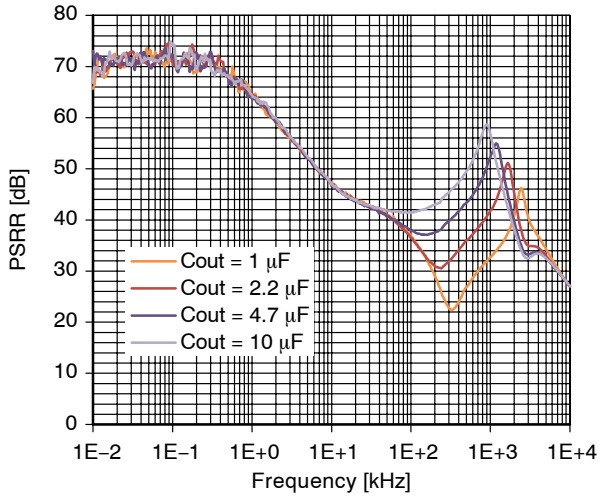


Figure 31. PSRR vs. Frequency

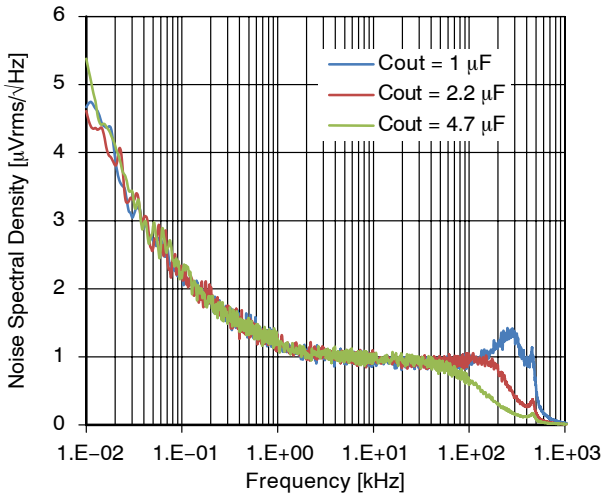


Figure 32. Noise vs. Frequency

TYPICAL CHARACTERISTICS – COMPARATOR

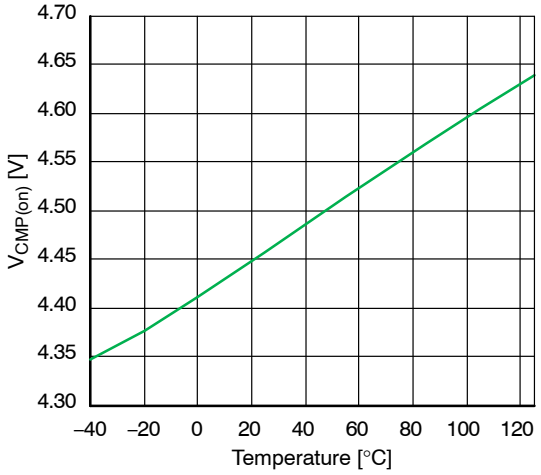


Figure 33. $V_{CMP(on)}$ vs. Temperature

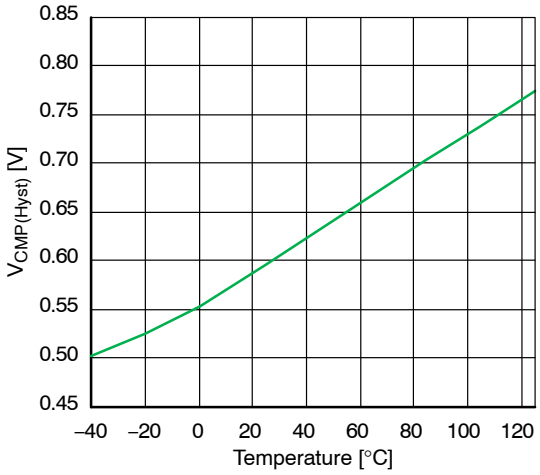


Figure 34. $V_{CMP(Hyst)}$ vs. Temperature

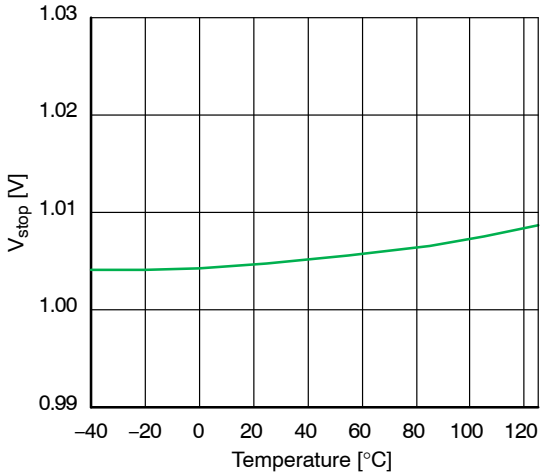


Figure 35. V_{stop} vs. Temperature

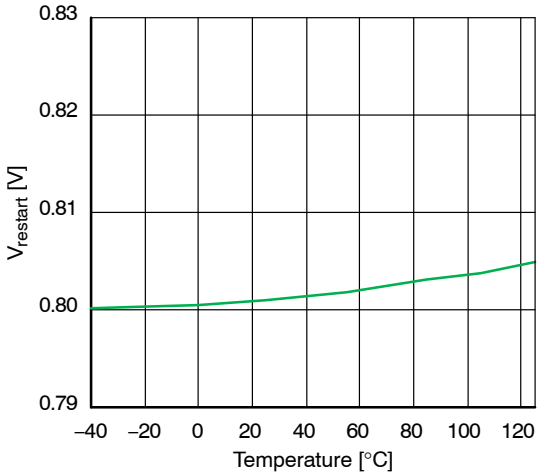


Figure 36. $V_{restart}$ vs. Temperature

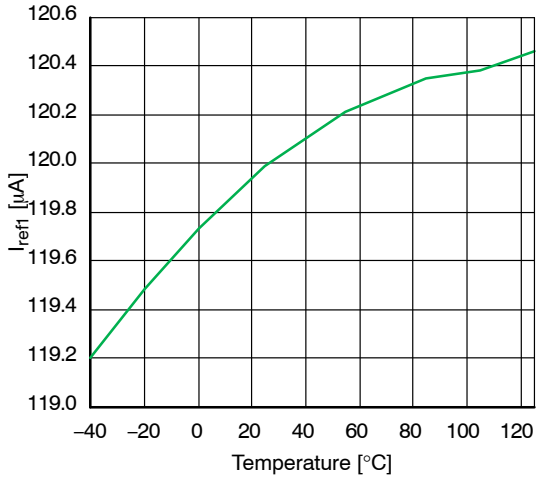


Figure 37. I_{ref1} vs. Temperature

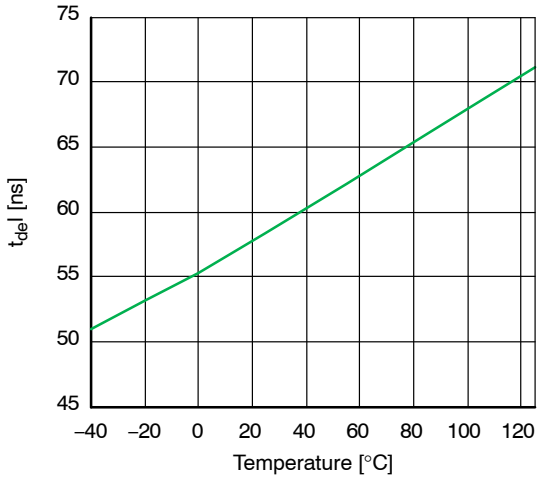


Figure 38. t_{del} vs. Temperature

APPLICATIONS INFORMATION

This NCP10970 integrated circuit associates a high−voltage switcher configured to drive a buck topology with a low−voltage die hosting a linear regulator and dedicated comparator circuitry. The buck circuit delivers output voltage up to 16 V (adjustable by resistor divider on FB pin) from universal mains input and using a proprietary downstream converter technique creates 3.3 V or 5 V in an effective way.

Current−mode operation with detection end of demagnetization: the high−voltage switcher uses fixed−frequency current−mode control architecture. A dedicated pin DMG permanently monitors the magnetic activity in the inductor and prevents from entering the continuous conduction mode (CCM). The DMG pin has to be connected through proper resistor value to the end of the inductor.

670 V MOSFET: the switcher contains a high−voltage low−power MOSFET with a 18 Ω $R_{DS(on)}$ @ T_J = 25°C. The dissipated heat of the power transistor is conducted out through the SOURCE pin.

Dynamic Self−Supply contains an internal high−voltage start−up current source. This device can be used in applications in which no auxiliary winding provides a supply voltage or in application with low output voltage, for example 5 V. For power dissipation concerns but also for best stand−by power performance, we recommend to disable DSS operation by providing a self−supply to the switcher.

Short circuit protection is permanently monitoring the COMP pin activity. The controller is able to detect the short−circuit condition and immediately reduce the output power for a total system protection. A fault timer is started as soon as the COMP current is below a threshold, $I_{COMPfault}$, which indicates the maximum peak current. If the fault is still present at the end of this timer, then the device enters a safe, auto−recovery burst mode, affected by a fixed timer recurrence, $t_{recovery}$. Once the short has disappeared, the controller resumes operations.

Built−in V_{CC} Over Voltage Protection is monitoring the voltage on the VCC pin. When the voltage exceeds a level of V_{OVP} (18 V typically), the controller immediately stops switching and waits for a time period given by a $t_{recovery}$ before attempting to restart. If the fault is gone, the controller resumes operation. If the fault is still there, the controller is again in protection mode and waits another time period $t_{recovery}$ before attempting to restart.

Soft−Start: a 4 ms soft−start ramp ensures a smooth startup sequence and reduces output overshoots.

Current control ensures a good efficiency for changing output power demands. The controller observes the COMP pin and control the current peak value. The switching frequency is setup to its maximum and keep based on the load condition by DMG control.

Skip operation ensures a good efficiency when the output power demand diminishes. By skipping un−needed switching cycles, the NCP10970 drastically reduces the power wasted during light load conditions.

Integrated linear regulator provides a 3.3 V or 5 V (based on chosen version) of output voltage on short−circuit protected output. Supplied by a raw dc voltage derived from the high−voltage buck in a proprietary way, it maintains a good efficiency while offering low quiescent current.

Comparator circuitry can be used for over−temperature detection. The input pin of comparator – CMPIN pin – is permanently biased by a precise constant current source. By connecting a pull−down PTC thermistor to this pin, the circuit can deliver a low signal in case a temperature runaway is sensed. The low signal is present on output pin of comparator – CMPOUT pin – that is an open drain type.

Standby circuit affects the speed of the Comparator t_{del} and also the current consumption of the Low Voltage part – I_{CCLV1} vs I_{CCLV4}. If the STBY pin is suddenly grounded (or after startup of the IC), the IC goes to the standby mode after 20 ms. When the IC is in standby mode and STBY pin goes to High State (>3 V on pin, pin max rating is 5.5 V), the IC goes to active mode after 4 μs max – it is called as wake−up time from standby mode to active mode.

Start−up Sequence of Switcher

During start−up sequence of NCP10970, the supply voltage for switcher (VCC pin) is created by an internal high−voltage start−up current source. This startup−up current source can be used as a DSS (Dynamic self−supply) in case that supply voltage is not present or doesn't reach the necessary voltage value.

The internal HV start−up current source is active when the voltage on DRAIN pin is above $V_{HV(min)}$ level. This start−up current source can charges up the C_{VCC} capacitor connected to VCC pin by typical current value I_{start1}. In case of damaged or missing C_{VCC} capacitor, the device is protected against self−destruction by limiting the start−up current to I_{start2} value till the voltage on VCC pin is higher than $V_{CC(th)}$ value. If the VCC voltage touches the $V_{CC(on)}$ level, the current source is turned off and the internal DRV pulses of switcher transistor are authorized. If the VCC voltage decreases below the $V_{CC(min)}$ level, the current source is turned on again till the VCC voltage increase to $V_{CC(on)}$ level, than the current source is turned off again. Figure 39 shows the internal start−up logic for control the high−voltage start−up current source.

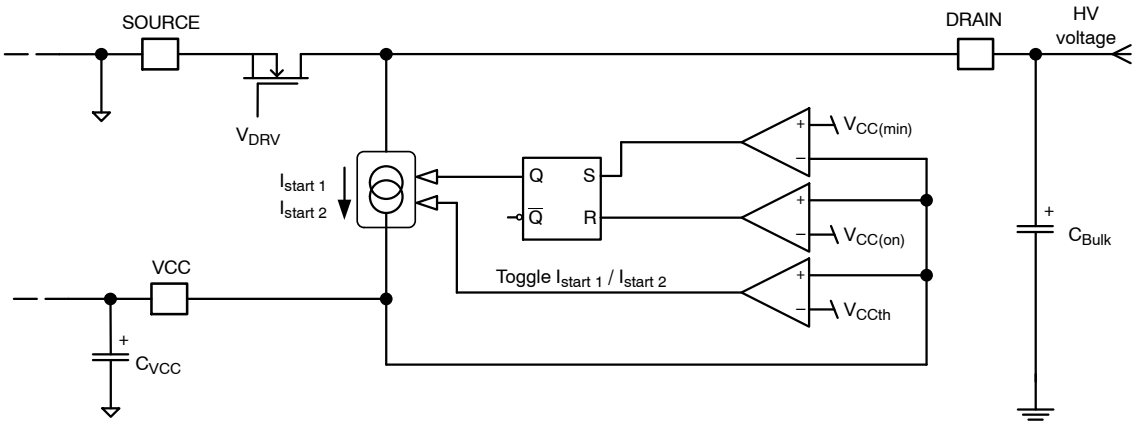


Figure 39. Internal Control Logic of HV Start−up Current Source

Soft−start

The NCP10970 features 4 ms soft−start ramp which reduces the power−on stress but also contributes to lower overshoot of output voltage. Figure 40 shows a typical operating waveform. Soft−start ramp is applied during first start of application and upon every restart, i.e. auto−recovery restart of application after fault state.

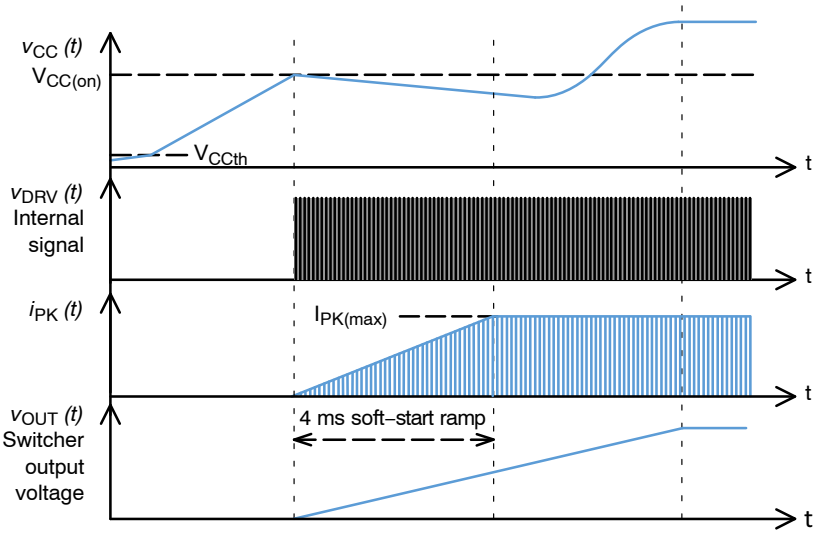


Figure 40. The 4 ms Soft−start Ramp during Start−up Sequence

Demagnetization Detection

To avoid the CCM operation during heavy load conditions, the switcher in NCP10970 is equipped by demagnetization detection block.

Demagnetization detection block affects the switching frequency of the switcher as it shown in Figure 41. Switching frequency is determined by a frequency oscillator when on−time plus off−time are shorter than switching period time. Otherwise, the switcher is forced to wait for the end of the inductor demagnetization although the end of the switching period came as first. Therefore, the demagnetization detection block doesn't authorize new switching cycle till the inductor demagnetization phase is not finished.

The end of demagnetization is sensed by threshold voltage level $V_{DMG(th)}$ which is valid for decreasing voltage. The new DRV pulse is present after propagation delay t_{dem} of the demagnetization detection block. The unwanted demagnetization detection is secured by a hysteresis on demagnetization threshold level and blanking time.

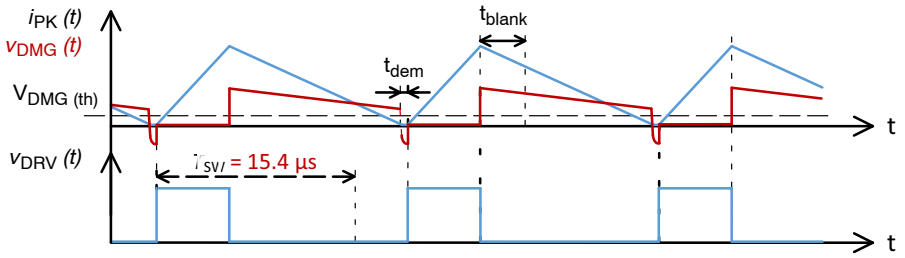


Figure 41. Switching Waveforms with Demagnetization Detection during Light and Heavy Load Operation

Recommended connection of DMG pin shows Figure 42. External resistor R_1 and internal resistor R_{int} create resistor divider. The divider ratio should be chosen with respect to $V_{DMG(th)}$ value, which is important for proper end of demagnetization detection. Resistance of external resistor R_1 has to be chosen based on maximum current value $I_{DMG,clamp}$ flowing through the clamp diode.

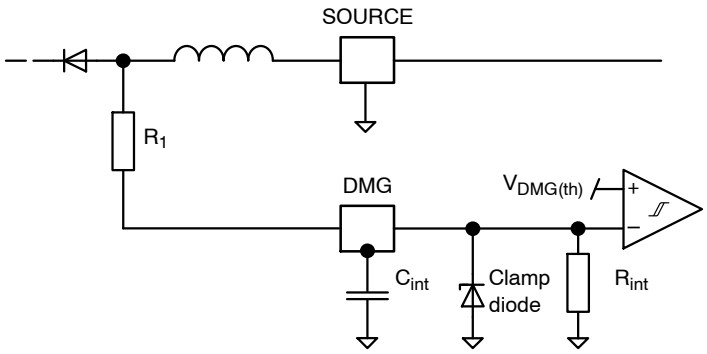


Figure 42. Recommended Connection of DMG Pin

Current and Switching Frequency Control

The improvement of the efficiency during light load and reduction of no−load standby power requires change of the switching frequency and current peak setpoint depending on the state of the load. Therefore, this device implements a current and switching frequency control when the COMP current passes a certain levels.

The current peak control mechanism is clearly described in Figure 43. The switching frequency control is based on interrupting of the switching in Skip mode. Out of the Skip mode, the full switching frequency is setup, but with limiting by the demagnetization detection block. It means, the switching frequency is determined by the application, not by a device itself.

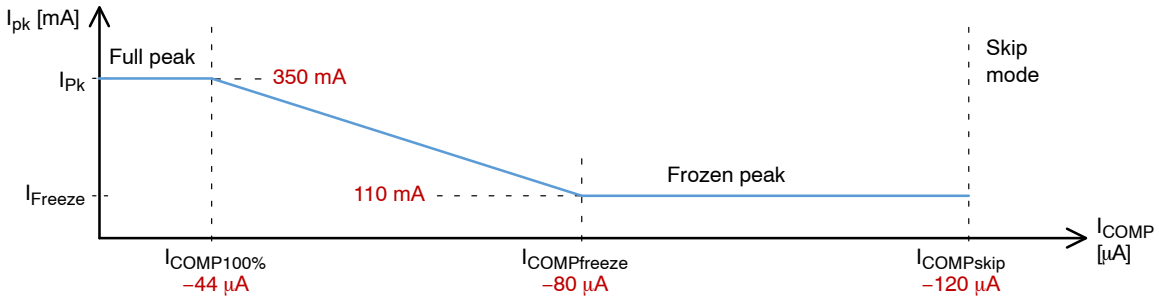


Figure 43. By Observing the Current on the COMP Pin, the Controller Changes its Current Peak Setpoint and Switching Frequency to Improved Performance at Light Load Conditions

COMP Pin

Figure 44 depicts the relationship between COMP pin voltage and current. The COMP pin operates linearly as the absolute value of COMP current (I_{COMP}) is above 40 µA. In this linear operating range, the dynamic resistance is 17.7 kΩ typically ($R_{COMP(up)}$) and the effective pull−up voltage is 2.7 V typically ($V_{COMP(REF)}$). When I_{COMP} is decreases, the COMP voltage is increased to 3.2 V.

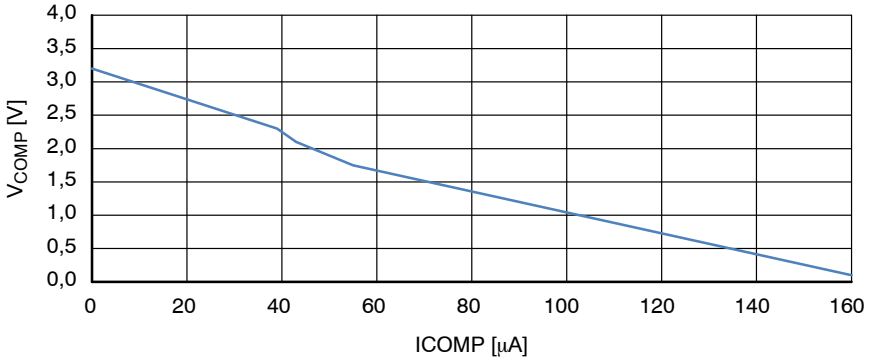


Figure 44. COMP Pin Voltage vs. COMP Current

FB Pin Function

The portion of the output voltage is connected into the pin. The pin voltage is compared with internal V_{REF} (3.3 V) using Operation Transconductance Amplifier (Figure 45). The OTAs output is connected to COMP pin. The compensation resistor network is connected to the COMP pin. The current capability of OTA is limited to −150 μA typically. The positive current is defined by internal $R_{COMP(up)}$ resistor and $V_{COMP(ref)}$ voltage. If FB path loop is broken (i.e. the FB pin is disconnected), an internal current I_{FB} (1 μA typ.) will pull up the FB pin and the IC stops switching to avoid uncontrolled output voltage increasing.

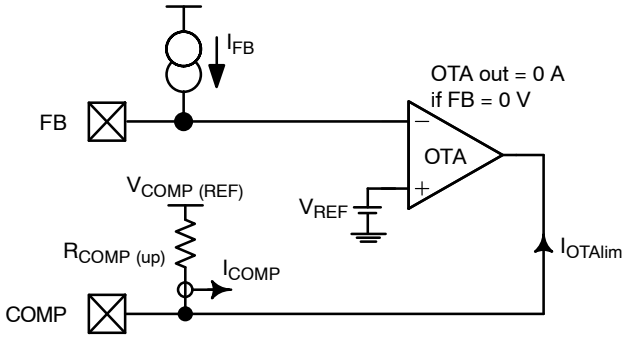


Figure 45. FB Pin Connection Schematic

Auto−recovery Over−Voltage Protection

The particular switcher of NCP10970 arrangement offers a simple way to prevent output voltage runaway when the compensation network fails. Therefore, a comparator monitors the VCC pin. If there is an over−voltage condition on the C_{VCC} capacitor, the controller considers it as an OVP situation. To avoid some unwanted OVP situation, there is implemented filter with time constant t_{OVP}. If fault is present for whole t_{OVP} time, the fault is confirmed and the internal pulses are immediately stopped. The controller enters to auto−recovery protection mode, and normal operation will be resumed after $t_{recovery}$ time constant. If the fault condition still exists, the device enters to the protection mode again.

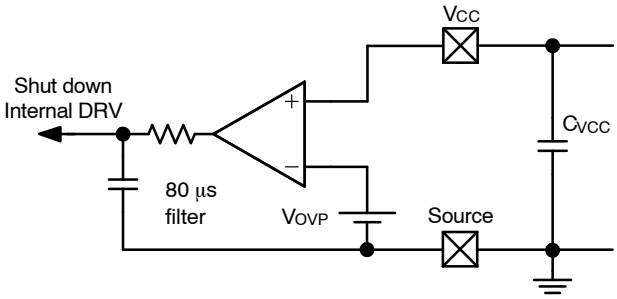


Figure 46. Realization of OVP Protection on VCC Pin

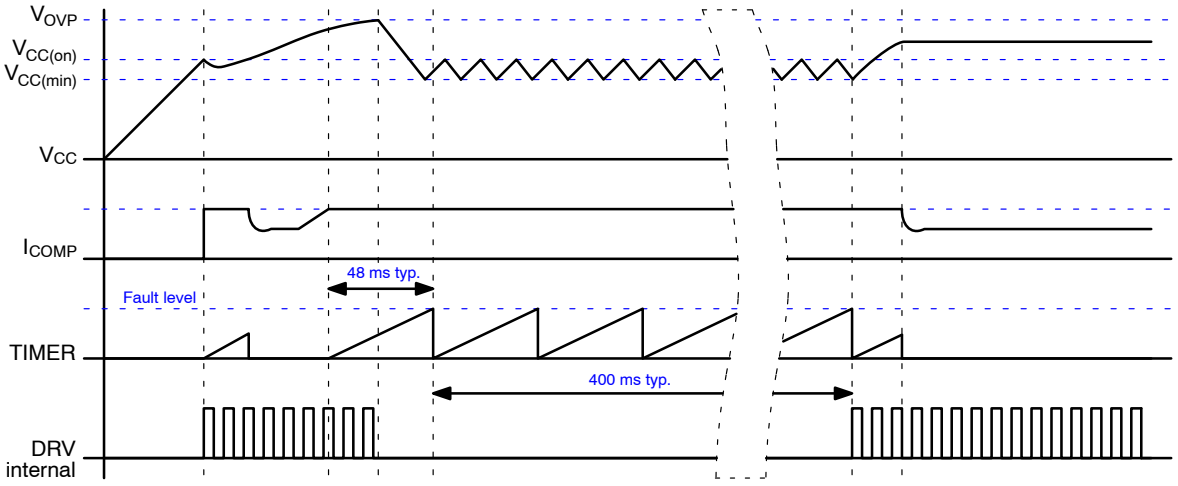


Figure 47. The Switcher Auto−recovers to Normal Operation after Over−voltage on VCC Pin

Auto−recovery Short−Circuit Protection

As soon as V_{CC} reaches $V_{CC(on)}$, drive pulses are internally enabled. If everything is correct, the output voltage rises and starts to supply the VCC capacitor. When the output voltage is not regulated, the current coming through COMP pin is below $I_{COMPfault}$ level (40 μA typically), which is not only during the startup period but also anytime an overload situation occurs, an internal error flag is asserted, Ipflag is indicating that the system has reached its maximum current limit setpoint. The assertion of this Ipflag triggers a fault counter t_{SCP} (48 ms typically). If Ipflag remains asserted when the t_{SCP} counter elapses, all driving pulses are stopped and in $t_{recovery}$ duration (about 400 ms). A new attempt to re−start occurs and will last 48 ms providing the fault is still present. When the fault disappears, the power supply quickly resumes operation. Figure 48 depicts this particular mode.

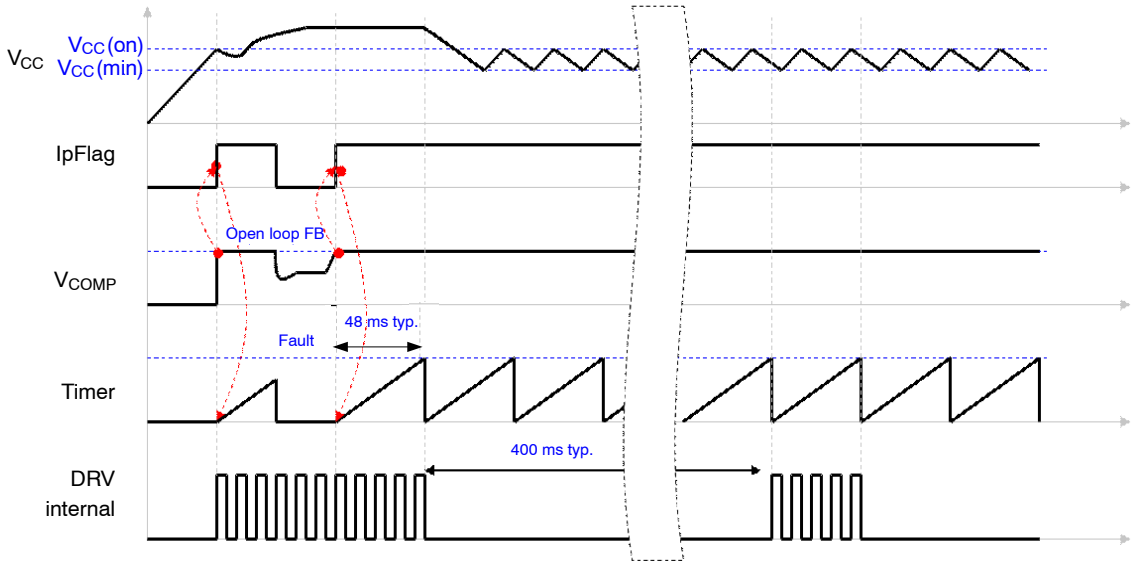


Figure 48. In Case of Short − circuit or Overload, the Switcher of NCP10970 Protects Itself and the Power Supply via a Low Frequency Burst Mode. The VCC is Maintained by the DSS Function of the Start−up Current Source

Start−up Sequence of Low Voltage Section

The switcher starts switching when the supply voltage V_{CC} reaches $V_{CC(on)}$ level and therefore the output voltage of the switcher is ramping−up. The supply pin VCCLV of the low voltage section is connected to the switcher output voltage. When the V_{CCLV} voltage reaches the $V_{CCLV(on)}$ level, the switch SW_{INT} is active to ramp−up the V_{RAW} voltage to its nominal value given by a $V_{SW(INT),H}$. During this start−up sequence is active the switch SW_{INT} only, i.e. the switch SW_{VCCLV} is blocked until the V_{RAW} voltage reaches the $V_{SW(INT),H}$ voltage level. The LDO output voltage is ramping−up after the V_{RAW} reaches its nominal value to achieve smooth and linear rise ramp of this voltage. Figure 49 shows the operation during start−up sequence.

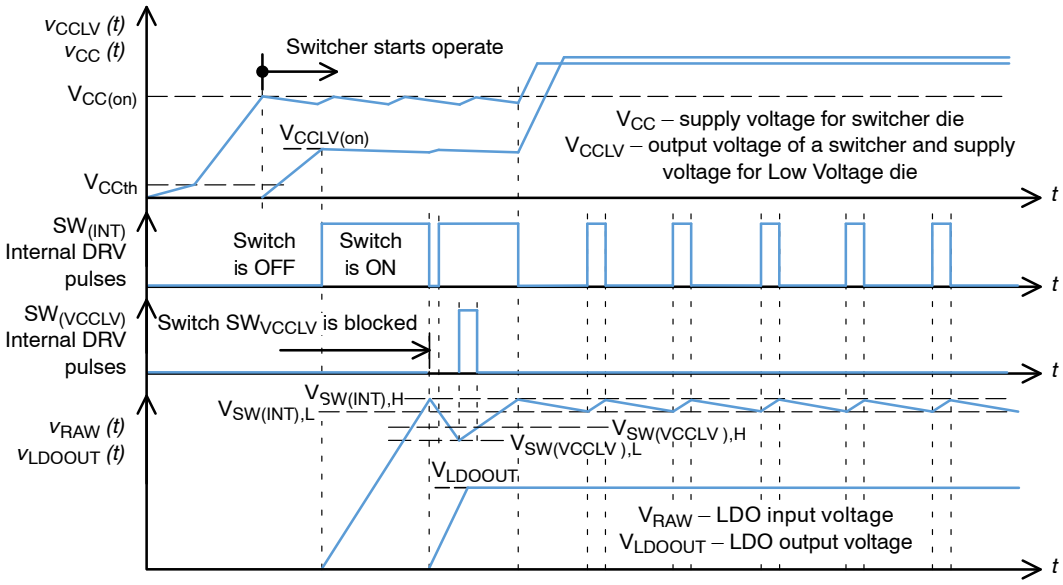


Figure 49. Startup Waveforms of the Switcher and Low Voltage Section with LDO

Steady−state and Transient Operation of Switcher and LDO

During steady−state operation, the switch SW_{INT} is switching to supply the LDO. If this energy delivering is not enough, there is a switch SW_{VCCLV}, which can supply the LDO from the output capacitor connected to switcher output rail. The switch SW_{VCCLV} is turned−on especially during transient states. Figure 50 shows the behavior of the switches during steady state and transient state, when the LDO output rail is heavy loaded. Both switches are turned−on when the V_{RAW} voltage touches the turn−on voltage reference, i.e. $V_{SW(INT),L}$ and $V_{SW(VCCLV),L}$, and turned−off when the V_{RAW} voltage touches turn−off voltage reference $V_{SW(VCCLV),H}$ and $V_{SW(INT),H}$.

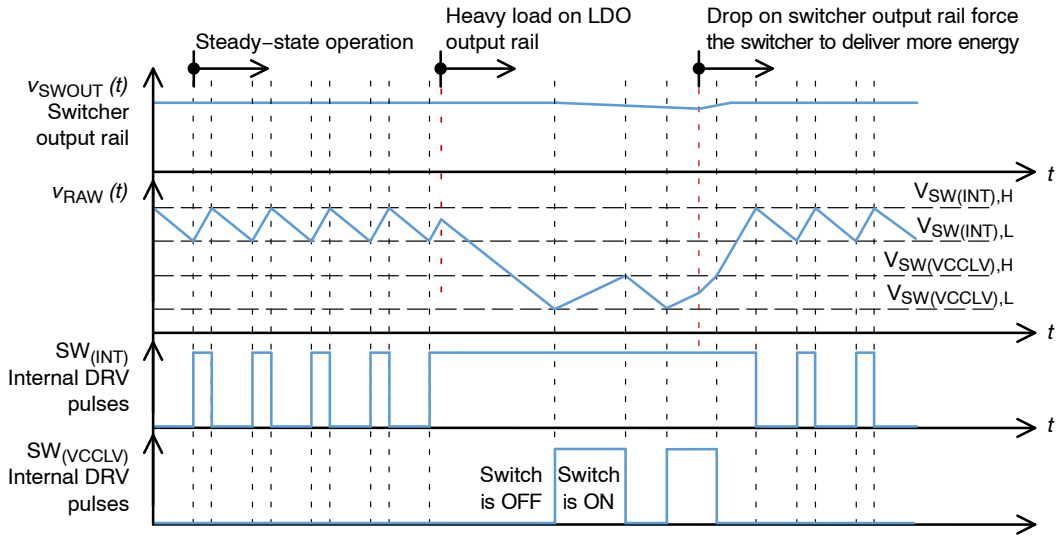


Figure 50. Steady State Waveforms of the Switcher and Low Voltage Section with LDO

Power−down Operation of Switcher and LDO

This operation mode is showing the behavior of the controller when the input HV voltage is unplugged. When the input voltage is no longer present, the energy for LDO cannot be ensured through INT switch, so the energy is transferred from capacitor on switcher output voltage rail through VCCLV switch. Figure 51 shows the behavior of the switches during power−down.

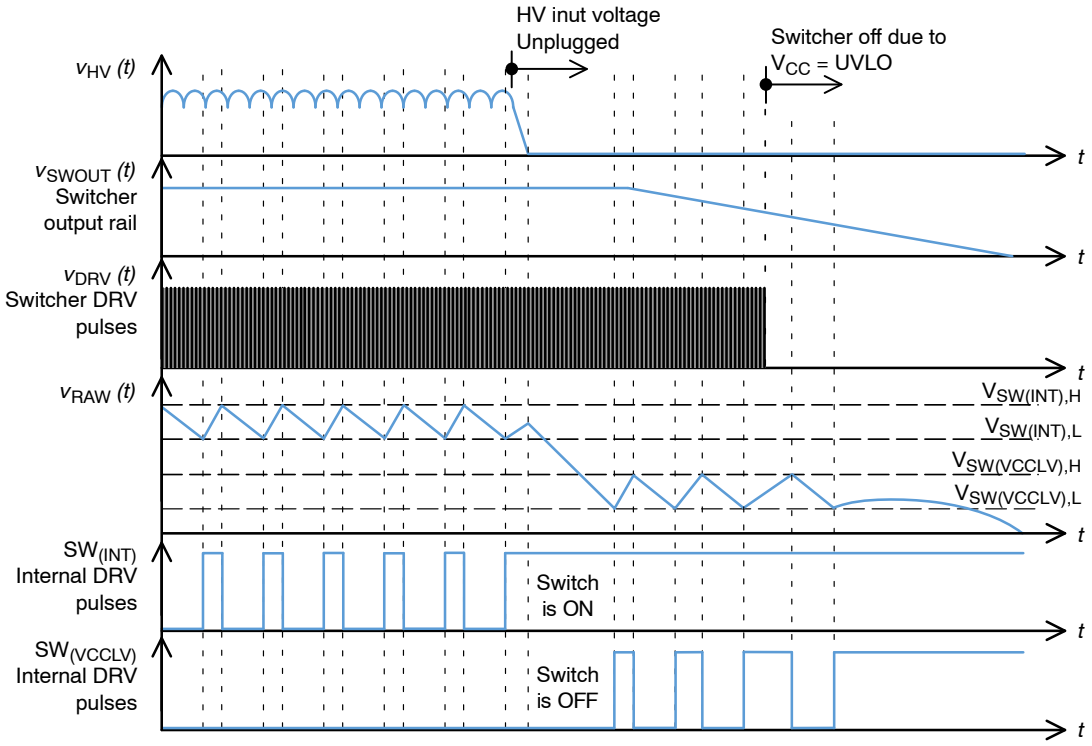


Figure 51. Power−down Behavior of the Switcher and Low Voltage Section with LDO

Linear Regulator

The integrated LDO regulator is an NMOS type for better output stability. The output voltage is fixed 3.3 V or 5 V based on chosen version (see ordering information table on page 22) and output current is limited to 260 mA @ T_J = 25°C as a short−circuit protection of LDO output.

The input voltage of LDO regulator is V_{RAW} voltage and the LDO is supplied from V_{CCLV} voltage.

Comparator

The input of this circuitry is CMPIN pin, which is biased by a current source during all operational conditions. Comparator connected to the CMPIN pin turns−on and off the internal MOSFET transistor connected to COMPOUT pin – this pin is open−drain. The Speed of the Comparator is determined by the active or standby of the IC, i.e. the Comparator is in standby mode when the STBY pin is grounded. Standby mode affects the propagation delay t_{del} of the comparator.

Over−temperature detection is based on pull−down PTC thermistor connected to CMPIN pin. Internal current source force the current value I_{ref1} = 120 μA through the PTC. If the over−temperature condition appears, the resistance of the PTC thermistor increases, i.e. the sensed voltage reaches the value V_{stop} = 1 V and the comparator turned−on the internal MOSFET, which force the CMPOUT pin to the Low state. The de−bouncing time constants t_{del1} = 50 μs and t_{del2} = 10 μs on comparator output can be implemented as an option. The CMPOUT pin goes back to High Z state, when the sensed voltage on PTC decreases below the value $V_{restart}$ = 0.8 V. Figure 52 shows the comparator operation with/without de−bouncing filter based on input voltage on CMPIN pin.

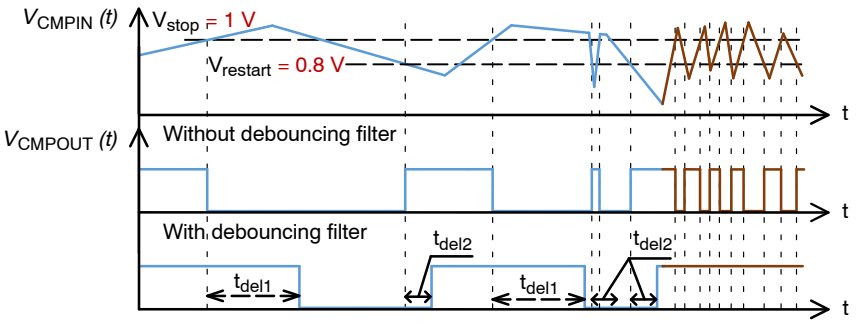


Figure 52. Over−temperature/Over−current Detection with/without De−bouncing Filter

The CMPOUT pin is forced low during startup independently of voltage on CMPIN pin when the supply voltage is between 2.5 V and $V_{CMP(on)}$ = 4.4 V. When the supply voltage V_{CCLV} touches the $V_{CMP(on)}$ = 4.4 V level, the CMPOUT pin is forced low or keep in High Z state based on input voltage on CMPIN pin. If the CMPIN voltage is above 0.8 V when the V_{CCLV} touches the $V_{CMP(on)}$ level, the CMPOUT pin is forced to low.

The internal current source I_{ref1} has its nominal value when supply voltage V_{CCLV} is above 3.7 V. Figure 53 shows the behavior of the comparator based on supply voltage V_{CCLV}.

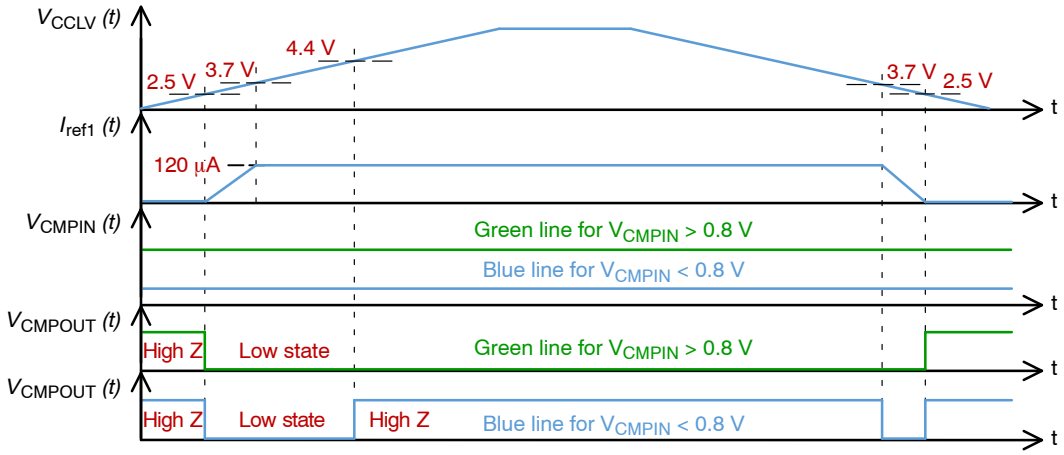


Figure 53. Operational Condition of the Comparator Based on Supply Voltage

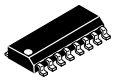
Thermal Shutdown

Internal TSD protects the silicon against self−destruction due to high temperature. If the temperature on silicon reaches 160°C typically, LDO output and input of over−temperature detection are disabled. The CMPOUT pin is set to Low state as an indication of the over−temperature condition. All components are enabled again when the silicon temperature fall by 20°C.

ORDERING INFORMATION

Device	Maximum Peak Current	VCCLV (on)	VCCLV Switch INT Switch References	LDO Output Voltage	Package	Shipping†
NCP10970A1DR2G	350 mA	8.4 V	3.60 V / 3.65 V 3.80 V / 3.85 V	3.3 V	SOIC−16NB (Pb−Free)	2500 / Tape & Reel
NCP10970B1DR2G	350 mA	8.4 V	5.30 V / 5.35 V 5.50 V / 5.55 V	5 V	SOIC−16NB (Pb−Free)	2500 / Tape & Reel

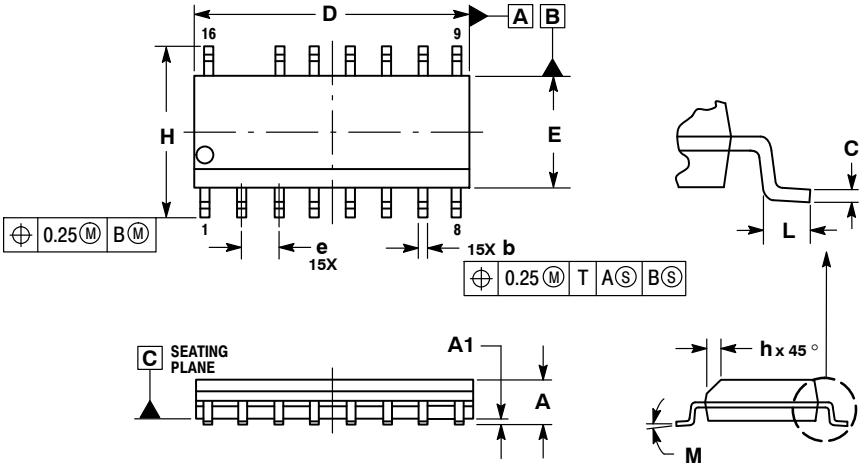
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

SOIC−16 NB, LESS PIN 15
CASE 752AC−01
ISSUE O

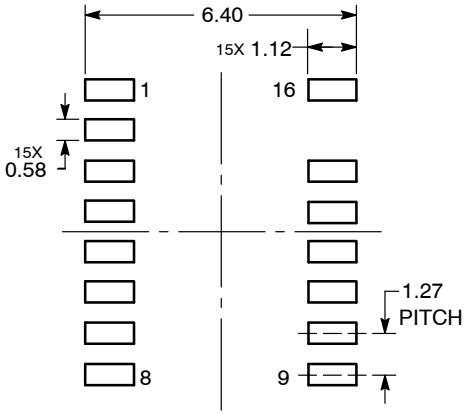
DATE 28 JAN 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

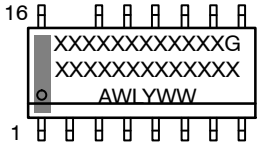
	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.35	0.49
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
M	0 °	7 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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