MICROCHIP

PIC32MZ W1

PIC32MZ W1 Software User's Guide

Introduction

This document describes the software features supported by the PIC32MZ W1 Family using the MPLAB® Harmony v3 framework. This framework is integrated with a development environment that works directly with the WFI32E01 module. The software release package enables a rich set of PIC32MZ1025W104 SoC features such as 802.11 b/g/n, Ethernet, USB, CAN, CAN-FD, SPI, I2C, SQI, UART and JTAG, which are supported by the PIC32MZ W1 Family.

Features

Harmony v3 Peripheral Support

- Three UART modules (one high-speed UART with dedicated pads and two user-configurable UART using Peripheral Pin Select)
- I^2C Master and Slave with Address Masking
- Two SPI Ports
  - One dedicated high-speed SPI
  - One user configurable SPI using PPS
- One USB OTG 2.0 (full-speed, device mode CDC console only)
- 35 Remappable GPIOs using PPS
- One Fast Ethernet (10/100) Reduced Media Independent Interface (RMII)
- Seven Timers
  - 16-bit timers/counters can be concatenated to form a single 32-bit timer
- Eight Channel Hardware DMA (Direct Memory Access) Controller with Automatic Data Size Detection supporting 32-bit CRC-checked Transfers of up to 64 KB in size
- Node Version Manager (NVM) Read/Write Support
- Watchdog Timer (WDT) for Fail Safe Operations
- 20 External Analog Inputs for Sampling/Conversion
- Four Output Compare Ports

Harmony v3 System Services Support

- Clock Support up to 200 MHz
- Four On-chip Integer PLLs:
  - USB (UPLL)
  - Ethernet/Wi-Fi® (EWPLL)
  - System (SPLL)
  - Bluetooth (BTPLL) (unused)
- Power-up Timer (PWRT) and Oscillator Start-up Timers (OST)
- Interrupts Enabled through Peripheral Libraries
- System Console for User Debug Log Messages
- Reset Source Selections:
  - Power-on Reset (POR)
  - Master Clear Reset ($\overline{MCLR}$)

  - Software Reset (SWR)
  - Brown-out Reset (BOR)
- Four System Ports (A, B, C and K)
- Device Configuration (DEVCON) for all Peripheral-related Bits including Clocks, Programming and Debugging

Harmony v3 Networking Support

- MPLAB Harmony v3 TCP/IP Stack
- WLAN STA and AP Networking Modes
  - TLS v1.2 with symmetric crypto acceleration
  - DHCP client/server, DNS client/server, ICMPv4, iPerf
- Wireless Network Security Standard (WEP, WPA/WPA2-Personal and WPA3 – FreeRTOS only)
- Protected Management Frames (802.11w)
- Wi-Fi Transmit Power Control
- Configurable Region Selection for Regulatory Compliance

Table of Contents

1. Quick References

1.1 Reference Documentation

For further details, refer to the following:

- *PIC32MZ1025W104 MCU and WFI32E01 Module with Wi-Fi® and Hardware-based Security Accelerator Data Sheet* (DS70005425)
- *PIC32 WFI32E Curiosity Board User's Guide* (DS50003028)

Note: For Reference Manuals, refer to the **Documents** page of the www.microchip.com/PIC32MZW1.

1.2 Hardware Prerequisites

- PIC32 WFI32E Curiosity Board Evaluation Kit
- MPLAB ICD3 Programmer/Debugger (optional)

1.3 Software Prerequisites

- MPLAB Integrated Development Environment (MPLAB X IDE) tool (version 5.35)
- MPLAB XC32 compiler (version 2.40)
- Terminal emulator utility program (Tera Term)

2. Functional Overview

This section describes the features supported by the PIC32MZ W1 software release package. This package enables Wi-Fi functionality on the device, supporting either STA or AP mode and WPA/WPA2/WPA3 security (optional). It also provides peripheral drivers, networking stack, network security and sample applications that are supported by the Harmony v3 framework. With extensive use of pin multiplexing, the PIC32MZ W1 Family can accommodate a large number of peripheral functions. The package has the following components:

- WLAN applications – For the list of WLAN applications supported by the PIC32MZ W1 Family, refer to the WLAN Examples.
- Peripheral libraries – For the list of peripheral libraries supported by the PIC32MZ W1 Family, refer to the Peripheral Examples.
- Core examples – For the list of core examples supported by the PIC32MZ W1 Family, refer to the Core Examples.
- Third party libraries – For the list of third party libraries supported by the PIC32MZ W1 Family, refer to the following:
  - wolfMQTT library
  - wolfSSL library
  - FreeRTOS library
- MPLAB Harmony Configurator (MHC) – For more information on how to install the MHC and how to get started using MPLAB Harmony, refer to MPLAB Harmony.
- WLAN Functional APIs – The following set of functions provide abstracted control plane functionality to the application:
  - Scanning and network discovery
  - Connection/disconnection to an AP (STA mode)
  - AP enable/disable and configuration (AP mode)
  - Support for implemented security configurations
  - Power control
  - Channel or region configuration

2.1 Hardware Setup

This section describes the hardware setup using the PIC32 WFI32E Curiosity Board Evaluation Kit.

2.1.1 Power Supply

The PIC32 WFI32E Curiosity Board can be powered using any of the following sources:

- External 5V (J201)
- PKOB3 micro-B USB (J302)
- Target VBUS micro-B (J204)

Note: For the jumper connections, refer to the *PIC32 WFI32E Curiosity Board User's Guide* (DS50003028).

The following table lists the power supply source details and its jumper positions.

Table 2-1. Power Supply Sources

Power Input	Description	Jumper Position (J202(1))
External 5V (J201(1))	Connect the Curiosity board to an external 5V power supply	P/S-VIN (2-1)
PKOB3 micro-B USB (J302(1))	Connect the Type-A male to micro-B USB cable to the USB debug port for power supply	PKOB-VIN (4-3)

...........continued

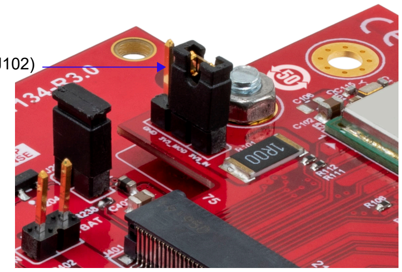
Power Input	Description	Jumper Position (J202[(1)])
Target VBUS micro-B (J204[(1)])	Connect the Type-A male to micro-B USB cable to the USB power port for power supply	VBUS-VIN (6-5)

Note:

1. For the jumper connections, refer to the *PIC32 WFI32E Curiosity Board User's Guide* (DS50003028).

The following figure illustrates the jumper positions for powering the Curiosity board.

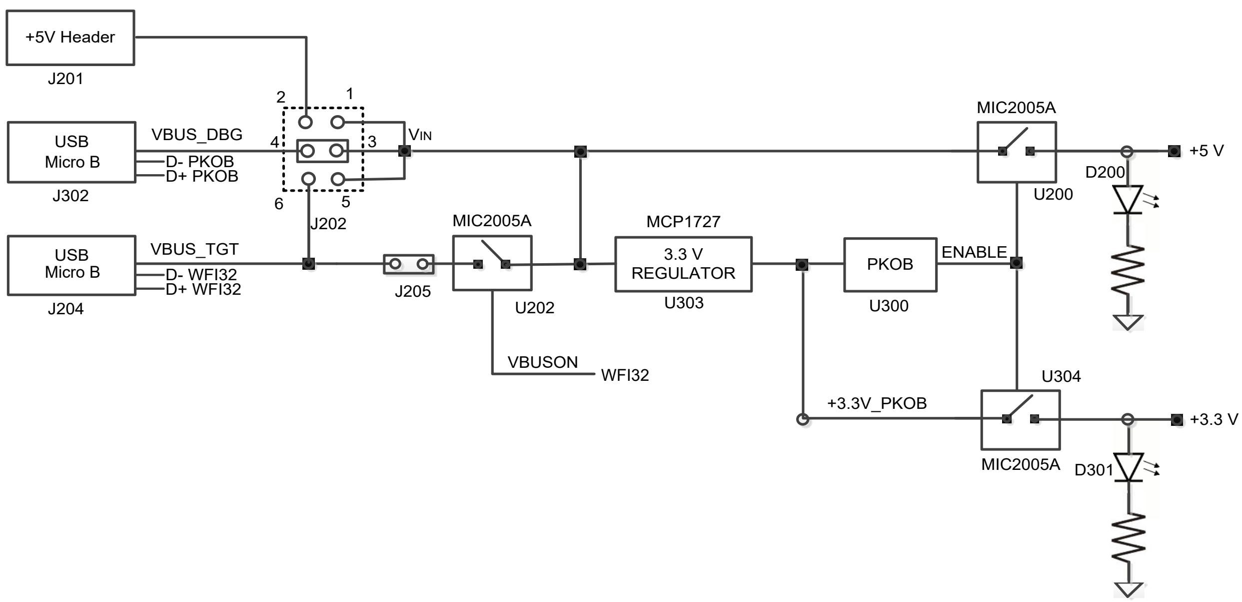
Figure 2-1. Jumper Configuration for Power Input



Note: Ensure that the 3V3_MOD and 3V3_IN of J102 are connected on the WFI32E01PC carrier board.

Use the J202 jumper to select the voltage source for the Curiosity board. The MCP1727 voltage regulator generates a +3.3V power supply for the MCU. Connect the PKOB debugger to a host PC. Turn on the power supply (+3.3V and +5V) to the Curiosity board via a power switch (MIC2005A) to drive the ENABLE signal to high.

Figure 2-2. Power Tree Diagram



2.1.2 Debugger/Programmer Selection

By default, the external debugger is connected to the programming pins (PGEC2 and PGED2) of the WFI32E01PC module. The following table lists the details of the debugger/programmer selection using the J301 header.

Note: For the jumper connections, refer to the *PIC32 WFI32E Curiosity Board User's Guide* (DS50003028).

Important: Use an external debugger such as MPLAB ICD 4, MPLAB PICkit 4 or MPLAB Snap for the best programming and debugging experience.

The PIC32 WFI32E Curiosity Board has an on-board debugger (PKOB3) based on the PIC24FJ256GB106 MCU. The on-board debugger enables the user to power, program and debug through the micro-B USB connector (J302).

Table 2-2. Debugger/Programmer Selection

Header Position (J301(1))	Debugger Used	Description
Pins 1-2 and 3-4 shorted	On-board	Selects the on-board debugger
Pins 1-2 and 3-4 open	External	Selects the external debugger (for more details, refer to 2.1.3 ICSP Header)

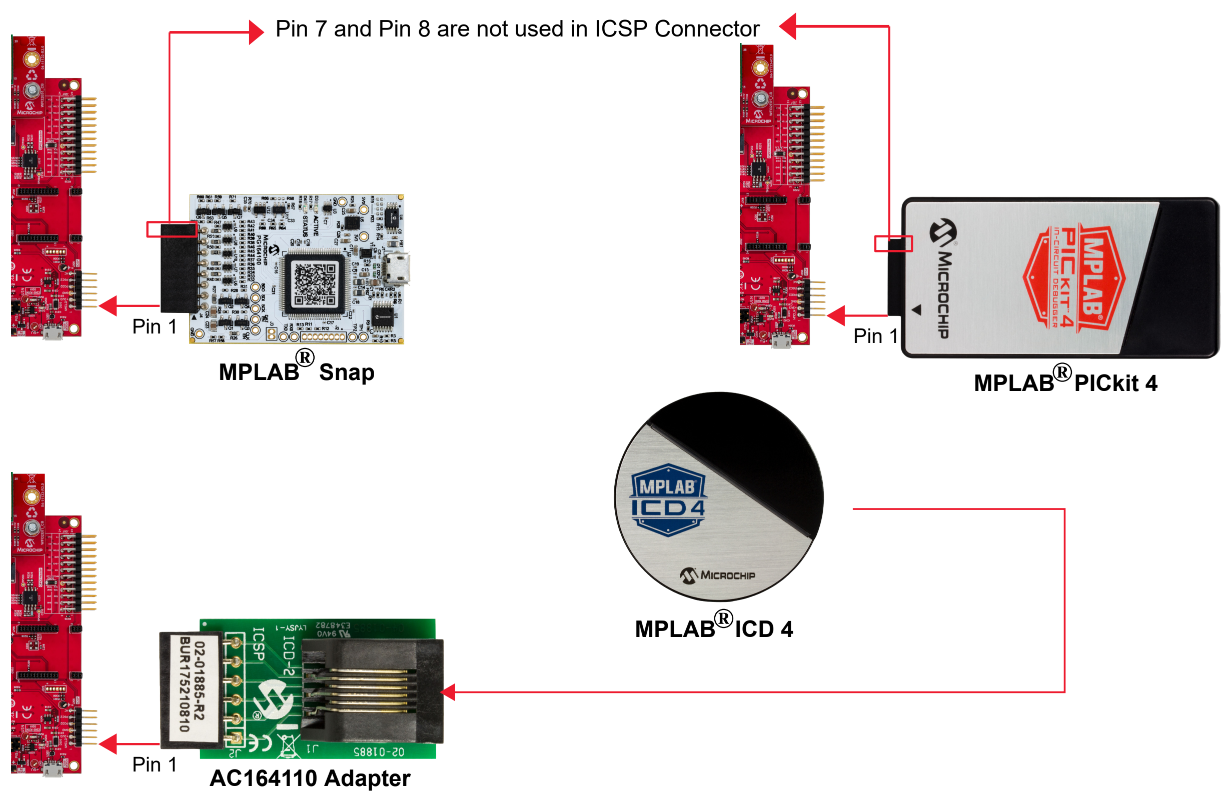
Note:

1. For the jumper connections, refer to the *PIC32 WFI32E Curiosity Board User's Guide* (DS50003028).

2.1.3 ICSP Header

The ICSP header (J206) is a standard 6-pin staggered header. It allows in-circuit emulation and debugging using Microchip's in-circuit emulator tools and it allows direct programming of the WFI32E01PC module. The ICSP header supports external debuggers, such as MPLAB ICD 4, MPLAB PICkit 4 and MPLAB Snap. Use the standard ICSP header to connect an MPLAB programmer or debugger to the PIC32 WFI32E Curiosity Board. The following figure illustrates the connection between the ICSP header, external debuggers and the PIC32 WFI32E Curiosity Board.

Figure 2-3. Connection Diagram



The following table provides the pin details and descriptions of the ICSP header.

Table 2-3. ICSP Header Description

Pin Number	Pin on ICSP Header	Pin Description of ICSP Header	Pin on WFI32E01PC Module(1)
1	$\overline{\text{MCLR}}$	Reset pin	$\overline{\text{MCLR}}$
2	3V3	3.3V power supply	+3V3
3	GND	Ground	GND

...........continued

Pin Number	Pin on ICSP Header	Pin Description of ICSP Header	Pin on WFI32E01PC Module[1]
4	PGD	ICSP™ programming data	PGD2/AN5/CVD5/CVDR5/CVDT2/RTCC/RPB5
5	PGC	ICSP™ programming clock	PGC2/AN4/CVD4/CVDR4/CVDT3/RPB4/RB4
6	NC	Not connected	NC

Notes:
1. For more details on the WFI32E01PC pins, refer to the *PIC32MZ1025W104 MCU and WFI32E01 Module with Wi-Fi® and Hardware-based Security Accelerator Data Sheet* (DS70005425).
2. Use an external debugger such as MPLAB ICD 4 or MPLAB Snap for the best programming and debugging experience.

2.2 Harmony Setup

The recommended configuration bits and clock configuration are automatically set to compile or build the project.

Note: For more information on how to install the MHC and how to get started using MPLAB Harmony, refer to MPLAB Harmony.

2.2.1 Configuration Bits

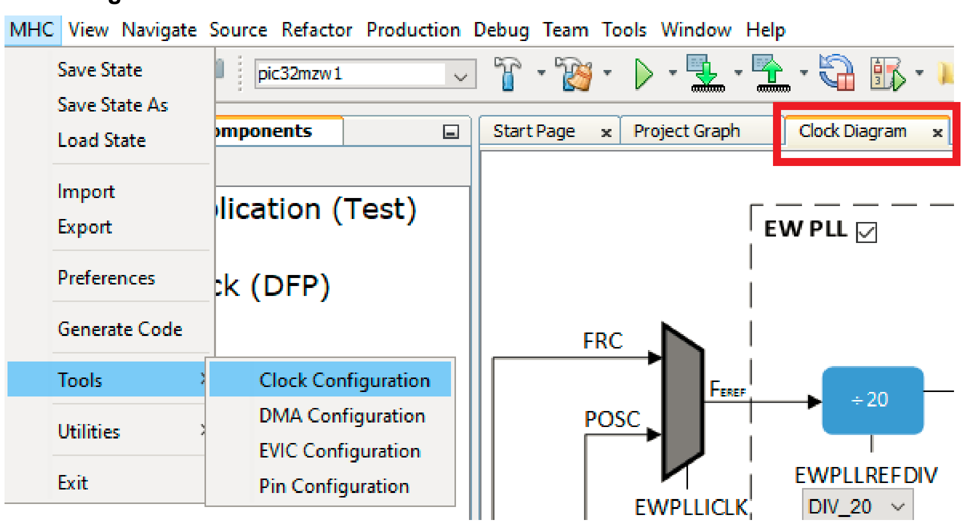
It is recommended to use the default configuration bits; the corresponding values are placed in the `initialization.c` file.
Note: For more details, refer to 3. Appendix A: Configuration Bits.

2.2.2 Clock Source Selection

In MHC, the **Clock Diagram** tab shows all the clocks available in the PIC32MZ1025W104 SoC and their configuration options. The permitted range of inputs is set to generate clock configurations for a pre-determined output range (via drop-down menus). Use the clock diagram for the following purposes:
Note: Use only to override defaults; usually not recommended.

- To configure any clock PLL in the PIC32MZ W1 Family if needed
- To reconfigure peripheral clock dividers if needed for a particular use case

Figure 2-4. Clock Diagram



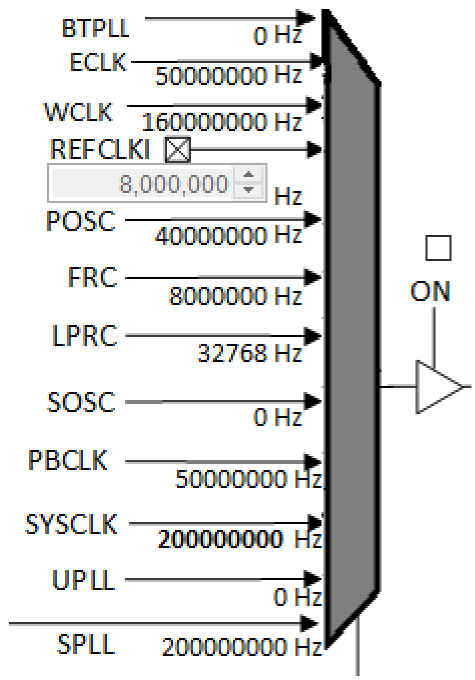
The following table lists the clock sources for all the peripherals supported by the PIC32MZ W1 Family.

Table 2-4. Clock Sources for PIC32MZ W1 Peripherals

PLL	Peripheral CLK	Peripherals
SPLL	PBCLK5	TRNG, BA414E, Symmetric Crypto
	PBCLK3	Ethernet, I2C2, ICAP-1/2/3/4, SQI1, OCMP-1/2/3/4, UART-1/2, SPI-1/2, USB
	PBCLK2	Ports (A, B, C, K), I2C1, CAN1, CAN2 (CAN-FD), ADC-HS
	PBCLK1	BOR, NVM, WDT, DMT, PPS, PTG, UART3, Timer 1-7, CFG

Route each PLL to inputs on the clock MUX and configure as a system clock source as shown in the following figure. Microchip recommends using SPLL to generate the system clock (through ROSEL1). The following figure shows the actual values used in this release.

Figure 2-5. PLL Clock Source Selection



By default, the system is set to operate at a maximum frequency of 200 MHz. All of the software demos are tested at this frequency. The following table lists the different clock frequencies supported by the PIC32MZ W1 Family.

Table 2-5. Clock Frequencies

Clock	Frequency (MHz)
ETHCLK	50
EWPLL	160
UPLL	96

The FRC (8 MHz) is a low frequency clock available at boot-up as the system clock and is mostly used to evaluate a new part during the initial development stage or until it switches to clock sources.

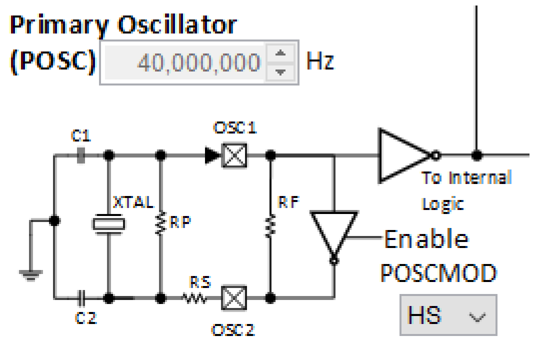
2.2.2.1 Clock Configuration Procedure

Perform the following steps to configure PLLs and peripheral clocks for recommended values:

1. Launch the MHC configuration menu for the main project.

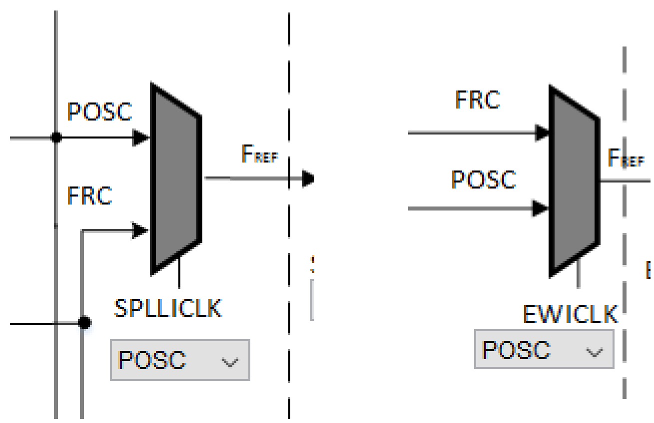
2. Open the Clock Diagram from the menu (*MHC > Tools > Clock Configuration*) as shown in 2.2.2 Clock Source Selection.
    2.1. Enable POSCMOD to HS (if not set).

Figure 2-6. Enable POSCMOD



    2.2. Select the input clock as POSC from the respective clock MUX for SPLLICLK and EWICLK as shown in the following figure.
    2.3. Click the **Auto-Calculate** button for each PLL block to set the proper divisor values to achieve the required output frequency.
    2.4. In all the example codes, the system clock (SYSCLK) is set to 200 MHz.

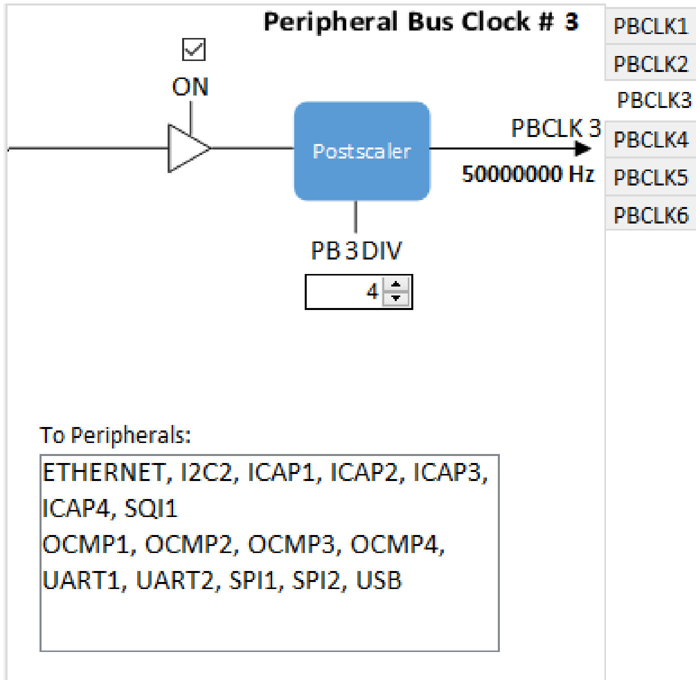
Figure 2-7. Set Input Voltage



Note: The following instructions are for specific use cases, where the configuration may need a modification. Generally, these configurations are done by default by Harmony and do not require a change for most of the cases.

3. Generate the peripheral clock (PBCLK1) as per the following requirements:
    3.1. Ensure from the Clock Diagram that the required frequencies are derived for peripheral clocks through the clock settings. Most of the peripheral clocks are SYSCLCK/2.
    3.2. Some applications may need to use 4 as the PBCLK3 divisor value (PB3DIV) to provide a 50 MHz clock for the required peripherals.

Figure 2-8. PBCLK3 Divisor Value



4. Save the settings and click on the 

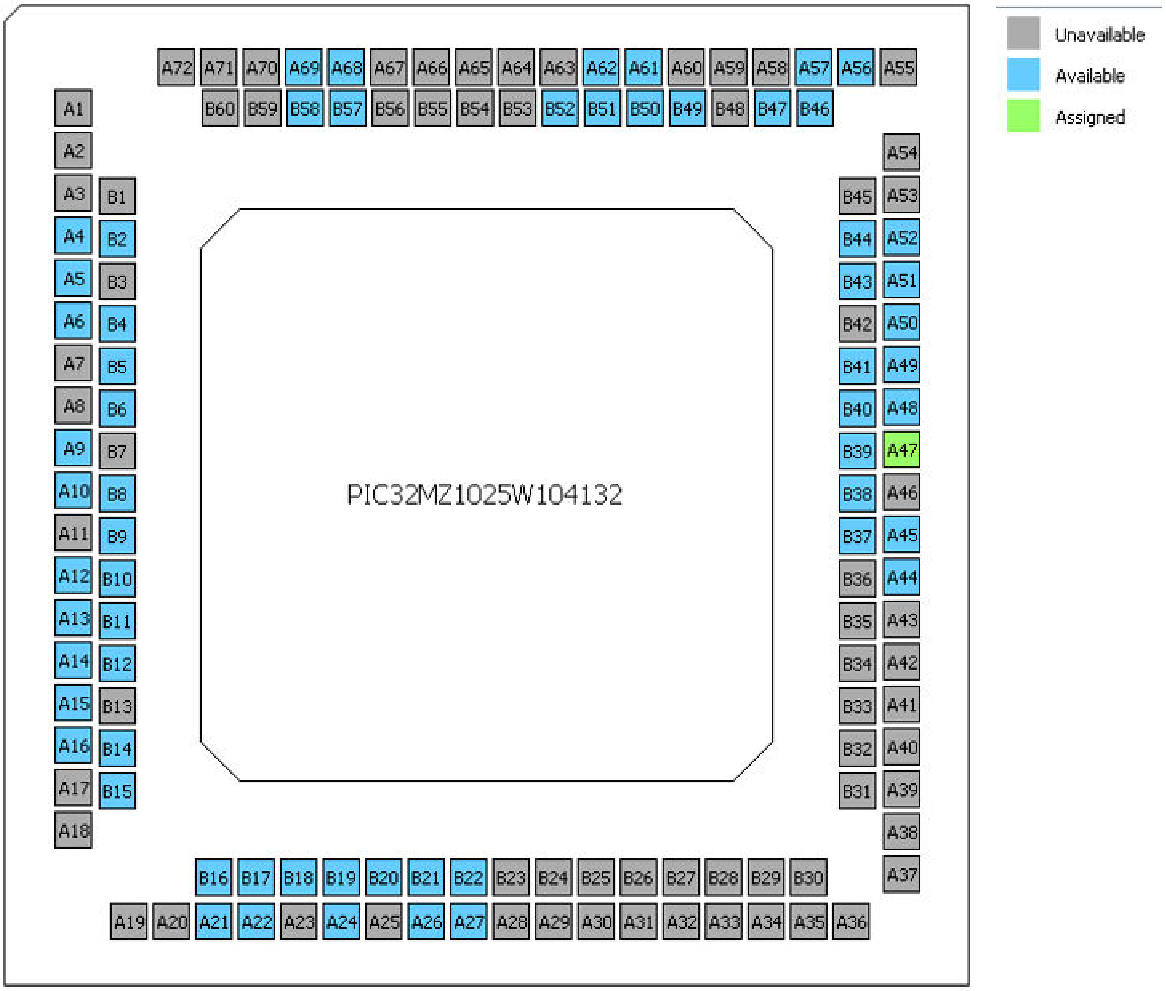
button to generate the code.
   4.1. Once the code generation is successful, click on the **Build Project** button.
   4.2. The “Build Successful” message in the output window of MPLAB X IDE confirms successful compilation.

Note: This procedure applies to all the existing examples or demo projects and for the development of new examples or application projects.

2.2.3 Pin Configuration using Pin Manager

The Pin Manager enables users to configure (assign peripheral function, set pin direction, configure pull-up or pull-down and so on) and map the I/O pins. It consists of **Pin Settings**, **Pin Diagram** and the **Pin Table** tabs. The following figure illustrates the pictorial representation of the available, assigned and not available pins of the MCU.

Figure 2-9. Pin Diagram



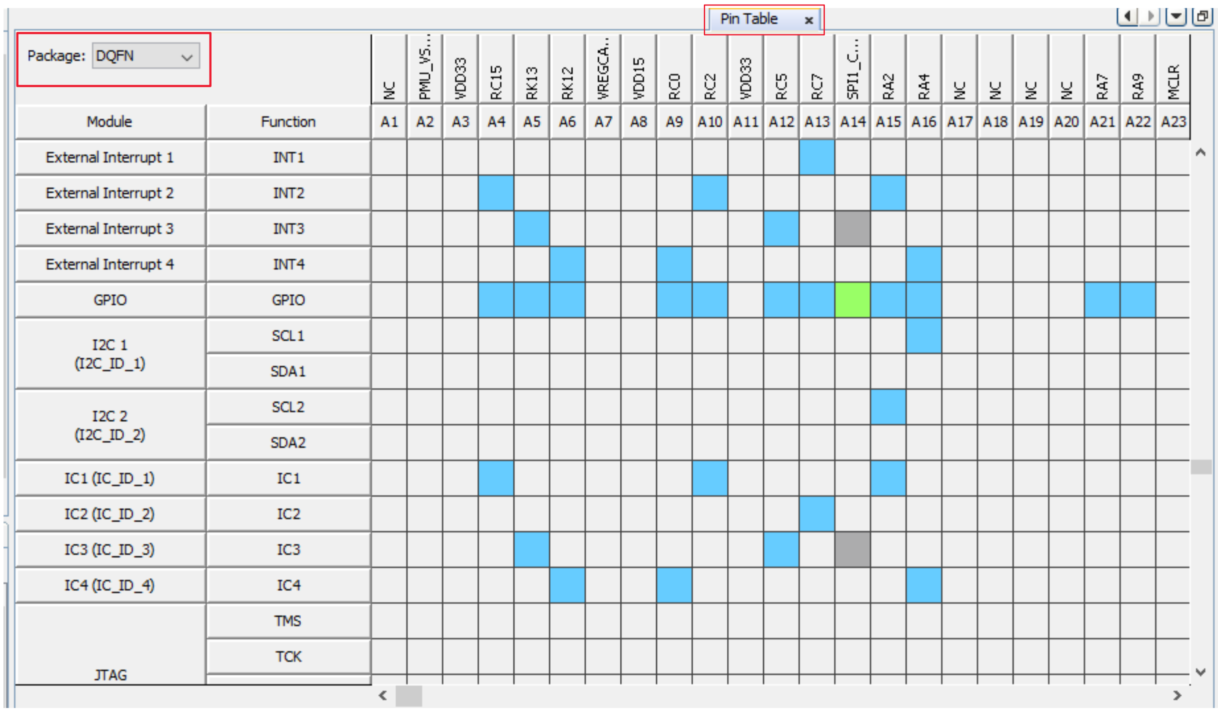
Notes: The following color combinations are associated with the pins in the graphical or table view:

- Gray – These pins are not used in the selected configuration. These pins are locked out by selected system functions and cannot be changed by the user.
- Blue – These pins are available and can be allocated to a module.
- Green – This pin is allocated and selected for a module. It displays either the name of the pin in the module’s context or a custom name entered. This pin is locked and not available for any new pin assignment.

The **Pin Table** tab provides the Pin Manager’s grid view. Select *DQFN* from the Package drop-down list.

- The package details display in the package view.
- The table view provides the pin numbers for the selected package. The leftmost columns in the table view indicate the module’s and the functionality name.

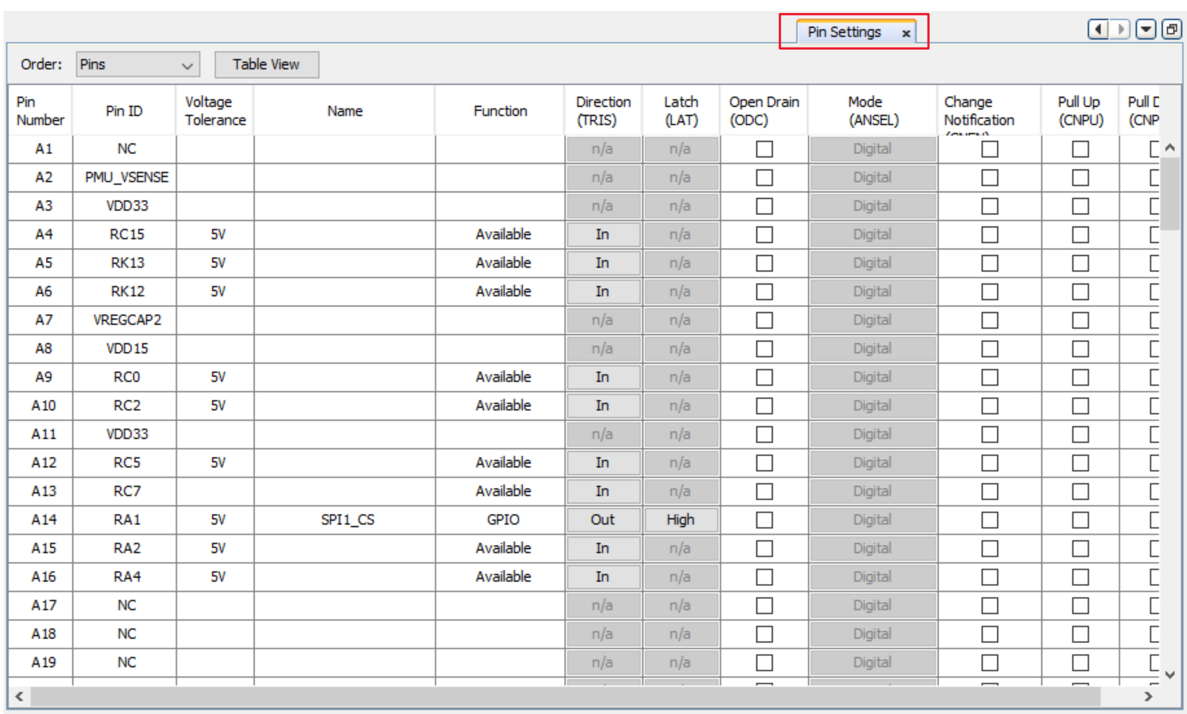
Figure 2-10. Pin Table



The **Pin Settings** tab enables the user to perform the following functions:

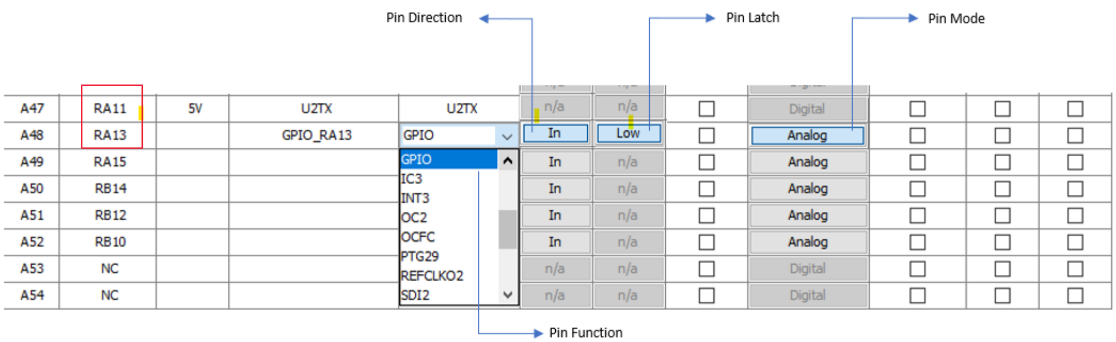
- To configure the pins
- To provide a custom name for the pin
- To change the pin function, direction, latch and other properties

Figure 2-11. Pin Settings



The following figure illustrates an example where the RA11 pin is configured as an U2TX (UART2 transmit pin). Similarly, it shows another example where the RA13 pin is configured as a *GPIO*. The highlighted buttons on the right side enable the user to set the Direction, Latch and the Mode of the selected pin.

Figure 2-12. Example of Pin Settings



Note: For more details on the Pin Manager, refer to *MPLAB Harmony Configurator User's Guide* (MPLAB Harmony).

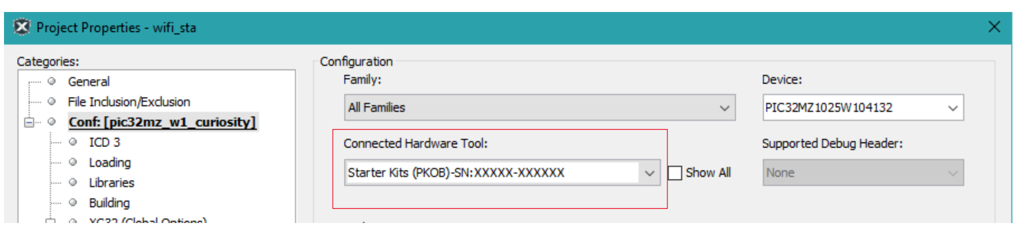
2.3 Programming MPLAB Projects

Note: For more information on how to install the MHC and how to get started using MPLAB Harmony, refer to MPLAB Harmony.

Perform the following steps in MHC for programming the project:

1. Open the MPLAB project.
2. In the Projects Properties window, select the on-board PKOB from the “Connected Hardware Tool” drop-down menu as shown in the following image.

   Figure 2-13. Selecting On-board PKOB

3. Use the following steps to build the project:
   3.1. Go to *Production* > *Build Main Project* or press F11 to build a project.
   3.2. Go to *Production* > *Set Main Project* > *Choose the project to program*.
   3.3. Go to *Debug* > *Debug Main Project*.

Note: For more details on programming and debugging of the Curiosity board, refer to *PIC32 WFI32E Curiosity Board User's Guide* (DSxxxxxxxx).

3. Appendix A: Configuration Bits

This section describes the configuration bits used for all of the application examples. The configuration bit details are part of the `initialization.c` file in any of the Harmony projects.

```
// ****************************************************************************
// ****************************************************************************
// Section: Configuration Bits
// ****************************************************************************
// ****************************************************************************
/*** FBCFG0 ***/
#pragma config BUHSWEN          = OFF
#pragma config PCSCMODE         = DUAL
#pragma config BOOTISA          = MIPS32


/*** DEVCFG0 ***/
#pragma config TDOEN            = ON
#pragma config TROEN            = OFF
#pragma config JTAGEN           = OFF
#pragma config FCPRI            = LRSA
#pragma config DMAPRI           = LRSA
#pragma config EXLPRI           = LRSA
#pragma config USBSSEN          = OFF
#pragma config PMULOCK          = OFF
#pragma config PGLOCK           = OFF
#pragma config PMDLOCK          = OFF
#pragma config IOLOCK           = OFF
#pragma config CFGLOCK          = OFF
#pragma config OC_ACLK          = OCMP_TMR2_TMR3
#pragma config IC_ACLK          = ICAP_TMR2_TMR3
#pragma config CANFDDIV         = 0
#pragma config PCM              = SFR
#pragma config UPLLHWMD         = OFF
#pragma config SPLLHWMD         = OFF
#pragma config BTPLLHWMD        = OFF
#pragma config ETHPLLHWMD       = OFF
#pragma config FECCCON          = OFF
#pragma config ETHTPSF          = RPSF
#pragma config EPGMCLK          = FRC

/*** DEVCFG1 ***/
#pragma config DEBUG            = EMUC
#pragma config ICESEL           = ICS_PGx2
#pragma config TRCEN            = ON
#pragma config FMIIEN           = OFF
#pragma config ETHEXEREF        = OFF
#pragma config CLASSBDIS        = DISABLE
#pragma config USBIDIO          = ON
#pragma config VBUSIO           = ON
#pragma config HSSPIEN          = OFF
#pragma config SMCLR            = MCLR_NORM
#pragma config USBDMTRIM        = 0
#pragma config USBDPTRIM        = 0
#pragma config HSUARTEN         = ON
#pragma config WDTPSS           = PSS1

/*** DEVCFG2 ***/
#pragma config DMTINTV          = WIN_63_64
#pragma config POSCMOD          = HS
#pragma config WDTRMCS          = LPRC
#pragma config SOSCSEL          = CRYSTAL
#pragma config WAKE2SPD         = ON
#pragma config CKSWEN           = ON
#pragma config FSCMEN           = ON
#pragma config WDTPS            = PS1
#pragma config WDTSPGM          = STOP
#pragma config WINDIS           = NORMAL
#pragma config WDTEN            = OFF
#pragma config WDTWINSZ         = WINSZ_25
#pragma config DMTCNT           = DMT31
#pragma config DMTEN            = OFF

/*** DEVCFG4 ***/
```

```
#pragma config SOSCCFG          = 0
#pragma config VBZPBOREN        = ON
#pragma config DSZPBOREN        = ON
#pragma config DSWDTPS          = DSPS1
#pragma config DSWDTOSC         = LPRC
#pragma config DSWDTEN          = OFF
#pragma config DSEN             = OFF
#pragma config SOSCEN           = OFF
```

4. Document Revision History

Revision	Date	Section	Description
A	09/2020	Document	Initial revision

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