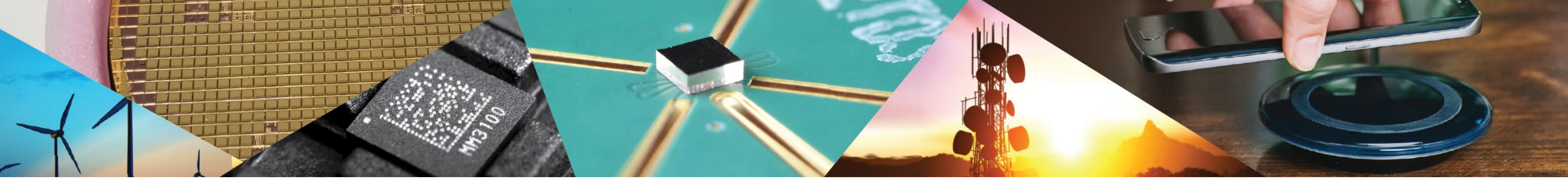


Preliminary Datasheet

MM5120 DC – 18 GHz RF SP4T with Integrated Driver

Product Overview

Description

The MM5120 is a high-power SP4T switch built on Menlo Micro's Ideal Switch® technology. This innovative technology enables highly reliable switches capable of greater than 25 W forward power. The MM5120 provides ultra-low insertion loss and superior linearity as an SP4T from DC to 18 GHz, with greater than 3 billion switching cycles. The MM5120 is an ideal solution for replacing large RF electromechanical relays, as well as RF/microwave solid-state switches in applications where linearity and insertion loss are critical parameters. The MM5120 features an integrated driver circuit with SPI and GPIO interface control options and an integrated charge pump to drive the gate.

Features

- DC to 18 GHz Frequency Range
- Integrated High-Voltage Driver
- 25 W (CW), 150 W (Pulsed) Max Power Handling
- Low On-State Insertion Loss: 0.4 dB @ 6.0 GHz
- High Linearity, IIP3 > 90 dBm
- 25 dB Isolation @ 6.0 GHz
- Very Low Current Consumption <1mA
- High Reliability > 3 billion Switching Operations
- 5.2 mm x 4.2 mm LGA Package

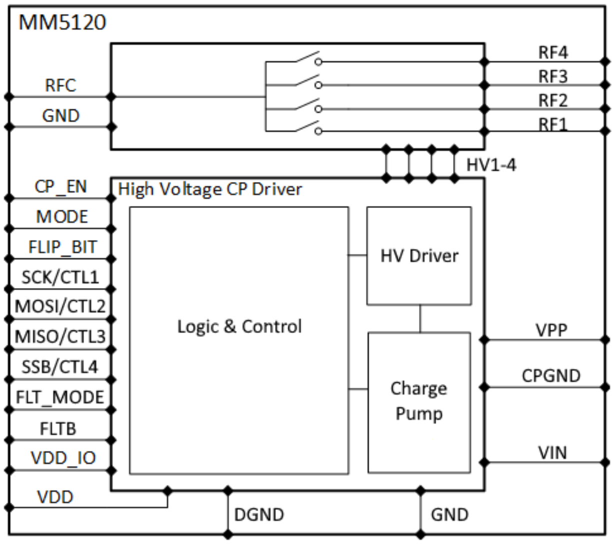
Markets

- Defense and Aerospace
- Test and Measurement
- Wireless Infrastructure

Applications

- Switched Filter Banks and Tunable Filters
- High Power RF Front-Ends
- Low-Loss Switch Matrices
- RF EM Relay Replacement
- Antenna Tuning
- Antenna Beam Steering
- Digital Step Attenuators

RoHS COMPLIANT



Electrical Characteristics

Operating Characteristics

Absolute Maximum Ratings

Exceeding the maximum ratings as listed in Table 1 below may reduce the reliability of the device or cause permanent damage. Operation of the MM5120 should be restricted to the limits indicated in the recommended operating conditions listed in Table 2.

Electrostatic Discharge (ESD) Safeguards

The MM5120 is a Class 0 ESD device. When handling the MM5120, observe precautions as with any other ESD sensitive device. Do not exceed the voltage ratings specified in Table 1 below.

Table 1 Absolute Maximum Ratings [1]

Parameter	Minimum	Maximum	Unit
CW Input Power @ 6 GHz		25	W
Peak Input Power @ 6 GHz		150	W
Open State Voltage Rating / Switch RF1-4 to RFC [2]	-150	150	V
Open State Voltage RF1-RF4, RFC to GND[2]	-150	150	V
Hot Switching Voltage [3]	-0.5	0.5	V
DC Supply Voltage (VDD)	-0.3	3.6	V
I/O Supply Voltage (VDD_IO)	-0.3	5.5	V
Charge Pump Input (VIN)	-0.3	5.5	V
Charge Pump High Voltage Output (VPP)	-0.3	105	V

[1] All parameters must be within recommended operating conditions. Maximum DC and RF power can only be applied during the on-state condition (cold-switched condition).
[2] This also applies to ESD events. This is a Class 0 device.
[3] See section

Hot Switch Restrictions for more information.

DC Steady State Current		500	mA
Logic Input Levels	-0.5	VDD_IO+0.3	V
Operating Temperature Range	-40	85	ºC
Storage Temperature Range [4]	-65	150	ºC
ESD Rating HBM RF Pins [5]		150	V
ESD Rating HBM Control and Power Pins [6]		2000	V
ESD Rating HBM VPP Pin		500	V
Mechanical Shock [7]		500	G
Vibration [8]		500	Hz

Table 2 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Conditions
Charge Pump Power Supply	VIN	4.5	5.5	V	
Low Voltage Digital Supply	VDD	3.0	3.6	V	
Logic Reference Level (VDD_IO)	VDD_IO	1.71	5.25	V	

[4] See section Storage and Shelf Life more information on shelf and floor life.
[5] RF pins include: RF1, RF2, RF3, RF4, and RFC.
[6] Control and power pins include: VIN, VDD, VDD_IO, FLT_MODE, FLTB, FLIP_BIT, CP_EN, MODE, and CTL1-4.
[7] See JESD22-B104 for mechanical shock test methodology at 1.0 ms, half-sine, 5 shocks/axis, 6 axis.
[8] See JESD22-B103 for vibration test methodology at 3.1 G and 30min/cycle, 1 cycle/axis, 3 axis.

Electrical Characteristics

All specifications valid over full supply voltage and operating temperature range unless otherwise noted. Operating with all RF, analog, and digital GND pins connected to system ground (0 V) and with input frequencies of greater than 10 MHz in a 50 Ω impedance system.

Table 3 RF Performance Specifications

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Operating Frequency Range		DC		18	GHz	
CW Power				25	W	Measured at 6 GHz, +85 °C
Peak Power				150	W	For 10 % Duty Cycle and 10 µs pulse width, measured at 6 GHz, +85ºC.
Insertion Loss			0.4 0.6 1.2		dB	@ 6 GHz @ 12 GHz @18 GHz
Input / Output Return Loss			15 15 12		dB	@ 6 GHz @ 12 GHz @18 GHz
Isolation			26 22 17		dB	@ 6 GHz @ 12 GHz @18 GHz
Channel to Channel Isolation			25		dB	@ 6 GHz
Third-Order Intercept Point	IP3		90		dBm	Measured at +25ºC.
Second Harmonic	H2		-130		dBc	Measured at 1.0 GHz and 2.0 GHz fundamental frequency and 35 dBm input power.
Third Harmonic	H3		-130		dBc	Measured at 1.0 GHz and 2.0 GHz fundamental frequency and 35 dBm input power.

Charge Pump Clock Feed Thru			-120		dBm	

Table 4 Switch AC and DC Electrical Specifications

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Switching Time Turn on Turn off			8.5 2.5		µs	Switching time measured from 50% rising edge of last SPI CLK to settling to within 0.05 dB of final value.
Full Cycle Frequency				10	kHz	
On/Off Operations (MM5120-01NDB) @25 ºC @85 ºC		$3x10^9$	30 $x10^9$ $1x10^8$		Cycle	Data taken from MM5130 reliability test results. Cold switched operations, measured at 10 kHz cycling rate, specified at 25 C ambient.
DC Steady State Current				500	mA	
Off-State RFC to RFx Leakage Current			15	150	nA	
On-State Resistance	R_{On}		1.2	3	Ω	Measured with 0.5 A after 1000 cycles.
Off-State Capacitance	C_{Off}		TBD		fF	Capacitance between input and output pins.
Video Feedthrough			16		mV_{Peak}	Performed with 1 MΩ termination.

Table 5 Charge Pump and Driver Electrical Specifications

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
VIN Current (Dynamic)	I_{VIND}		1.5	2.5	mA	SPI mode, Charge pump on, Outputs switching at 10 kHz, CLoad = 2 pF (per output).
VIN Quiescent Current	I_{VINQ}		1.25	2.0	mA	Charge pump on, all I/O and outputs static.
VDD UVLO Rising Threshold	$UVLO_{RISE}$	2.77	-	2.95	V	
VDD UVLO Falling Threshold	$UVLO_{FALL}$	2.72		2.90	V	
Low Voltage Digital Current	IDD	-	400	500	µA	SPI mode, Outputs Switching at 10 kHz, CL = 2 pF (per channel).
Low Voltage Digital Quiescent Current	IDD_Q	-	285	350	µA	Charge pump On, All I/O & RF channels static.
Low Voltage Digital Sleep Mode Current	IDD_{SLEEP}	-	<1	10	µA	Charge pump Off, SPI and inputs in static state.
I/O Logic Supply Current	I_{DD_IOQ}		<10	50	µA	

Fault Indicator Open-Drain Output	FLTB	0	-	VDD_IO	V	
Logic I/O Level High)	I/O_{VH}	0.7*VDD_IO	-	VDD_IO	V	
Logic I/O Level Low	I/O_{VL}	0	-	0.3* VDD_IO	V	
SDO Load Capacitance	C_{SDO}	-	-	10	pF	Specification is for design guidance only. SDO load capacitance is SDI input capacitance pin and PCB trace capacitance from SDO to SDI.
SDO Source Current () @ VDD_IO: 5 V 3.3V 1.8V	I_{SDOH}	180 75 20	290 140 35	-	mA	Measured at V_{OUT} = 0.8 x VDD_IO.
SDO Sink Current @ VDD_IO: 5.0 V 3.3 V 1.8 V	I_{SDOL}	140 65 20	260 140 40	-	mA	Measured at V_{OUT} = 0.2 x VDD_IO.
CP_EN pin toggle low time	T_{TOGGLE}	500	-	-	ns	Minimum time CP_EN has to be held low to re-start the IC from fault condition.
FLTB pin max sink current		65	140	-	mA	FLTB active low, measured with VDD_IO = 3.3V.

Logic I/O Hysteresis (SCK only)	I/O_{VH}	-	0.25	-	V	
Start-Up Time	T_{ST}	-	20	33	ms	CP_EN=1 (CPEN bit=1) to VPP rises to 90% of set value.
Power-On-Reset	POR	-	1.25	2.5	ms	Time for logic input signals to be considered valid after application of VIN and VDD.

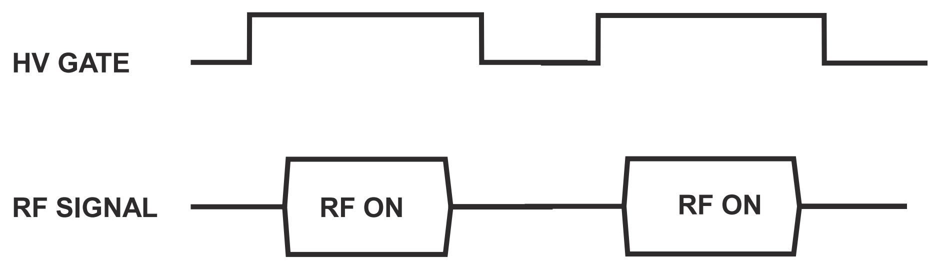
Table 6 Driver Interface Timing Specifications

Parameter	Sym	Min	Typ	Max	Unit
SPI Clock Frequency SCK	f_{CLK}	-	-	33	MHz
SDI Valid to SCK Setup Time	t_{SU}	2	-	-	ns
SDI Valid to SCK Hold Time	t_{HD}	5	-	-	ns
SCK High Time	t_{HI}	15.5	-	-	ns
SCK Low Time	t_{LO}	15.5	-	-	ns
SSB Pulse Width	t_{CSH}	15	-	-	ns
LSB SCK to SSB High)	t_{CSHLD}	15	-	-	ns
SSB Low to SCK High)	t_{CSSU}	15	-	-	ns
SDO Propagation Delay from SCK Falling Edge	t_{SDOH}	10	-	-	ns
SDO Output Valid after SSB Low	t_{CSDO}	20	-	-	ns
SSB Inactive to SDO High Impedance)	t_{SDOZ}	-	-	10	ns

See Programming section for driver interface timing diagrams and details.

Hot Switch Restrictions

The MM5120 is not intended for hot switching applications and care should be taken to insure that switching occurs at less than 0.5 V as illustrated below. Further, the voltage at the switch terminals must be within +/-0.5 V relative to RF ground. .



Floating Node Restrictions

RF pins must not be allowed to electrically float during switch operation and therefore require some form of DC path to ground to prevent charge accumulation. DC paths can be an inductor or high value resistance which serves as a discharge path. Floating node examples are:

- Unconnected RF pins, resistively terminate or tie to ground.
- Series capacitance coupling which floats RF pin, shunt with DC path to ground.

See Menlo Micro application note ***Avoiding Floating Nodes*** for detailed explanation of the hazard conditions to avoid and recommended solutions.

Functional Block Diagram

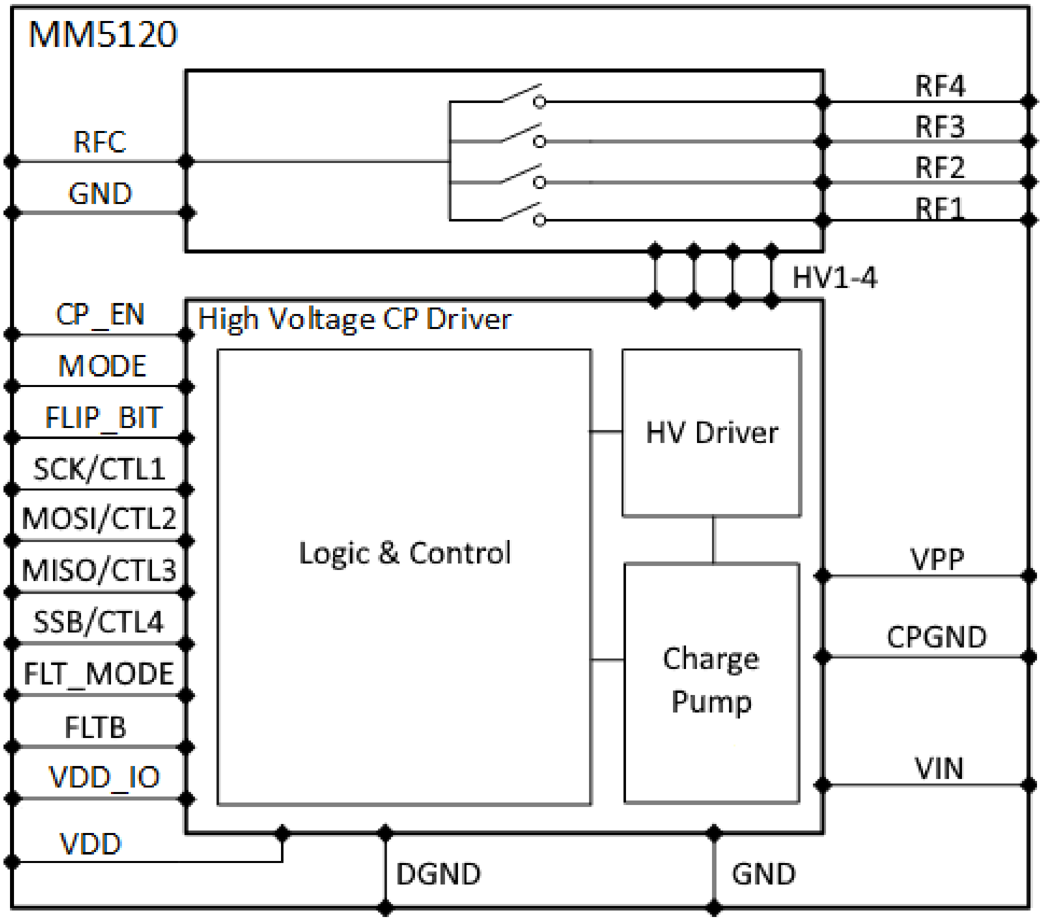


Figure 1: Functional Block Diagram

Package / Pinout Information

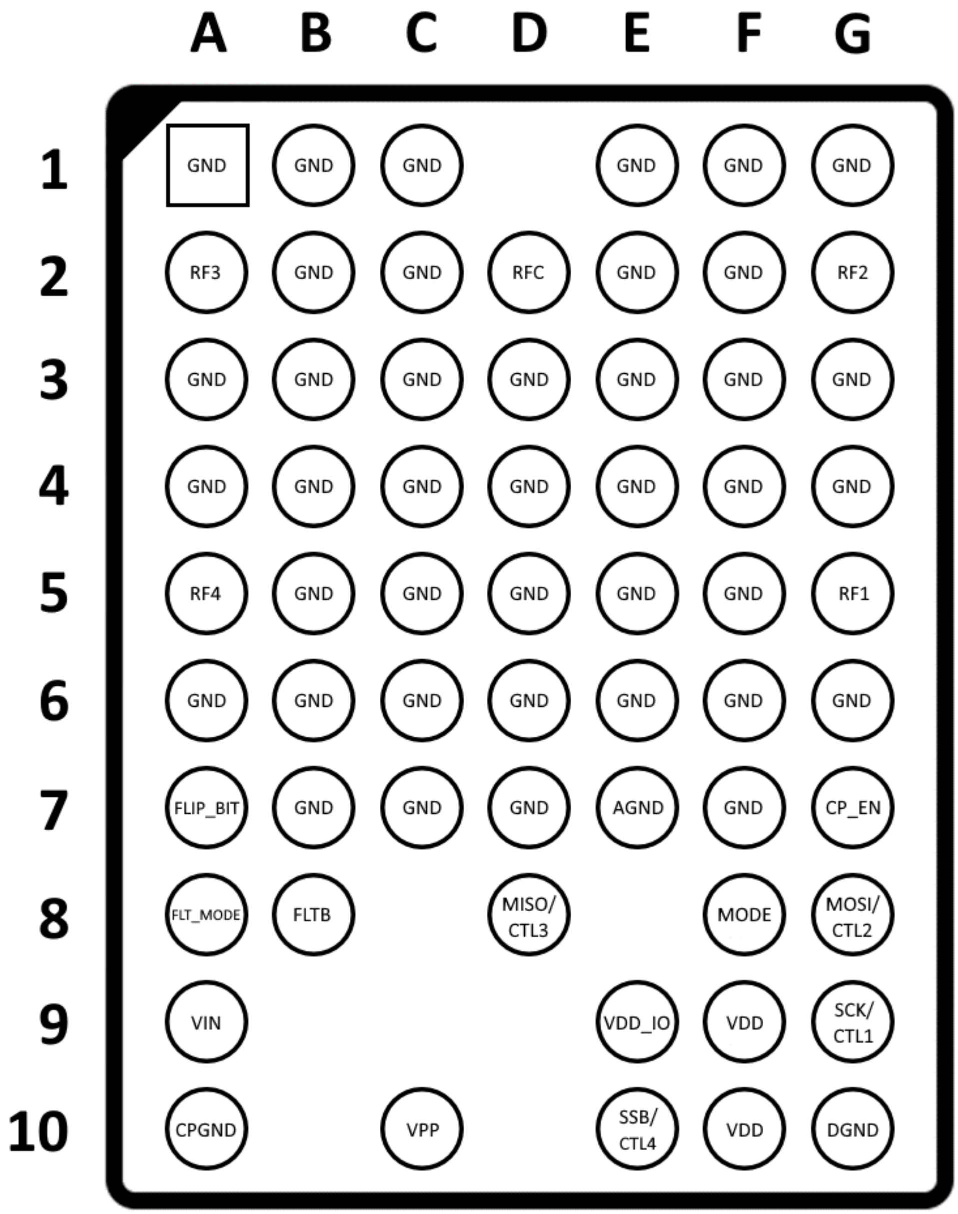


Figure 2: MM5120 5.2 mm x 4.2 mm LGA package pinout (Top View/As Mounted)

Table 7 Detailed Pin Description

Pin #	Pin Name	Description
A1, A3, A4, A6, B1-B7, C1-C7, D3-D7, E1-E6, F1-F7, G1, G3, G4, G6	GND	Connect to common ground. These pins are internally connected to the RF ground reference.
A2	RF3	RF channel 3 input/output.
A5	RF4	RF channel 4 input/output.
A7	FLIP_BIT	This pin has an internal pull-down resistor. In SPI mode, spread spectrum is enabled if high. In GPIO mode FLIP_BIT controls the logic mapping between CTL1-4 and RF1-4. When FLIP_BIT is low, CTL1 enables RF1 when high, and so on for CTL2-4. When FLIP_BIT is high, refer to **Table 8**.
A8	FLT_MODE	Fault Mode select in GPIO mode. Fault Mode is disabled if high. Has a built-in pull-down resistor. Pin is ignored in SPI mode.
A9	VIN	Connect to 5 V power supply. Bypass with a low ESR 1 µF ceramic capacitor. See TBD app note if using external high-voltage supply.
A10	CPGND	Charge pump ground, should be connected to PCB ground.
B8	FLTB	Fault indicator in GPIO and SPI modes. Open drain output to allow “Wire-OR” of multiple ICs. Goes low when fault is detected. Can be left open if not used. Pull-up voltage must be ≤ VDD_IO.
C10	VPP	High-voltage input to the output drivers. Bypass with a 4.7 nF, 200 V, 10 % C0G ceramic capacitor, to the CPGND pin.
D2	RFC	RF common input/output.
D8	MISO/CTL3	SPI data output in SPI mode; RF channel control in GPIO mode. Has an internal pull-down resistor.
E7	AGND	Analog ground, should be connected to PCB ground.
E9	VDD_IO	For 3.3 V nominal digital I/O levels, connect to VDD. For alternate I/O levels, connect to a separate supply (+1.8V to +5.0V). Bypass with a low ESR 1 µF ceramic capacitor if separate from VDD.

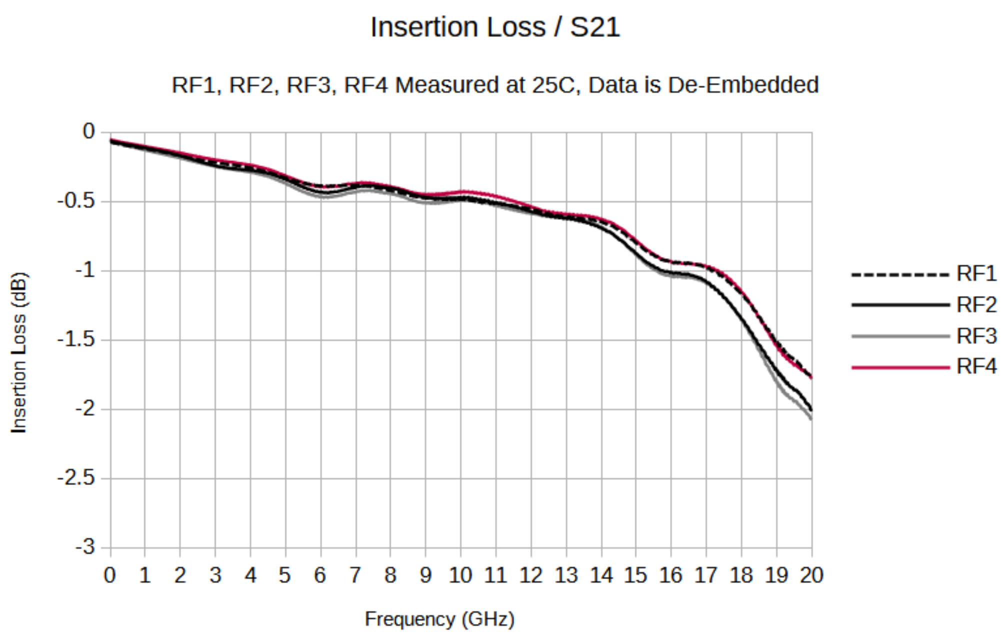
Pin #	Pin Name	Description
E10	SSB/CTL4	Chip select in SPI mode; RF4 channel enable in ode. Has an internal pull-up resistor in SPI mode, and an internal pull-down resistor in GPIO mode.
F8	MODE [9]	Logic level input to switch inputs between SPI and GPIO modes. MODE = 0 is SPI mode. MODE = 1 is GPIO mode.
F9, F10	VDD	3.3 V nominal input to digital logic and internal level translators. Bypass with a low ESR 1 μF ceramic capacitor.
G2	RF2	RF channel 2 input/output.
G5	RF1	RF channel 1 input/output.
G7	CP_EN	Charge pump enable pin in GPIO mode. Pull-up to VDD to enable the charge pump. Has a built-in pull-down resistor. Pin is ignored in SPI mode.
G8	MOSI/CTL2	SPI data input in SPI mode; RF2 channel enable in GPIO mode. Has an internal pull-down resistor.
G9	SCK/CTL1	Clock input in SPI mode; RF1 channel enable in GPIO mode. Has an internal pull-down resistor.
G10	DGND	Digital ground, should be connected to PCB ground.

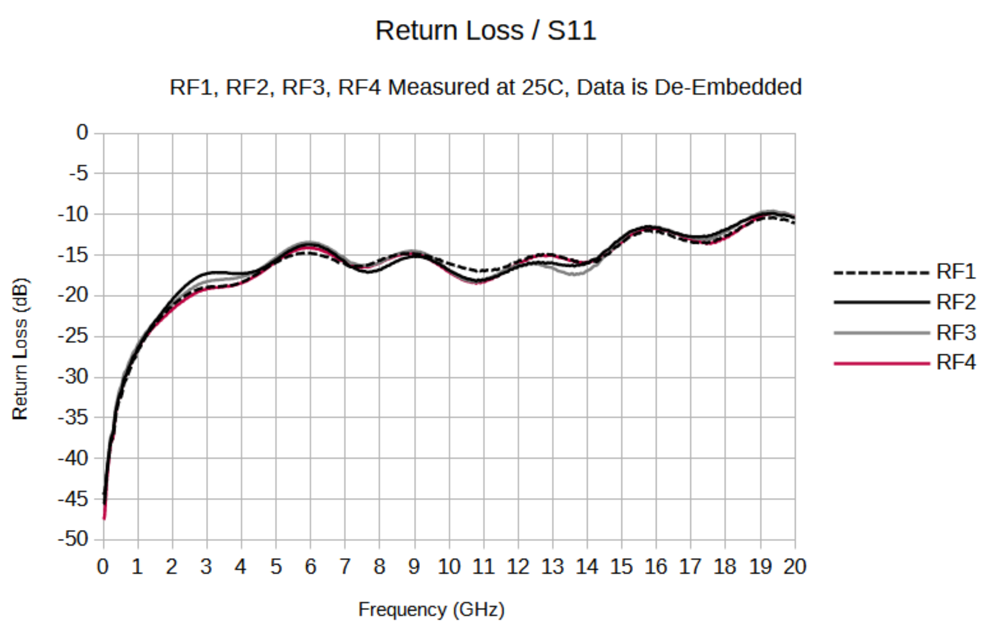
[9] MODE should be tied to GND or VDD_IO if the use case is SPI or GPIO control, respectively.

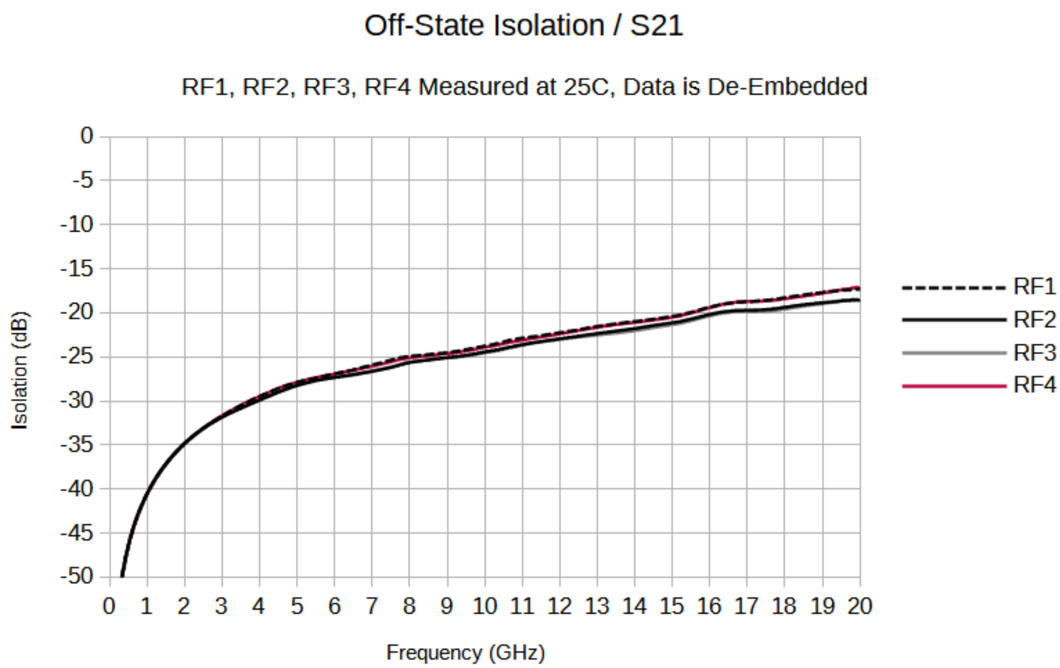
RF Performance

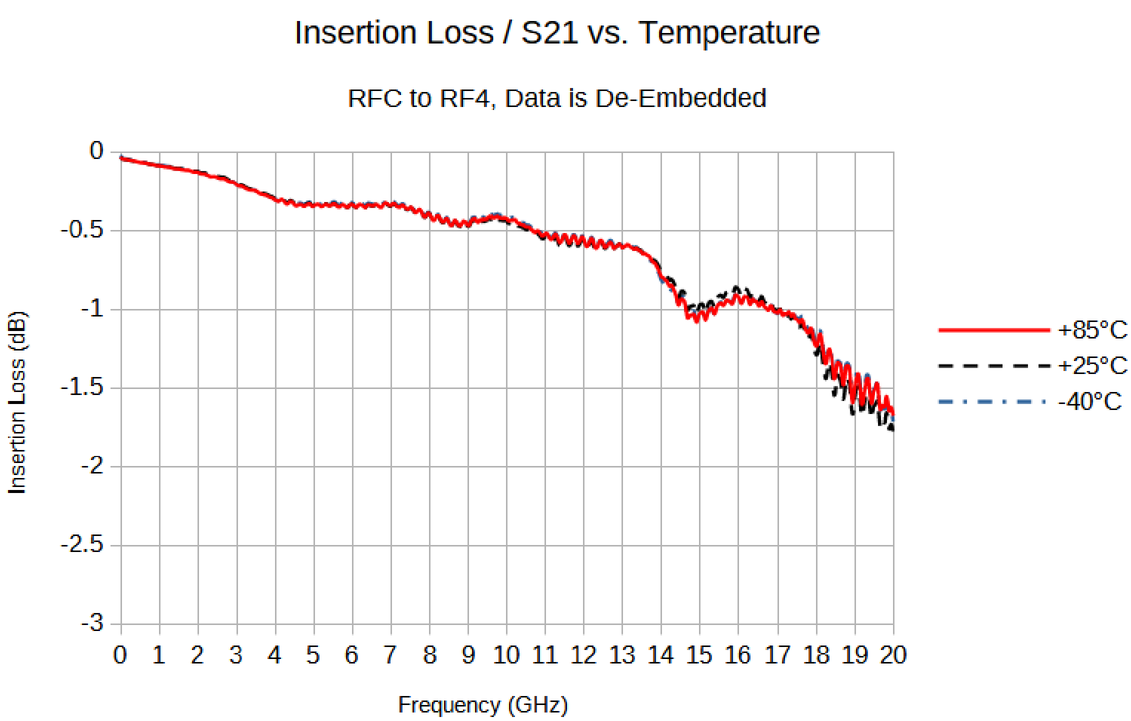
Normal Mode (SP4T)

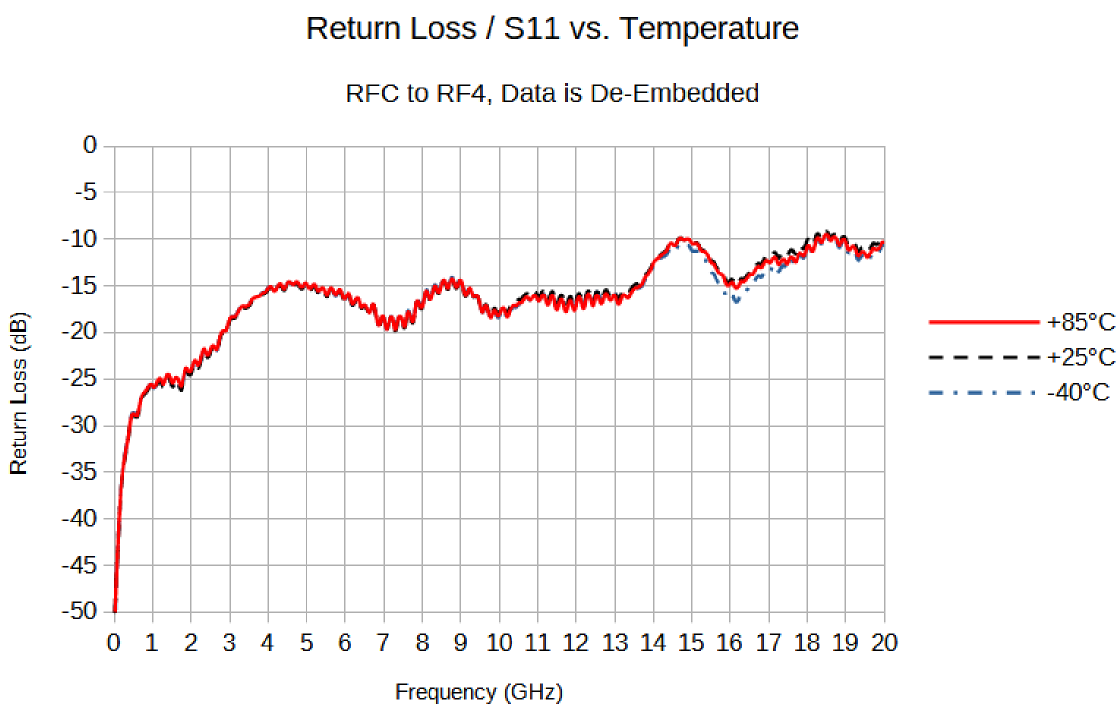
Typical device performance measured on MM5120 evaluation board, de-embedded.

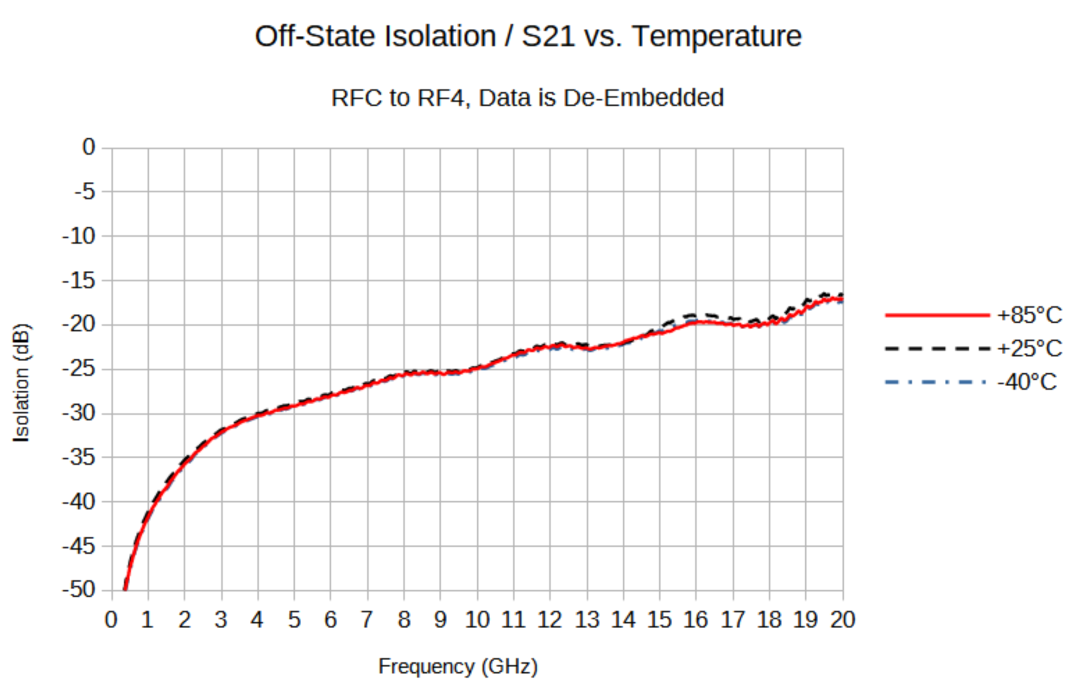





Off-State Isolation / S21
RF1, RF2, RF3, RF4 Measured at 25C, Data is De-Embedded
Isolation (dB)
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Frequency (GHz)
RF1
RF2
RF3
RF4

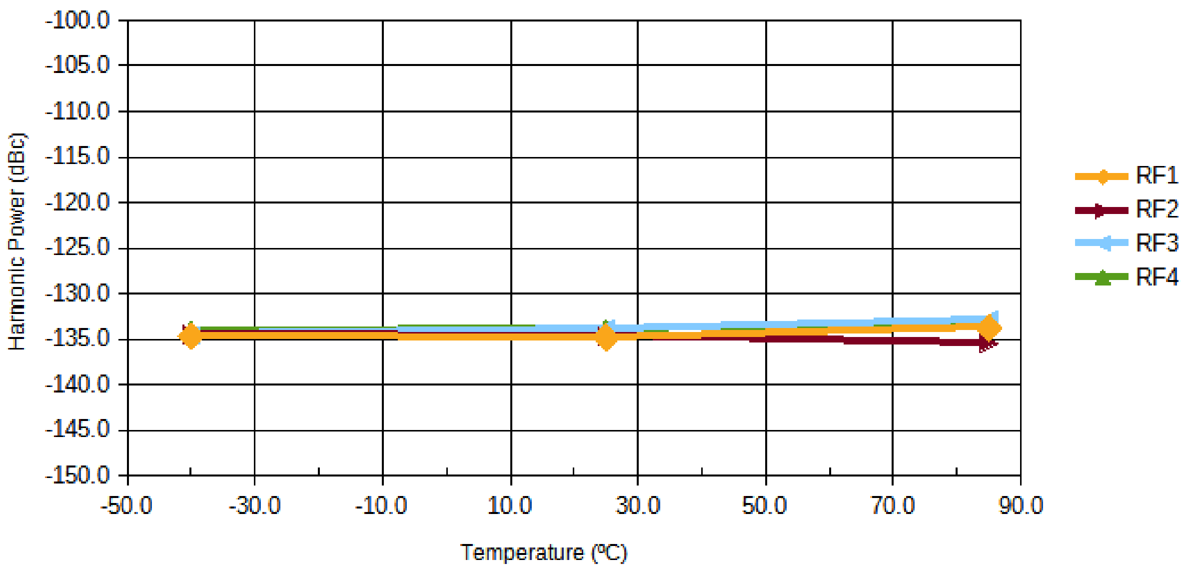

Insertion Loss / S21 vs. Temperature
RFC to RF4, Data is De-Embedded
Insertion Loss (dB)
0
-0.5
-1
-1.5
-2
-2.5
-3
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Frequency (GHz)
+85°C
+25°C
-40°C


Return Loss / S11 vs. Temperature
RFC to RF4, Data is De-Embedded
Return Loss (dB)
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Frequency (GHz)
+85°C
+25°C
-40°C


Off-State Isolation / S21 vs. Temperature
RFC to RF4, Data is De-Embedded
Isolation (dB)
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Frequency (GHz)
+85°C
+25°C
-40°C

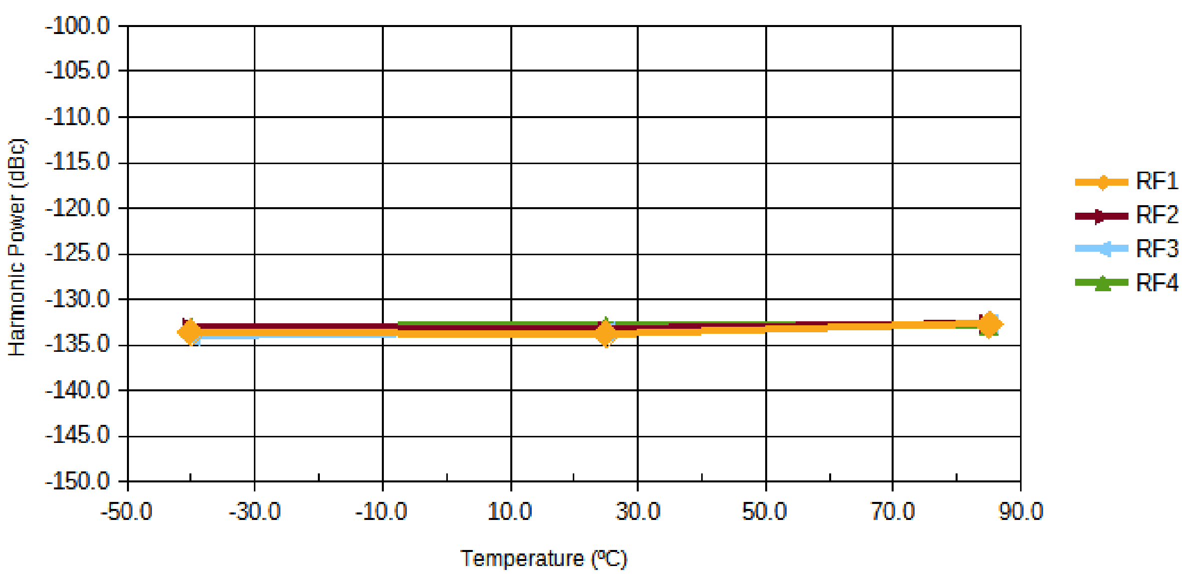
Second Harmonic Power vs. Temperature

f0 = 1.0 GHz, 36 dBm

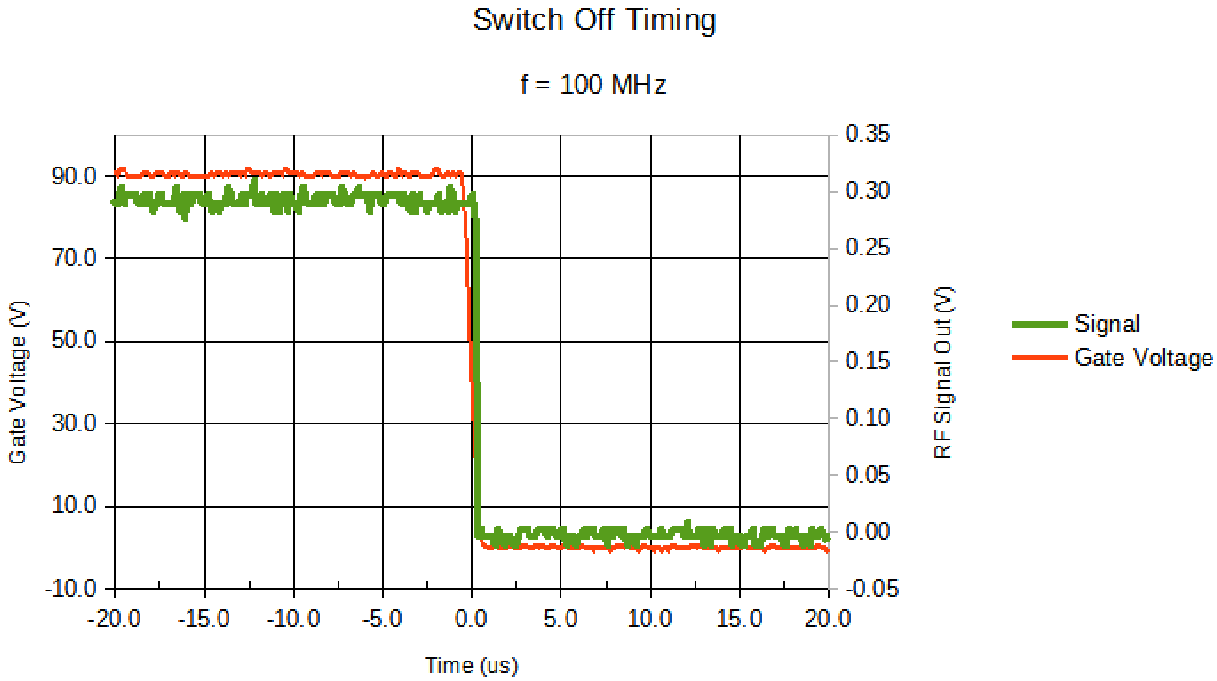


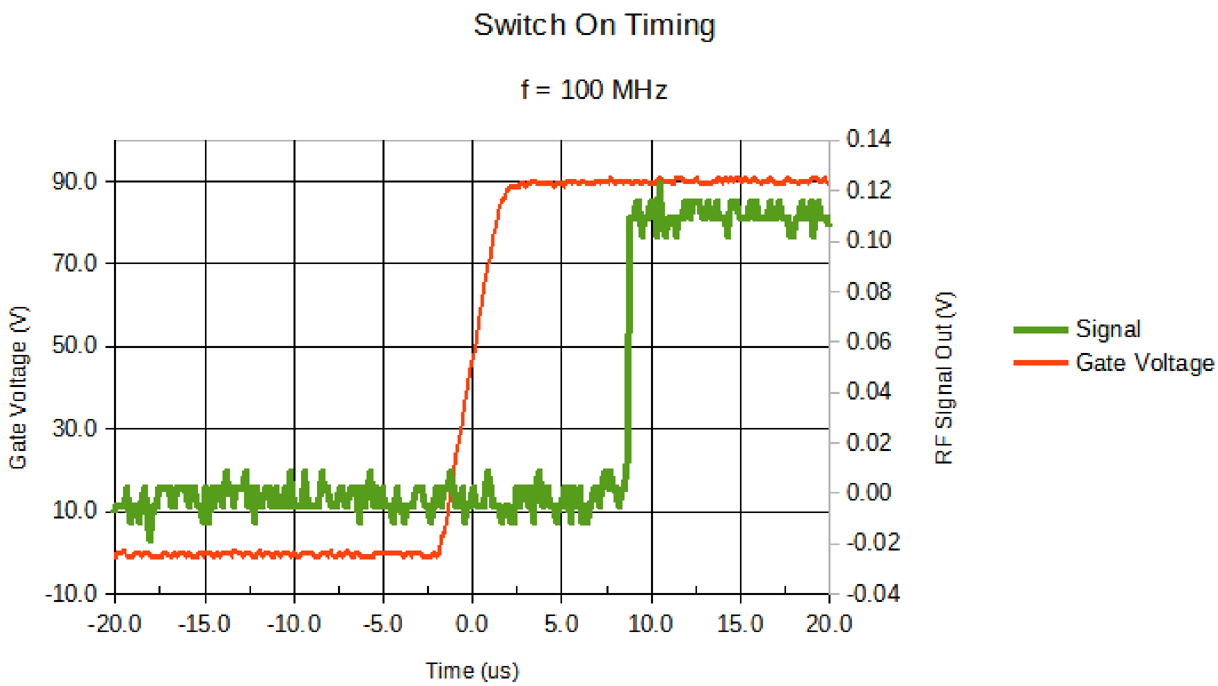
Third Harmonic Power vs. Temperature

f = 1.0 GHz, 36 dBm

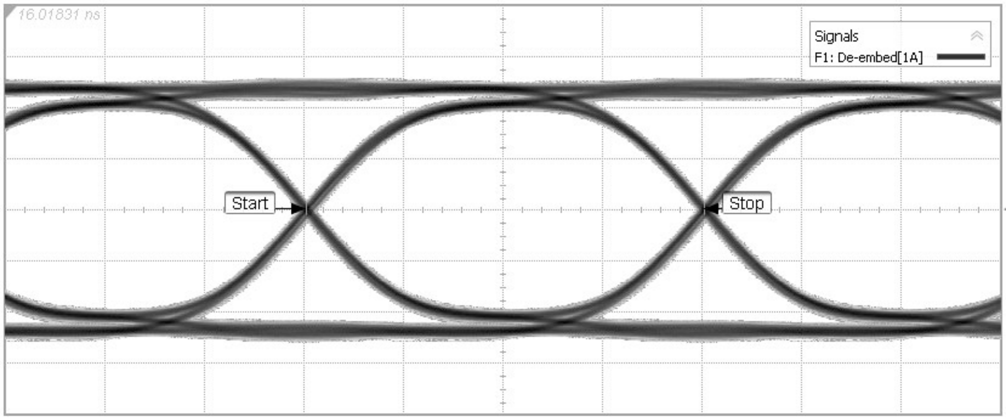


On / Off Switching Time



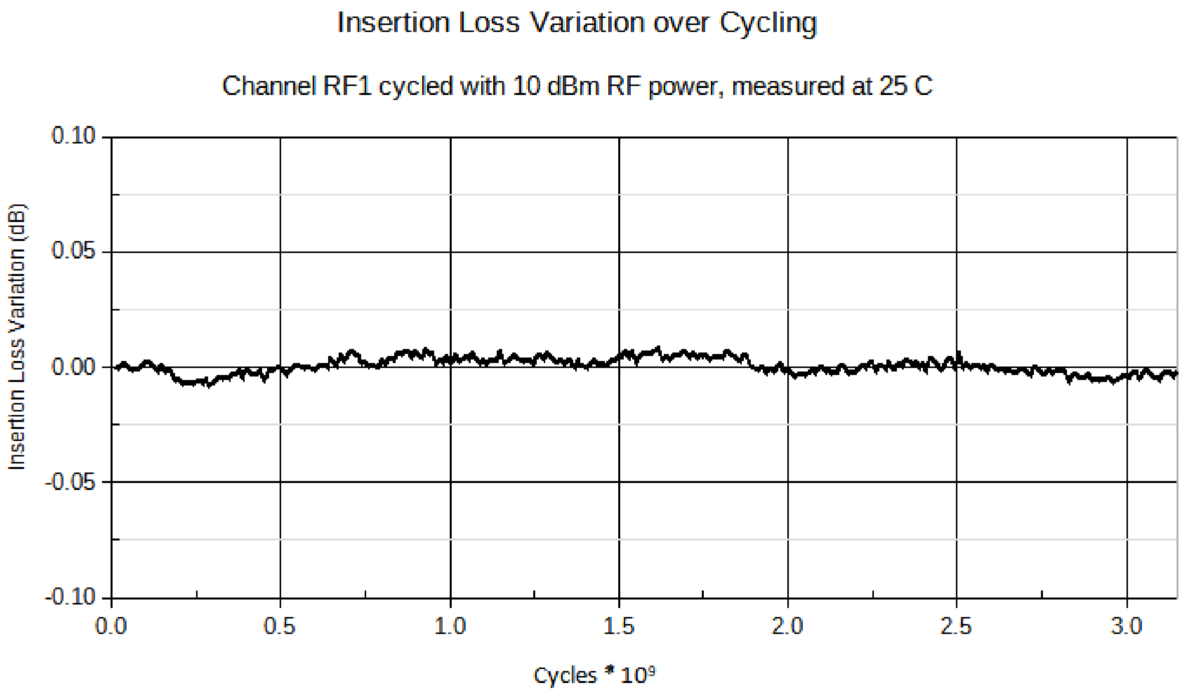


Single-Ended Eye Diagram Measurement



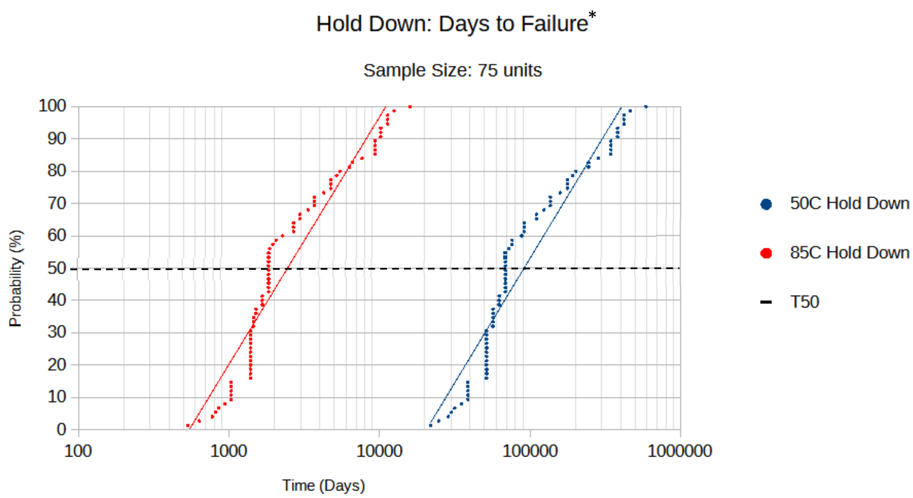
Test Cases	Bit rate	Eye Height	Eye Width	Jitter (Pk to Pk)	Rise Time	Fall Time
Baseline-Test System	20.000 Gbps	440.00 mV	48.16 ps	1.99 ps	14.99 ps	14.33 ps
MM5120 EVK	20.000 Gbps	339.80 mV	48.20 ps	2.16 ps	24.00 ps	24.34 ps

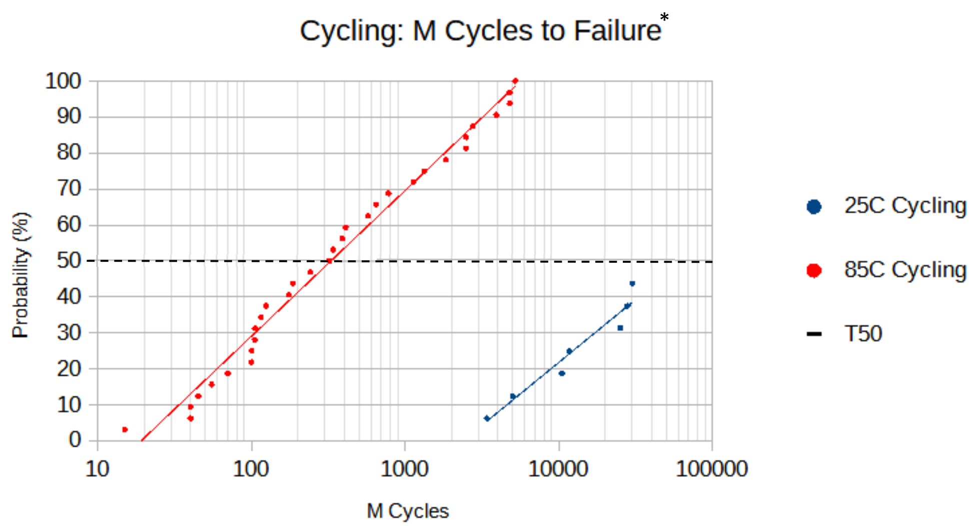
Typical Hot-switching Performance



Switch Reliability Test Results

Switch hold-down duration and actuation cycling reliability test results [10] are plotted below. Hold Down median failure is 68675 days (188 years) @ 50C and 1836 days (5.0 years) @ 85C. Cycling median failure is greater than 30 billion cycles @ 25C and 320 million cycles @ 85C.





*Failure definition is 20% shift in pull-in voltage (VPI).

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[10] Data taken from MM5130 reliability test results.

Programming

Communication Interface

The driver interface two modes of operation; **Serial Peripheral Interface (SPI)** and **GPIO**, selected by the **MODE** input pin.

All the SPI pins (except SSB pin), the FLIP_BIT and the MODE pin have an internal pull-down resistor to ensure that no digital input pins can float.

The SSB pin has a pull-up current source in SPI mode. This ensures that the IC defaults to a disabled state in SPI mode. In GPIO mode, this pin is VIN4. In this case, the SSB pin has a pull-down resistor. This ensures that the input is low by default in GPIO mode.

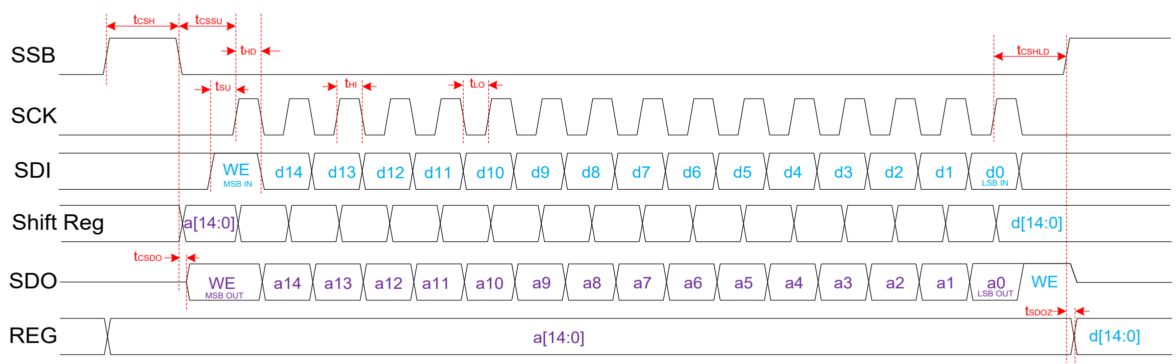


Figure 4: SPI Timing Diagram

SPI Communication

MODE = 0, activates the 16-Bit Serial Peripheral Interface (SPI) module for operation. Multiple devices can be daisy-chained to drive multiple ICs using one SPI bus. (See Daisy Chain Operation figures 7 to 9)

The SPI works at any frequency up to a maximum of 33 MHz, and may operate at significantly lower frequencies if the logic signals adhere to the data setup and hold requirements.

SPI Interface Mode

SPI timing diagrams are provided in Figures 4 to 9. In SPI mode, data transmission starts when SSB goes Low, causing the Target to output the Most Significant Bit (MSB) of data to the SDO (MISO) pin. Data transfer from Host to Target takes place during the rising edge of the clock (SCK), which is idle when SSB is High. This mode of operation requires data for Host and Target to be present on SDI (MOSI) before the rising edge of the clock (defining SDI to SCK setup time). Data is pushed out of the SDO (MISO) pin during the falling edge of the clock. After the first 16-bit transaction, Host writes the latest data (D_N) to Target, while Target passes its previous (D_N-1) stored data to the Host. Data is latched into the internal registers at the rising edge of SSB, if WR_EN = 1.

SPI Data Format

SPI data is sent in a 16-bit format. The first MSB bit (WE), if high, enables the Write mode. The following 7 MSB bits hold the Control and Fault Status bits. The 8 LSB bits hold the Switch State bits.

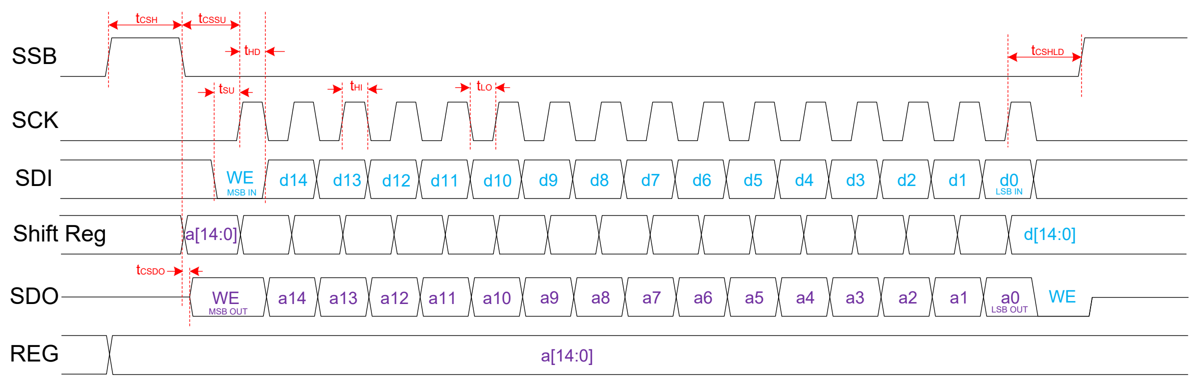


Figure 3: SPI Read Only (1 IC, No Daisy Chain)

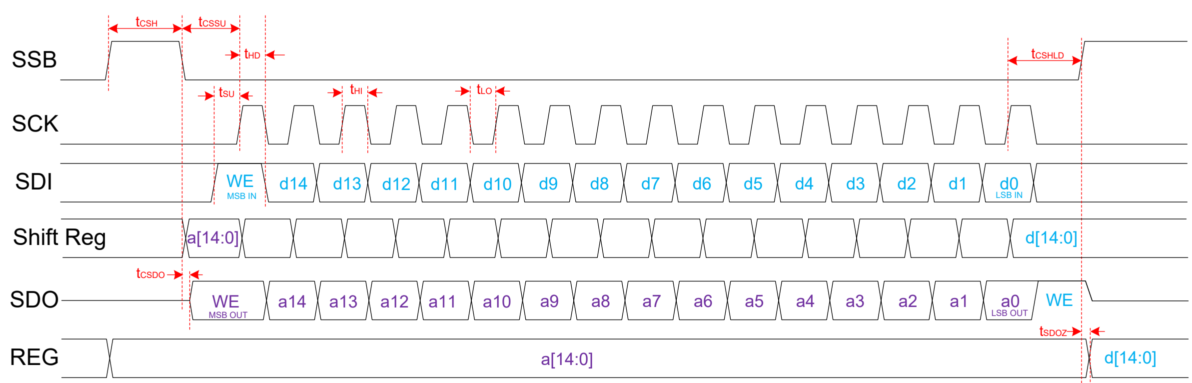


Figure 4: SPI Read & Write (1 IC, No Daisy Chain)

SPI Control Registers

The SPI interface provides access to two 8-bit Internal Registers: Register STATE and Register CONTROL that are Read/Write registers. Register data is read by toggling SSB low and monitoring the data at the SDO pin while clocking the SCK pin.

Register STATE holds the state of the 4 switches and is updated when SSB goes from LOW to HIGH, if the Write Enable bit is high.

Register CONTROL holds four control bits (CPEN, VPPCOMP, FLT_MODE, and SLEEP), and the fault status bit (FSTAT). The MSB bit enables the Write mode if high.

In SPI mode, the CP_EN and FLT_MODE pins are ignored. Settings in the CONTROL register are used instead.

Note: The first row of the register tables below shows the read/write type, and default state. At power-on-reset (POR), all bits in both registers are set to LOW internally.

STATE REGISTER

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W – 0
0	0	0	0	RF4	RF3	RF2	RF1
bit 7							bit 0

bit 7: **Low**
Set this bit low.
bit 6: **Low**
Set this bit low.
bit 5: **Low**
Set this bit low.
bit 4: **Low**
Set this bit low.
bit 3: **RF4**
1 = RFC to RF4 is Enabled
0 = RFC to RF4 is Disabled
bit 2: **RF3**
1 = RFC to RF3 is Enabled
0 = RFC to RF3 is Disabled
bit 1: **RF2**
1 = RFC to RF2 is Enabled
0 = RFC to RF2 is Disabled
bit 0: **RF1**
1 = RFC to RF1 is Enabled
0 = RFC to RF1 is Disabled

CONTROL REGISTER

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W – 0
WR_EN	FSTAT	SLEEP	FLTMODE	VPPCOMP	X	CPEN	X
bit7							bit 0

bit 7: **WR_EN**
1 = Enable write mode
0 = Disable Write mode (read only)

bit 6: **FSTAT**[11]
1 = VPP OR VDD Fault status = faulted
0 = VPP OR VDD Fault status = NOT faulted

bit 5: **SLEEP**[12]
1 = SLEEP mode active (all analog circuits disabled)
0 = SLEEP mode inactive (all analog circuits enabled)

bit 4: **FLTMODE**
1 = Fault Mode Disabled (shutdown Disabled)
0 = Fault Mode Enabled (shutdown Enabled)

bit 3: **VPPCOMP**
1 = VPP under-voltage comparator is disabled
0 = VPP under-voltage comparator is active

bit 2: **Do Not Care**
This bit can be set to either state without effecting performance.

bit 1: **CPEN**
1 = Charge Pump is enabled
0 = Charge Pump is disabled

bit 0: **Do Not Care**
This bit can be set to either state without effecting performance.

---

[11] VPP and VDD faults are latched. Once this bit is set high, it must be written to 0 to clear the fault.
[12] The SLEEP bit is forced low in GPIO mode.

Daisy Chain Operation

Daisy chaining the ICs is permitted and involves connecting the SDO of one chip to the SDIN of the next chip in the chain, as shown in Figure 5. SPI timing diagrams with daisy-chained devices are provided in Figure 6 and Figure 7.

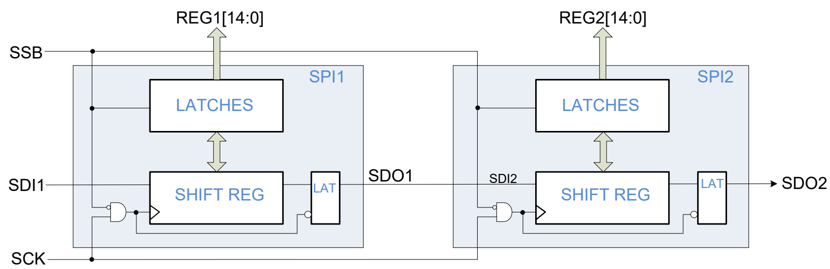


Figure 5: SPI with 2 ICs Daisy-chained

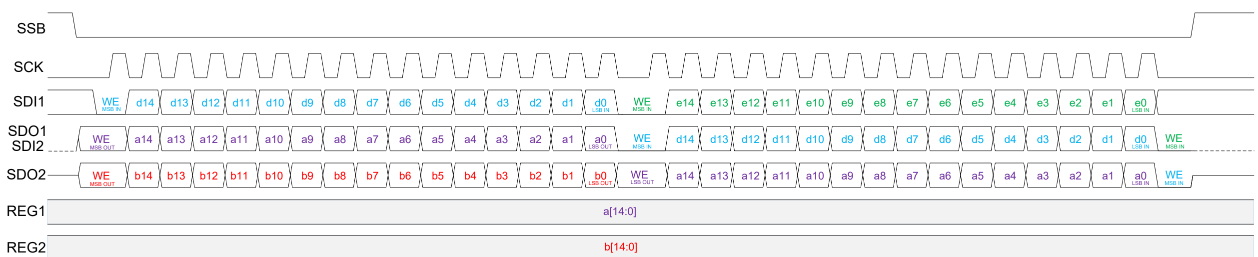


Figure 6: SPI Read Only (2 ICs Daisy-chained)

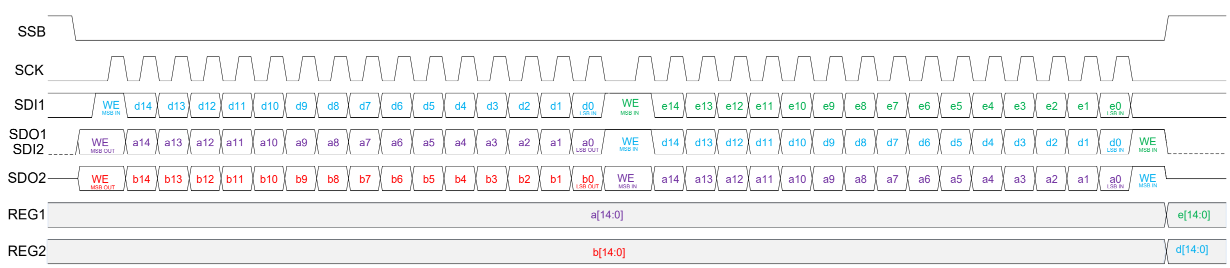


Figure 7: SPI Read & Write (2 ICs Daisy-chained)

GPIO Communication

MODE = 1 activates the GPIO (General Purpose Input Output or Parallel Mode) Communication Mode. In this mode of operation, the SPI Interface pins act as parallel inputs, as described in the Detailed Pin Description Table 7.

Table 8 Switch State Table in GPIO Mode

#	FLIP_BIT	CTL4	CTL3	CTL2	CTL1	RF4	RF3	RF2	RF1
0	1	0	0	0	0	OFF	OFF	OFF	OFF
1	1	0	0	0	1	OFF	OFF	OFF	**ON**
2	1	0	0	1	0	OFF	OFF	**ON**	OFF
3	1	0	0	1	1	OFF	**ON**	OFF	OFF
4	1	0	1	0	0	**ON**	OFF	OFF	OFF
5	1	0	1	0	1	OFF	OFF	OFF	OFF
6	1	0	1	1	0	OFF	OFF	OFF	OFF
7	1	0	1	1	1	OFF	OFF	OFF	OFF
8	1	1	0	0	0	OFF	OFF	OFF	OFF
9	1	1	0	0	1	**ON**	OFF	OFF	**ON**
10	1	1	0	1	0	OFF	**ON**	**ON**	OFF
11	1	1	0	1	1	**ON**	OFF	**ON**	OFF
12	1	1	1	0	0	**ON**	OFF	**ON**	OFF
13	1	1	1	0	1	**ON**	OFF	**ON**	OFF
14	1	1	1	1	0	OFF	**ON**	OFF	**ON**
15	1	1	1	1	1	OFF	OFF	OFF	OFF

#	FLIP_BIT	CTL4	CTL3	CTL2	CTL1	RF4	RF3	RF2	RF1
16	0	0	0	0	0	OFF	OFF	OFF	OFF
17	0	0	0	0	1	OFF	OFF	OFF	**ON**
18	0	0	0	1	0	OFF	OFF	**ON**	OFF
19	0	0	0	1	1	OFF	OFF	**ON**	**ON**
20	0	0	1	0	0	OFF	**ON**	OFF	OFF
21	0	0	1	0	1	OFF	**ON**	OFF	**ON**
22	0	0	1	1	0	OFF	**ON**	**ON**	OFF
23	0	0	1	1	1	OFF	**ON**	**ON**	**ON**
24	0	1	0	0	0	**ON**	OFF	OFF	OFF
25	0	1	0	0	1	**ON**	OFF	OFF	**ON**
26	0	1	0	1	0	**ON**	OFF	**ON**	OFF
27	0	1	0	1	1	**ON**	OFF	**ON**	**ON**
28	0	1	1	0	0	**ON**	**ON**	OFF	OFF
29	0	1	1	0	1	**ON**	**ON**	OFF	**ON**
30	0	1	1	1	0	**ON**	**ON**	**ON**	OFF
31	0	1	1	1	1	**ON**	**ON**	**ON**	**ON**

Fault Conditions

There are two comparators[13] that can signal a fault condition - VDD under voltage fault and VPP under voltage fault. Faults are reported differently depending on the mode of communication - SPI or GPIO.

The outputs of the VDD and VPP fault comparators are logically OR'ed. The output of the OR gate controls the FLTB pin. FLTB is an open-drain output and is ON (low impedance) if either fault is detected. In SPI mode, bit 6 of the CONTROL register provides VDD and VPP fault status.

At start-up, the FLTB pin is held OFF (high impedance). It is allowed to change state only after each voltage goes past its Enable threshold (VDD goes higher than $UVLO_{RISE}$ and VPP goes higher than V_{EN}). This prevents a race condition at startup.

Once VDD and VPP go above their thresholds, the comparators monitoring VDD and VPP actively monitor for faults. If VDD goes below $UVLO_{FALL}$ or VPP goes below VPP_{DIS}, a fault condition is signaled by setting the FLTB pin low and the Fault Status bit high (bit 6 in the CONTROL register). The FLTB pin returns to an open state when the fault condition is cleared – the FSTAT bit remains latched high until it is cleared via a SPI write.

If Fault Mode is enabled (in GPIO mode, FLT_MODE pin = 0, in SPI mode, FLT_MODE bit = 0), the outputs are all set low and the charge pump is turned off. The user must toggle the CP_EN pin (GPIO mode) or the CPEN register bit (SPI mode) low and then high to re-start the device.

If Fault Mode is disabled (in GPIO mode, FLT_MODE pin = 1; in SPI mode, FLT_MODE bit = 1), no action is taken by the IC. The fault condition is reported but does not affect the charge pump operation or switch states.

[13] The VPP under voltage comparator can be disabled. In SPI mode, it is disabled when the VPPCOMP bit in the CONTROL register is high. In GPIO mode, the comparator is disabled when CP_EN pin is set low.

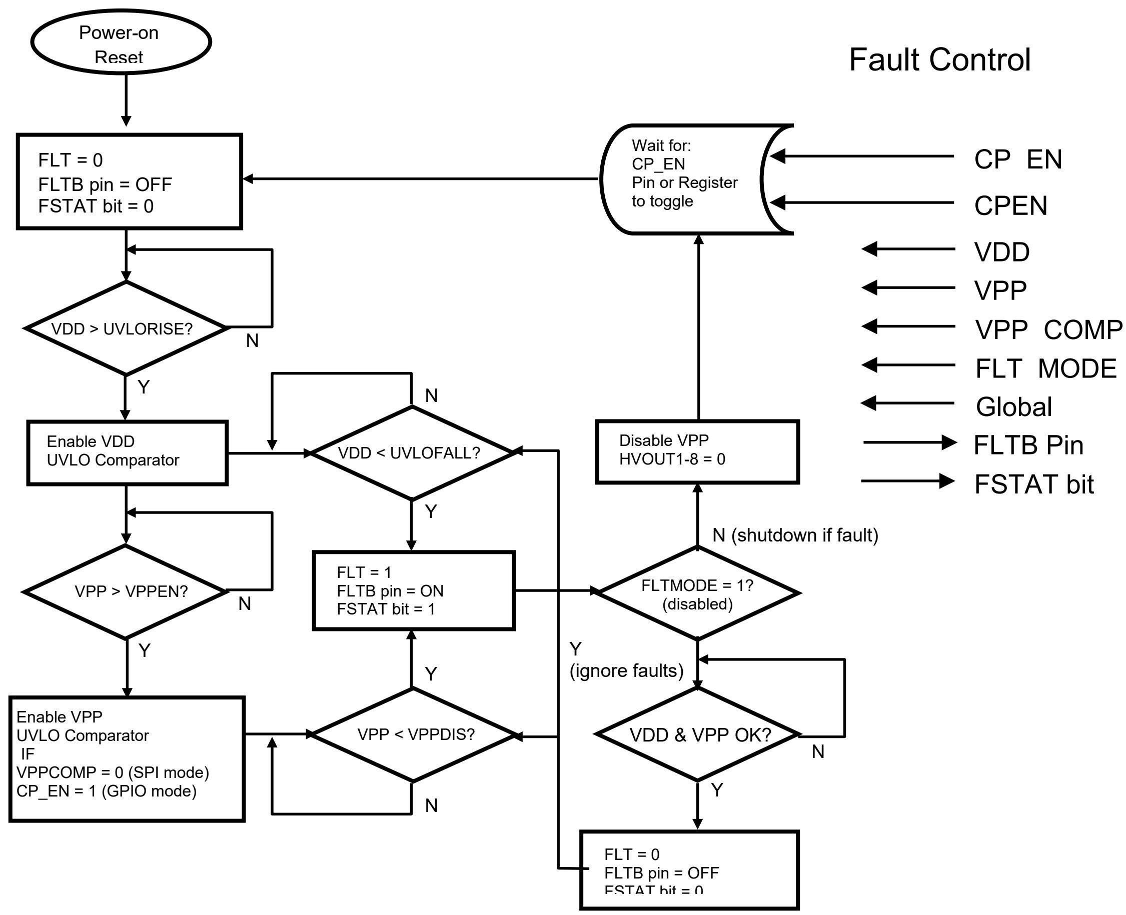


Figure 3: Flowchart for Fault

Notes:

1) The un-faulted supply continues to be monitored when a fault occurs. The FLT signal remains faulted until both supplies are above their brownout trip level.
2) VDD_IO is not monitored unless it is connected to VDD.
3) VPP is not monitored if: VPPCOMP = 1 in SPI mode OR the CP_EN pin is low In GPIO mode.

External Circuitry

The MM5120's internal driver requires external circuitry to operate its charge pump. The diagram below shows the suggested bypass capacitors that have been used with good results. Menlo Micro recommends selecting components with equal or better performance.

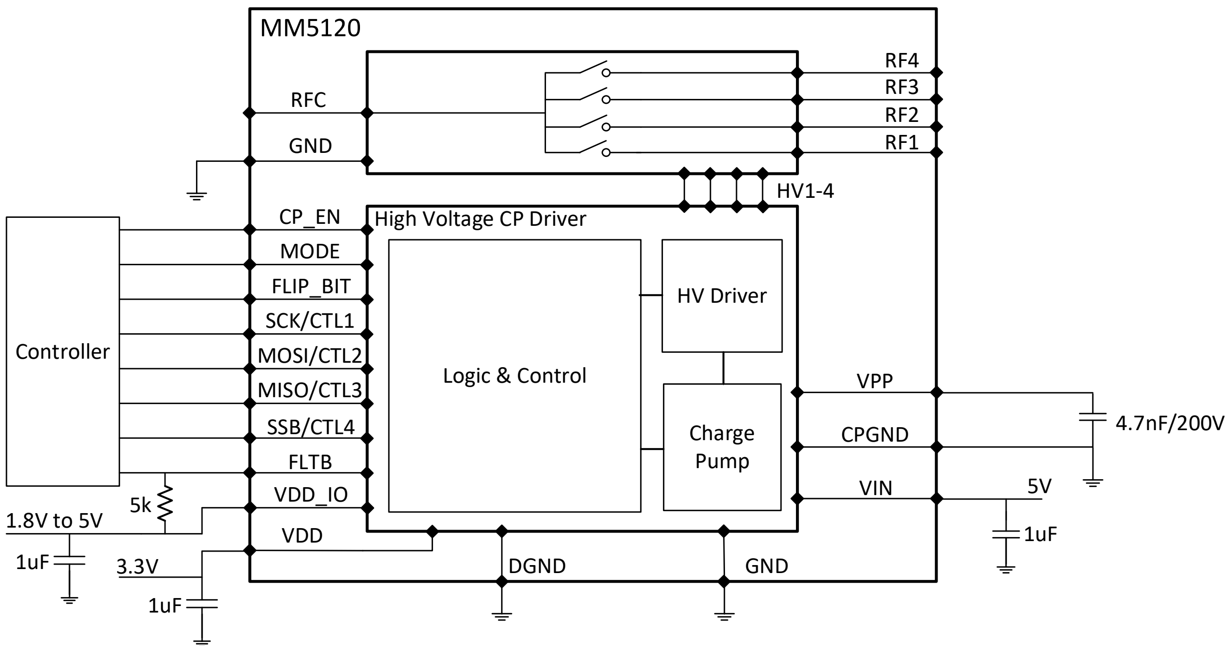
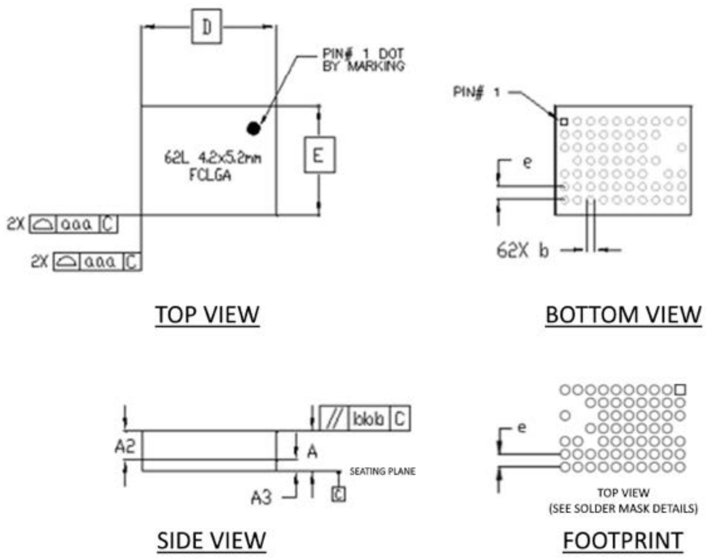


Figure 8: MM5120 Application Diagram

Package Drawing

62 Pin LGA Package

Dimensions are given in millimeters.



Dimensional Tol.	
aaa	0.100
bbb	0.100

Dimensional Ref.			
REF.	Min.	Nom	Max.
A	-	-	1.772
A2	-	-	1.325
A3	0.365	0.406	0.447
D	5.200 BSC		
E	4.200 BSC		
b	0.270	0.300	0.330
e	0.500 BSC		

Figure 9: Package Drawing

The pin array is located symmetrically on the package body as specified in JEDEC Design Guide 4.25B for JEDEC LGA.

Solder Mask Details

Dimensions are given in millimeters.

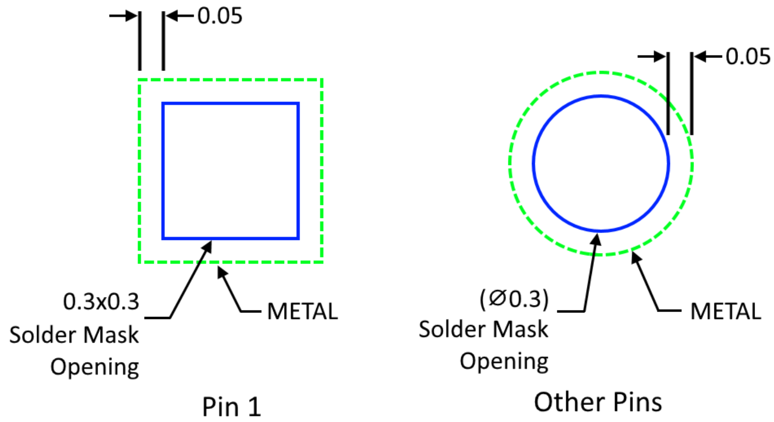


Figure 10: Solder Mask Details

Recommended PCB layout and SMT Parameters

- Use solder mask defined pads to allow a solid grounding plane under the part.
  - See Package Drawing for recommended solder mask opening.
- Open space around the package can have grounded thru holes.
- Use Type 5 solder paste.

Figure 11 below shows an example layout. This example uses a Rogers 4350b core with a thickness of 254 microns. 50Ω coplanar waveguide transmission lines are used to route the RF, with a trace thickness of 383 microns, and ground spacing of 152 microns.

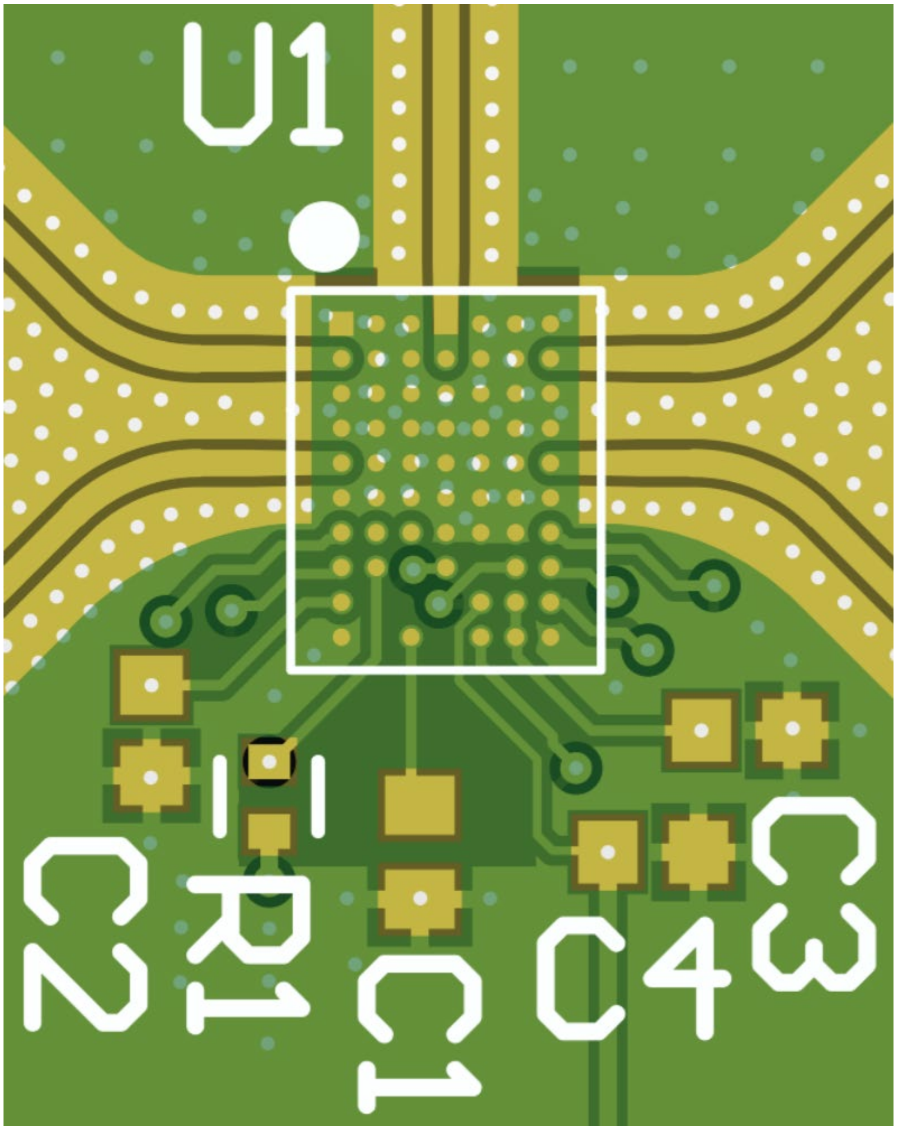


Figure 11: Example PCB Layout

Recommended Solder Reflow Profile

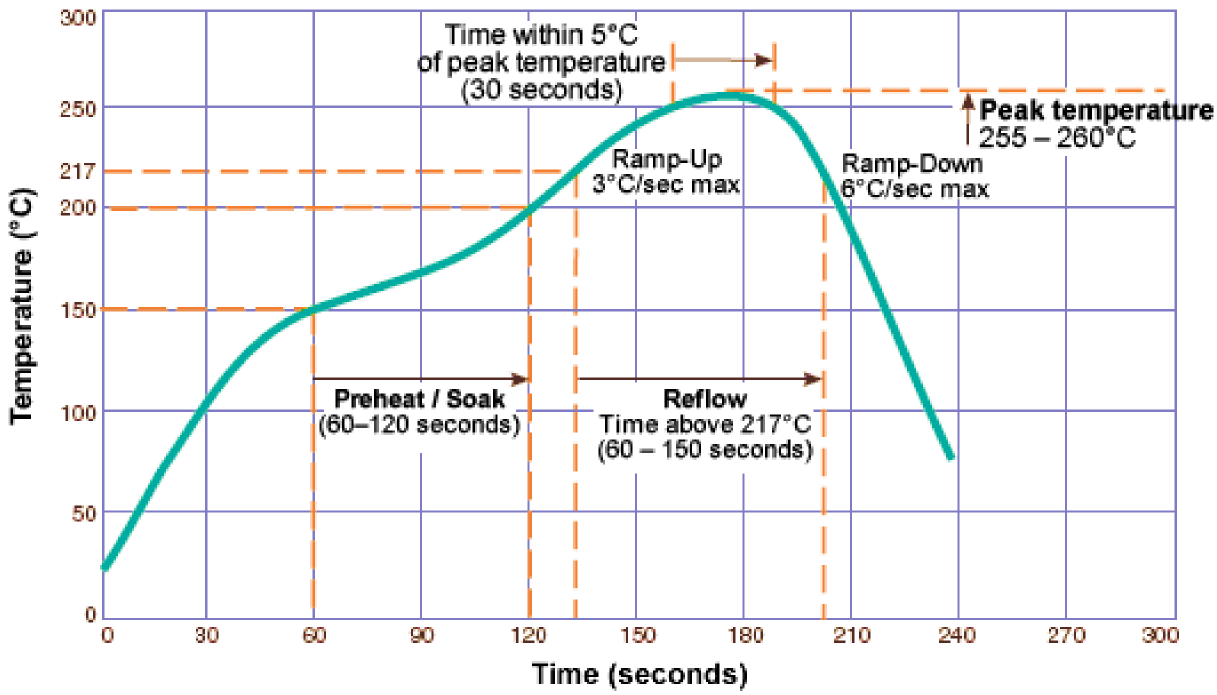


Figure 12: Recommended Reflow Profile

A ROHS compliant Solder Alloy used is SAC alloy: 96.5% Sn, 3.0%Ag, 0.5%Cu. These are the nominal percentages of the components. This alloy is designed to replace SnPb solders to eliminate Lead (Pb) from the process, requiring a higher reflow temperature. Moisture resistance performance may be impacted if not using the Pb-Free reflow conditions.

Follow Moisture Sensitivity Level (MSL) 3 handling precautions specified in IPC/JEDEC J-STD-020.

Storage and Shelf Life

Under typical industry storage conditions (≤30 °C/60% RH) in Moisture Barrier Bags:

- Customer Shelf Life: 24 months from customer receipt date
- Extended Shelf Life: 60 months from customer receipt date if re-bagged every 32 months or less.

Package Materials Information

Tape and reel details will be included in a future revision.

Package Options and Ordering Information

Part Number	ECCN	Package	Temp Range	Device Marking [14]
MM5120-01NDB **MM5120-01NDB-TR**	EAR99	DC-18GHz - SP4T - 5mm x 4mm LGA Industrial Temp with 3B Cycles Mechanical Endurance at 25°C DC-18GHz - SP4T - 5mm x 4mm LGA Industrial Temp with 3B Cycles Mechanical Endurance at 25°C. Tape and Reel (Qty 250)	-40°C to +85°C	BExxxxx
MM5120-01NDC **MM5120-01NDC-TR**	EAR99	DC-18GHz - SP4T - (high temp cycling) 5mm x 4mm LGA Industrial Temp with 3B Cycles Mechanical Endurance at 85°C DC-18GHz - SP4T - (high temp cycling) 5mm x 4mm LGA. Industrial Temp with 3B Cycles Mechanical Endurance at 85°C,Tape and Reel (Qty 250)	-40°C to +85°C	BExxxxx
MM5120EVK	EAR99	Evaluation Board MM5120 <18 GHz		

[14] Additional markings may be present, including logo or lot trace code information. This information may be a 2D barcode or other human-readable markings. Note that 'x' is place holder for 5-digit numerical code.

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