MP6539C

80V, Three-Phase BLDC Motor Pre-Driver

DESCRIPTION

The MP6539C is a gate driver IC designed for three-phase brushless DC (BLDC) motor driver applications. It is capable of driving three half-bridges consisting of six N-channel power MOSFETs, up to 80V.

The MP6539C uses a bootstrap (BST) capacitor (C_{BST}) to generate a supply voltage for the high-side MOSFET (HS-FET) driver. An internal charge pump maintains the high-side (HS) gate drive if the output is held high for an extended period.

Internal safety features include shoot-through protection, adjustable dead-time (DT) control, under-voltage lockout (UVLO), and thermal shutdown.

The MP6539C is similar to the MP6539 but does not include automatic BST charging or over-current protection (OCP). The MP6539C removes the VIN and LDO pins, and is only powered from the VDD pin.

The MP6539C is available in a QFN-28 (4mmx5mm) package with an exposed thermal pad.

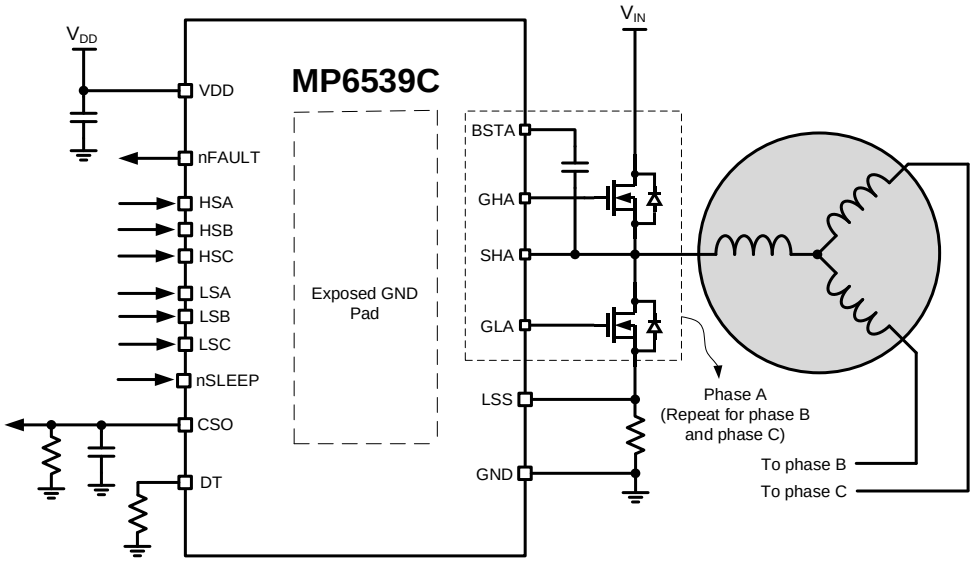
FEATURES

- Supports Up to 80V Operation
- 100V Maximum Bootstrap (BST) Voltage (V_{BST})
- Integrated Current-Sense Amplifier
- Low-Power Sleep Mode for Battery-Powered Applications
- Adjustable Dead-Time (DT) Control to Prevent Shoot-Through
- Thermal Shutdown and Under-Voltage Lockout (UVLO) Protection
- Fault Indication Output
- Available in a Thermally Enhanced, Surface-Mount Package
- Available in a QFN-28 (4mmx5mm) Package

APPLICATIONS

- Three-Phase Brushless DC (BLDC) Motors and Permanent Magnet Synchronous Motors (PMSMs)
- Power Drills
- E-Bikes

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP6539CGV*	QFN-28 (4mmx5mm)	*See Below*	2

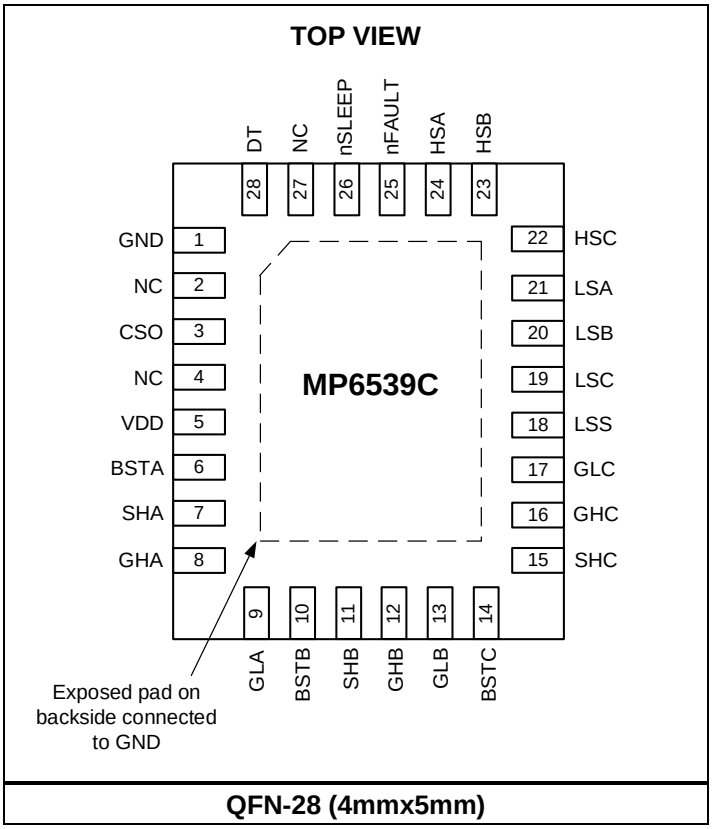
* For Tape & Reel, add suffix -Z (e.g. MP6539CGV-Z).

TOP MARKING

MPSYWW
M6539C
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
M6539C: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



QFN-28 (4mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	GND	**Ground.**
2	NC	**No connection.**
3	CSO	**Current-sense output.**
4	NC	**No connection.**
5	VDD	**Gate driver supply voltage.**
6	BSTA	**Bootstrap output of phase A.**
7	SHA	**High-side (HS) source connection of phase A.**
8	GHA	**HS gate drive of phase A.**
9	GLA	**Low-side (LS) gate drive of phase A.**
10	BSTB	**Bootstrap output of phase B.**
11	SHB	**HS source connection of phase B.**
12	GHB	**HS gate drive of phase B.**
13	GLB	**LS gate drive of phase B.**
14	BSTC	**Bootstrap output of phase C.**
15	SHC	**HS source connection of phase C.**
16	GHC	**HS gate drive of phase C.**
17	GLC	**LS gate drive of phase C.**
18	LSS	**LS source connection.**
19	LSC	**LS input of phase C.**
20	LSB	**LS input of phase B.**
21	LSA	**LS input of phase A.**
22	HSC	**HS input of phase C.**
23	HSB	**HS input of phase B.**
24	HSA	**HS input of phase A.**
25	nFAULT	**Fault indication.** The nFAULT pin is the open-drain output. nFAULT is pulled logic low if a fault condition occurs.
26	nSLEEP	**Sleep mode input.** Pull the nSLEEP pin logic low to enter low-power sleep mode; pull the pin high to enable the device. nSLEEP has an internal pull-down resistor.
27	NC	**No connection.**
28	DT	**Dead-time setting.**

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{DD}), GLA, GLB, or GLC ..... -0.3V to +14.5V
BSTA, BSTB, or BSTC ..... -0.3V to +100V
GHA, GHB, or GHC ..... -0.3V to (BST - SH) + 0.3V
GHA, GHB, or GHC (transient, 2µs) ..... -8V to (BST - SH) + 0.3V
LSS ..... -0.3V to +4V
LSS (transient, 2µs) ..... -1V to +4V
SHA, SHB, or SHC ..... -5V to +90V
SHA, SHB, or SHC (transient, 2µs) ..... -8V to +90V
All other pins to GND ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-28 (4mmx5mm)..... 3.1W
Storage temperature ..... -55°C to +150°C
Junction temperature (T_J) ..... 150°C
Lead temperature (solder) ..... 260°C

Recommended Operating Conditions (3)

Motor voltage (V_{IN})..... 8V to 80V
Input voltage (V_{DD})..... 8.5V to 14V
Operating junction temp (T_J)..... -40°C to +150°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-28 (4mmx5mm)..... 40 ..... 9.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Gate driver supply voltage	V_{DD}		8.5		14	V
Quiescent current	I_Q	nSLEEP = 1, not switching		1.1		mA
	I_{SLEEP}	nSLEEP = 0		2		µA
Control Logic						
Input logic low threshold	V_{IL}				0.8	V
Input logic high threshold	V_{IH}		2			V
Logic input current	I_{IN_H}	V_{IH} = 0.8V	-2.4		+2.4	µA
	I_{IN_L}	V_{IL} = 5V	-14		+14	µA
nSLEEP pull-down resistance	R_{PD_SLEEP}			500		kΩ
Internal pull-down resistance	R_{PD}			500		kΩ
Fault Output (Open-Drain Output)						
Output low voltage	V_{OL}	I_{OUT} = 5mA			0.15	V
Output high leakage current	I_{OH}	V_{OUT} = 3.3V			1	µA
Protection Circuits						
V_{DD} under-voltage lockout (UVLO) rising threshold	$V_{DD\_UVLO\_RISING}$		6.3	7.3	8.3	V
V_{DD} UVLO falling threshold	$V_{DD\_UVLO\_FALLING}$		6	6.8	7.6	V
V_{DD} UVLO hysteresis	V_{DD_HYS}			500		mV
Bootstrap (BST) voltage (V_{BST}) UVLO threshold	V_{BST_UVLO}	Voltage between the SHx and BSTx pins		6.4		V
Wake-up time from sleep mode	t_{WAKE}	At nSLEEP rising		70		µs
Thermal shutdown (5)	T_{TSD}			178		°C
Thermal shutdown hysteresis (5)	T_{TSD_HYS}			30		°C
Gate Drive						
BST diode forward voltage	V_{FWD_BST}	I_D = 10mA			1.2	V
		I_D = 50mA			2.3	V
Maximum source current (5)	I_{SOURCE}			0.8		A
Maximum sink current (5)	I_{SINK}			1		A
Gate drive pull-up resistance	R_{UP}	V_{DS} = 1V		7		Ω
High-side (HS) gate drive pull-down resistance	R_{HS_DOWN}	V_{DS} = 1V	0.5		5.5	Ω
Low-side (LS) gate drive pull-down resistance	R_{LS_DOWN}	V_{DS} = 1V	0.5		5.5	Ω

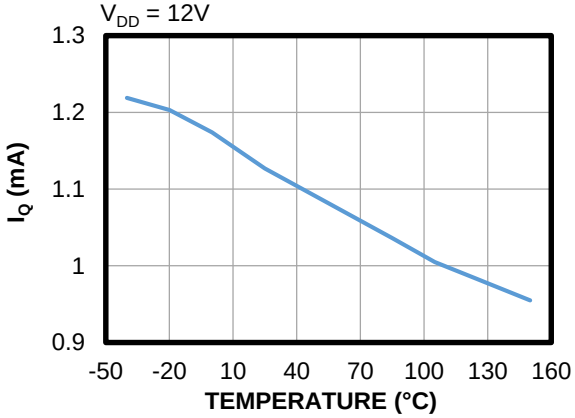
Note:

5) Guaranteed by design.

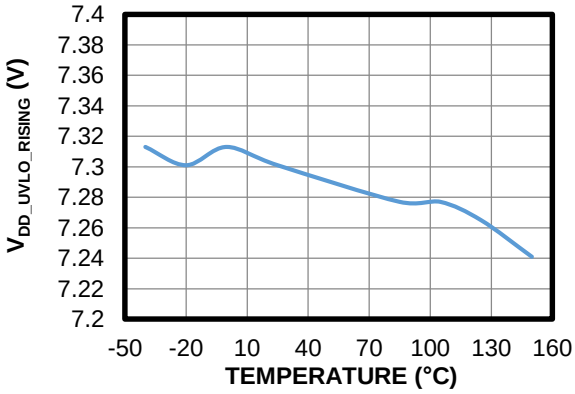
TYPICAL CHARACTERISTICS

Quiescent Current vs. Temperature

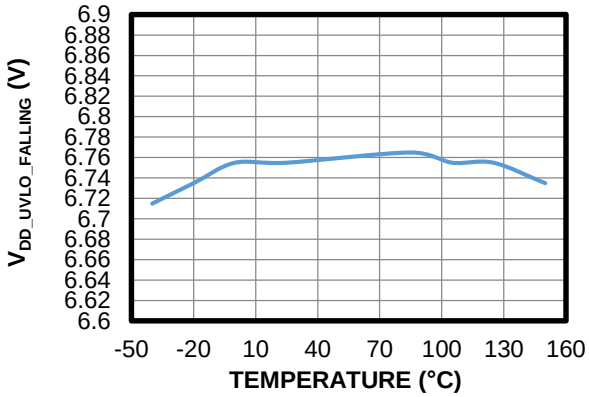
V_{DD} = 12V



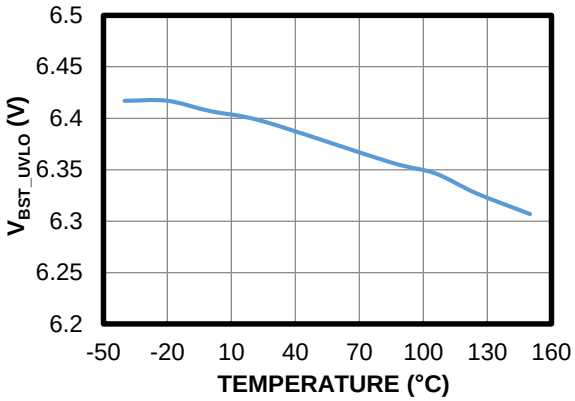
V_{DD} UVLO Rising Threshold vs. Temperature



V_{DD} UVLO Falling Threshold vs. Temperature



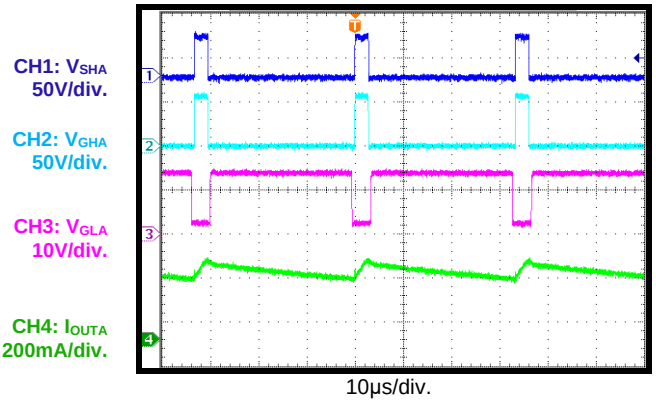
V_{BST} UVLO Threshold vs. Temperature



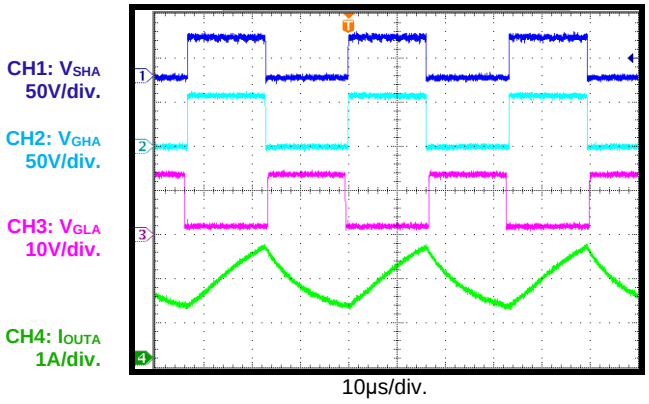
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, V_{DD} = 12V, phase A switching, phase B's LS gate drive on, f_{PWMA} = 30kHz, T_A = 25°C, resistor + inductor load: 5Ω + 1mH/phase with a star connection, unless otherwise noted.

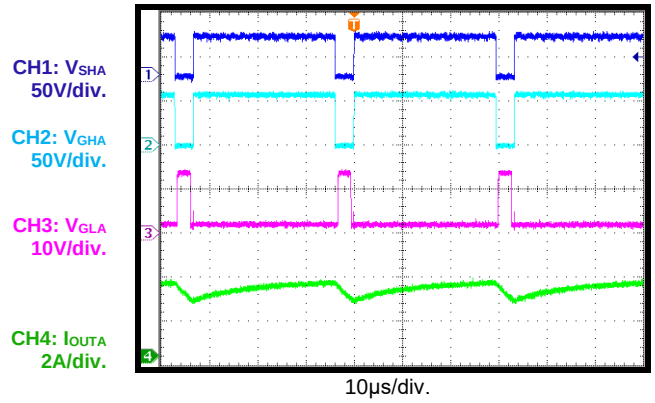
Steady State
Duty = 10%



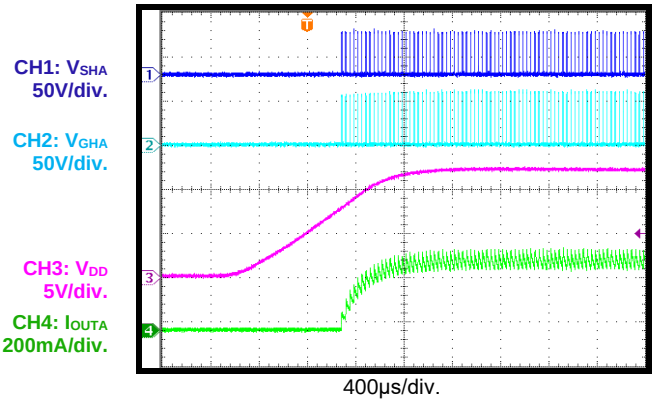
Steady State
Duty = 50%



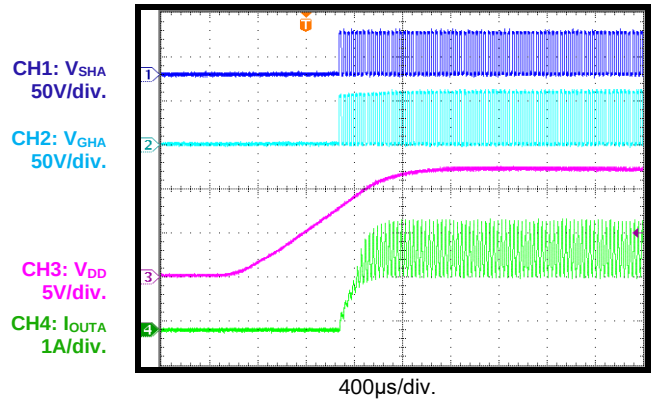
Steady State
Duty = 90%



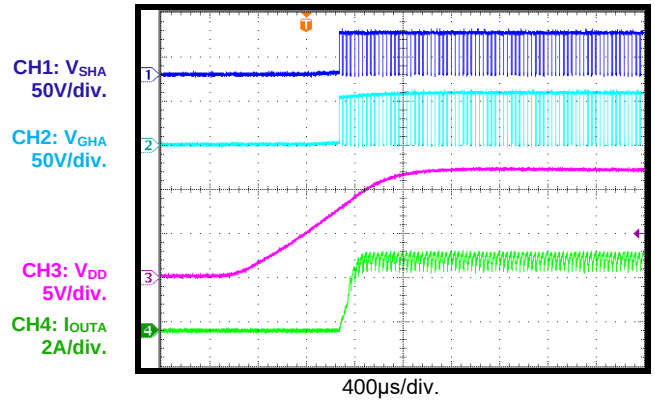
Power Ramping Up
Duty = 10%



Power Ramping Up
Duty = 50%



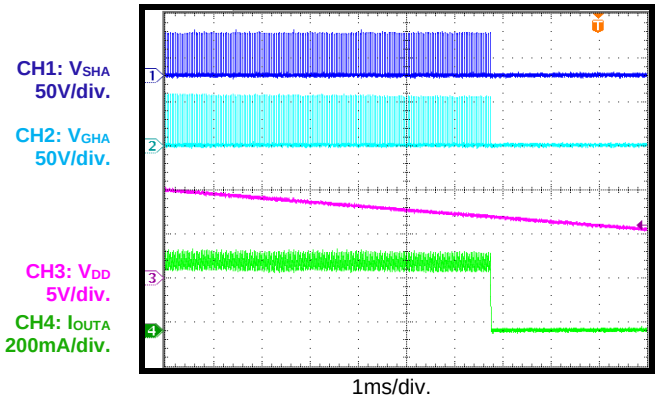
Power Ramping Up
Duty = 90%



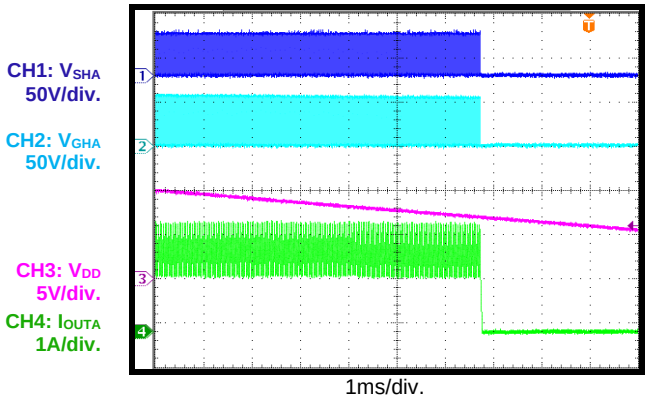
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{DD} = 12V, phase A switching, phase B's LS gate drive on, f_{PWMA} = 30kHz, T_A = 25°C, resistor + inductor load: 5Ω + 1mH/phase with a star connection, unless otherwise noted.

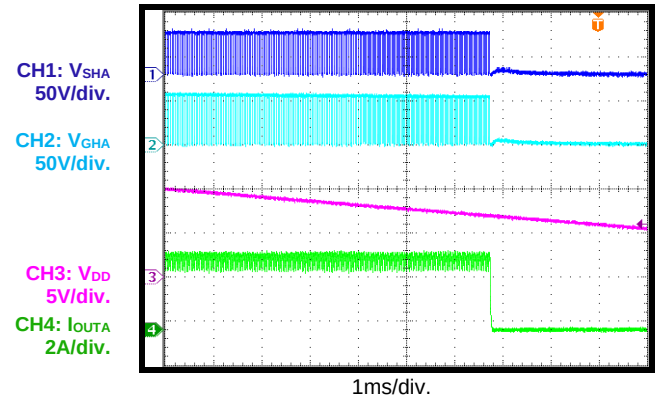
Power Ramping Down
Duty = 10%



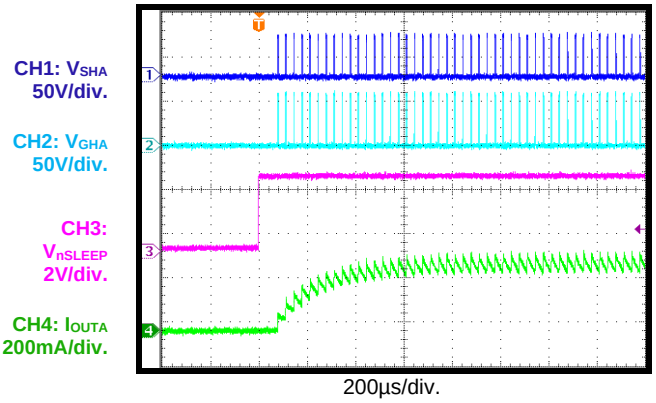
Power Ramping Down
Duty = 50%



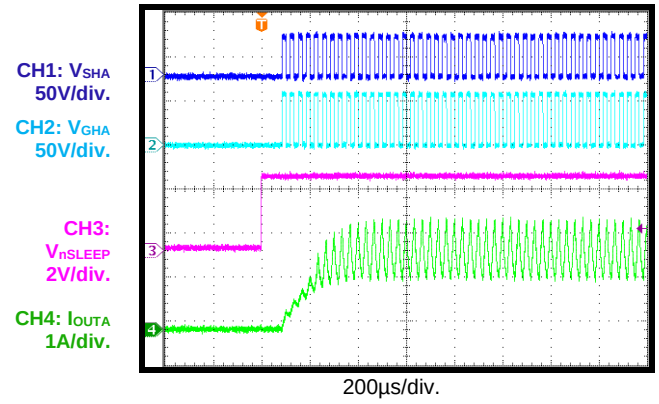
Power Ramping Down
Duty = 90%



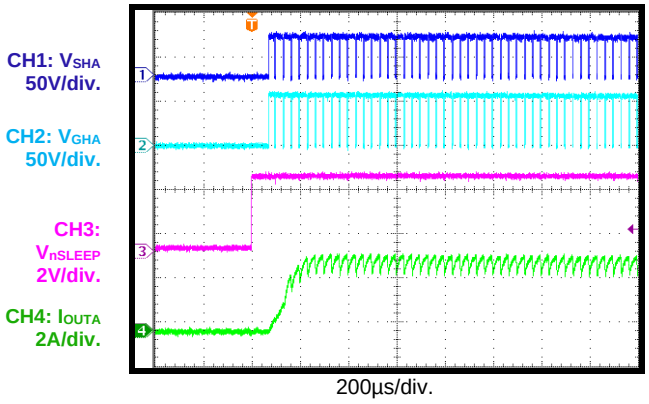
Sleep Recovery
Duty = 10%



Sleep Recovery
Duty = 50%



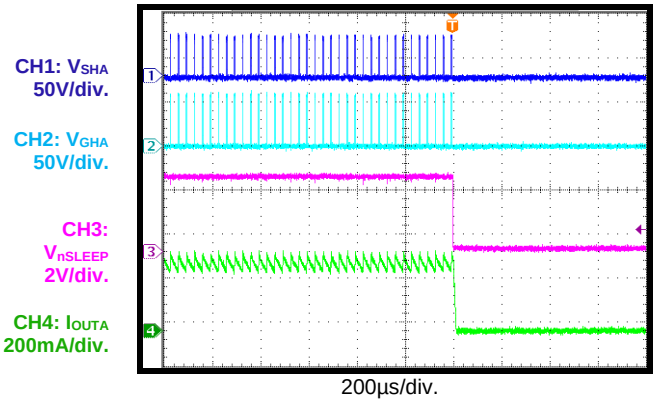
Sleep Recovery
Duty = 90%



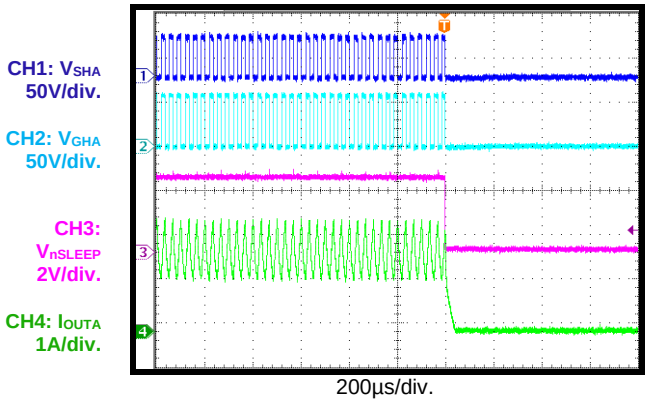
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{DD} = 12V, phase A switching, phase B's LS gate drive on, f_{PWMA} = 30kHz, T_A = 25°C, resistor + inductor load: 5Ω + 1mH/phase with a star connection, unless otherwise noted.

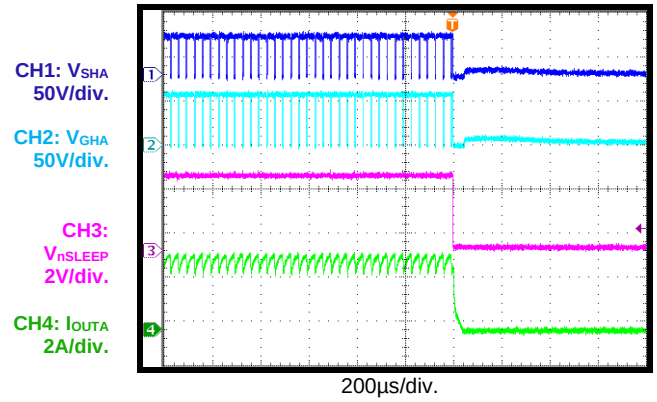
Sleep Entry
Duty = 10%



Sleep Entry
Duty = 50%



Sleep Entry
Duty = 90%



FUNCTIONAL BLOCK DIAGRAM

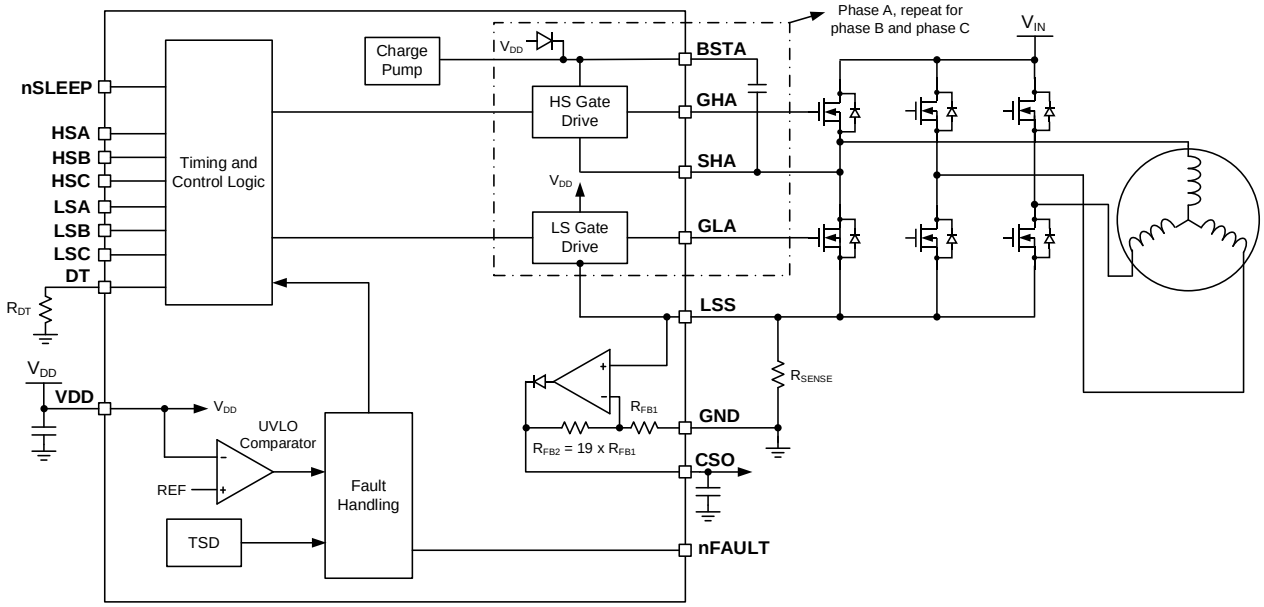


Figure 1: Functional Block Diagram

OPERATION

The MP6539C is a three-phase, brushless DC (BLDC) motor pre-driver that drives three half-bridges with 0.8A source current and 1A sink current capability. It can operate across a motor supply voltage range up to 80V. The MP6539C features low-power sleep mode, which disables the device and draws a very low supply current.

Start-Up Sequence

Apply a voltage to VDD to initiate the start-up sequence. V_{DD} must exceed the 7.3V V_{DD} under-voltage lockout (UVLO) threshold to initiate start-up.

It is recommended to pull each output low to provide an initial charge to the bootstrap (BST) capacitors (C_{BST}) before pulling an output high. The MP6539C does not perform this BST charge automatically.

The start-up process takes about 70µs. Once start-up is complete, the MP6539C responds to logic inputs and drives the outputs.

Input Logic

Pull the nSLEEP pin low to force the MP6539C into a low-power sleep state. In this state, all internal circuits are disabled. All inputs are ignored when nSLEEP is active low. To exit sleep mode, about 70µs must pass before issuing a pulse-width modulation (PWM) command to allow the internal circuitry to stabilize.

The HSx pin (where x = A, B, or C) controls the gate driver for the high-side MOSFET (HS-FET) of each phase. The LSx pin (where x = A, B, or C) controls the gate driver for the low-side MOSFET (LS-FET). A positive dead time (DT) is enforced by the device to prevent shoot-through. If both HSx and LSx are driven high or low, neither MOSFET is driven (see Table 1).

Table 1: Input Logic Truth Table

LSx	HSx	SHx
H	H	Hi-Z
H	L	GND
L	H	VIN
L	L	Hi-Z

nFAULT

nFAULT reports to the system if a fault condition, such as an over-temperature (OT) fault, is detected. nFAULT is an open-drain output and is pulled low if a fault condition occurs. Once the fault condition is removed, an external pull-up resistor pulls nFAULT high.

Current-Sense Amplifier

An integrated current-sense amplifier amplifies the voltage on LSS (relative to GND) by a factor of 20. This voltage is the output to the CSO pin.

The current-sense amplifier only sources current. A minimum 1nF external capacitor must be connected between CSO and ground for stability.

During the PWM on time, current flowing through the output MOSFETs also flows through the shared low-side (LS) current-sense resistor, generating a voltage that is amplified by the current-sense amplifier. This voltage charges the external capacitor on CSO. During the PWM off time, current recirculates through the LS-FETs and does not pass through the sense resistor, meaning there is 0V across the resistor. During this time, the capacitor discharges via the internal feedback resistor (about 450kΩ) as well as via any external resistor connected to ground. Select an external resistor and capacitor to provide a filter that holds the current sense during the PWM off time. The external resistor should be a minimum of 1kΩ.

If the current-sense amplifier is not used, connect LSS directly to ground.

Charge Pump and Bootstrap (BST)

The high-side (HS) gate drive voltage is typically generated from C_{BST}, which is connected between the SHx and BSTx pins (where x = A, B, or C). C_{BST} is charged whenever the LS-FET turns on.

If the output is held high for a long period, C_{BST} discharges slowly. This eventually results in gate driver loss for the HS-FET. To prevent this, an internal charge pump generates a voltage to maintain the C_{BST} charge.

The BST voltage (V_{BST}) is monitored by an under-voltage (UV) detection circuit. If V_{BST} drops below the V_{BST} UVLO threshold (V_{BST_UVLO}), its corresponding HS output is

disabled. V_{BST_UVLO} does not cause the nFAULT signal to be pulled low.

Dead-Time (DT) Adjustment

To prevent shoot-through in any of the bridge's phases, a dead time (t_{DEAD}) must be inserted between the HS-FET or LS-FET turning off and the next complementary turn-on event. t_{DEAD} for all three phases is set by a single dead-time resistor (R_{DT}) between the DT pin and ground, and it can be calculated with Equation (1):

$$t_{DEAD}\ (\mu s) = 0.044 \times R_{DT}\ (k\Omega) + 0.1 \quad (1)$$

If the DT pin is directly connected to GND, apply an internal minimum t_{DEAD} of 77ns. The 100kΩ maximum allowable resistance to ground generates a 4.5μs t_{DEAD}.

V_{DD} Under-Voltage Lockout (UVLO) Protection and Shutdown

If the voltage on VDD (V_{DD}) drops below the V_{DD} UVLO threshold, the outputs are disabled and the nFAULT signal asserts. Operation resumes when V_{DD} exceeds its UVLO threshold.

If V_{DD} drops below its UVLO threshold, the HS and LS outputs pull low to turn off the MOSFETs. As V_{DD} drops further, the outputs eventually enter high-impedance (Hi-Z) state. If V_{DD} turns off while the MOSFETs are powered, it is recommended to add external pull-down resistors between the gate and source of the MOSFETs.

Thermal Shutdown

If the die temperature exceeds safe limits, the MP6539C disables all gate drive outputs, and nFAULT pulls active low. Operation resumes automatically once the die temperature drops to a safe level.

APPLICATION INFORMATION

Comparing the MP6539 and MP6539C

The MP6539C is similar to the MP6539, aside from the following changes:

1. The VIN pin and its corresponding circuitry are removed. Power is only provided through the VDD pin, which was previously the VREG pin.
2. The automatic BST charging function at start-up is removed, which reduces the start-up time to about 70µs.
3. Over-current protection (OCP) and drain-to-source voltage (V_{DS}) sensing are removed. The only protection circuits implemented are V_{DD} UVLO, over-temperature protection (OTP), and V_{BST} UVLO.
4. Since there is no VIN pin, the gate drive outputs enter Hi-Z state once V_{DD} drops to 0V.

Bootstrap (BST) Components

The primary source of the charge to enable the HS-FETs is provided by C_{BST}. There are several considerations when selecting the size of these capacitors.

When the output is driven low, C_{BST} is charged from V_{DD} via an internal diode. To turn on the HS-FET, the charge in C_{BST} is transferred to the gate of the HS-FET to turn it on. If C_{BST} is too small, there is insufficient charge to fully enhance the MOSFET.

The minimum allowable C_{BST} depends on the HS-FET's total gate charge (Q_T), the internal BST diode forward voltage (V_{FWD_BST}), and the voltage drop tolerance from the VDD supply voltage (ΔV_{BOOT}) to enhance the MOSFET. C_{BST} can be calculated with Equation (2):

$$C_{BST} \geq Q_T / (\Delta V_{BOOT} - V_{FWD\_BST}) \quad (2)$$

It is recommended to use a capacitance that exceeds the minimum allowable C_{BST} by two to four times. It is also important to consider the capacitance change under bias conditions for ceramic capacitors.

For example, for a MOSFET with 50nC Q_T, 12V V_{DD}, and a minimum desired gate drive of 10V, C_{BST} is 62nF, where $C_{BST} \geq$ 50nC / (12V - 10V - 1.2V). Therefore, a 100nF or 220nF capacitor is sufficient.

If C_{BST} is too large, charging takes a very long time when the output is low due to the limited current sourcing capability via the BST diode. The total power dissipated in the BST diode can also be a concern.

Bootstrap (BST) Pre-Charge

At both start-up and whenever the device is disabled for some time, C_{BST} is discharged. Before attempting to drive an output high, C_{BST} must be pre-charged. This function is not automatically performed by the MP6539C.

Pre-charge is achieved by turning on each LS-FET, one at a time. This allows current to flow from VDD through the internal BST diode and the capacitor, then through the LS-FET.

If a large C_{BST} (exceeding 220nF) is used, pre-charge should be completed using multiple pulses at a 20% duty cycle to limit the amount of power dissipated in the BST diodes.

PCB Layout Guidelines

Efficient PCB layout is critical to optimize the performance of the MOSFET gate drivers. In particular, the connection between the HS source and LS drain must be as direct as possible to avoid a negative undershoot on the phase node due to parasitic inductance. The pre-driver is designed to accommodate a negative undershoot, but excessive negative undershoot can result in unstable operation or damage to the IC. For the best results, refer to Figure 2 and follow the guidelines below:

1. Use surface-mounted N-channel MOSFETs that allow for a very short connection between the HS-FET and LS-FET.
2. Use wide copper areas for all of the high-current paths.
3. Place the supply bypass capacitors very close to the IC.
4. Place multiple thermal vias under the exposed pad to improve thermal dissipation. This allows heat to move between the IC and a plane located on the backside of the PCB.

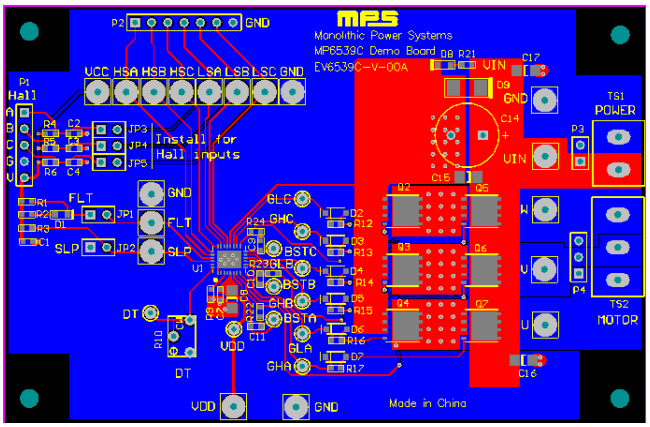


Figure 2: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

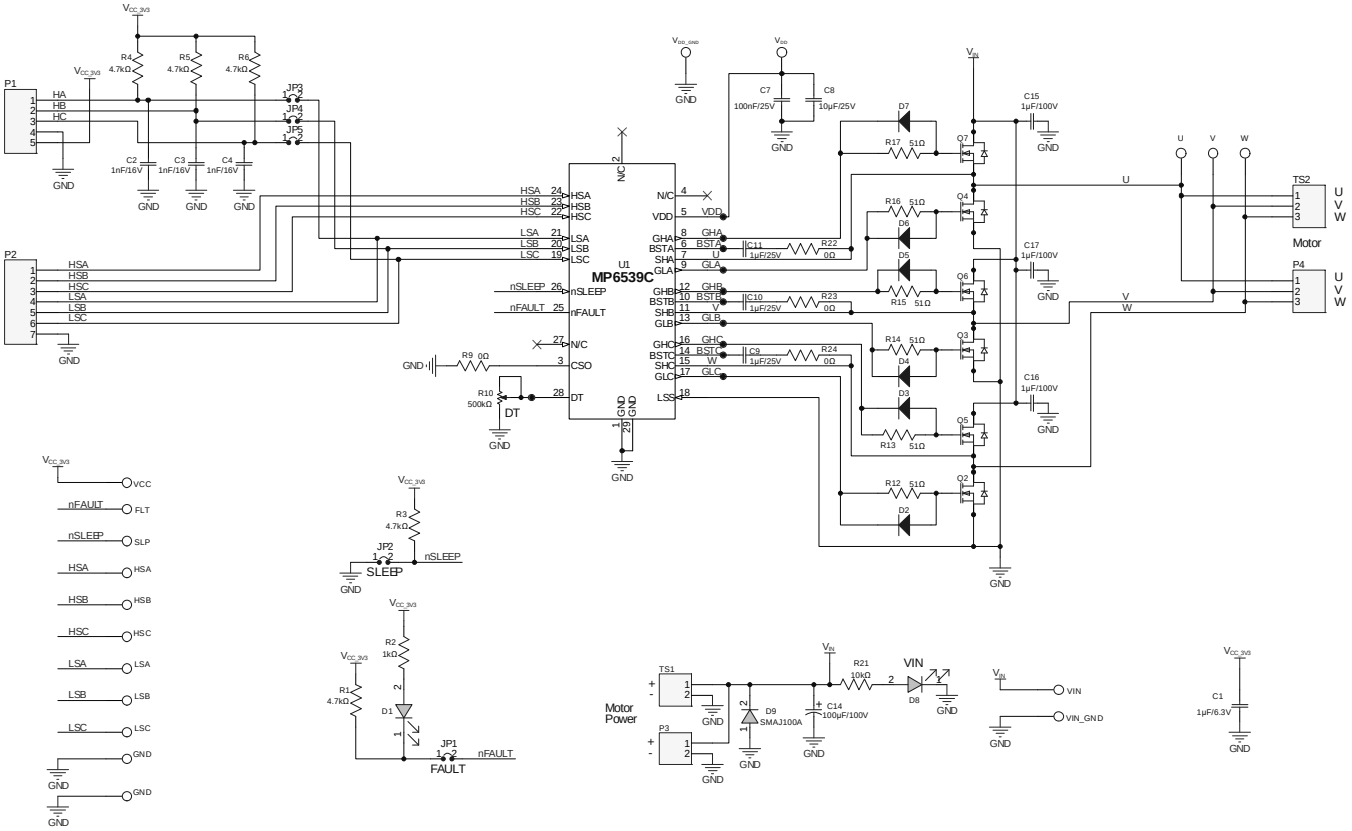
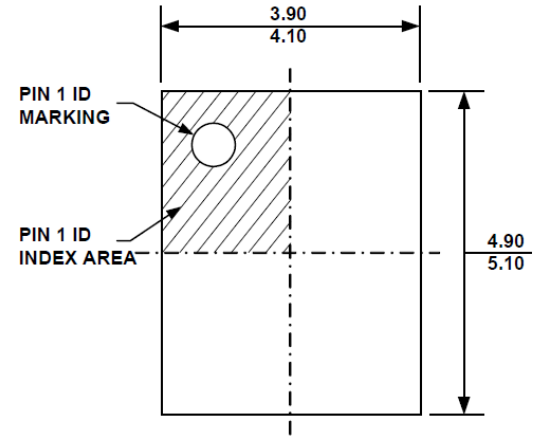


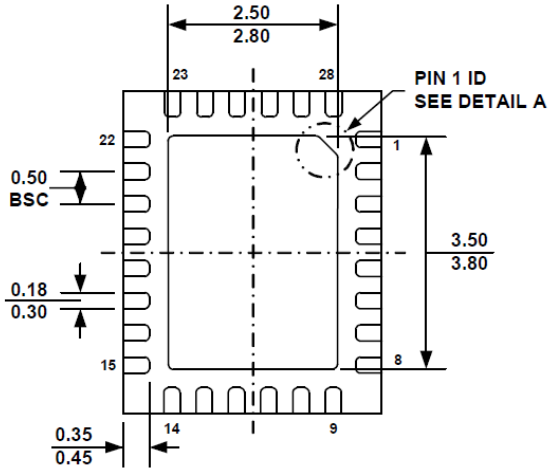
Figure 3: Typical Application Circuit

PACKAGE INFORMATION

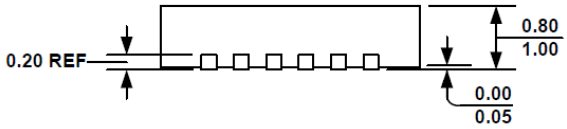
QFN-28 (4mmx5mm)



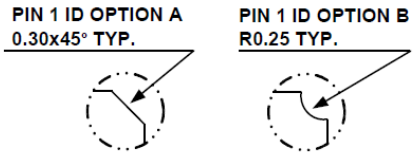
TOP VIEW



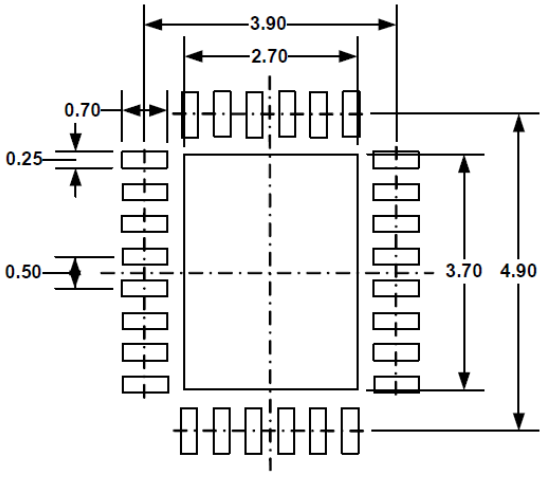
BOTTOM VIEW



SIDE VIEW



DETAIL A

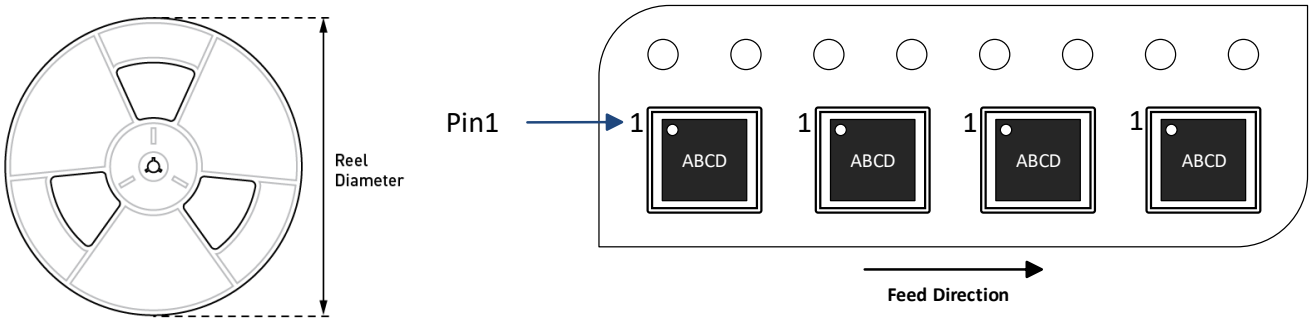


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VHGD-3.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6539CGV-Z	QFN-28 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/2/2024	Initial Release	-