MPQ8785

16V, 40A, Scalable, Digital, Synchronous Step-Down Converter with PMBus

DESCRIPTION

The MPQ8785 is a fully integrated, PMBus-compliant, high-frequency, synchronous buck converter. The MPQ8785 offers a very compact solution that achieves up to 40A of output current (I_{OUT}) per phase, with excellent load and line regulation across a wide input voltage (V_{IN}) supply range. The MPQ8785 operates at a high efficiency across the wide I_{OUT} load range.

The PMBus interface provides converter configurations and monitors key parameters.

The MPQ8785 adopts MPS's proprietary, digital, multi-phase constant-on-time (MCOT) control, which provides fast transient response and facilitates loop stabilization. The MCOT scheme also allows multiple MPQ8785 devices to be connected in parallel, with excellent current sharing and phase interleaving for high-current applications.

Fully integrated protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MPQ8785 requires a minimal number of readily available, standard external components, and it is available in a TLGA-37 (5mmx6mm) package.

FEATURES

- PMBus 1.3 Compliant
- Scalable Multi-Phase Operation
- 3.1V to 16V Input Voltage (V_{IN}) with External 3.3V VCC Bias
- Continuous 40A of Output Current (I_{OUT})
- Phase Redundancy to Ensure Uninterrupted Operation
- Lossless and Accurate On-Die Current Sensing with Auto-Matching

FEATURES *(continued)*

- Accurate Current Balance Control in Multi-Phase Operation
- Quiet Switcher™ Technology (QST) to Mitigate Switching Noise
- Fault Recording (BBOX) to Ease Failure Analysis
- Automatic PMBus Address Assignment to Provide Auxiliary Phase Data Reading
- Adaptive Multi-Phase Constant-On-Time (MCOT) Control for Ultra-Fast Transient Response
- Stable with Zero-ESR Output Capacitors
- 0.5% Reference Voltage (V_{REF}) Across 0°C to 85°C Junction Temperature (T_J) Range
- 1% V_{REF} Across -40°C to +125°C T_J Range
- Output Voltage (V_{OUT}) Adjustable from 0.35V to 0.9 x V_{IN}, Up to 5.5V Max
- V_{OUT}, I_{OUT}, V_{IN}, and T_J Reporting
- Built-In Multiple-Time Programmable (MTP) Memory to Store Custom Configurations with Cyclic Redundancy Check (CRC)/Check Sum
- Configurable via the PMBus:
  - V_{OUT}
  - I_{OUT} Limit
  - Soft-Start Time
  - Selectable 300kHz Up to 2MHz Switching Frequency (f_{SW})
  - Over-Current Protection (OCP), Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), and Over-Temperature Protection (OTP) with Options for Hiccup or Latch-Off Mode
  - Ramp Compensation
- Available in a TLGA-37 (5mmx6mm) Package

APPLICATIONS

- Telecom and Networking Systems
- Base Stations
- Servers

TYPICAL APPLICATIONS (1)

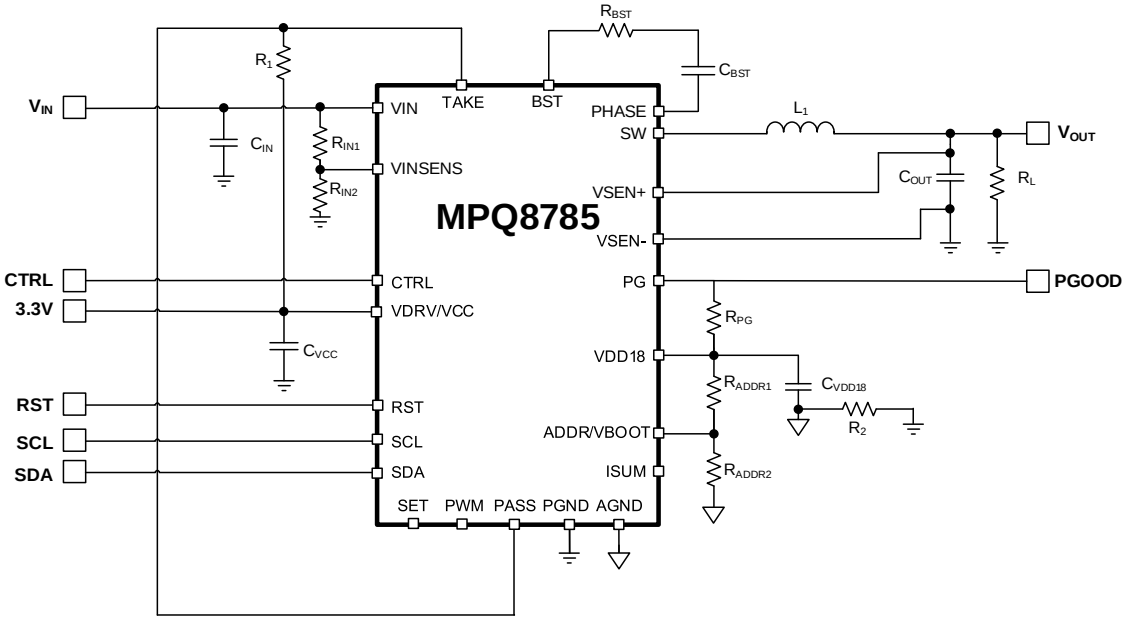


Figure 1: Single-Phase Operation

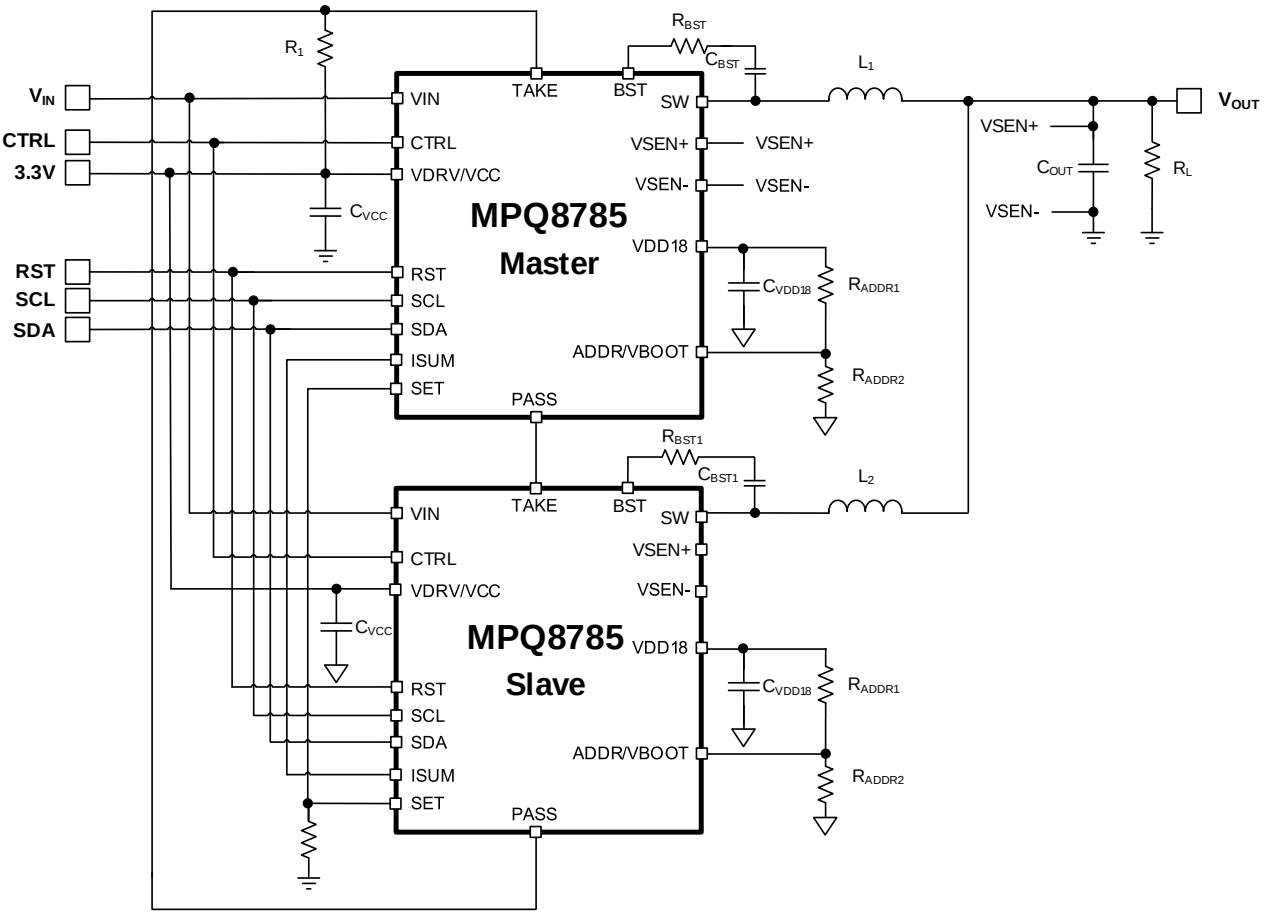


Figure 2: Dual-Phase Operation

TYPICAL APPLICATIONS *(continued)* (1)

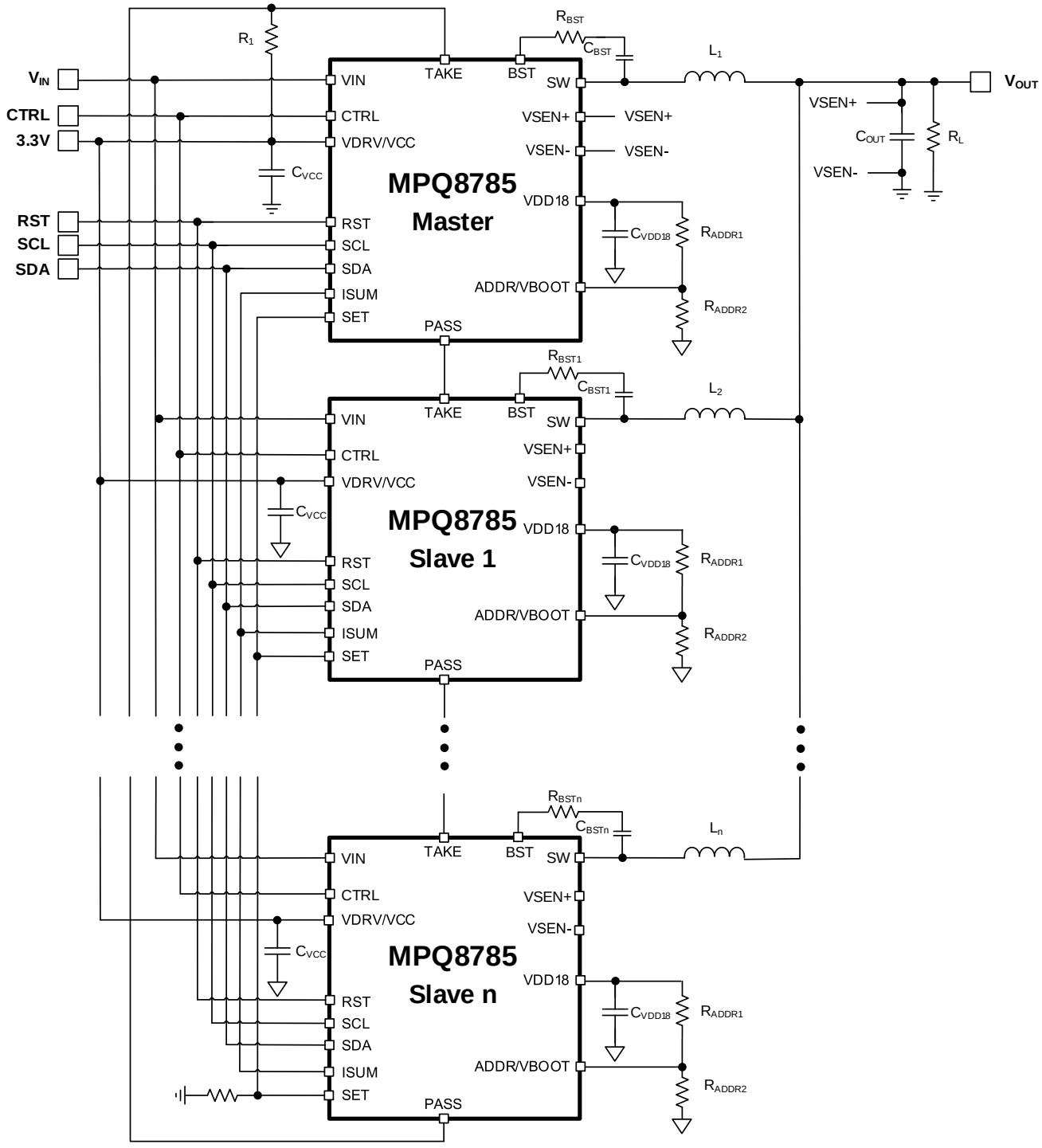


Figure 3: Multi-Phase Operation

Note:

1) The connection of VSNE+/VSEN- of slave phases are only needed when master fault skip feature is enabled.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ8785GMJT-xxxx**	TLGA-37 (5mmx6mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MPQ8785GMJT-xxxx-Z).

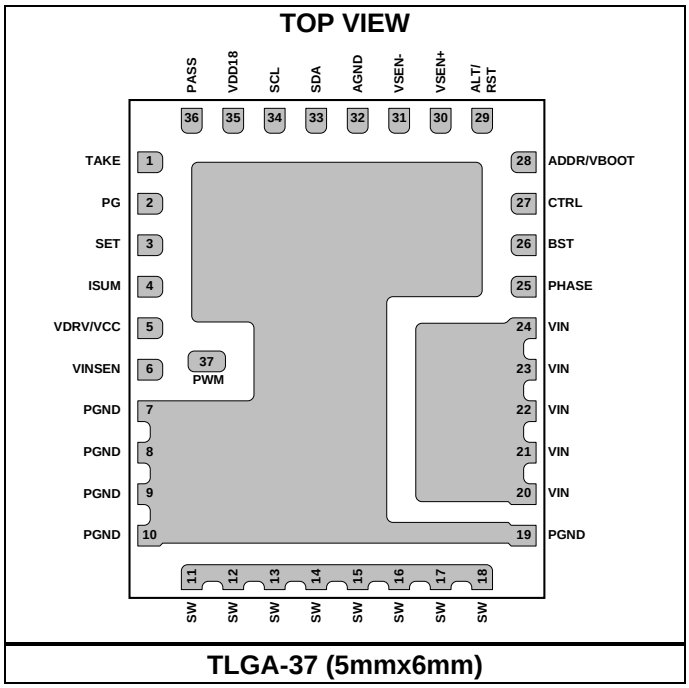
** “xxxx” is the configuration code identifier for the register settings stored in the MTP. The default number is “0000”. Each “x” is a hexadecimal value between 0 and F. The default code is “0000”. Work with an MPS FAE to create this unique number, even if ordering the “0000” code.

TOP MARKING

MPSYYWW
MP8785
LLLLLLL
T

MPS: MPS prefix
YY: Year code
WW: Week code
MP8785: First four digits of the part number
LLLLLLL: Lot number
T: Product code

PACKAGE REFERENCE



TLGA-37 (5mmx6mm)

PIN FUNCTIONS

Pin #	Name	Description
1	TAKE	**Receive the run signal from the previous phase.** The TAKE pin is used for master detection during initial start-up. For the master phase, TAKE must be pulled high through a resistor. For the slave phase, TAKE is connected to the PASS pin of the previous phase.
2	PG	**Power good output.** The PG pin is an open-drain output. PG requires a pull-up resistor connected to a DC voltage; PG indicates high if the output voltage (V_{OUT}) is within regulation. It is recommended to pull up PG to VDD18.
3	SET	**COMP signal.** SET turns the high-side MOSFET (HS-FET) on when a run signal is present. For multi-phase operation, connect the SET pins of all phases together, and connect a 100kΩ resistor from SET to PGND.
4	ISUM	**Current sensing output.** For single-phase operation, keep ISUM floating. For multi-phase operation, connect the ISUM pins of all phases together for current balancing.
5	VDRV/ VCC	**3.3V power supply input.** VDRV/VCC powers the driver and control circuits. Decouple VDRV/VCC with a minimum 1µF ceramic capacitor placed as close as possible to VDRV/VCC. X7R or X5R grade dielectric ceramic capacitors are recommended.
6	VINSEN	**Input voltage sensing.** Connect VINSEN to VIN through a resistor divider.
7, 8, 9, 10, 19	PGND	**System ground.** PGND is the reference ground of the regulated V_{OUT}. Because of this, care must be taken in the PCB layout. Use wide PCB traces to make the connection.
11, 12, 13, 14, 15, 16, 17, 18	SW	**Switch output.** Connect SW to the inductor. SW is driven up to VIN by the high-side switch during the PWM duty cycle on time. The inductor current drives SW low during the off time. Use wide PCB traces to make the connection.
20, 21, 22, 23, 24	VIN	**Input voltage.** VIN supplies power for the internal MOSFET and regulator. The input capacitors are needed to decouple the input rail. Use wide PCB traces to make the connection.
25	PHASE	**Switch output.** A dedicated SW pin to connect the bootstrap capacitor. Connect a 2.2Ω resistor and a 0.1µF to 0.22µF capacitor between BST and PHASE to form a floating supply across the high-side switch driver.
26	BST	**Bootstrap.** Connect a 2.2Ω resistor and a 0.1µF to 1µF capacitor (1/2 to 1/3 of the VCC capacitance) between BST and PHASE to form a floating supply across the high-side switch driver.
27	CTRL	**PMBus control pin.** The CTRL pin is an input signal that controls whether the regulator is on or off depending on the ON_OFF_CONFIG (02h) configuration. Do not float CTRL.
28	ADDR/ VBOOT	**Multi-function pin. PMBus address setting and boot voltage (V_{BOOT}) setting.** Connect ADDR/VBOOT to VDD18 through a resistor divider. Select the resistor divider ratio to obtain the target PMBus address and V_{BOOT}.
29	ALT/RST	**Multi-function pin. PMBus alert and output voltage reset.** When the ALT function is selected, this pin is active low, so it must be connected to 3.3V through a pull-up resistor. When the RST function is selected, V_{OUT} resets to the boot voltage (V_{BOOT}) when RST is pulled low.
30	VSEN+	**Output voltage sensing positive return.** Connect VSEN+ directly to the output voltage of the load. It should be routed differentially with VSEN-.
31	VSEN-	**Output voltage sensing negative return.** Connect VSEN- directly to the ground of the load. It should be routed differentially with VSEN+.
32	AGND	**Analog ground.**
33	SDA	**PMBus data.** The SDA pin is the data signal transmitted between the PMBus controller and the MPQ8785.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
34	SCL	**PMBus clock.** The SCL pin is the source synchronous clock from the PMBus controller.
35	VDD18	**1.8V LDO output.** The VDD18 pin provides a power supply for the internal digital circuit. Connect a 1µF bypass capacitor from VDD18 to AGND, placed as close to VDD18 as possible.
36	PASS	**Pass the run signal to the next phase.**
37	PWM	**PWM signal.** Internal connection only. Leave the PWM pin floating.

ABSOLUTE MAXIMUM RATINGS (2)

Supply voltage (V_{IN}) 18V
V_{IN} - V_{SW} (DC) .....-0.3V to +24V
V_{IN} - V_{SW} (10ns).....-5V to +32V
V_{SW} (DC) .....-0.3V to +18.3V
V_{SW} (25ns) (2) .....-5V to +25V
V_{BST} - V_{SW} (DC) 4V
V_{BST} - V_{SW} (25ns) (3)..... 8V
V_{DRV}/V_{CC} .....-0.3V to +4V
V_{DD18}.....-0.3V to +2.2V
V_{SEN-} .....-0.3V to +0.3V
ADDR/VBOOT, VINSEN.....-0.3V to +2.2V
All other pins .....-0.3V to +4V
Junction temperature (T_J) .....170°C
Lead temperature.....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....Class 1C
Charged-device model (CDM).....Class C2B

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) .....3.1V to 16V
V_{DRV}/V_{CC}.....3.1V to 3.6V
Output voltage (V_{OUT}).....0.35V to 5.5V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (5) θ_{JB} θ_{JC_TOP}

TLGA-37 (5mmx6mm)..... 2.8.....10.6 . °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) Specified by design. Measured using a differential oscilloscope probe.
4) The device is not guaranteed to function outside of its operating conditions.
5) θ_{JB} is the thermal resistance from the junction to the board around the PGND soldering point. θ_{JC_TOP} is the thermal resistance from the junction to the top of the package.

ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, CTRL = 2V, V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Remote-Sense Amplifier						
Bandwidth (6)	$GBW_{(RSA)}$			20		MHz
VSEN+ current	I_{VSEN+}	VSEN+ = 3.3V, VSEN- = 0V			50	µA
VSEN- current	I_{VSEN-}	VSEN+ = 3.3V, VSEN- = 0V	-50			µA
CTRL						
CTRL rising threshold	V_{CTRL_RISE}		1.12	1.2	1.28	V
CTRL falling threshold	V_{CTRL_FALL}			0.835		V
CTRL input current	IIH_{CTRL}	V_{CTRL} = 3.3V		3.1	5	µA
CTRL delay (7)	t_{DELAY}	CTRL high to PWM ready		10		µs
CTRL delay in low-power mode (LPM) (7)	t_{DELAY_LPM}	CTRL high to PWM ready		600		µs
Pulse-Width Modulation (PWM) Outputs						
Output low voltage	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = 400µA		10	100	mV
Output middle voltage	$V_{OM(PWM)}$	$I_{PWM(SINK)}$ = -100µA	1.2	1.5	1.7	V
Output high voltage	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = -400µA	3.15	V_{CC} - 0.02		V
Rising and falling time (6)		C = 10pF		10		ns
PWM tri-state range	$V_{TRI(PWM)}$		1.1		1.8	V
PASS						
Output low voltage	$V_{OL(PASS)}$	$I_{PWM(PASS)}$ = 400µA		10	100	mV
Output high voltage	$V_{OH(PASS)}$	$I_{PWM(PASS)}$ = -400µA	3.15	V_{CC} - 0.02		V
PASS tri-state range	$V_{TRI(PASS)}$		1.1		1.8	V
Rising and falling time (6)		C = 10pF		10		ns
TAKE						
TAKE leakage current	I_{TAKE_LEAK}	V_{TAKE} = 3.3V		0	200	nA
TAKE input high voltage	$V_{IH(TAKE)}$		2.2			V
TAKE input low voltage	$V_{IL(TAKE)}$				0.8	V
SET						
Output low voltage	$V_{OL(SET)}$	$I_{SET(SINK)}$ = 10mA			150	mV
Output high voltage	$V_{OH(SET)}$	$I_{SET(SOURCE)}$ = -10mA	3.05	V_{CC} - 0.1		V
SET input high voltage	$V_{IH(SET)}$	As slave IC	2.2			V
SET input low voltage	$V_{IL(SET)}$	As slave IC			0.8	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 3.3V, CTRL = 2V, V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Good (PG)						
PG high threshold (7)	V_{PG_HIGH}	ECh, bits[9:8] = 2b'01	90%	95%	97.5%	V_{REF}
PG low threshold	$V_{PG\_LOW\_RISE}$	EBh, bits[4:2] = 2b'010	117%	120%	123%	V_{REF}
	$V_{PG\_LOW\_FALL}$	EBh, bits[8:7] = 2'b01	67%	70%	73%	V_{REF}
PG sink current capability	V_{PG}	I_{PG} = 10mA			0.3	V
PG leakage current	I_{PG_LEAK}	V_{PG} = 3.3V		50	200	nA
PG low-to-high delay (7)	$V_{PG\_DELAY\_HIGH}$	1LSB = 100µs	0		25.6	ms
PG high-to-low delay (7)	$V_{PG\_DELAY\_LOW}$	Circuit inherent delay		200		ns
RST						
RST falling threshold	V_{RST_FALL}		0.8	1.0	1.2	V
RST hysteresis	V_{RST_HYS}			170		mV
RST input current	IIH_{RST}	V_{RST} = 3.3V		0	500	nA
VINSEN						
VIN_ON range (6)			3		16	V
VIN_OFF range (6)			2.9		15.9	V
VINSEN leakage current	I_{VINSEN_LEAK}	CTRL is low, V_{VINSEN} = 2.2V			200	nA
Output Over-Voltage Protection (OVP)						
OVP threshold entry max	$V_{OV\_ENTRY\_MAX}$	EBh, bits[4:2] = 3'b111	142%	145%	148%	V_{REF}
OVP threshold entry min	$V_{OV\_ENTRY\_MIN}$	EBh, bits[4:2] = 3'b000	107%	110%	113%	V_{REF}
OVP threshold exit max	$V_{OV\_EXIT\_MAX}$	EBh, bits[6:5] = 2'b11	99.5%	102.5%	105.5%	V_{REF}
OVP threshold exit min	$V_{OV\_EXIT\_MIN}$	EBh, bits[6:5] = 2'b00	17%	20%	23%	V_{REF}
Output Under-Voltage Protection (UVP)						
UVP threshold max	$V_{UV\_TH\_MAX}$	EBh, bits[8:7] = 2'b11	87%	90%	93%	V_{REF}
UVP threshold min	$V_{UV\_TH\_MIN}$	EBh, bits[8:7] = 2'b00	57%	60%	63%	V_{REF}
VDRV/VCC Supply						
Supply current	I_{VCC}	Normal power mode, CTRL is low		18	25	mA
		Low-power mode, CTRL is low		110	600	µA
VDRV voltage (V_{DRV})/VCC voltage (V_{CC}) under-voltage lockout (UVLO) threshold voltage rising	V_{VCC_RISE}	V_{CC} is rising		2.88	3.05	V
V_{DRV}/V_{CC} UVLO threshold voltage falling	V_{VCC_FALL}	V_{CC} is falling	2.55	2.76		V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 3.3V, CTRL = 2V, V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
1.8V Regulator						
1.8V regulator output voltage	VDD18		1.760	1.8	1.840	V
1.8V regulator load capability	I_{VDD18}	I_{LOAD} = 30mA, T_J = 25°C	1.772	1.79	1.808	V
Output Voltage TON_RISE and TON_DELAY_TIME						
TON_RISE (soft start) time (6)	t_{ON}	1LSB = 100µs	0.1		51.1	ms
TON_RISE time typical (7)	t_{ON_TYP}	61h, bits[8:0] = 0x1E	2.85	3	3.15	ms
t_{ON} delay time (7)	t_{ON_DELAY}	1LSB = 100µs	0		102.3	ms
Output Voltage TOFF_FALL and TOFF_DELAY_TIME						
TOFF_FALL (soft shutdown) time (6)	t_{OFF}	1LSB = 100µs	0.1		51.1	ms
TOFF_FALL time (typical) (7)	t_{OFF_TYP}	65h, bits[8:0] = 0x1E	2.7	3	3.3	ms
t_{OFF} delay time (6)	t_{OFF_DELAY}	1LSB = 100µs	0		102.3	ms
Frequency and Timer						
Switching frequency (7)	f_{SW}	V_{OUT} = 1V	300		2000	kHz
Switching frequency (typical) (7)		D1h, bits[8:0] = 0x32	780	800	820	kHz
Analog-to-Digital Converter (ADC)						
REF		T_J = 25°C	1.595	1.6	1.605	V
		-40°C < T_J < +125°C	1.560	1.6	1.640	V
Voltage range			0		1.6	V
ADC resolution				10		Bits
DNL					1	LSB
Sample rate (6)				780		kHz
VID Digital-to-Analog Converter (DAC) (Reference Voltage)						
Voltage range (6)	FS_{DAC_VID}			0.35 - 1.55		V
Resolution/LSB (6)	Δ_{DAC_VID}	10-bit DAC		1.5625		mV
Output Accuracy						
Output voltage (V_{OUT}) accuracy	VID = 0.5V to 1.5V	25°C	-0.5		+0.5	%
		0°C < T_J < 85°C (5)	-0.5		+1	%
		-40°C < T_J < 125°C	-1		+1.5	%
Output Slew Rate						
V_{OUT} slew rate max (6)				20		mV/µs
Configurable Thermal Protection						
TP fault rising threshold (7)	T_{TH_RISE}	1LSB = 1°C, 4Fh = 0x91		145		°C
Hysteresis (7)	T_{TH_HYS}	EBh, bits[1:0] = 2b'00		20		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 3.3V, CTRL = 2V, V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Current Limit						
Output current limit (inductor valley)	$I_{LIM\_VALLEY\_TYP}$	EAh, bits[15:8] = 0x28		40		A
Output current limit (DC) (7)	$I_{LIM\_DC(TYP)}$	46h, bits[15:0] = 0x00C8		200		A
Low-side negative over-current limit (NOCP) (7)	I_{NOCP_TYP}	EAh, bits[7:0] = 0x14		-20		A
PWM on time during NOCP (7)	t_{NOCP}	D4h, bits[13:10] = 4b'0100		160		ns
V_{IN} Supply						
Supply current	I_{VIN}	CTRL is low		20	40	µA
V_{IN} UVLO threshold voltage rising	V_{IN_RISE}	V_{IN} is rising	2.40	2.60	2.80	V
V_{IN} UVLO threshold voltage falling	V_{IN_FALL}	V_{IN} is falling	2.05	2.25	2.45	V
MOSFET						
On resistance ($R_{DS(ON)}$)	$R_{DS(ON)\_HS}$	T_J = 25°C		4.1		mΩ
	$R_{DS(ON)\_LS}$	T_J = 25°C		1.1		
Switch leakage	SW_{LKG_LS}	T_J = 25°C, SW = 12V		0	200	nA
	SW_{LKG_HS}	T_J = 25°C, SW = 0V		0	200	
Monitoring Parameters						
V_{OUT} monitor range (7)	M_{VOUT_RANGE}		0		5.5	V
V_{OUT} monitor accuracy (7)		V_{OUT} = 0.35V to 0.5V, VDIFF_GAIN = 1, EBh, bit[10] = 1'b0	-4%		+4%	
		V_{OUT} = 0.5V to 1.55V, VDIFF_GAIN = 1, EBh, bit[10] = 1'b0	-3%		+3%	
		V_{OUT} = 1.55V to 3V, VDIFF_GAIN = 0.5, EBh, bit[10] = 1'b1	-3%		+3%	
V_{OUT} bit resolution (7)		Linear mode, VDIFF GAIN = 1, EBh, bit[10] = 1'b0		1.953125		mV
		Linear mode, VDIFF GAIN = 0.5, EBh, bit[10] = 1'b1		3.90625		mV
V_{IN} monitor accuracy	M_{VIN_ACC}	VINSENSE = 0.75V	-2.5%		+2.5%	
Output current monitor accuracy (7)	M_{IOUT_ACC}	V_{OUT} = 1.2V, f_{SW} = 800kHz, I_{OUT} = 35A, 25°C	-8%		+8%	
		V_{OUT} = 1.2V, f_{SW} = 800kHz, I_{OUT} = 40A , 0°C < T_J < 70°C	-10%		+10%	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 3.3V, CTRL = 2V, V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PMBus DC Characteristics						
Input high voltage	V_{IH}		1.35			V
Input low voltage	V_{IL}				0.8	V
Input leakage current			-1		+1	µA
Output low voltage	V_{OL}	SDA sinks 2mA			0.4	V
Maximum voltage (6) (SDA, SCL)	V_{MAX}	Transient voltage including ringing	-0.3	3.3	+3.6	V
Pin capacitance (6)	C_{PIN}				10	pF
PMBus Timing Characteristics (6)						
Operating frequency range			10		1000	kHz
Bus free time		Between stop and start command	0.5			µs
Holding time			0.26			µs
Repeated start command set-up time			0.26			µs
Stop command set-up time			0.26			µs
Data hold time			0			ns
Data set-up time			50			ns
Clock low timeout			25		35	ms
Clock low period			0.5			µs
Clock high period			0.26		50	µs
Clock/data falling time					120	ns
Clock/data rising time					120	ns

Notes:

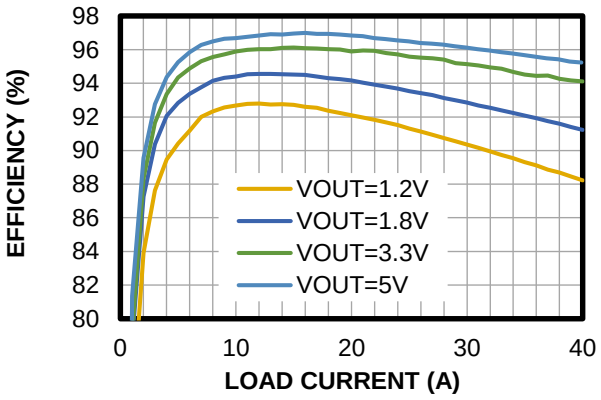
6) Guaranteed by design.
7) Guaranteed by design; not tested in production. The parameter is tested during parameter characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, V_{DRV}/V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

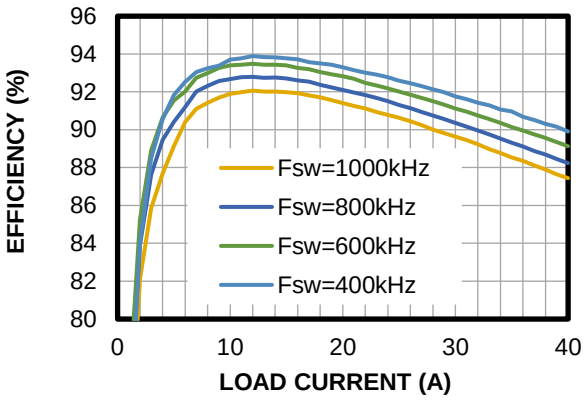
Efficiency vs. Load Current

1-phase CCM, f_{SW} = 800kHz,
L = 150nH/0.17mΩ

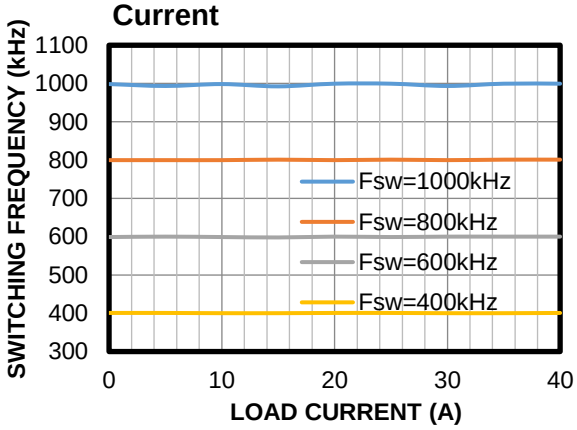


Efficiency vs. Load Current

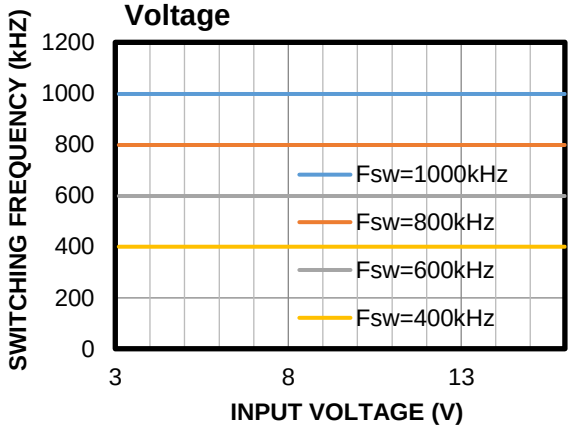
1-phase CCM, V_{OUT} = 1.2V,
L = 150nH/0.17mΩ



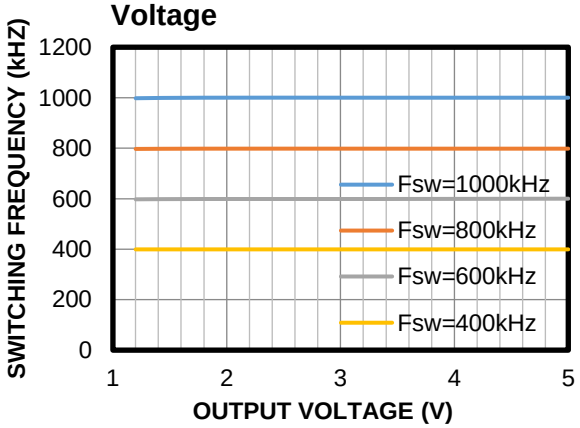
Switching Frequency vs. Load Current



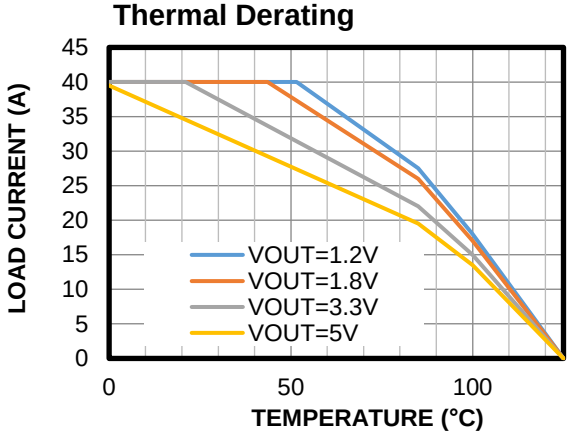
Switching Frequency vs. Input Voltage



Switching Frequency vs. Output Voltage



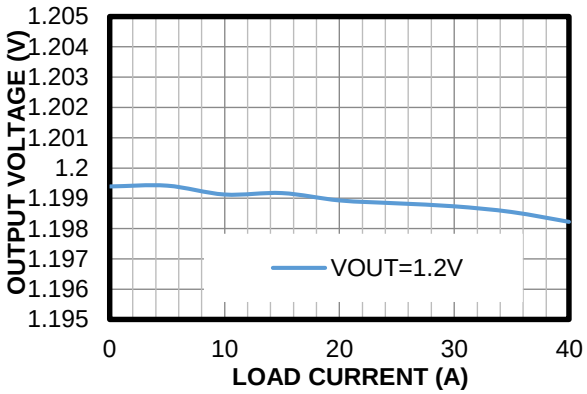
Thermal Derating



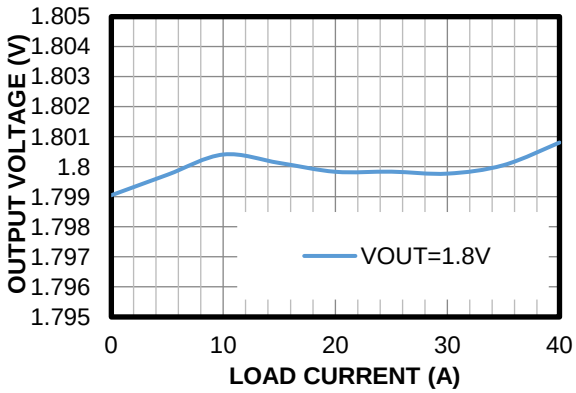
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, V_{DRV}/V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

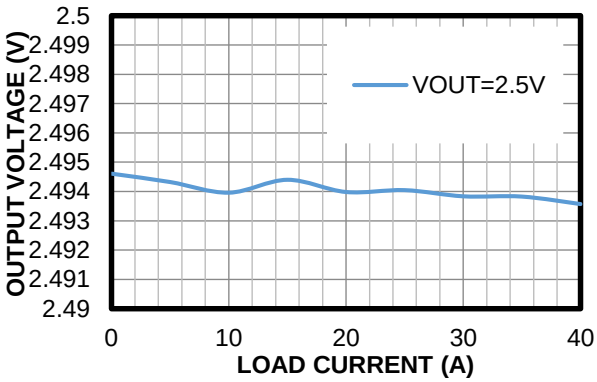
Load Regulation



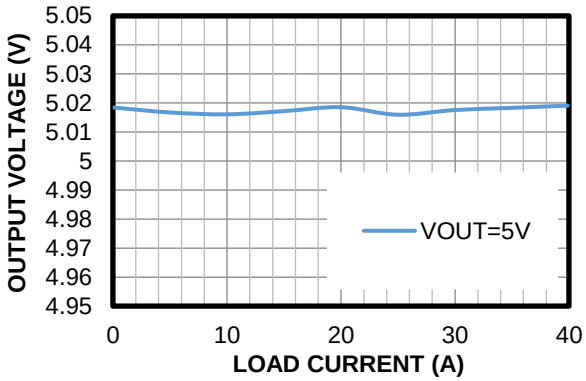
Load Regulation



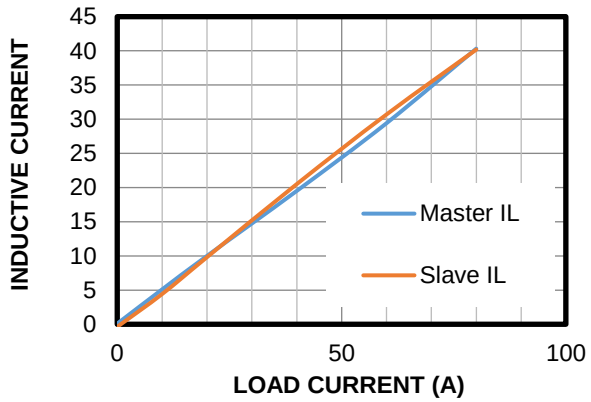
Load Regulation



Load Regulation



Current Balance

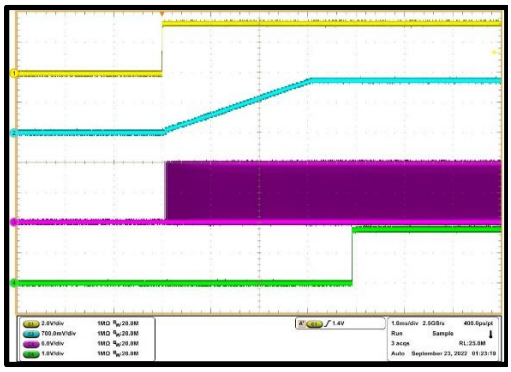


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, V_{DRV}/V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

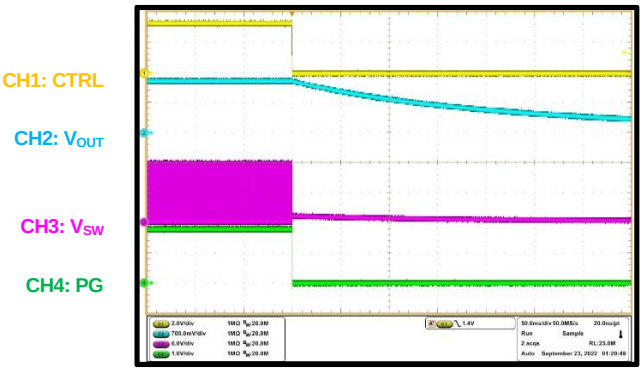
CTRL Power-On

I_{OUT} = 0A, t_{ON} delay = 0ms, regular power mode



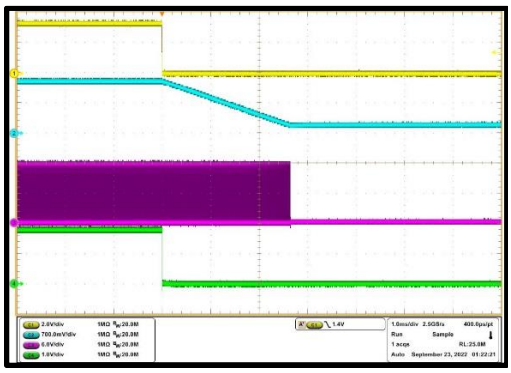
CTRL Power-Off

I_{OUT} = 0A, Hi-Z shutdown



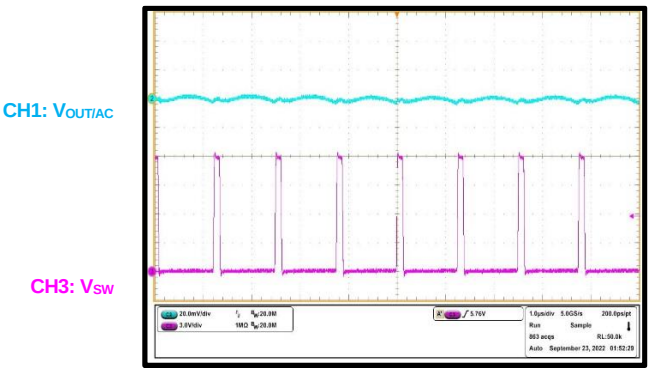
CTRL Power-Off

I_{OUT} = 0A, soft shutdown, t_{OFF} fall = 0.4ms



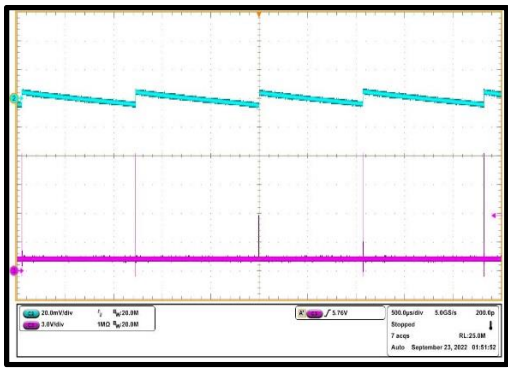
Steady State

1-phase CCM, I_{OUT} = 0A



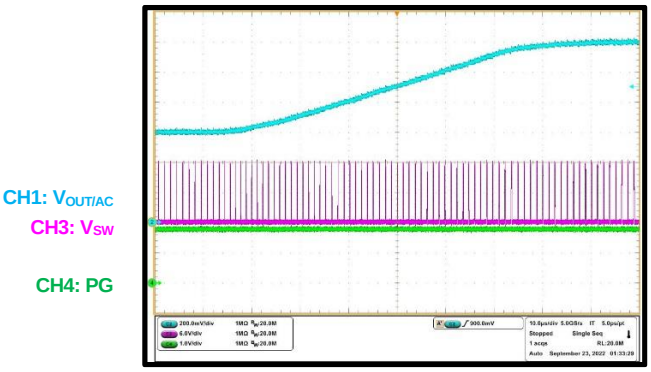
Steady State

1-phase DCM, I_{OUT} = 0A



DVID Up

DVID from 0.6V to 1.2V, R = 10mV/µs

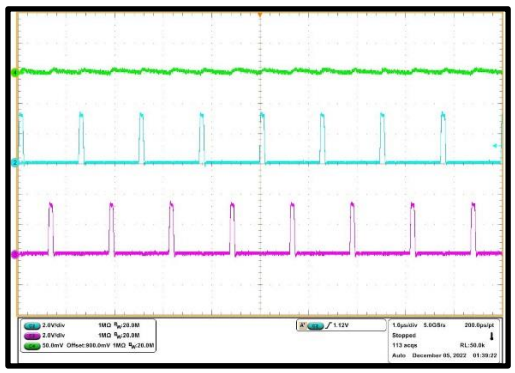


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, V_{DRV}/V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

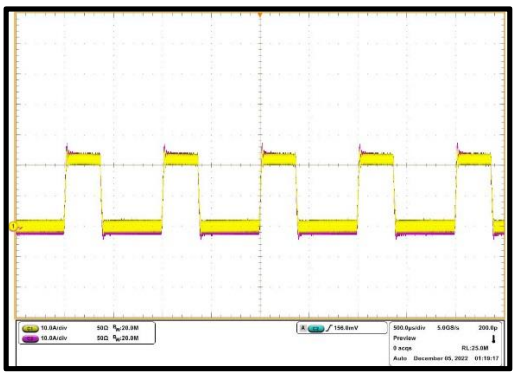
2-Phase Steady State

CCM, I_{OUT} = 0A



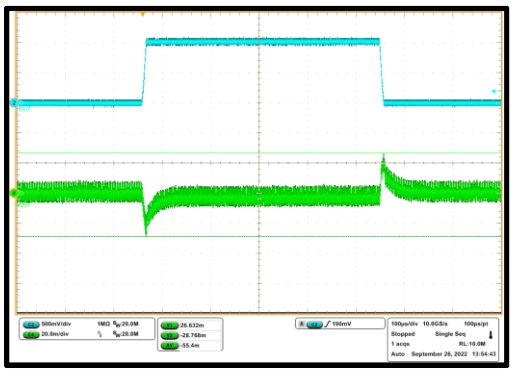
2-Phase Current Balance

0A to 40A load transient response



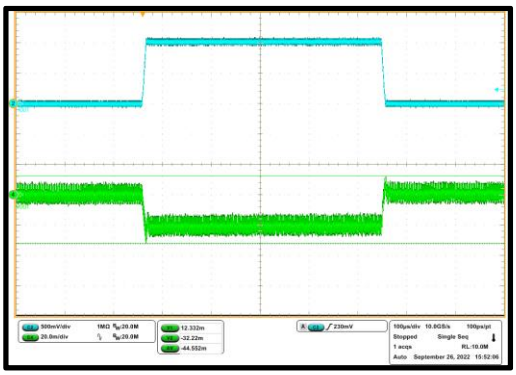
Load Transient with AC Load Line

R_{LL} = 1.5625mΩ, 0 to 20A, slew rate = 2.5A/μs



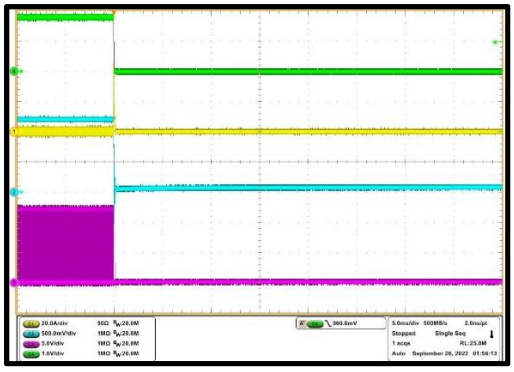
Load Transient with DC Load Line

R_{LL} = 1.5625mΩ, 0 to 20A, slew rate = 2.5A/μs



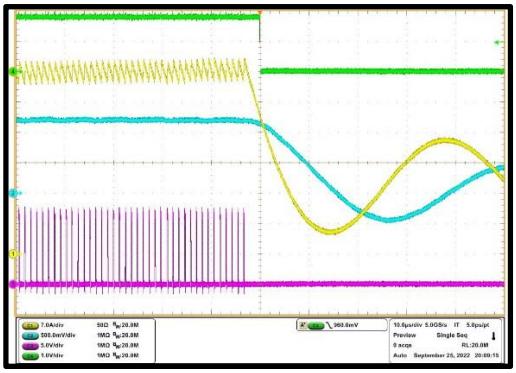
OCP_PHASE = 40A

Latch-off mode



OCP_PHASE = 40A

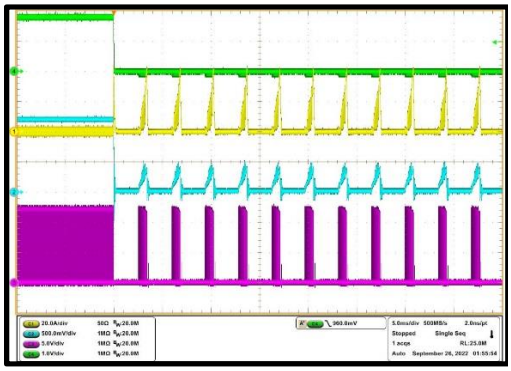
Latch-off mode, zoom in



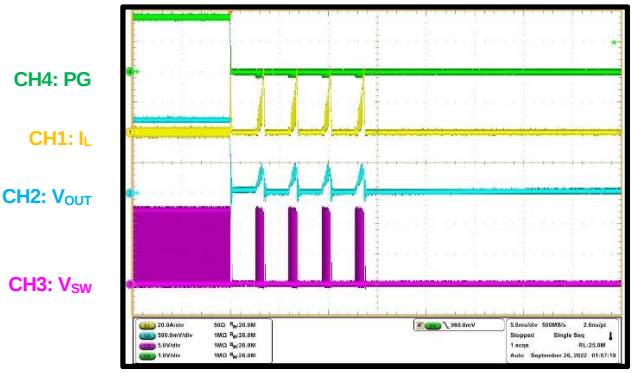
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, V_{DRV}/V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

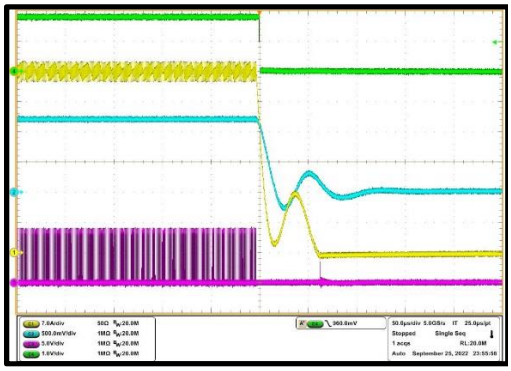
OCP_PHASE = 40A
Hiccup mode



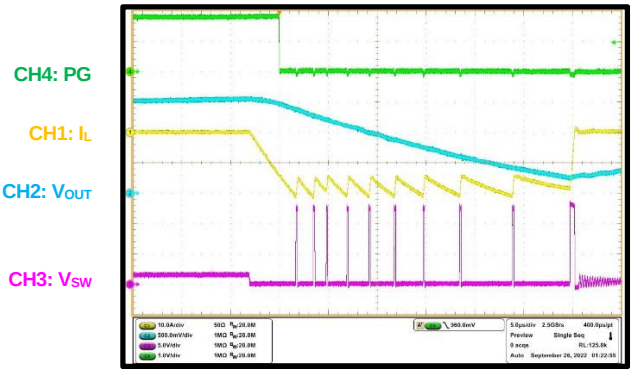
OCP_PHASE = 40A
Retry 4 times



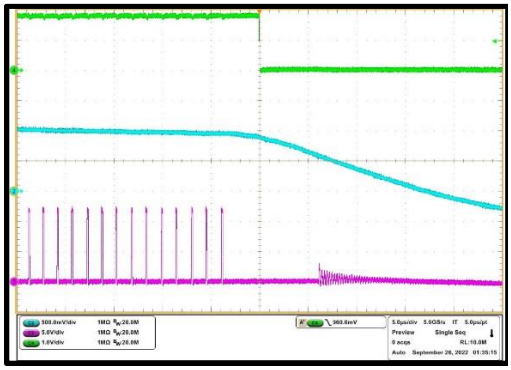
OCP_TDC
OCP_TDC = 45A,
OCP_TDC trigger delay = 7.5ms, latch-off mode



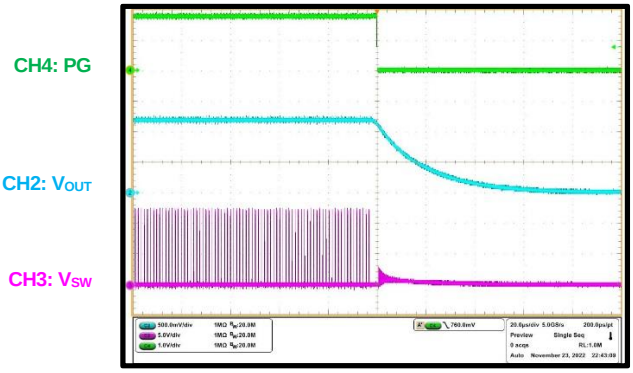
OVP/NOCP
OVP level = 130% of VID, NOCP = -20A,
OVP trigger delay = 1µs, hiccup mode



UVP
UVP level = 80% of VID,
UVP delay = 5µs, hiccup mode



OTP
OTP level = 165°C, hiccup mode, 20°C hysteresis



FUNCTIONAL BLOCK DIAGRAM

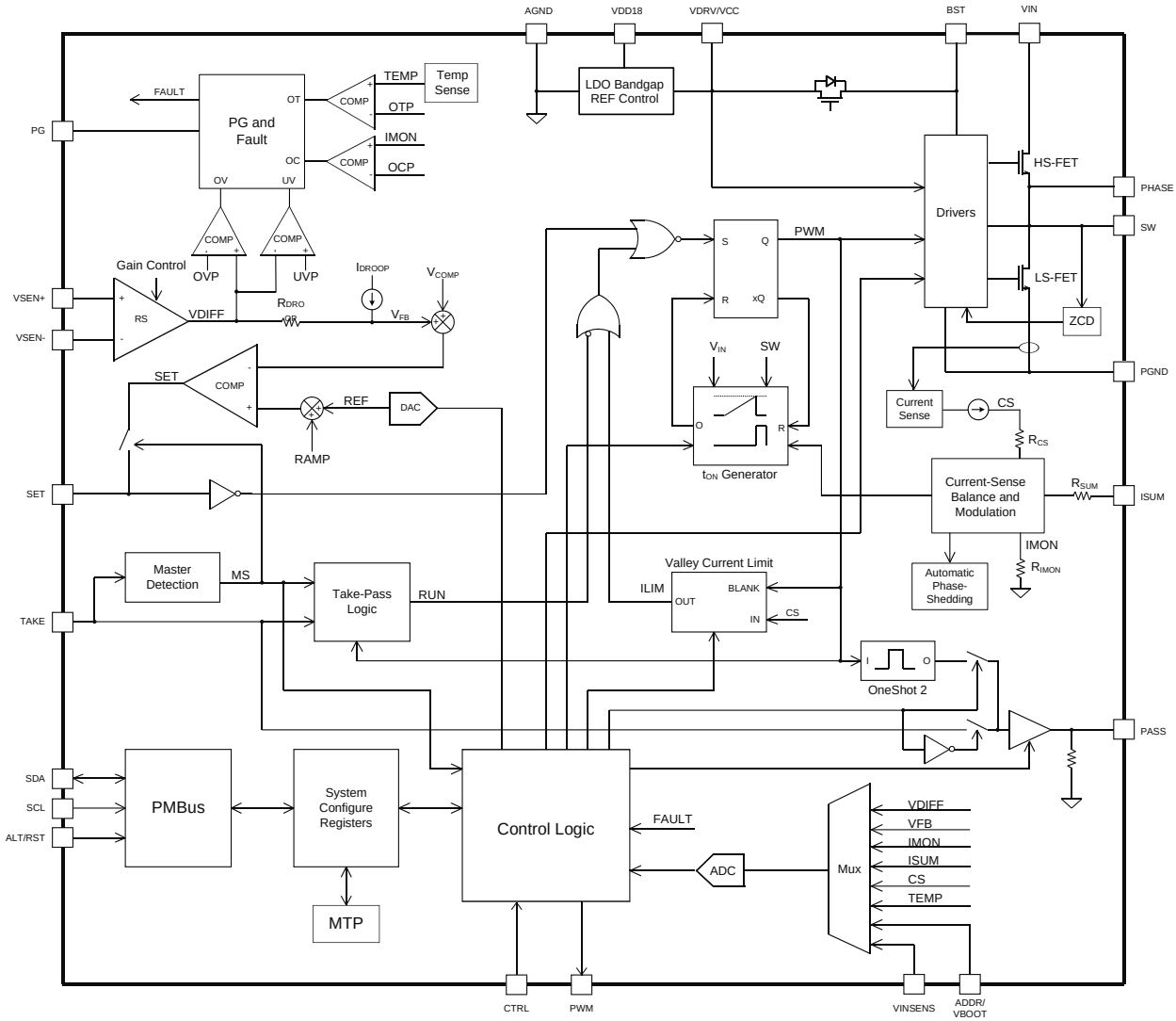


Figure 4: Functional Block Diagram

MULTI-PHASE OPERATION

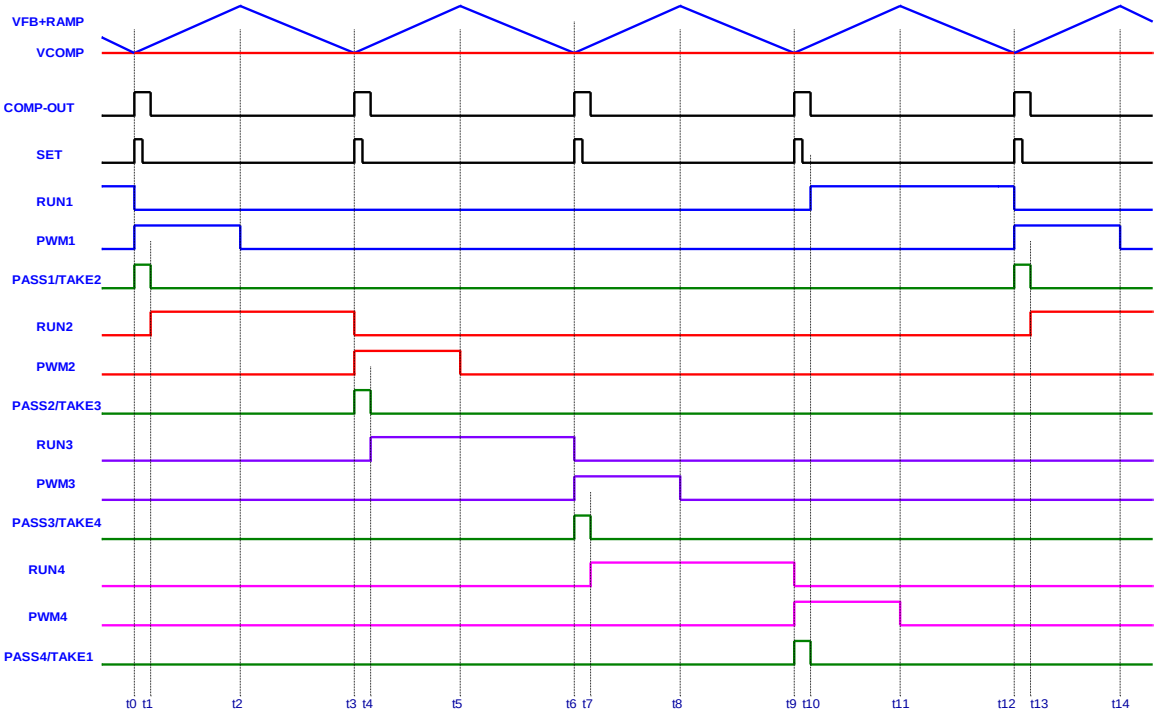


Figure 5: Multi-Phase Interleaved Operation (Steady State)

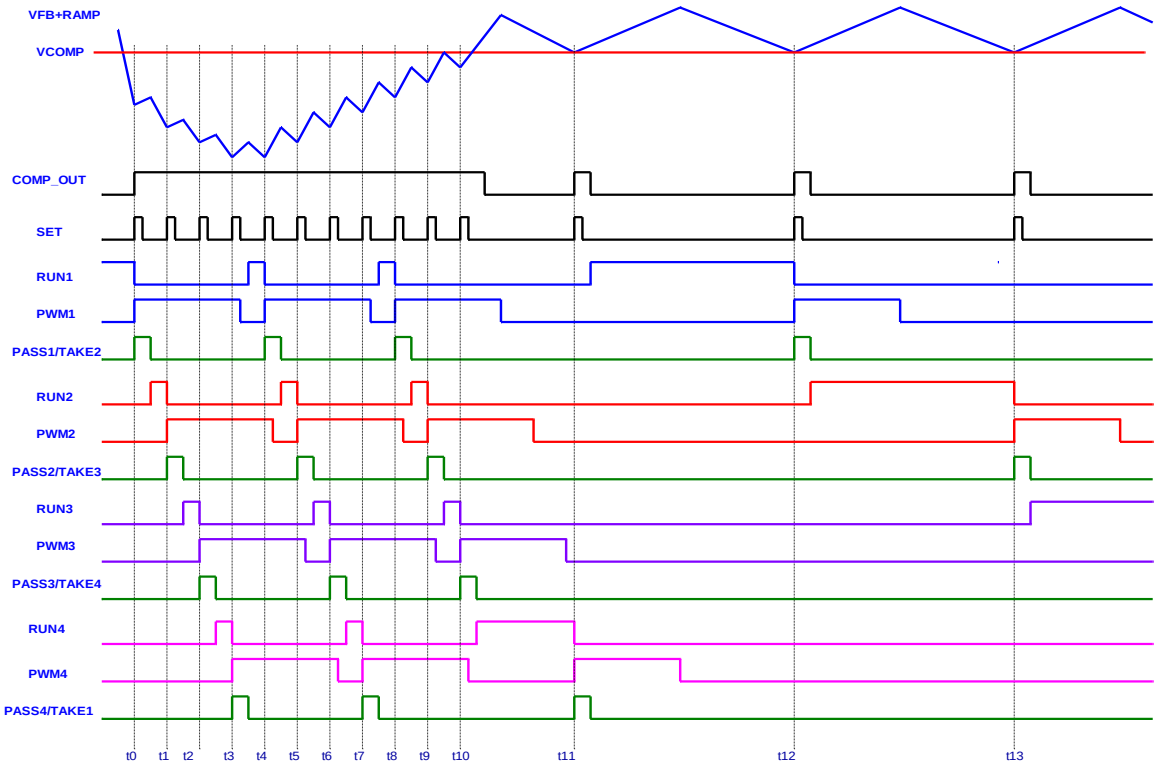


Figure 6: Multi-Phase Interleaved Operation (Load Step-Up Response)

OPERATION

The MPQ8785 is a fully integrated, synchronous, step-down switch-mode converter that uses multi-phase constant-on-time (MCOT) control to provide a fast transient response. It can achieve up to 40A of current per phase. It also contains a precise digital-to-analog converter (DAC) and analog-to-digital converter (ADC), differential remote voltage-sense amplifier, fast comparators, current-sense amplifiers, and internal slope compensation.

The MPQ8785 provides rich configurable functions with a PMBus 1.3 interface. The on-chip non-volatile memory (NVM) can store customer configurations and automatically record the fault type when a protection occurs. Configurable functions include the switching frequency (f_{SW}), output voltage (V_{OUT}), loop stability parameters, protection thresholds and behaviors, and load-line parameters.

The MPQ8785 provides protection features including input voltage (V_{IN}) under-voltage lockout (UVLO), V_{IN} over-voltage protection (OVP), V_{OUT} OVP, over-current protection based on TDC (OCP_TDC), cycle-by-cycle phase-current limiting for over-current protection (OCP_PHASE), negative over-current protection (NOCP), and over-temperature protection (OTP).

Multi-Phase Constant-On-Time (MCOT) Operation

Pulse-Width Modulation (PWM) Control and Switching Frequency (f_{SW})

The MPQ8785 applies MPS's unique, digital pulse-width modulation (PWM) control to provide fast load transient response and simple loop compensation. f_{SW} can be set via the PMBus.

The PWM on time (t_{ON}) of each phase updates in real time according to V_{IN}, V_{OUT}, and the adaptive phase f_{SW}. t_{ON} can be calculated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (1)$$

Where V_{OUT} is the real-time output voltage, V_{IN} is the input voltage, and f_{SW} is the switching frequency set by PMBus command MFR_FS (D1h).

Master/Slave Detection and Operation

The master phase is required for both single-phase and multiple-phase operation. To be configured as the master phase, the relevant phase's TAKE pin must be pulled high. The PASS/TAKE pins of all the phases are connected in a daisy chain configuration. The PASS pin of the last phase is connected to the TAKE pin of the first (master) phase. For single-phase operation, the PASS and TAKE pins are connected together. After start-up, the master phase is determined, and the rest of the phases act as slave phases.

Master Operation

The master phase performs the following functions:

- Accepts both write and read commands through the PMBus.
- Generates the SET signals.
- Manages start-up, shutdown, and all protections.
- Monitors for any fault alerts from the slave phases through the PG pin.
- Starts the first on pulse.
- Starts the on pulse when receiving TAKE and SET signals.
- Determines the on pulse width of its own phase based on the per-phase and total current.
- Sends the PASS/TAKE signal.

Slave Operation

The slave phase performs the following functions:

- Accepts write commands through the PMBus.
- Takes the SET signal from the master.
- Sends over-voltage (OV), under-voltage (UV), and over-temperature (OT) alerts to the master through the PG pin.
- Starts the on pulse when receiving TAKE and SET signals.
- Determines the on pulse width of its own phase based on the per-phase and total current.

- Carries the PASS/TAKE signal.

Figure 5 on page 18 shows of MCOT operation, described in greater detail below.

t0: The feedback voltage (V_{FB}) + RAMP drops below the reference level in the master phase and generates a SET signal. All phases receive this SET signal, but only the phase that has the active RUN signal takes action (in this case, the master). Then the master turns on the high-side MOSFET (HS-FET). Meanwhile, a fixed on pulse is generated on the PASS pin. This signal is passed to Slave 1's TAKE pin.

t1: The falling edge of Slave 1's TAKE pin activates the RUN signal. From this point on, Slave 1 waits for the SET signal to turn on the HS-FET.

t2: The master phase's on pulse expires, and the HS-FET turns off. The on-pulse width is fixed with the given V_{IN}, V_{OUT}, and selected f_{SW}. The on pulse width is fine-tuned based on the per-phase and total currents.

t3: V_{FB} + RAMP drops below the reference level in the master phase again. Only Slave 1 has an active RUN signal, so it turns on its HS-FET. All other phases ignore the SET signal. Meanwhile, Slave 1 generates a fixed on pulse on PASS. This on pulse is passed to Slave 2's TAKE pin.

The above operation (t0 through t3) continues, and the slave phase(s) turn on their HS-FETs one by one for a fixed on time. The operation continues through the PASS/TAKE loop, and only the phase with the active RUN signal turns on its HS-FET when the SET signal is ready.

The MPQ8785 utilizes constant-on-time (COT) control to provide ultra-fast load transient response.

During load step-up, V_{FB} is below the reference voltage (V_{REF}), so the SET signal is generated more frequently than during steady state to respond to the load transient. The SET signal interval during load step-up depends on the load transient step size and slew rate. The SET signal can be generated with the minimum interval, which means the next phase can be turned on in the minimum interval after the previous phase turns on to provide ultra-fast load transient response. Figure 6 on page 18 shows the detailed operation.

Low-Power Mode (LPM)

The MPQ8785 can be configured to low-power mode (LPM) or regular power mode.

When LPM is enabled and CTRL is low, PMBus communication is disabled, and the quiescent current (I_Q) is reduced.

In regular power mode, PMBus communication is available when CTRL is low.

Quiet Switcher™ Technology (QST)

The MPQ8785 has quiet switcher™ technology (QST), which is a proprietary feedback control architecture that controls the effect of parasitic kickback in the circuit to suppress the level of voltage overshoot during fast switching.

Start-Up Sequence

The MPQ8785 is supplied a 3.3V voltage by the VCC pin, which provides the biased supply for the analog circuit and internal 1.8V LDO. The 1.8V LDO produces the 1.8V supply for the digital circuit.

The system is reset by the internal power-on reset (POR) signal after the VCC supply is ready. After the system comes out of POR, the data in the MTP is loaded into the operating registers to configure the VR's operation.

Figure 7 on page 21 shows the start-up sequence in regular power mode, which is described in greater detail below.

t0 to t1: At t0, VCC is supplied a 3.3V voltage. V_{CC} reaches its UVLO threshold at t1. VDD18 reaches 1.8V once the VCC pin exceeds 1.8V.

t1 to t2: At t1, the data in the NVM starts loading into the operating registers. During this stage, the PMBus address detects whether the user selects the voltage on the ADDR pin to set the PMBus address.

t2 to t3: At t2, after NVM copying is finished, the MPQ8785 waits for the CTRL pin to pull high. The PMBus is available at this stage.

t3 to t4: If the PMBus OPERATION (01h) command is preset to the off state after CTRL pulls high, then the MPQ8785 stops at this stage and waits for an OPERATION on command. If OPERATION (01h) is preset to the on state, the turn-on delay time (t_{ON} delay) starts counting. The delay time can be configured to be between

0ms and 102.3ms via TON_DELAY (60h), bits[9:0].

t4 to t5: When t_{ON} delay expires, the VID DAC starts ramping up V_{REF} to the boot voltage (V_{BOOT}) with the configured slew rate. The start-up sequence is complete at t5.

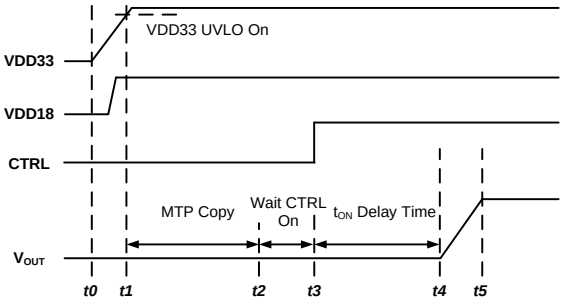


Figure 7: Start-Up Sequence in Regular Power Mode

Figure 8 shows the start-up sequence of the MPQ8785 in low-power mode.

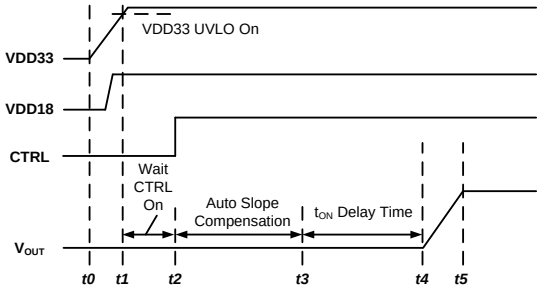


Figure 8: Start-Up Sequence in Low-Power Mode

Shutdown

The MPQ8785 can be shut down by receiving an OPERATION off command, the CTRL pin, V_{CC} UVLO, or a protection shutdown. The shutdown sequences for these different scenarios are described below.

1. VCC shutdown: If the VCC power supply falls below the UVLO falling threshold, the MPQ8785 shuts down immediately.
2. CTRL pin turns off: The MPQ8785 provides Hi-Z shutdown and soft shutdown with a selectable slew rate when the CTRL pin toggles to low in regular power mode. During CTRL pin Hi-Z shutdown, all PWMs enter tri-state when the CTRL pin pulls low, and V_{OUT} is discharged by the load current (I_{LOAD}). During soft shutdown, V_{OUT} ramps down with the selected slew rate until V_{REF} falls to the VID shutdown level (160mV). Then all PWMs enter tri-state.

   When the CTRL pin turns off in low-power mode, the MPQ8785 initiates a HI-Z shutdown immediately with a turn-off delay and enters standby mode with the smallest possible power consumption. The PMBus is unavailable until the CTRL pin is pulled high.
3. OPERATION command off: The MPQ8785 provides Hi-Z shutdown and soft shutdown after receiving an OPERATION off command. When OPERATION is set to Hi-Z shutdown, all PWMs enter tri-state and V_{OUT} is discharged by I_{LOAD}. When OPERATION is set to soft shutdown, V_{OUT} begins a soft shutdown with the slow slew rate until V_{REF} reaches the VID shutdown level. Then all PWMs enter tri-state.
4. Protection shutdown: If a V_{IN} OVP, V_{IN} UVLO, V_{OUT} UVP, OCP_TDC, OCP_PHASE, or OTP fault is triggered, the MPQ8785 enters Hi-Z shutdown immediately.

   If V_{OUT} OVP is triggered, the MPQ8785 turns on all the active low-side MOSFETs (LS-FETs) to discharge V_{OUT} and shut down immediately until V_{OUT} falls below the VID shutdown level.

Figure 9 shows the CTRL pin's soft shutdown power sequence.

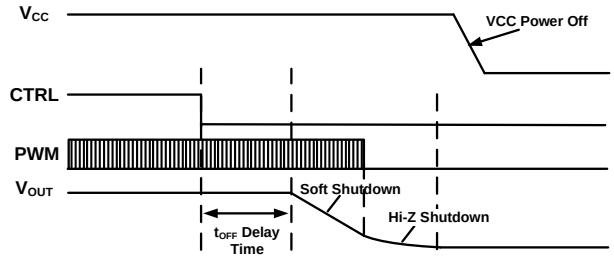


Figure 9: Shutdown Sequence with Soft Shutdown

Figure 10 shows the CTRL pin's Hi-Z shutdown power sequence.

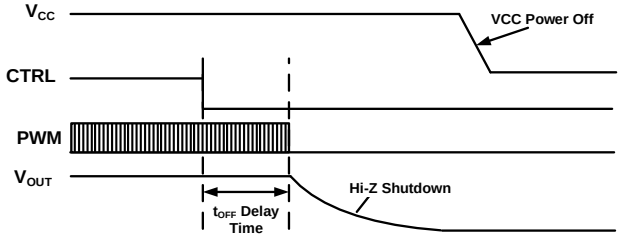


Figure 10: Shutdown Sequence with Hi-Z Shutdown

Output Voltage Reference

The MPQ8785 has a 10-bit VID digital-to-analog converter (DAC) to provide the output voltage reference (V_{REF}) (see Figure 11). The output voltage data format is set via PMBus command MODE_SEL (20h). If configured to linear mode, VID is 1.953125mV per step. If configured to VID or direct mode, VID is 1.5625mV per step.

The commanded voltage is compared to the V_{OUT} limits set by the VOUT_MAX (24h) and VOUT_MIN (2Bh) commands. If the commanded voltage creates a V_{OUT} the exceeds the maximum (V_{OUT_MAX}) or is below the minimum (V_{OUT_MIN}), the PMBus device limits the command voltage to V_{OUT_MAX} or V_{OUT_MIN}. The PMBus ALT pin can assert as a warning.

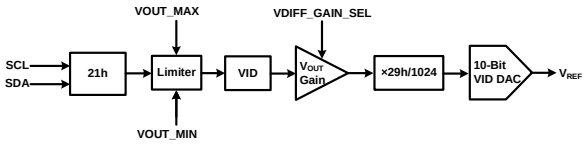


Figure 11: Output Voltage Reference

The remote-sense amplifier gain is used for the calculated final input value into the VID DAC. The VID DAC generates the final reference voltage, which is compared to the sensed output voltage to adjust the duty cycle of the PWM.

Output Voltage Sensing

The voltage at the load is sensed with the differential voltage-sense amplifier (see Figure 12). This type of sensing improves load regulation. The remote-sense amplifier gain can be configured to x1 or x0.5 via PMBus command MFR_VDIFF_GAIN_SEL (EBh).

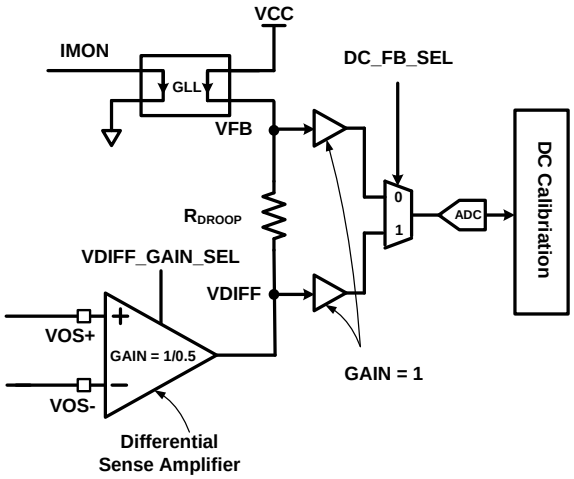


Figure 12: DC Loop Gain Selection

The MPQ8785 senses the voltage on either the VDIFF or VFB pin with the analog-to-digital converter (ADC) for DC voltage calibration to provide highly accurate voltage regulation. Table 1 shows the voltage supporting ranges for different VID steps and sensing gains.

Table 1: Voltage Support Range

Output Divider	VID Step (20h, Bits[6:5])	VDIFF Gain (EBh, Bit[10])	V_{OUT} Range
No	1.5625mV	1	0.35V to 1.55V
No	1.953125mV		
No	1.5625mV	0.5	1.55V to 3.1V
No	1.953125mV		
Yes	1.5625mV/ 1.953125mV	1	0.35V to 5.5V

In applications where V_{OUT} > 3.1V, an external resistor divider is needed. The MPQ8785 provides an output divider with remote sense connection. Set the resistor dividing ratio via VOUT_SCALE_LOOP (29h).

Figure 13 shows the remote sense connection.

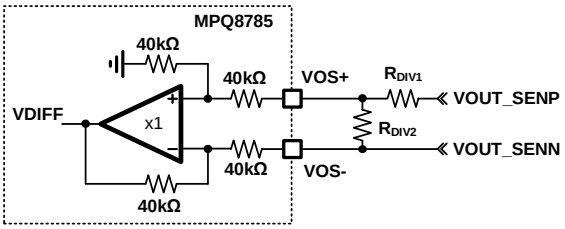


Figure 13: Output Divider with Remote Sense

The voltage divider ratio can be estimated with Equation (2).

$$K_R = \frac{V_{REF}}{V_{OUT}} = \frac{1}{(\frac{1}{R_{DIV1}} + \frac{1}{R_{DIV2}} + \frac{1}{80k\Omega}) \times R_{DIV1}} \quad (2)$$

VOUT_SACLE (in 29h) can be calculated with Equation (3).

$$VOUT\_SCALE = 1024 \times K_R \quad (3)$$

If there is no external voltage divider, then VOUT_SACLE_LOOP (in 29h) is always 1024.

Setting the Boot-Up Voltage (V_{BOOT})

V_{BOOT} can be set via a pin or PMBus command MFR_CONFIG_A (D0h).

If V_{BOOT} is set by a pin (D0h, bit[4] = 1), connect a resistor divider between VDD18 and GND, and tap to the ADDR/VBOOT pin. The internal ADC converts the pin voltage to set V_{BOOT}. Table 3 on page 29 shows V_{BOOT} for different resistor values.

If V_{BOOT} is set by a register (D0h, bit[4] = 0), V_{BOOT} is set via MFR_VBOOT (FCh). The V_{BOOT} step is the same as the VID step.

Output Minimum Load

When VIN and VCC are applied to the MPQ8785 while the CTRL pin is low, there is 165µA current coming out from the SW pin. If there is no minimum load at the output, this current charges V_{OUT}. To avoid residual V_{OUT}, it is required to place a 1kΩ resistor as a minimum load to keep V_{OUT} below 200mV.

Dynamic Voltage Identification (DVID)

The MPQ8785 supports dynamic V_{OUT} transitions by changing the VID code via the PMBus interface.

In PMBus override control mode, the DVID slew rate is set via MFR_VOUT_RATE (D3h). The maximum slew rate is 20mV/µs.

Input Voltage (V_{IN}) Sensing

The input power supply voltage is sampled at VINSEN and used for V_{OUT} regulation, and acts as the feed-forward control for V_{IN} UVLO, V_{IN} OVP, and V_{IN} monitoring via the PMBus.

A resistor divider network outside the chip is connected to VINSEN (see Figure 14). A 10nF filtering capacitor is recommend at VINSEN.

The MFR_VIN_SCALE (E4h) command sets the divider ratio for the input voltage divider network. This can be used to calculate the V_{IN} for monitoring and protection.

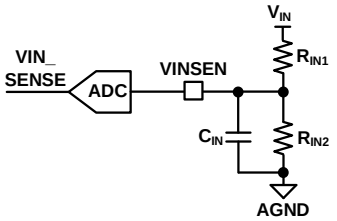


Figure 14: V_{IN} Sensing Block Diagram

Inductor Current (I_L) Sensing and Reporting

The MPQ8785 achieves inductor current sensing. The cycle-by-cycle sensed inductor current is used for multi-phase current balancing, thermal balancing, and per-phase current limitation.

Current Balance

The MPQ8785 provides a current balance loop to regulate current sharing in multi-phase mode when different circuit impedances lead to phase current differences.

The phase current is sensed and calculated with the current reference in the current loop. Each phase's PWM on time is individually adjusted to balance the currents accordingly.

The MPQ8785 applies sigma-delta (Σ-Δ) modulation and delay line-loop (DLL) technology for current balance modulation. This increases the current balance modulation resolution and greatly reduces PWM jitter. The digital system's time resolution is 5ns. By applying Σ-Δ modulation and DLL technology, the digital PWM resolution can be increased to 0.08ns.

The bandwidth of the current loop is relatively low compared to the V_{OUT} regulation loop, meaning the current loop does not impact V_{OUT} regulation.

Automatic Phase-Shedding (APS)

To improve the efficiency across the entire load range, the MPQ8785 supports automatic phase-shedding (APS) according to the load current report.

During APS, the device can be optimized to adjust the phase count to automatically balance the performance between the transient response and power consumption.

Figure 15 on page 24 shows 7-phase operation. The VR works at 7-phase continuous conduction mode (CCM) under heavy loads, then it works at 1-phase CCM under light loads to optimize efficiency. The MPQ8785 enters 1-phase discontinuous conduction mode (DCM) under extremely light loads to further reduce switching loss.

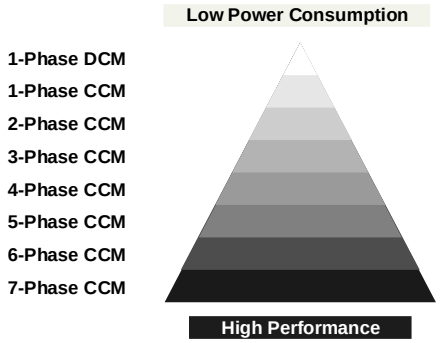


Figure 15: APS Function Diagram in 7-Phase Mode

APS is implemented by comparing the sensed I_{LOAD} with each power state's current threshold. The MPQ8785 provides two types of registers to configure the APS function.

MFR_PHL (C5h), bits[5:0] sets the phase-shedding level, while bits[9:6] configure the hysteresis value to prevent the converter from changing the power state back and forth at a steady load current. Figure 16 shows the APS current threshold setting from 4-phase CCM to 3-phase CCM.

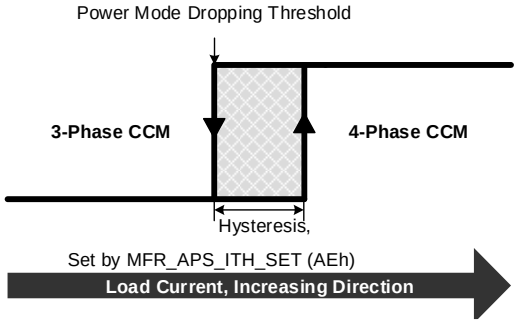


Figure 16: APS Threshold Setting

In addition to the sensed I_{OUT} comparison, the MPQ8785 provides three conditions to exit APS mode immediately and run in full-phase CCM operation to accelerate the load transient response and reduce V_{OUT} undershoot.

Power Good (PG)

The MPQ8785 indicates the power good status with the PG pin. PG is an open-drain output. Pull it up to VDD18 with a resistor.

During soft-start, when V_{REF} rises to the PG rising threshold (set by MFR_PG_ON_SEL register (DCh) bits[9:8]), the MPQ8785 starts the power good delay time counting and asserts PG when the delay time ends. The delay time can be configured via MFR_PG_DELAY (DCh), bits[7:0].

If the MPQ8785 is in a Hi-Z shutdown or soft shutdown status due to a fault protection, PMBus operation off command, or the CTRL pin pulling low, the PG pin pulls low. PG cannot be pulled high again until a new soft start is initialized.

Figure 17 shows the PG indication in regular power mode.

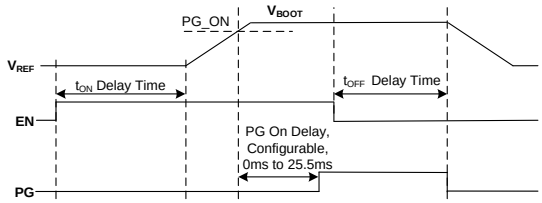


Figure 17: Power Good On/Off Sequence

Fault Monitoring and Protections

The MPQ8785 supports flexible fault monitoring, indication, and protections. These are described below.

V_{IN} Under-Voltage Lockout (UVLO), Over-Voltage Protection (OVP)

The MPQ8785 shuts off immediately by forcing the PWM signal to tri-state if the sensed V_{IN} is below the VIN_OFF threshold, and restarts again when the sensed V_{IN} exceeds the VIN_ON threshold. The V_{IN} UVLO threshold can be configured via VIN_ON (35h) and VIN_OFF (36h) with 200mV/LSB.

The MPQ8785 shuts off if V_{IN} exceeds the V_{IN} OVP threshold that is set via VIN_OV_FAULT_LIMIT (55h).

Over-Current Protection (OCP_TDC)

The MPQ8785 features on-die current sensing and a configurable, positive current-limit threshold. The MPQ8785 provides both inductor valley current limiting (set via PMBus command MFR_NOCP_OCP_SET (EAh)) and output DC limiting (set via PMBus command IOUT_OC_FAULT_LIMIT (46h)).

The output DC current is sensed and monitored during operation. During an OC condition, if the sensed output DC current exceeds the IOUT_OC_FAULT_LIMIT (46h) setting, the device enters OCP immediately.

Once this OCP is triggered, the device enters hiccup mode or latches off, depending on the PMBus selection.

If the device latches off, the power on VCC or VIN must be recycled to enable the device again. The output over-current DC limit can be configured via IOUT_OC_FAULT_LIMIT (46h), which limits the rail's total output current.

Inductor Valley Over-Current Protection (OCP_PHASE)

While the LS-FET is on, the SW current (inductor current) is sensed and monitored cycle by cycle. When V_{FB} drops below V_{REF}, the HS-FET is only allowed to turn on whenever no OC condition is detected while the LS-FET is on. This limits the inductor current cycle by cycle.

Once this OCP is triggered, the device enters hiccup mode or latches off, depending on the PMBus selection. If the device latches off, the power on VCC or VIN must be recycled to enable the device again.

The inductor valley over-current limit can be configured via MFR_NOCP_OCP_SET (EAh), bits[15:8]. These bits only set the per-phase inductor valley current limit, regardless of whether the device is operating in single-phase or multi-phase operation.

Negative Inductor Current Limit (NOCP)

When the LS-FET detects a negative current below the limit set via MFR_NOCP_OCP_SET (EAh), bits[7:0], the part turns off the LS-FET for a certain period of time to limit the negative current. This period is set via MFR_PWM_TIME_CFG (D4h), bits[13:10].

Under-Voltage Protection (UVP)

The MPQ8785 monitors V_{OUT} using the FB pin connected to the tap of a resistor divider to detect a UV condition. If the FB voltage drops below the UVP threshold (set via the PMBus command), UVP is triggered.

After UVP is triggered, the device enters hiccup mode or latches off, depending on the PMBus selection. If the device latches off, the power on VCC or CTRL must be recycled to enable the device again.

Over-Voltage Protection (OVP)

The MPQ8785 monitors V_{OUT} using the VSEN+/VSEN- pins to detect an OV condition.

The MPQ8785 employs an output-sinking mode (OSM) to regulate V_{OUT} to the targeted value. When V_{FB} exceeds 105% of V_{REF} but is below the OVP threshold, OSM is triggered. During OSM, the MPQ8785 runs in forced continuous conduction mode (FCCM). The MPQ8785 exits OSM when the HS-FET turns back on. OSM can be enabled via MFR_NOCP_OCP_SET (EAh), bit[9].

Over-Temperature Protection (OTP)

The MPQ8785 has OTP. The IC monitors the junction temperature (T_J) internally. If T_J exceeds the threshold, the converter shuts off. After OTP is triggered, the device enters hiccup mode or latches off, depending on the PMBus selection. If the device latches off, the power on VCC or CTRL must be recycled to enable the device again.

Phase Redundancy: Master Fault Skip

The master phase role transfer function during a master phase fault can only be used if there are more than 3 phases. This function can be enabled via MFR_PS_CTRL (EDh), bit[1]. If bit[1] = 1, the master fault skip function is enabled.

When this function is used, follow the requirements below:

1. The total phase number should exceed 3.
2. The master phase's VSEN+ and VSEN- pins must be connected to the slave phases' VSEN+ and VSEN- pins, respectively.
3. The delay time when the slave phase obtains the master priority is determined by MFR_PS_CTRL (EDh), bits[4:2]. This delay time must be shorter than 200ns.

Phase Redundancy: Slave Fault Skip

The slave fault skip is set MFR_PS_CTRL (EDh), bit[0]. When bit[0] = 1, the slave phase bypasses the take and pass signal when the phase has fault.

If one slave fault occurs, the TAKE and PASS pins short themselves, which bypasses this slave phase.

PMBUS INTERFACE

PMBus Serial Interface Description

The power management bus (PMBus) is an open-standard power management protocol that defines a means of communication with power conversion and other devices.

The PMBus is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the lines, a master device generates an SCL signal and device address, and arranges the communication sequence. This is based on I^2C operation principles. The MPQ8785 is a PMBus slave that supports both standard mode (100kHz) and fast mode (400kHz and 1000kHz). The PMBus interface adds flexibility to the power supply solution.

Start and Stop Commands

The start and stop commands are signaled by the master device, which signifies the beginning and the end of the PMBus transfer. The start command is defined as the SDA signal transitioning from high to low while the SCL line is high. The stop command is defined as the SDA signal transitioning from low to high while the SCL line is high (see Figure 18).

The master generates the SCL clocks, and transmits the device address and the read/write (R/W) direction bit on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data must be followed by an acknowledge (ACK) bit.

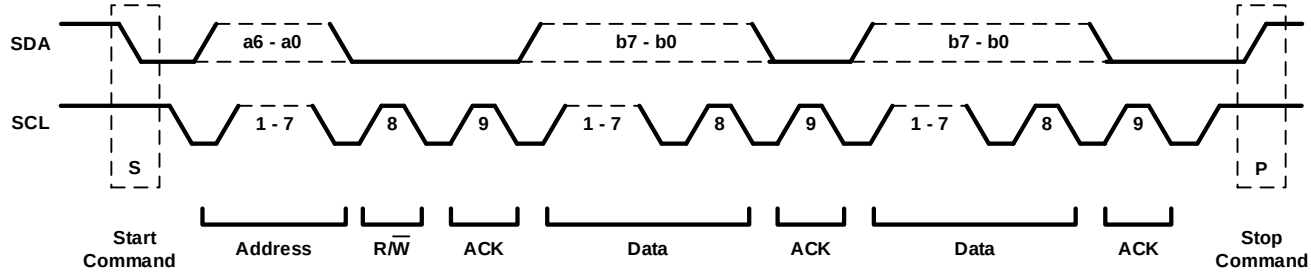


Figure 18: Data Transfer over PMBus

PMBus Update Sequence

The MPQ8785 requires a start command, a valid PMBus address, a register address byte, and a data byte for a single data update. The device acknowledges that is has received each byte by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the MPQ8785, and the device performs an update on the falling edge of the LSB byte.

Protocol Usage

All PMBus transactions on the MPQ8785 are executed using defined bus protocols. The following protocols are implemented with packet error checking (PEC):

- End byte with PEC
- Receive byte with PEC
- Write byte with PEC
- Read byte with PEC
- Write word with PEC
- Read word with PEC
- Block read with PEC

PMBus Message Format

In Figure 19 on page 27, the unshaded cells indicate that the bus host is actively driving the bus, and the shaded cells indicate that the MPQ8785 is driving the bus. The abbreviations are defined below.

- S = Start command
- Sr = Repeated start command
- P = Stop command
- R = Read bit
- $\overline{W}$ = Write bit
- A = Acknowledge bit (0)
- $\overline{A}$ = Acknowledge bit (1)

A represents the acknowledge (ACK) bit. The ACK bit is typically active low (logic 0) if the transmitted byte is received successfully by a device. However, when the receiving device is the bus master, the ACK bit for the last byte read

is a logic 1, indicated by $\overline{A}$ (see Figure 19).

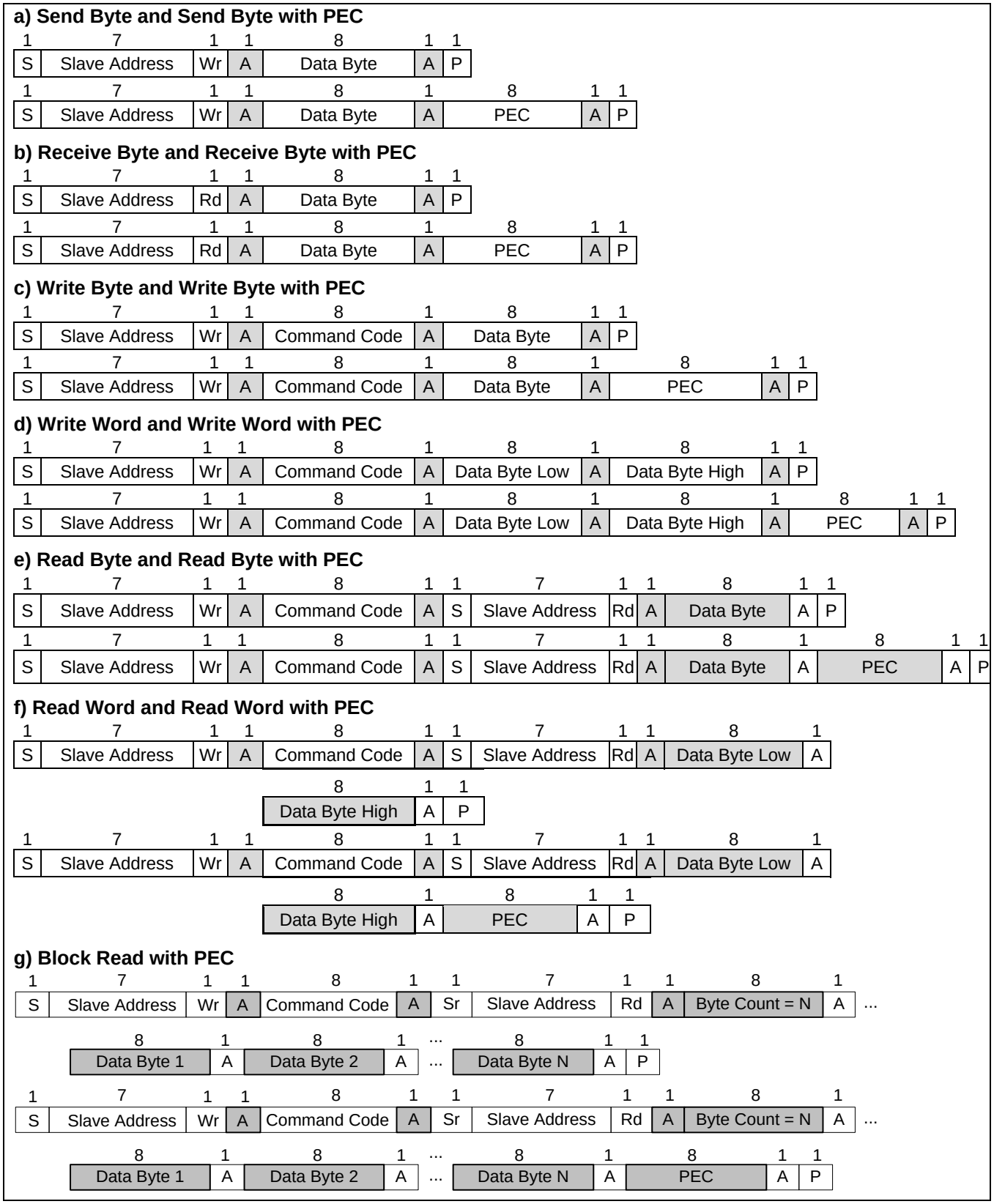


Figure 19: PMBus Message Format

Packet Error Checking (PEC)

The MPQ8785 PMBus interface supports the use of the PEC byte. The PEC byte is transmitted by the MPQ8785 during a read transaction or sent by the bus host during a write transaction.

The PEC byte is used by the bus host or the MPQ8785 to detect errors during a bus transaction (depending on whether the transaction is a read or a write). If the host determines that the PEC byte read during a read transaction is incorrect, it can decide to repeat the read if necessary. If the MPQ8785 determines that the PEC byte sent during a write transaction is incorrect, it ignores the command (does not execute it) and sets a status flag. Within a group command, the host can choose whether to send a PEC byte as part of the message to the MPQ8785.

Data and Numerical Formats

The MPQ8785 uses a direct format for its internal registers to represent real-world values such as voltage, current, power, and temperature.

All numbers without a suffix in this document are decimals, unless explicitly designated otherwise.

Numbers in the binary format are indicated by the prefix “n’b”, where n is the binary count. For example, 5’b01010 indicates a 5-bit binary data, and the data is 01010.

The suffix “h” indicates a hexadecimal format, which is used for the register address numbers in this document.

The symbol “0x” indicates a hexadecimal format, which is used for the value in the register. For example, 0xA3 is a 1-byte number whose hexadecimal value is A3.

PMBus Communication Failure

A data transmission fault occurs when the data is not properly transferred between the devices. There are several types of data transmission faults:

- Sending too little data
- Reading too little data
- Sending too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte

PMBus Reporting and Status Monitoring

The MPQ8785 supports real-time monitoring for some operation parameters and statuses through the PMBus interface (see Table 2).

Table 2: PMBus Monitored Parameters and Status

Parameter/Status	PMBus
Output voltage (V_{OUT})	VID Step
Output current (I_{OUT})	62.5mA/LSB
Temperature	1°C/LSB
Input voltage (V_{IN})	25mV/LSB
V_{IN} OV	✓
V_{IN} UVLO	✓
V_{IN} OV warning	✓
V_{IN} UV warning	✓
V_{OUT} OV	✓
V_{OUT} UV	✓
Over-temperature (OT)	✓
OT warn	✓
I_{OUT} OC	✓
I_{OUT} OC warning	✓

PMBus/I²C Address and V_{BOOT}

To support multiple devices used with the same PMBus/I²C interface, the register MFR_ADDR_PMBUS (D2h) or ADDR pin can be used to configure the PMBus address (see Figure 20).

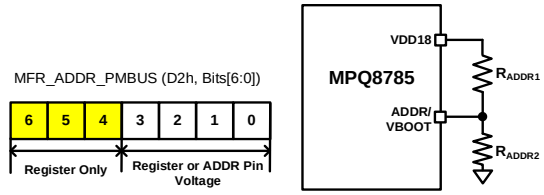


Figure 20: Pin Connection for ADDR/VBOOT

The address is a 7-bit code. The 3MSB is set by the register, while the 4LSB address can either be set by the register or by the ADDR voltage. Address 00h is reserved as an all-call address which can be set for a single chip.

When MFR_ADDR_PMBUS (D2h), bit[7] = 1, the PMBus address of the MPQ8785 is determined by MFR_ADDR_PMBUS (D2h), bits[6:0].

When MFR_ADDR_PMBUS (D2h), bit[7] = 0, the PMBus address of the MPQ8785 is determined by MFR_ADDR_PMBUS (D2h), bits[6:4], and the voltage of the ADDR/VBOOT pin. Connect a resistor divider between VDD18 and GND, and ensure that it is tapped to ADDR/VBOOT (see Figure 20 on page 28). The

internal ADC converts the pin's voltage to select the 4LSB of the PMBus address. Table 3 shows the PMBus address for different resistor values selected for R_{ADDR2}.

Table 3: PMBus Address/VBOOT vs. ADDR Resistor (R_{ADDR1} = 3.32kΩ)

R_{ADDR2} (kΩ)	Slave Address (8)	V_{BOOT} (mV)
0.047	X0h	VBOOT1; 4Dh, bits[9:0]
0.0715	X1h	
0.124	X2h	
0.174	X3h	
0.226	X4h	VBOOT2; 5Eh. bits[9:0]
0.316	X5h	
0.43	X6h	
0.576	X7h	
0.768	X8h	VBOOT3; 5Fh, bits[9:0]
1.05	X9h	
1.43	XAh	
2	XBh	
2.94	XCh	
4.64	XDh	
8.66	XEh	VBOOT4; 6Ah, bits[9:0]
16.5	XFh	

Note:

8) *X* can be 0h~7h, as determined by MFR_ADDR_PMBUS (D2h), bits[6:4]. The default *X* is 2.

If MPQ8785 devices are used in a multi-phase configuration, it is recommended to set the same PMBus address for the master and slave phases.

The voltage of the ADDR/VBOOT pin also determines V_{BOOT}, if this option is selected via MFR_CONFIG_A (D0h), bit[4]. Table 3 also shows V_{BOOT} for different resistor values selected by R_{ADDR2}.

- The X0h~X3h addresses share the same V_{BOOT}, which is controlled by 4Dh, bits[9:0].
- The X4h~X7h addresses share the same V_{BOOT}, which is controlled by 5Eh, bits[9:0].
- The X8h~XDh addresses share the same V_{BOOT}, which is controlled by 5Fh, bits[9:0].
- The XEh~XFh addresses share the same V_{BOOT}, which is controlled by 6Ah, bits[9:0].

Multi-Time Programmable (MTP) Memory

The MPQ8785 provides multiple-time programmable (MTP) memory to store custom configurations. A 4-digit part number suffix is assigned for each application. The default configuration values can be pre-configured at the MPS factory. Customers can also make the configuration by using the STORE_USER_ALL (15h) command via the I^2C master or MPS's PMBus kit.

SUPPORTED PMBUS COMMANDS

Command Code	Command Name	Type	Bytes	Page 0
00h	PAGE	RW	1	✓
01h	OPERATION	RW	1	✓
02h	ON_OFF_CONFIG	RW	1	✓
03h	CLEAR_FAULT	RW	0	✓
08h	CLEAR_LAST_FAULT	RW	0	✓
0Ch	LAST_FAULT_RESTORE	RW	0	✓
10h	WRITE_PROTECTION	RW	1	✓
15h	STORE_ALL	RW	0	✓
16h	RESTORE_ALL	RW	0	✓
19h	CAPABILITY	R	1	✓
1Ch	PMBUS_PS_NUM	RW	1	✓
20h	VOUT_MODE	RW	1	✓
21h	VOUT_COMMAND	RW	2	✓
24h	VOUT_MAX	RW	2	✓
25h	VOUT_MARGIN_HIGH	RW	2	✓
26h	VOUT_MARGIN_LOW	RW	2	✓
29h	VOUT_SCALE_LOOP	RW	2	✓
2Bh	VOUT_MIN	RW	2	✓
30h	COEFFICIENT	Block R	5	✓
35h	VIN_ON	RW	2	✓
36h	VIN_OFF	RW	2	✓
38h	IOUT_CAL_GAIN	RW	2	✓
39h	IOUT_CAL_OFFSET	RW	2	✓
46h	IOUT_OC_FAULT_LIMIT	RW	2	✓
4Ah	IOUT_OC_WARN_LIMIT	RW	2	✓
4Dh	VBOOT_SET_FOR_X0h_ADDR	RW	2	✓
4Fh	OT_FAULT_LIMIT	RW	2	✓
51h	OT_WARN_LIMIT	RW	2	✓
55h	VIN_OV_FAULT_LIMIT	RW	2	✓
57h	VIN_OV_WARN_LIMIT	RW	2	✓
5Eh	VBOOT_SET_FOR_X4h_ADDR	RW	2	✓
5Fh	VBOOT_SET_FOR_X8h_ADDR	RW	2	✓
60h	TON_DELAY	RW	2	✓
61h	TON_RISE	RW	2	✓
64h	TOFF_DELAY	RW	2	✓
65h	TOFF_FALL	RW	2	✓
6Ah	VBOOT_SET_FOR_XEh_ADDR	RW	2	✓
79h	STATUS_WORD	R	2	✓
7Ah	STATUS_VOUT	R	1	✓
7Bh	STATUS_IOUT	R	1	✓
7Ch	STATUS_INPUT	R	1	✓
7Dh	STATUS_TEMPERATURE	R	1	✓
7Eh	STATUS_CML	R	1	✓
80h	REV_ID	R	1	✓
88h	READ_VIN	R	2	✓
8Bh	READ_VOUT	R	2	✓
8Ch	READ_IOUT	R	2	✓
8Dh	READ_TEMPERATURE	R	2	✓
98h	PMBUS_REV_CONST	R	1	✓
99h	MFR_ID	Block R	3	✓
9Bh	MFR_REVISION	Block R	1	✓
C0h	MFR_CONFIG_ID	RW	2	✓
C1h	MFR_CONFIG_CODE_REV	RW	2	✓

SUPPORTED PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	Page 0
C2h	MFR_PRODUCT_REV_USER	RW	2	✓
C3h	MFR_SILICON_REV	RW	1	✓
C5h	MFR_APS_LEVEL	RW	2	✓
D0h	MFR_CONFIG_A	RW	2	✓
D1h	MFR_FS_CFG	RW	2	✓
D2h	MFR_ADDR_PMBUS	RW	2	✓
D3h	MFR_VOUT_RATE	RW	2	✓
D4h	MFR_PWM_TIME_CFG	RW	2	✓
D5h	MFR_PWM_TIME_CFG2	RW	2	✓
D6h	MFR_PHASE_BLANK_TIME	RW	2	✓
D7h	MFR_PHASE_SLOPE_BLANK_TIME	RW	2	✓
D8h	MFR_SLOPE_BLANK_TIME	RW	2	✓
D9h	MFR_BLANK_TIME_LV	RW	2	✓
DAh	MFR_SLOPE_CNT_DCM	RW	2	✓
DBh	MFR_SLOPE_SR_DCM	RW	2	✓
DCh	MFR_SW_BLOCK_LIMIT	RW	2	✓
DDh	MFR_VCOMP	RW	2	✓
DEh	MFR_DROOP_CFG	RW	2	✓
DFh	MFR_CONFIG_B	RW	2	✓
E0h	MFR_DC_LOOP_CTRL	RW	2	✓
E1h	MFR_CB_LOOP_CTRL	RW	2	✓
E2h	MFR_FS_LOOP_CTRL	RW	2	✓
E3h	MFR_VIN_CFG	RW	2	✓
E4h	MFR_VIN_SCALE	RW	2	✓
E5h	MFR_TEMP_TUNE	RW	2	✓
E6h	MFR_PROTECT_CFG	RW	2	✓
E7h	MFR_PROTECT_LEVEL	RW	2	✓
E8h	MFR_PRT_DELAY	RW	2	✓
E9h	SMBALERT_MASK	RW	2	✓
EAh	MFR_NOCP_OCP_SET	RW	2	✓
EBh	MFR_LEVEL_SEL2	RW	2	✓
ECh	MFR_PG_CFG	RW	2	✓
EDh	MFR_PS_CTRL	RW	2	✓
EEh	MFR_PMBUS_LOCK	RW	2	✓
EFh	MFR_SET_SYNC_CFG	RW	2	✓
F0h	MFR_SLAVE_PROTECT	RW	2	✓
F1h	MFR_CTRL	RW	2	✓
F2h	MFR_AUTO_SLOPE_CFG	RW	2	✓
F3h	MFR_SLOPE_DELTA_LIMIT	RW	2	✓
F4h	MFR_RETRY_TIMES	RW	2	✓
F5h	MFR_CFG_EXT	RW	2	✓
F6h	MFR_CDROOP_SET	RW	2	✓
F7h	MFR_CFG_BACKUP	RW	2	✓
F8h	CHECK_SUM_FUNC	R	2	✓
FAh	PROTECTION	R	2	✓
FBh	PROTECTION_LAST	R	2	✓
FCh	MFR_VBOOT_CFG	RW	2	✓
FEh	CLEAR_NVM_FAULT	RW	0	✓

PAGE 0 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 0 provides the ability to configure, control, and monitor all registers — including the non-volatile memory (NVM) and test mode — through only one physical address.

Bits	Access	Bit Name	Description
7:1	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
0	R/W	PAGE	Selects the register page. 1'b0: All PMBus operating commands on Page 0 1'b1: All PMBus test mode commands

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 0 turns the output on or off in conjunction with the input from the CTRL pin, and sets the output voltage (V_{OUT}) to the upper or lower margin voltages. The MPQ8785 remains in the mode set by the OPERATION command until a subsequent OPERATION command is received or a different CTRL state changes the MPQ8785 to another mode.

Bits	Access	Bit Name	Description
7	R/W	ON_OFF_STATE	Controls whether the PMBus device output is on or off. 1'b0: The output is off 1'b1: The output is on
6	R/W	TURN_OFF_ BEHAVIOR	Controls the shutdown behavior. If bit[7] is set to 1, then bit[6] is ignored. If bit[7] is cleared to 0, then: 1'b0: High-impedance (Hi-Z) off 1'b1: Soft shutdown
5:4	R/W	VOLT_CMD_ SOURCE	If the PMBus device output is on (bit[7] = 1), then these bits control the basic source of the V_{OUT} command. 2'b00: The nominal V_{OUT} is set by the PMBus VOUT_COMMAND data 2'b01: The nominal V_{OUT} is set by the PMBus VOUT_MARGIN_LOW data 2'b10: The nominal V_{OUT} is set by the PMBus VOUT_MARGIN_HIGH data 2'b11: Not supported
3:2	R/W	MARGIN_FAULT_ RESPONSE	If the PMBus device output is on (bit[7] = 1) and a margin command causes V_{OUT} to exceed the limit set by the VOUT_OV_FAULT_LIMIT or VOUT_UV_FAULT_LIMIT commands, then bits[3:2] select whether a fault is generated. 2'b01: Faults caused by selecting VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW as the nominal V_{OUT} source are ignored 2'b10: Faults caused by selecting VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW as the nominal V_{OUT} source are triggered according to the settings of the VOUT_OV_FAULT_RESPONSE and VOUT_UV_FAULT_RESPONSE data bytes
1	R/W	TRANSITION_CTRL	Not supported.
0	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.

ON_OFF_CONFIG (02h)

Format: Unsigned binary

The ON_OFF_CONFIG command on Page 0 configures the combination of the CTRL pin input and serial bus commands required to turn the MPQ8785 on and off.

Bits	Access	Bit Name	Description
7:5	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
4:2	R/W	CONFIG_BEHAVIOR	Selects the on/off behavior. 3'b0xx: The device starts up and operates when bias power is available, regardless of the setting on bits[3:0] of this command 3'b1x0: The device turns on and off only by the commands received across the serial bus 3'b101: The device turns on and off only by the CTRL pin 3'b111: The device turns on only when both the commands are received across the serial bus and the CTRL pin commands the device to turn on
1	R/W	CTRL_POLARITY	Sets the polarity of the CTRL pin. 1'b0: Active low (pull CTRL low to start up the device) 1'b1: Active high (pull CTRL high to start up the device)
0	R/W	CTRL_OFF_ACTION	Sets the CTRL pin's action when commanding the device to shut down. 1'b0: Use the configured turn-off delay and falling time 1'b1: Turn off the output and stops transferring energy to the output as quickly as possible

CLEAR_FAULT (03h)

The CLEAR_FAULT command on Page 0 clears all the status faults for the read-only STATUS registers (e.g. STATUS_WORD).

CLEAR_LAST_FAULT (08h)

The CLEAR_LAST_FAULT command on Page 0 clears the last fault that is stored to the NVM during the last power-on. PROTECTION (FAh) indicates the current faults. The last protection values are restored from the multiple-time programmable (MTP) memory and returned to PROTECTION_LAST (FBh). This command clears faults in the NVM, and it also can be configured to clear the restored NVM's last fault (PROTECTION_LAST (FBh)) via MFR_CFG_EXT (F5h), bit[6].

LAST_FAULT_RESTORE (0Ch)

The LAST_FAULT_RESTORE command on Page 0 restores the last faults stored in the NVM to FBh.

WRITE_PROTECTION (10h)

Format: Unsigned binary

The WRITE_PROTECTION command on Page 0 controls writing to the PMBus device.

Bits	Access	Bit Name	Description
7:0	R/W	WRITE_ PROTECTION	8'h00: Enables writes to all commands 8'h20: Disables all writes except to the WRITE_PROTECTION, OPERATION, PAGE, ON_OFF_CONFIG, and VOUT_COMMAND commands 8'h40: Disables all writes except to the WRITE_PROTECTION, OPERATION, and PAGE commands 8'h80: Disables all writes except to the WRITE_PROTECTION commands

STORE_ALL (15h)

The STORE_ALL command on Page 0 stores all registers to the NVM.

RESTORE_ALL (16h)

The RESTORE_ALL command on Page 0 restores all registers from the NVM.

CAPABILITY (19h)

Format: Unsigned binary

The CAPABILITY command on Page 0 provides 1 byte to return key PMBus features supported by the IC.

Bits	Access	Bit Name	Description
7	R	PEC_SUPPORT	1’b0: Packet error checking (PEC) is not supported 1’b1: PEC is supported
6:5	R	MAX_BUS_SPEED	2’b00: The maximum supported bus speed is 100kHz 2’b01: The maximum supported bus speed is 400kHz 2’b10: The maximum supported bus speed is 1MHz 2’b11: Reserved
4	R	SMBALERT_ SUPPORT	1’b0: The device does not have a SMBALERT# pin and does not support the SMBus Alert Response protocol 1’b1: The device has a SMBALERT# pin and does support the SMBus Alert Response protocol
3	R	NUMERIC_FORMAT	1’b0: The numeric data is in Linear11, ULinear16, SLinear16, or direct format 1’b1: The numeric data is in IEEE half-precision floating-point format
2	R	AVSBUS_SUPPORT	1’b0: AVSBus is not supported 1’b1: AVSBus is supported
1:0	R	RESERVED	Unused. Writes are ignored and reads are always 0.

PMBUS_PS_NUM (1Ch)

Format: Unsigned binary

The PMBUS_PS_NUM command on Page 0 sets the phase number when using the PMBus phase-shedding function. When inputting the phase number, the system drops phases to meet this commanded value. This value cannot be stored to the NVM.

Bits	Access	Bit Name	Description
7:6	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
5:0	R/W	PMBUS_PS_NUM	Sets the PMBus phase number.

VOUT_MODE (20h)

Format: Unsigned binary

The VOUT_MODE command on Page 0 sets the V_{OUT} data format.

Bits	Access	Bit Name	Description
7	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
6:5	R/W	MODE_SEL	Selects the voltage data format. 2’b00: Linear format. The exponent is forced to -9 in bits[4:0] of this command 2’b01: VID. The parameter of bits[4:0] of this command is forced to zero 2’b1X: Direct format. The parameter of bits[4:0] of this command is forced to zero and the coefficient is block read in 30h
4:0	R/W	PARAMETERS	Provides more information about the selected mode. If bits[6:5] of this command is selected as VID or direct mode: 5’b00000 If bits[6:5] of this command is selected as linear mode: 5’b10111

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND on Page 0 sets the VID reference voltage (V_{REF}) in PMBus override mode. This value is the real output value, including the VOUT_SCALE coefficient.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:0	R/W	VOUT_COMMAND	Linear mode: VOUT_COMMAND = VID_REF/LSB; LSB = 1.953125mV/LSB. VID mode or direct mode: VOUT_COMMAND = VID_REF/LSB; LSB = 1.5625mV/LSB.

VOUT_MAX (24h)

Format: Unsigned binary

The VOUT_MAX command on Page 0 sets the maximum V_{OUT} limit. This value is the real output value, including the VOUT_SCALE coefficient.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:0	R/W	VOUT_MAX	Sets the maximum V_{REF}. Linear mode: VOUT_MAX = VID_MAX/LSB; LSB = 1.953125mV/LSB. VID mode or direct mode: VOUT_MAX = VID_MAX/LSB; LSB = 1.5625mV/LSB.

VOUT_MARGIN_HIGH (25h)

Format: Unsigned binary

This VOUT_MARGIN_HIGH command on Page 0 sets V_{REF} when OPERATION (01h) is set to margin high. This value is the real output value, including the VOUT_SCALE coefficient.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:0	R/W	VOUT_MARGIN_HIGH	Linear mode: VOUT_MARGIN_HIGH = VID/LSB; LSB = 1.953125mV/LSB. VID mode or direct mode: VOUT_MARGIN_HIGH = VID/LSB; LSB = 1.5625mV/LSB.

VOUT_MARGIN_LOW (26h)

Format: Unsigned binary

This VOUT_MARGIN_LOW command on Page 0 sets V_{REF} when OPERATION (01h) is set to margin low. This value is the real output value, including the VOUT_SCALE coefficient.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:0	R/W	VOUT_MARGIN_LOW	Linear mode: VOUT_MARGIN_LOW = VID/LSB; LSB = 1.953125mV/LSB. VID mode or direct mode: VOUT_MARGIN_LOW = VID/LSB; LSB = 1.5625mV/LSB.

VOUT_SCALE_LOOP (29h)

Format: Unsigned binary

The VOUT_SCALE_LOOP command on Page 0 sets the V_{OUT} divider ratio.

Bits	Access	Bit Name	Description
15:11	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
10:0	R/W	VOUT_SCALE_LOOP	The VOUT_SCALE_LOOP value can be calculated with the following equation: $VOUT\_SCALE\_LOOP = 1024 \times K_R$ K_R can be calculated with the following equation: $K_R = 1 / (R_{DIV1} \times (1 / R_{DIV1} + 1 / R_{DIV2} + 1/80k\Omega))$

VOUT_MIN (2Bh)

Format: Unsigned binary

The VOUT_MIN command on Page 0 sets the minimum V_{OUT} limit. This value is the real output value, including the VOUT_SCALE coefficient.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:0	R/W	VOUT_MIN	Sets the minimum V_{REF}. Linear mode: VOUT_MIN = VID_MIN/LSB; LSB = 1.953125mV/LSB. VID mode or direct mode: VOUT_MIN = VID_MIN/LSB; LSB = 1.5625mV/LSB.

COEFFICIENT (30h)

Format: Unsigned binary

The COEFFICIENT command on Page 0 returns the coefficient value for direct mode. It is block read only.

Byte	Access	Byte Name	Description
4	R	COEFFICIENT1	Returns the coefficient value for direct mode, 0x01.
3	R	COEFFICIENT2	Returns the coefficient value for direct mode, 0x00.
2	R	COEFFICIENT3	Returns the coefficient value for direct mode, 0x00.
1	R	COEFFICIENT4	Returns the coefficient value for direct mode, 0x00.
0	R	COEFFICIENT5	Returns the coefficient value for direct mode, 0x40.

VIN_ON (35h)

Format: Unsigned binary

The VIN_ON command on Page 0 sets the V_{IN} under-voltage lockout (UVLO) rising threshold.

Bits	Access	Bit Name	Description
15:7	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
6:0	R/W	VIN_ON	Sets the V_{IN} UVLO rising threshold. 200mV/LSB, up to 25.4V.

VIN_OFF (36h)

Format: Unsigned binary

The VIN_OFF command on Page 0 sets the V_{IN} UVLO falling threshold.

Bits	Access	Bit Name	Description
15:7	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
6:0	R/W	VIN_OFF	Sets the V_{IN} UVLO falling threshold. 200mV/LSB, up to 25.4V.

IOUT_CAL_GAIN (38h)

Format: Unsigned binary

The IOUT_CAL_GAIN command on Page 0 sets the gain for the output current (I_{OUT}) PMBus report. The reported I_{OUT} is returned via PMBus command READ_IOUT (8Ch).

Bits	Access	Bit Name	Description
15:11	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
10:0	R/W	IOUT_CAL_GAIN	Fixed to 1024.

IOUT_CAL_OFFSET (39h)

Format: Unsigned binary

The IOUT_CAL_OFFSET command on Page 0 sets the offset for the I_{OUT} PMBus report. The reported I_{OUT} is returned via PMBus command READ_IOUT (8Ch).

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	IOUT_CAL_OFFSET	Adds an offset to the I_{OUT} report. 62.5mA/LSB. It is two's complement format.

IOUT_OC_FAULT_LIMIT (46h)

Format: Unsigned binary

The IOUT_OC_FAULT_LIMIT command on Page 0 sets the I_{OUT} total over-current protection (OCP) fault threshold.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	IOUT_OC_FAULT_ LIMIT	The IOUT_OC_FAULT_LIMIT value can be calculated with the following equation: IOUT_OC_FAULT_LIMIT = Actual Value / LSB Where LSB = 1A/LSB.

IOUT_OC_WARN_LIMIT (4Ah)

Format: Unsigned binary

The IOUT_OC_WARN_LIMIT command on Page 0 sets the I_{OUT} total OCP warning threshold.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	IOUT_OC_WARN_ LIMIT	The IOUT_OC_WARN_LIMIT value can be calculated with the following equation: IOUT_OC_WARN_LIMIT = Actual Value / LSB Where LSB = 1A/LSB.

VBOOT_SET_FOR_X0h_ADDR (4Dh)

Format: Unsigned binary

The VBOOT_SET_FOR_X0h_ADDR command on Page 0 sets the boot-up voltage (V_{BOOT}) for X0h, X1h, X2h, and X3h. Resolution = 4 x VID step.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	VBOOT_SET_FOR_X0h_ADDR	Sets V_{BOOT} for X0h, X1h, X2h, and X3h. Resolution = 4 x VID step, where the VID step is determined by 20h (on Page 0), bits[6:5]. These bits work when both D2h, bit[7] = 0 and D0h, bit[4] = 1. Linear mode: 7.81252mV/LSB. VID mode or direct mode: 6.25mV/LSB.

OT_FAULT_LIMIT (4Fh)

Format: Unsigned binary

The OT_FAULT_LIMIT command on Page 0 sets the over-temperature protection (OTP) threshold.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	OT_FAULT_LIMIT	The OT_FAULT_LIMIT value can be calculated with the following equation: OT_FAULT_LIMIT = Actual Value / LSB Where LSB = 1°C/LSB.

OT_WARN_LIMIT (51h)

Format: Unsigned binary

The OT_WARN_LIMIT command on Page 0 sets the over-temperature (OT) warning threshold.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	OT_WARN_LIMIT	The OT_WARN_LIMIT value can be calculated with the following equation: OT_WARN_LIMIT = Actual Value / LSB Where LSB = 1°C/LSB.

VIN_OV_FAULT_LIMIT (55h)

Format: Unsigned binary

The VIN_OV_FAULT_LIMIT command on Page 0 sets the V_{IN} over-voltage protection (OVP) threshold.

Bits	Access	Bit Name	Description
15:7	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
6:0	R/W	VIN_OV_FAULT_LIMIT	Sets the V_{IN} OVP threshold. 200mV/LSB, up to 25.4V.

VIN_OV_WARN_LIMIT (57h)

Format: Unsigned binary

The VIN_OV_WARN_LIMIT command on Page 0 sets the V_{IN} over-voltage (OV) warning threshold.

Bits	Access	Bit Name	Description
15:7	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
6:0	R/W	VIN_OV_WARN_LIMIT	Sets the V_{IN} OV warning threshold. 200mV/LSB, up to 25.6V.

VBOOT_SET_FOR_X4h_ADDR (5Eh)

Format: Unsigned binary

The VBOOT_SET_FOR_X4h_ADDR command on Page 0 sets V_{BOOT} for X4h, X5h, X6h, and X7h. Resolution = 4 x VID step.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	VBOOT_SET_FOR_X4h_ADDR	Sets V_{BOOT} for X4h, X5h, X6h, and X7h. Resolution = 4 x VID step, where the VID step is determined by 20h (on Page 0), bits[6:5]. These bits work when both D2h, bit[7] = 0 and D0h, bit[4] = 1. Linear mode: 7.81252mV/LSB. VID mode or direct mode: 6.25mV/LSB.

VBOOT_SET_FOR_X8h_ADDR (5Fh)

Format: Unsigned binary

The VBOOT_SET_FOR_X8h_ADDR sets V_{BOOT} for X8h, X9h, XAh, XBh, XCh, and XDh. Resolution = 4 x VID step.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	VBOOT_SET_FOR_X8h_ADDR	Sets V_{BOOT} for X8h, X9h, XAh, XBh, XCh, and XDh. Resolution = 4 x VID step, where the VID step is determined by 20h (on Page 0), bits[6:5]. These bits work when both D2h, bit[7] = 0 and D0h, bit[4] = 1. Linear mode: 7.81252mV/LSB. VID mode or direct mode: 6.25mV/LSB.

TON_DELAY (60h)

Format: Unsigned binary

The TON_DELAY command on Page 0 sets the delay time from when a start command is received (as configured by the ON_OFF_CONFIG command) to when V_{REF} starts to rise.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	TON_DELAY	The TON_DELAY value can be calculated with the following equation: TON_DELAY = Actual Value / LSB Where LSB = 0.1ms/LSB.

TON_RISE (61h)

Format: Unsigned binary

The TON_RISE command on Page 0 sets the time from when V_{REF} starts to rise to when V_{REF} reaches the target voltage.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	TON_RISE	The TON_RISE value can be calculated with the following equation: TON_RISE = Actual Value / LSB Where LSB = 0.1ms/LSB.

TOFF_DELAY (64h)

Format: Unsigned binary

The TOFF_DELAY command on Page 0 sets the delay time from when a stop command is received (as configured by the ON_OFF_CONFIG command) to when V_{REF} starts to shut down.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	TOFF_DELAY	The TOFF_DELAY value can be calculated with the following equation: TOFF_DELAY = Actual Value / LSB Where LSB = 0.1ms/LSB.

TOFF_FALL (65h)

Format: Unsigned binary

The TOFF_FALL command on Page 0 sets the time from when V_{REF} starts to shut down to when V_{REF} drops to 0V.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	TOFF_FALL	The TOFF_FALL value can be calculated with the following equation: TOFF_FALL = Actual Value / LSB Where LSB = 0.1ms/LSB.

VBOOT_SET_FOR_XEh_ADDR (6Ah)

Format: Unsigned binary

The VBOOT_SET_FOR_XEh_ADDR sets V_{BOOT} for XEh and XFh. Resolution = 4 x VID step.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	VBOOT_SET_FOR_XEh_ADDR	Sets V_{BOOT} for XEh and XFh. Resolution = 4 x VID step, where VID step is determined by 20h (on Page 0), bits[6:5]. These bits work when both D2h, bit[7] = 0 and D0h, bit[4] = 1. Linear mode: 7.81252mV/LSB. VID mode or direct mode: 6.25mV/LSB.

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command on Page 0 returns 2 bytes of information with a summary of the device's fault/warning condition. The higher byte provides more detailed information of the fault conditions. The lower byte is shared with STATUS_BYTE (78h).

Bits	Access	Bit Name	Description
15	R	VOUT	Indicates that a V_{OUT} fault or warning has occurred.
14	R	IOUT_POUT	Indicates that an output current (I_{OUT}) or output power (P_{OUT}) fault or warning has occurred.
13	R	INPUT	Indicates that a V_{IN}, input current (I_{IN}), or input power (P_{IN}) fault or warning has occurred.
12	R	RESERVED	Unused.
11	R	PG_STATUS	Indicates power good.
10:9	R	RESERVED	Unused. Writes are ignored and reads are always 0.

8	R	WATCH_DOG	Indicates an internal calculation state machine watchdog overflow fault.
7	R	BUSY	The PMBus cannot be written because it is in MTP copy state.
6	R	OFF	This bit is asserted if the MPQ8785 is not providing power to the output, regardless of the reason, including not being enabled.
5	R	VOUT_OV_FAULT	Indicates that an output over-voltage (OV) fault has occurred.
4	R	IOUT_OC_FAULT	Indicates that an output over-current (OC) fault has occurred.
3	R	RESERVED	Unused. Writes are ignored and reads are always 0.
2	R	TEMPERATURE	Indicates that a temperature fault or warning has occurred.
1	R	CML	Indicates that a communication, memory, or logic fault has occurred.
0	R	DRMOS_FAULT	Indicates a DrMOS fault.

STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 0 returns 1 byte of information with the detailed V_{OUT} fault and warning status.

Bits	Access	Bit Name	Description
7	R	VOUT_OV_FAULT	Indicates an output over-voltage (OV) fault
6:5	R	RESERVED	Unused. Writes are ignored and reads are always 0.
4	R	VOUT_UV_FAULT	Indicates an output under-voltage (UV) fault.
3	R	VOUT_MAX_MIN	Indicates that an attempt has been made to set V_{OUT} to exceed the limit allowed by the VOUT_MAX command or below the limit allowed by the VOUT_MIN command.
2:0	R	RESERVED	Unused. Writes are ignored and reads are always 0.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 0 returns 1 byte of information with the detailed I_{OUT} fault and warning status.

Bits	Access	Bit Name	Description
7	R	IOUT_OC_FAULT	Indicates an output over-current (OC) fault.
6	R	IOUT_OC_LV_FAULT	Indicates an output OC and low voltage fault.
5	R	IOUT_OC_WARNING	Indicates an output OC warning.
4	R	IOUT_UC_FAULT	Indicates an output under-current fault.
3	R	CYCLE_BY_CYCLE_OCP	Indicates per-phase OCP.
2:0	R	RESERVED	Unused. Writes are ignored and reads are always 0.

STATUS_INPUT (7Ch)

Format: Unsigned binary

The STATUS_INPUT command on Page 0 returns 1 byte of information with detailed input fault and warning status.

Bits	Access	Bit Name	Description
7	R	VIN_OV_FAULT	Indicates an input over-voltage (OV) fault.
6	R	VIN_OV_WARNING	Indicates an input OV warning.

5:4	R	RESERVED	Unused. Writes are ignored and reads are always 0.
3	R	VIN_UVLO	Indicates V_{IN} under-voltage lockout (UVLO).
2:0	R	RESERVED	Unused. Writes are ignored and reads are always 0.

STATUS_TEMPERATURE (7Dh)

Format: Unsigned binary

The STATUS_TEMPERATURE command on Page 0 returns 1 byte of information with the temperature-related fault and warning status.

Bits	Access	Bit Name	Description
7	R	OT_FAULT	Indicates an over-temperature (OT) fault.
6	R	OT_WARNING	Indicates an OT warning.
5:1	R	RESERVED	Unused. Writes are ignored and reads are always 0.
0	R	OT_SELF	Sets the controller's die OT condition.

STATUS_CML (7Eh)

Format: Unsigned binary

The STATUS_CML command on Page 0 returns 1 byte of information with PMBus communication-related faults.

Bits	Access	Bit Name	Description
7	R	RESERVED	Indicates invalid or unsupported command received.
6	R	INVALID_DATA	Indicates invalid or unsupported data received.
5	R	PEC_FAILED	Indicates that the PMBus PEC failed.
4	R	MTP_CRC_FAULT	Indicates that the NVM has a cyclic redundancy check (CRC) fault.
3:2	R	RESERVED	Unused. Writes are ignored and reads are always 0.
1	R	COMMU_OTHER_ FAULT	Indicates two communication faults: a reading invalid command, or a start/stop command that occurs when the command data is communicating.
0	R	MTP_FAULT	Indicates that the NVM has a signature fault.

REV_ID (80h)

Format: Unsigned binary

The REV_ID command on Page 0 reads the silicon revision number.

Bits	Access	Bit Name	Description
7:0	R	REV_ID	Reads the silicon revision number.

READ_VIN (88h)

Format: Unsigned binary

The READ_VIN command on Page 0 provides 2 bytes to return the sensed V_{IN} based on the VINSENS pin. READ_VIN = (VINSENS (in V) / 1.6 x 1024 + E3h, bits[3:0]) x 2^8 / E4h, bits[10:0].

Bits	Access	Bit Name	Description
15:0	R	READ_VIN	This bit is in VID mode with 25mV/LSB.

READ_VOUT (8Bh)

Format: Unsigned binary

The READ_VOUT command on Page 0 returns the sensed (VSEN+) - (VSEN-) voltage in the same format as the VOUT_MODE command. It includes the VOUT_SCALE_LOOP coefficient.

Bits	Access	Bit Name	Description
15:0	R	READ_VOUT	Linear mode: V_{OUT_ACTUAL} = READ_VOUT x LSB; LSB = 1.953125mV/LSB. Direct mode or VID mode: V_{OUT_ACTUAL} = READ_VOUT x LSB; LSB = 1.5625mV/LSB. The maximum supported voltage is 6.4V.

READ_IOUT (8Ch)

Format: Unsigned binary

The READ_IOUT command on Page 0 returns the sensed I_{OUT}.

Bits	Access	Bit Name	Description
15:0	R	READ_IOUT	The sensed I_{OUT} can be calculated with the following equation: I_{OUT} = READ_IOUT x LSB Where LSB = 62.5mA/LSB.

READ_TEMPERATURE (8Dh)

Format: Unsigned binary

The READ_TEMPERATURE command on Page 0 returns the sensed temperature.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R	READ_ TEMPERATURE	The sensed temperature can be calculated with the following equation: Temperature = READ_TEMPERATURE x LSB Where LSB = 1°C/LSB.

PMBUS_REV_CONST (98h)

Format: Unsigned binary

The PMBUS_REV_CONST command on Page 0 returns the revision of PMBus to which the device is compliant.

Bits	Access	Bit Name	Description
7:0	R	PMBUS_REV_ CONST	Always returns 0x33. This means the IC supports PMBus revision to 1.3.

MFR_ID (99h)

Format: Unsigned binary

The MFR_ID command on Page 0 reads the unique identification for the voltage regulator (VR) vendor. It is a read-only block.

Byte	Access	Byte Name	Description
2	R	ID_CONST1	Returns the unique identification for the VR vendor, 0x4D, which presents “M.”
1	R	ID_CONST2	Returns the unique identification for the VR vendor, 0x50, which presents “P.”
0	R	ID_CONST3	Returns the unique identification for the VR vendor, 0x53, which presents “S.”

MFR_REVISION (9Bh)

Format: Unsigned binary

The MFR_REVISION command on Page 0 reads the silicon revision track number.

Byte	Access	Byte Name	Description
0	R	REV_CONST	Reads the manufacturer's revision number. This value can be configured via C3h.

MFR_CONFIG_ID (C0h)

Format: Unsigned binary

The MFR_CONFIG_ID command on Page 0 provides 2 bytes to set the product's 4-digit part number suffix. Contact an MPS FAE to obtain the 4-digit code.

Bits	Access	Bit Name	Description
15:0	R/W	MFR_CONFIG_ID	Sets the 4-digit part number suffix.

MFR_CONFIG_CODE_REV (C1h)

Format: Unsigned binary

The MFR_CONFIG_CODE_REV command on Page 0 provides 2 bytes to recognize different parts and set the configuration code revision.

Bits	Access	Bit Name	Description
15:13	R/W	PART_ RECOGNIZATION	Recognizes different parts.
12:0	R/W	MFR_CONFIG_ CODE_REV	Sets the configuration code revision.

MFR_PRODUCT_REV_USER (C2h)

Format: Unsigned binary

The MFR_PRODUCT_REV_USER command on Page 0 provides 2 bytes for users to track the product revision.

Bits	Access	Bit Name	Description
15:0	R/W	MFR_PRODUCT_ REV_USER	Allows the customer to store the product revision.

MFR_SILICON_REV (C3h)

Format: Unsigned binary

The MFR_SILICON_REV command on Page 0 stores the silicon revision number. It can also read through 9Bh.

Bits	Access	Bit Name	Description
7:0	R/W	MFR_SILICON_REV	Stores the silicon revision number.

MFR_APS_LEVEL (C5h)

Format: Unsigned binary

The MFR_APS_LEVEL command on Page 0 sets the automatic phase-shedding (APS) current threshold.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:6	R/W	MFR_APSI_HYS	Sets the current hysteresis for APS. 1A/LSB.
5:0	R/W	MFR_PHL	Reserved.

MFR_CONFIG_A (D0h)

Format: Unsigned binary

The MFR_CONFIG_A command on Page 0 sets some IC configurations.

Bits	Access	Bit Name	Description
15:14	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
13	R/W	MFR_ZCD_BLANK_EN	Fixed to 0.
12	R/W	MFR_ZCD_EN	Fixed to 0.
11	R/W	MFR_OSR_MODE	Selects the pulse-width modulation (PWM) behavior in overshoot reduction (OSR) mode. When OSR is detected, PWM is forced low until OSR is cleared. This results in two options for PWM behavior: 1’b0: Continues outputting PWM 1’b1: Outputs PWM until the next SET signal
10	R/W	MFR_OSR_EN	Enables the OSR function. 1’b0: Disabled 1’b1: Enabled
9	R/W	MFR_PHASE_UPD_CFG	Reserved.
8	R/W	MFR_SLOPE_LEAKAGE	Enables the low leakage switch of the slope in discontinuous conduction mode (DCM). 1’b0: Disabled 1’b1: Enabled
7	R/W	MFR_NOCP_EN	Enables the negative over-current protection (NOCP) function. PWM is forced high for some time when this function is enabled. 1’b0: Disabled 1’b1: Enabled
6	R	MFR_HIZ_HIGH_BLOCK_EN	Fixed to 1.
5	R/W	MFR_OCP_SS_BLK	Selects whether OCP is blocked during the soft-start period. 1’b0: Do not block OCP during soft start 1’b1: Block OCP during soft start
4	R/W	MFR_VBOOT_CFG	Configures V_{BOOT} via the register or VBOOT pin. 1’b0: The register configures V_{BOOT} via FCh, bits[11:0] 1’b1: The pin configures V_{BOOT} via the ADDR/VBOOT pin
3:0	R/W	MFR_DELAY_MASTER	Reserved.

MFR_FS_CFG (D1h)

Format: Unsigned binary

The MFR_FS_CFG command on Page 0 configures the system's switching frequency (f_{SW}) and initial slope.

Bits	Access	Bit Name	Description
15:9	R/W	MFR_SLOPE_SW_INIT	Sets the initial slope before P_{OUT}. This bit outputs the slope before V_{OUT} compensation, which reduces overshoot at the beginning. Bit[15] is the enable bit. If this function is enabled, the slope counter is fixed to 10'd80, and the slope capacitor is fixed to 1.85pF. Bits[14:9] set the initial slope value by configuring the slope current. 250nA/LSB.
8:0	R/W	MFR_FS	Configures the system's operating f_{SW}. It has a minimum limit of 300kHz when the input data is 0. 10kHz/LSB. The final f_{SW} can be calculated with the following equation: (MFR_FS x 10 + 300) (in kHz)

MFR_ADDR_PMBUS (D2h)

Format: Unsigned binary

The MFR_ADDR_PMBUS command on Page 0 sets the PMBus address.

Bits	Access	Bit Name	Description
15:11	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
10:8	R/W	MFR_I2C_TIMEOUT_CFG	Configures the I^2C timeout function. Bit[10] sets whether the I^2C timeout resets the I^2C state machine. 1'b0: Do not reset 1'b1: Reset Bit[9] sets whether the SDA line timeout is enabled. 1'b0: Disabled 1'b1: Enabled Bit[8] sets whether the CLK line timeout is enabled. 1'b0: Disabled 1'b1: Enabled
7	R/W	MFR_ADDR_CFG	Selects the PMBus address, which is configured via the ADDR/VBOOT pin or register. When this bit is configured by ADDR/VBOOT, the final PMBus address is MFR_ADDR, bits[6:4] with ADDR/VBOOT configured via 4 bits. When this bit is configured via the register, the final PMBus address is set via bits[6:0]. 1'b0: Configured via ADDR/VBOOT 1'b1: Configured via the register
6:0	R/W	MFR_ADDR	Defines the final PMBus address. If the final PMBus address is configured to 7'h00, this bit is forced to 7'h3F to avoid 00h, which is the all-call address.

MFR_VOUT_RATE (D3h)

Format: Unsigned binary

The MFR_VOUT_RATE command on Page 0 sets the dynamic VID transition slew rate. The slew rate is VOUT_RATE_STEP / VOUT_RATE_TIME. The final slew rate is also related to the V_{OUT} divider.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:9	R/W	VOUT_RATE_STEP	Configures the DVID step. The final step is VOUT_RATE_STEP + 1. It is 1.5625mV/LSB for the internal reference.
8:0	R/W	VOUT_RATE_TIME	Configures the time of each VID step to control the DVID slew rate. 200ns/LSB.

MFR_PWM_TIME_CFG (D4h)

Format: Unsigned binary

The MFR_PWM_TIME_CFG command on Page 0 configures the minimum PWM time.

Bits	Access	Bit Name	Description
15:14	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
13:10	R/W	MFR_NOCP_TIME	Configures the on time (t_{ON}) when NOCP is detected. 40ns/LSB.
9:6	R/W	MFR_MINON_TIME	Configures the minimum t_{ON}. 10ns/LSB. The minimum value is limited to 30ns.
5:0	R/W	MFR_MIN_HIZ_TIME	Configures the minimum PWM Hi-Z time. 10ns/LSB. The minimum time is limited to 100ns.

MFR_PWM_TIME_CFG2 (D5h)

Format: Unsigned binary

The MFR_PWM_TIME_CFG2 command on Page 0 configures the minimum PWM time.

Bits	Access	Bit Name	Description
15:11	R/W	MFR_OSR_BLOCK_ TIME	Sets the OSR signal filter time. It filters the positive and negative narrow pulse of OSR. 10ns/LSB.
10:6	R/W	MFR_MINOFF_TIME	Sets the minimum PWM off time (t_{OFF}). 20ns/LSB.
5:0	R/W	MFR_MIN_LOW_ TIME	Sets the PWM minimum low time. 10ns/LSB.

MFR_PHASE_BLANK_TIME (D6h)

Format: Unsigned binary

The MFR_PHASE_BLANK_TIME command on Page 0 sets the phase blank time between two consecutive phases.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:6	R/W	MFR_PHASE_ BLANK_TIME2	Reserved.
5:0	R/W	MFR_PHASE_ BLANK_TIME1	Reserved.

MFR_PHASE_SLOPE_BLANK_TIME (D7h)

Format: Unsigned binary

The MFR_PHASE_SLOPE_BLANK_TIME command on Page 0 sets the slope compensation reset time and phase blank time between two consecutive phases.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:6	R/W	MFR_SLOPE_ BLANK_TIME1	Reserved.
5:0	R/W	MFR_PHASE_ BLANK_TIME3	Reserved.

MFR_SLOPE_BLANK_TIME (D8h)

Format: Unsigned binary

The MFR_SLOPE_BLANK_TIME command on Page 0 sets the slope compensation reset time.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:12	R/W	MFR_TON_EXT_EN	Fixed to 0.
11:6	R/W	MFR_SLOPE_ BLANK_TIME3	Reserved.
5:0	R/W	MFR_SLOPE_ BLANK_TIME2	Reserved.

MFR_BLANK_TIME_LV (D9h)

Format: Unsigned binary

The MFR_BLANK_TIME_LV command on Page 0 sets the phase number threshold for the slope compensation reset time and phase blanking time between two consecutive phases.

Bits	Access	Bit Name	Description
15:13	R/W	MFR_ZCD_LEVEL_ SEL	Fixed to 0.
12:10	R/W	MFR_ZCD_BLANK_ TIME	Fixed to 0.
9:5	R/W	MFR_BLANK_TIME_ LV2	Reserved.
4:0	R/W	MFR_BLANK_TIME_ LV1	Reserved.

MFR_SLOPE_CNT_DCM (DAh)

Format: Unsigned binary

The MFR_SLOPE_CNT_DCM command on Page 0 sets the DCM slope compensation count.

Bits	Access	Bit Name	Description
15:10	R/W	MFR_VCOMP_TUNE	Reserved.
9:0	R/W	MFR_SLOPE_CNT_ DCM	Sets the slope count in DCM. 5ns/LSB.

MFR_SLOPE_SR_DCM (DBh)

Format: Unsigned binary

The MFR_SLOPE_SR_DCM command on Page 0 sets the slope current and capacitances for DCM.

Bits	Access	Bit Name	Description
15:10	R/W	MFR_VCOMP_TUNE	Reserved.
9:6	R/W	MFR_SLOPE_SR_ DCM	Sets the slope capacitance with 1.85pF/LSB.
5:0	R/W	MFR_SLOPE_SR_ DCM	Sets the slope current with 250nA/A.

MFR_SW_BLOCK_LIMIT (DCh)

Format: Unsigned binary

The MFR_SW_BLOCK_LIMIT command on Page 0 sets the SET signal block time when exiting DCM and detecting the load transient threshold with the f_{SW} compressed method.

Bits	Access	Bit Name	Description
15:10	R/W	MFR_SW_HLF_LIMIT	Sets the high- and low-frequency detection threshold. It also detects the load transient. This period is the SET signal period and automatically calculates the theoretical SET signal period according to the phase number and f_{SW}. The threshold is related to the SET signal period. Bit[15] enables the high-frequency detection threshold. 1'b0: Disabled 1'b1: Enabled Bits[14:13] set the high-frequency detection threshold. 2'b00: Invalid 2'b01: Invalid 2'b10: 81/128 of the theoretical set period 2'b11: 72/128 of the theoretical set period Bits[12:10] are fixed to 0.
9:4	R/W	MFR_SW_LIMIT	Sets the count number for detecting load transient with the f_{SW} compressed method. When a load transient occurs, the SET signal is compressed to a high frequency. If the SET signal continues to be compressed with a number bigger than this register value, then the controller acknowledge it as a load transient. Bits[9:7] set the high-frequency detection count number. Bits[6:4] are fixed to 0.
3:0	R/W	MFR_SW_BLOCK_SET	Sets the blank time to block the SET signal when exiting DCM. It is effective when MFR_SLOPE_LEAKAGE is enabled, as this may result in noise for the slope when the switch turns on. 10ns/LSB.

MFR_VCOMP (DDh)

Format: Unsigned binary

The MFR_VCOMP command on Page 0 sets the compensation voltages in DCM and CCM.

Bits	Access	Bit Name	Description
15:13	R/W	MFR_RSUM_SEL	Selects R_{SUM}, which has 8 selections: 3'b000: 0.25kΩ 3'b001: 0.5kΩ 3'b010: 0.75kΩ 3'b011: 1kΩ 3'b100: 1.25kΩ 3'b101: 1.5kΩ 3'b110: 1.75kΩ 3'b111: 2kΩ
12:10	R/W	MFR_IMON_GAIN	Selects the IMON current gain, which has 8 selections: 3'b000: 1/8 gain 3'b001: 2/8 gain 3'b010: 3/8 gain 3'b011: 4/8 gain 3'b100: 5/8 gain 3'b101: 6/8 gain 3'b110: 7/8 gain 3'b111: 8/8 gain

9:5	R/W	MFR_VCOMP_DCM	Sets the compensation voltage in DCM. The resolution to V_{OUT} is different according to the remote-sense gain. If gain = 1, the resolution is 2.5mV/LSB. If gain = 1/2, the resolution is 5mV/LSB.
4:0	R/W	MFR_VCOMP_CCM	Sets the compensation voltage in CCM. The resolution to V_{OUT} is different according to the remote-sense gain. If gain = 1, the resolution is 2.5mV/LSB. If gain = 1/2, the resolution is 5mV/LSB.

MFR_DROOP_CFG (DEh)

Format: Unsigned binary

The MFR_DROOP_CFG command configures the droop function and VID filter function.

Bits	Access	Bit Name	Description
15	R/W	MFR_RIMON_SEL	Selects R_{IMON}. 1'b1: 5kΩ 1'b0: 2.5kΩ
14	R/W	MFR_FILTER_ON_EN	Enables the VID DAC filter. 1'b1: Enabled 1'b0: Disabled
13	R/W	MFR_DC_DROOP_SEL	Selects the droop resistors (R_{DROOP}).
12:10	R/W	MFR_DROOP_GAIN_SEL	Sets the droop current gain with 8 selections. The gain is 8/64 to 15/64. 3'b000: 8/64 3'b001: 9/64 3'b010: 10/64 3'b011: 11/64 3'b100: 12/64 3'b101: 13/64 3'b110: 14/64 3'b111: 15/64
9:7	R/W	MFR_AC_DROOP_SEL	Selects the AC droop reference point and bandwidth. Bit[9] is fixed to 0. Bits[8:7] select the AC droop bandwidth. 2'b00: 25kHz 2'b01: 50kHz 2'b10: 6kHz 2'b11: 10kHz
6:5	R/W	MFR_DC_DROOP_SEL	Selects R_{DROOP}. 3'b000: DROOP R0. Disconnect 3'b001: DROOP R1. 0.125kΩ 3'b010: DROOP R2. 0.25kΩ 3'b011: DROOP R3. 0.375kΩ 3'b100: DROOP R4. 0.625kΩ 3'b101: DROOP R5. 1kΩ 3'b110: DROOP R6. 1.5kΩ 3'b111: DROOP R7. 2.5kΩ
4	R/W	MFR_DROOP_SET	Selects the droop mode. 1'b0: DC droop mode 1'b1: AC droop mode

3:0	R/W	MFR_FILTER_SET	Sets the VID filter function. Bit[3] is fixed to 1. Bit[2] is fixed to 1. Bits[1:0] select the VID filter bandwidth. 2'b00: 1µs 2'b01: 3µs 2'b10: 5µs 2'b11: 7µs

MFR_CONFIG_B (DFh)

Format: Unsigned binary

The MFR_CONFIG_B command on Page 0 sets some IC configurations.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14	R/W	MFR_MASTER_SET_CFG	Reserved.
13	R/W	MFR_RAMP_SET_CFG	Fixed to 0.
12:10	R/W	MFR_RAMP_DISC	Configures the RAMP discharge ability. 3'b000: x1 gain of discharge 3'b001: x2 gain of discharge 3'b010: x3 gain of discharge 3'b011: x4 gain of discharge 3'b100: x5 gain of discharge 3'b101: x6 gain of discharge 3'b110: x7 gain of discharge 3'b111: x8 gain of discharge
9	R/W	MFR_CTRLOFF_CFG	Configures the CTRL pin's off mode. 1'b0: Soft shutdown 1'b1: Hi-Z off
8:6	R/W	MFR_TRANS_CFG	Configures the load transient detection. Bit[8] enables high-/low-frequency detection. 1'b0: Disabled 1'b1: Enabled Bit[7] is fixed to 0. Bit[6] enables positive/negative 25mV detection. 1'b0: Disabled 1'b1: Enabled
5	R/W	MFR_MASTER_ALT	Reserved.
4	R/W	MFR_CS_DIS_EN	Reserved.
3	R/W	MFR_DLL_FUNC_RN	Enables the delay line loop line (DLL) function. When the DLL function is enabled, the t_{ON} resolution can be 0.625ns. 1'b0: Disables DLL function 1'b1: Enables DLL function
2	R/W	MFR_SDM_FRAC_EN	Enables the TON_FRAC sigma-delta modulation function. 1'b0: Disables the TON_FRAC sigma-delta modulation function 1'b1: Enables the TON_FRAC sigma-delta modulation function

1	R/W	MFR_DCM_TON_CFG	Configures whether t_{ON} decreases in DCM. If it is enabled, t_{ON} is 3/4 of that in CCM. 1'b0: Disables the t_{ON} reduction function in DCM 1'b1: Enables the t_{ON} reduction function in DCM
0	R/W	MFR_PG_RST_SEL	Selects the ALT/RST pin function. 1'b0: RST function 1'b1: ALT function

MFR_DC_LOOP_CTRL (E0h)

Format: Unsigned binary

The MFR_DC_LOOP_CTRL command on Page 0 sets DC loop configurations.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14	R/W	DC_LOOP_EN_SLAVE	Fixed to 0.
13	R/W	DC_LOOP_EN_CCM	Enables the DC loop in CCM. 1'b0: Disables the DC loop in CCM 1'b1: Enables the DC loop in CCM
12	R/W	DC_LOOP_EN_DCM	Enables the DC loop in DCM. 1'b0: Disables the DC loop in DCM 1'b1: Enables the DC loop in DCM
11:10	R/W	DC_LOOP_TRANS_CTRL	Determines whether to hold the DC loop calculation when a transient or phase number change occurs. Bit[11] determines whether to hold the DC loop in transient. 1'b0: Enables the DC loop in transient 1'b1: Disables the DC loop in transient Bit[10] determines whether to hold the DC loop when the phase number changes. 1'b0: Enables the DC loop when the phase number changes 1'b1: Disables the DC loop when the phase number changes
9:4	R/W	DC_LOOP_PI	Sets the PI value of the DC loop.
3:0	R/W	DC_LOOP_CNT	Sets the time to hold the DC loop when bit[11] or bit[10] is enabled. 100µs/LSB.

MFR_CB_LOOP_CTRL (E1h)

Format: Unsigned binary

The MFR_CB_LOOP_CTRL command on Page 0 sets the current balance loop configurations.

Bits	Access	Bit Name	Description
15:13	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
12	R/W	CB_LOOP_EN_MASTER	Fixed to 0.
11	R/W	CB_LOOP_EN	Reserved.
10:8	R/W	CB_LOOP_TRANS_CTRL	Reserved.
7:4	R/W	CB_LOOP_PI	Reserved.
3:0	R/W	CB_LOOP_CNT	Reserved.

MFR_FS_LOOP_CTRL (E2h)

Format: Unsigned binary

The MFR_FS_LOOP_CTRL command on Page 0 sets the frequency loop configurations.

Bits	Access	Bit Name	Description
15	R/W	FS_LOOP_EN_ SLAVE	Fixed to 0
14	R/W	FS_LOOP_EN	Enables the FS loop. 1'b0: Disabled 1'b1: Enabled
13:11	R/W	FS_LOOP_TRANS_ CTRL	Holds the FS loop when a load transient, DVID, and phase number occur. Bit[13] holds the FS loop in load transient. Bit[12] holds the FS loop when the phase number changes. Bit[11] holds the FS loop in DVID.
10:4	R/W	FS_LOOP_PI	Sets the FS loop PI value.
3:0	R/W	FS_LOOP_CNT	Sets the FS loop hold time. 100μs/LSB.

MFR_VIN_CFG (E3h)

Format: Unsigned binary

The MFR_VIN_CFG command on Page 0 configures the V_{IN}-sense related functions.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8	R/W	MFR_VIN_MUX_SEL	Selects V_{IN} to calculate t_{ON}. There are two options: 1'b0: The real-time sampled V_{IN} to calculate t_{ON} 1'b1: V_{IN} beyond MFR_VIN_HYS to calculate t_{ON}
7:4	R/W	MFR_VIN_HYS	Sets the V_{IN} sense hysteresis, which can be used for t_{ON} calculation. The resolution can be calculated with the following equation: Resolution = 6400 x 4 / MFR_VIN_SCALE (in mV/LSB) MFR_VIN_SCALE is E4h, bits[10:0] in decimal value.
3:0	R/W	MFR_VIN_TUNE	Adjusts and tunes the V_{IN} sense offset. The resolution can be calculated with the following equation: Resolution = 6400 x 2 / MFR_VIN_SCALE (in mV/LSB) MFR_VIN_SCALE is E4h, bits[10:0] in decimal value. It is in two's complement format.

MFR_VIN_SCALE (E4h)

Format: Unsigned binary

The MFR_VIN_SCALE command on Page 0 sets the V_{IN} sense scale loop.

Bits	Access	Bit Name	Description
15:11	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
10:0	R/W	MFR_VIN_SCALE	Sets the V_{IN} sense scale loop, which can be calculated with the following equation: V_{IN} x R1 / (R1 + R2) / 1.6 x 1024 x 512 / MFR_VIN_SCALE / 2 = V_{IN} x 40 Where 40 means the V_{IN} report is 25mV/LSB. The MFR_VIN_SCALE value can be calculated with the following equation: MFR_VIN_SCALE = 4096 x R1 / (R1 + R2)

MFR_TEMP_TUNE (E5h)

Format: Unsigned binary

The MFR_TEMP_TUNE command on Page 0 sets the temperature-sense gain and offset. The temperature is (V_{TEMP} (in V) / 2 / 1.6 x 1024 + TEMP_OFFSET_TUNE - 192) x GAIN_TUNE / 256 = real temperature (1°/LSB).

Bits	Access	Bit Name	Description
15:8	R/W	MFR_TEMP_ OFFSET_TUNE	Sets the temperature sense offset tune.
7:0	R/W	MFR_GAIN_TUNE	Sets the temperature sense gain. The digital temperature sense can be calculated with the following equation: Digital Temperature Sense = T (in °C) x Gain / 2 / 1.6 x 1024 The temperature report can be calculated with the following equation: Temperature Report = Digital Temperature Sense x MFR_GAIN_TUNE / 256

MFR_PROTECT_CFG (E6h)

Format: Unsigned binary

The MFR_PROTECT_CFG command on Page 0 sets the protection configurations.

Bits	Access	Bit Name	Description
15	R/W	MFR_OVP_OFF_ CFG	Configures the V_{OUT} behavior when OVP occurs. 1'b0: Hi-Z off 1'b1: Discharge off Regardless of which mode is selected, the system waits until V_{OUT} enters the OV_EXIT threshold, then starts recycling the power if it is in retry or hiccup mode.
14	R/W	MFR_HIZ_OFF_EN	Reserved.
13	R/W	MFR_OTP_SELF_EN	Enables the controller's OTP function. 1'b0: Disabled 1'b1: Enable
12	R/W	MFR_PROTECT_ ASSERT	Fixed to 1.
11	R/W	MFR_SLAVE_ HICCUP_EN	Reserved.
10	R/W	MFR_SLAVE_ FAULT_EN	Reserved.
9	R/W	MFR_PRD_FAULT_ EN	Enables the PWM period fault. This fault detects whether VOUT_SCALE_LOOP is correctly configured with a proper V_{OUT} divider resistor. If it is not configured correctly, the PWM period is different than the target value. When this function is enabled, the system enters the Hi-Z off state when this fault occurs. 1'b0: Disabled 1'b1: Enabled
8	R/W	MFR_PROTECT_ RECORD	Enables the protection record function. When enabled, this protection is recorded to the NVM. 1'b0: Disabled 1'b1: Enabled
7	R/W	MFR_FAULT_ DETECT	Fixed to 0.

6	R/W	MFR_DRMOS_ FAULT_EN	Enables the DRMOS fault. 1'b0: Disabled 1'b1: Enabled
5	R/W	MFR_OCP_TOTAL_ EN	Enables the OCP total function, which compares READ_IOUT with IOUT_OC_FAULT_LIMIT. If READ_IOUT exceeds IOUT_OC_FAULT_LIMIT for some time, then it triggers this protection. 1'b0: Disabled 1'b1: Enabled
4	R/W	MFR_OCP_PHASE_ EN	Enables the OCP phase shutdown function. The analog sends an OCP signal to the digital. If this signal lasts for some time, then it triggers this protection. 1'b0: Disabled 1'b1: Enabled
3	R/W	MFR_VOUT_UVP_ EN	Enables the V_{OUT} UVP function. 1'b0: Disabled 1'b1: Enabled
2	R/W	MFR_VOUT_OVP_ EN	Fixed to 1.
1	R/W	MFR_OTP_PWR_EN	Enables the DrMOS OTP function. 1'b0: Disabled 1'b1: Enabled
0	R/W	MFR_VIN_ PROTECT_EN	Enables the V_{IN} OVP function. 1'b0: Disabled 1'b1: Enabled

MFR_PROTECT_LEVEL (E7h)

Format: Unsigned binary

The MFR_PROTECT_LEVEL command on Page 0 configures some protection levels, including OSM, frequency protection, and retry delay time.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:8	R/W	MFR_OSM_CFG	Configures OSM protection. Bits[11:8] configures the OSM entry level and OSM exit level. Bit[11] selects the OSM exit level. 1'b1: 105% of VID 1'b0: 102% of VID Bit[10] selects the OSM entry level. 1'b1: 110% of VID 1'b0: 105% of VID Bit[9] configures the OSM exit delay. 1'b1: Delay 4 PWM pulses 1'b0: Delay 8 PWM pulses Bit[8] enables the OSM function. 1'b1: Enables OSM mode 1'b0: Disables OSM mode
7:4	R/W	MFR_TS_CFG	Configures frequency protection. This function detects if the V_{OUT} divider conflicts with the register configuration. The controller compares the real switch period with the theoretical period. If the delta value exceeds this configured value, then it triggers this protection. 160ns/LSB.

3:0	R/W	MFR_RETRY_DELAY	Configures the protection retry delay time. 100µs/LSB. The retry delay time can be calculated with the following equation: t_{RETRY_DELAY} = E7h, bits[3:0] x E7h, bits[3:0] x 100µs

MFR_PRT_DELAY (E8h)

Format: Unsigned binary

The MFR_PRT_DELAY command on Page 0 sets the delay time of OVP, UVP, per-phase OCP, and total OCP.

Bits	Access	Bit Name	Description
15:12	R/W	VOUT_OVP_DELAY	Sets the OVP delay time. 200ns/LSB, up to 3µs.
11:8	R/W	VOUT_UVP_DELAY	Sets the UVP delay time. 1µs/LSB, up to 15µs.
7:4	R/W	PHASE_OCP_DELAY	Sets the per-phase OCP delay. 1 PWM count/LSB, up to 15 PWMs.
3:0	R/W	TOTAL_OCP_DELAY	Sets the total OCP delay. It can be selected by F5h, bit[4] with 100µs/LSB or 500µs/LSB, up to 1.5ms or 7.5ms.

SMBALERT_MASK (E9h)

Format: Unsigned binary

The SMBALERT_MASK command on Page 0 sets the PMBus ALT# mask function. When this function is enabled, some protections do not trigger PMBus ALT# to pull low, where 1’b1 means PMBus ALT# is masked, and 1’b0 means PMBus ALT# is not masked.

Bits	Access	Bit Name	Description
15:0	R/W	SMBALERT_MASK	For SMBALERT, there are 16 conditions that can pull ALT# low. SMBALERT_MASK can used to block these conditions, as listed below: Bit[15] is fixed to 1 Bit[14] is STATUS_CML, bit[6] Bit[13] is STATUS_CML, bit[5] Bit[12] is STATUS_CML, bit[1] Bit[11] is STATUS_VOUT, bit[7] Bit[10] is STATUS_VOUT, bit[4] Bit[9] is STATUS_VOUT, bit[3] Bit[8] is STATUS_IOUT, bit[7] Bit[7] is STATUS_IOUT, bit[6] Bit[6] is STATUS_INPUT, bit[7] Bit[5] is STATUS_INPUT, bit[4] Bit[4] is STATUS_TEMPERATURE, bit[7] Bit[3] is STATUS_WORD, bit[15] Bit[2] is STATUS_WORD, bit[14] Bit[1] is STATUS_WORD, bit[13] Bit[0] is STATUS_WORD, bit[2]

MFR_NOCP_OCP_SET (EAh)

Format: Unsigned binary

The MFR_NOCP_OCP_SET command on Page 0 sets the per-phase OCP threshold and NOCP threshold.

Bits	Access	Bit Name	Description
15:8	R/W	MFR_OCP_SET	Sets the per-phase OCP threshold. 1A/LSB.
7:0	R/W	MFR_NOCP_SET	Sets the NOCP threshold. 1A/LSB.

MFR_LEVEL_SEL2 (EBh)

Format: Unsigned binary

The MFR_LEVEL_SEL2 command on Page 0 sets some protection thresholds.

Bits	Access	Bit Name	Description
15:14	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
13:12	R/W	MFR_NP_VID_SEL	Selects the N25mV and P25mV threshold. Bit[13] selects the N25mV threshold. 1'b0: -25mV 1'b1: -20mV Bit[12] selects the P25mV threshold. 1'b0: 25mV 1'b1: 20mV
11	R/W	RESERVED	Unused. X indicates writes are ignored and reads are always 0.
10	R/W	MFR_VDIFF_GAIN_SEL	Selects the V_{DIFF} gain. 1'b0: The V_{DIFF} gain is 1 1'b1: The V_{DIFF} gain is 0.5
9	R/W	MFR_ISUM_FILT_SEL	Fixed to 1.
8:7	R/W	MFR_UV_ENTRY_SEL	Selects the UVP threshold. 2'b00: 60% of VID 2'b01: 70% of VID 2'b10: 80% of VID 2'b11: 90% of VID
6:5	R/W	MFR_OV_EXIT_SEL	Selects the OVP exit threshold. 2'b00: 20% of VID 2'b01: 50% of VID 2'b10: 80% of VID 2'b11: 102.5% of VID
4:2	R/W	MFR_OV_ENTRY_SEL	Sets the OVP entry level. 3'b000: 110% VID 3'b001: 115% VID 3'b010: 120% VID 3'b011: 125% VID 3'b100: 130% VID 3'b101: 135% VID 3'b110: 140% VID 3'b111: 145% VID
1:0	R/W	MFR_OTP_HYS	Selects the OTP hysteresis. 2'b00: 20°C 2'b01: 25°C 2'b10: 30°C 2'b11: 35°C

MFR_PG_CFG (ECh)

Format: Unsigned binary

The MFR_PG_CFG command on Page 0 configures the power good signal behaviors.

Bits	Access	Bit Name	Description
15:13	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.

12	R/W	MFR_PASS_LPM_CFG	Fixed to 1.
11	R/W	MFR_VCOMP_SET_CFG	Selects when V_{COMP} ramps up during start-up. This bit is fixed to 0. 1'b1: V_{COMP} starts up when the SET signal appears 1'b0: V_{COMP} starts up at the beginning of soft start
10	R/W	MFR_SLAVE_PG_CFG	Reserved.
9:8	R/W	MFR_PG_ON_SEL	Selects the power good threshold. 2'b00: 97.5% of the VID target 2'b01: 95% of the VID target 2'b10: 92.5% of the VID target 2'b11: 90% of the VID target
7:0	R/W	MFR_PG_DELAY	Sets the power good delay time. 100µs/LSB.

MFR_PS_CTRL (EDh)

Format: Unsigned binary

The MFR_PS_CTRL command on Page 0 configures the phase-shedding-related configurations.

Bits	Access	Bit Name	Description
15:14	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
13:11	R/W	MFR_TRANS_DELAY	Sets the transient hold APS time. The APS hold time can be calculated with the following equation: APS Hold Time = (2 x MFR_TRANS_DELAY + 1) x 100µs
10:8	R/W	MFR_PS_DELAY	Sets the phase-shedding delay. 100µs/LSB.
7	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
6	R/W	MFR_PS_MODE	Selects the phase-shedding mode. 1'b0: PMBus-controlled phase-shedding 1'b1: APS
5	R/W	MFR_PS_EN	Enables phase-shedding. 1'b0: Disabled 1'b1: Enabled
4:2	R/W	MFR_M2S_DELAY	Sets the delay time when the slaves get master priority. 50ns/LSB.
1	R/W	MFR_FAULT_SKIP_EN_M	Enables the master fault skip function. When enabled, the master outputs the PASS pin with a middle voltage if there is a fault. Then the slave receives this signal and becomes the master. If the slave is experiencing a fault, it transfers the signal to the next slave. 1'b0: Disabled 1'b1: Enabled If this bit is enabled, it only asserts when the total phase number exceeds 2 (≥3), and it only skips the first two phases. The third phase is not skipped, and it pulls the PG pin low for a protection.
0	R/W	MFR_FAULT_SKIP_EN_S	Enables the slave fault skip function. When enabled, if the slave experiences a fault, it bypasses the TAKE and PASS signals. 1'b0: Disabled 1'b1: Enabled

MFR_PMBUS_LOCK (EEh)

Format: Unsigned binary

The MFR_PMBUS_LOCK command on Page 0 configures the PMBus one-time lock function.

Bits	Access	Bit Name	Description
15:2	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
1:0	R/W	MFR_PMBUS_LOCK	Configures the one-time PMBus lock function. 2'b00: Reset value. No PMBus lock 2'b01: Lock the registers, except 21h 2'b11: Lock all the registers A PG negative toggle can reset these bits to 00h.

MFR_SET_SYNC_CFG (EFh)

Format: Unsigned binary

The MFR_SET_SYNC_CFG command on Page 0 configures the SET signal chop function.

Bits	Access	Bit Name	Description
15:8	R/W	MFR_SET_TIME_CFG	Configures the SET signal chop function. MFR_SET_TIME_CFG, bits[7:4] configure the SET high time. MFR_SET_TIME_CFG, bits[3:0] configure the SET low time. It is only effective when the SET signal has a long high pulse. 5ns/LSB.
7:0	R/W	MFR_PWM_SYNC_CFG	Fixed to 0.

MFR_SLAVE_PROTECT (F0h)

Format: Unsigned binary

The MFR_SLAVE_PROTECT command on Page 0 is reserved.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9	R/W	MFR_PRD_FAULT_EN	Reserved.
8	R/W	MFR_PROTECT_RECORD	Reserved.
7	R/W	MFR_DRMOS_FAULT_DETECT	Reserved.
6	R/W	MFR_DRMOS_FAULT_EN	Reserved.
5	R/W	MFR_OCP_TOTAL_EN	Reserved.
4	R/W	MFR_OCP_PHASE_EN	Reserved.
3	R/W	MFR_VOUT_UVP_EN	Reserved.
2	R/W	MFR_VOUT_OVP_EN	Reserved.
1	R/W	MFR_OTP_PWR_EN	Reserved.
0	R/W	MFR_VIN_PROTECT_EN	Reserved.

MFR_CTRL (F1h)

Format: Unsigned binary

The MFR_CTRL command on Page 0 configures some advanced functions for the IC.

Bits	Access	Bit Name	Description
15	R/W	MFR_I2C_VOL_SET	Configures the I^2C voltage. 1'b1: 1.8V 1'b0: 3.3V
14	R/W	MFR_I2C_NACK_CFG	Reserved.
13	R/W	MFR_LPM_CFG	Fixed to 0.
12	R/W	MFR_LPM_CFG	Enables low-power mode (LPM). 1'b0: Disabled 1'b1: Enabled
11	R/W	CLR_MTP_LAST_FAULT_EN	Fixed to 1.
10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9	R/W	MFR_NVM_COPY_EN	Enables restoring the NVM when the system is outputting power. If this function is enabled, it asserts after soft start. 1'b0: Disabled 1'b1: Enabled
8	R/W	MFR_CRC_PROTECT_EN	Enables the NVM CRC function. 1'b0: Disabled 1'b1: Enabled
7	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
6	R/W	MFR_CAL_WATCH_DOG_EN	Enables the calculation watch dog function. This can prevent the calculation state machine from going out of control. If enabled, the calculation state machine resets once the state remains unchanged for longer than 700µs. 1'b0: Disabled 1'b1: Enabled
5	R/W	MFR_BG_CHOP_EN	Fixed to 1.
4:0	R/W	MFR_GATECLK_CFG	Fixed to 0.

MFR_AUTO_SLOPE_CFG (F2h)

Format: Unsigned binary

The MFR_AUTO_SLOPE_CFG command on Page 0 configures the automatic slope calculation.

Bits	Access	Bit Name	Description
15:14	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
13	R/W	MFR_SLOPE_CNT_SEL	Selects the maximum slope counter. 1'b1: x1.125 of the theoretical slope counter 1'b0: x1.25 of the theoretical slope counter
12:9	R/W	MFR_DELTA_CNT_ACT	Compensates the delay time of the slope discharge switch. It involves the digital-to-analog transmission delay, switch turn-off delay, and comparator delay. 5ns/LSB.
8:5	R/W	MFR_MAX_ADJ_TIMES	Reserved.

4:0	R/W	MFR_SYS_DELAY	Compensates the system delay time, which involves analog delay to digital delay, synchronous delay, ramp discharge delay, and switch turn-on/turn-off delay. 5ns/LSB.

MFR_SLOPE_DELTA_LIMIT (F3h)

Format: Unsigned binary

The MFR_SLOPE_DELTA_LIMIT command on Page 0 sets the slope limit.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:7	R/W	MFR_DELTA_VID	Reserved.
6:0	R/W	MFR_SLOPE_ DELTA_LIMIT	Reserved.

MFR_RETRY_TIMES (F4h)

Format: Unsigned binary

The MFR_RETRY_TIMES command on Page 0 sets the protection mode, including latch-off, retry, and hiccup, where 4'h0 means latch-off, 4'h1~4'hE mean retry (the retry times is the register value), and 4'hF means hiccup.

Bits	Access	Bit Name	Description
15:12	R/W	MFR_OTP_RETRY_ TIMES	Sets the DrMOS OTP mode.
11:8	R/W	MFR_VOUT_OV_ RETRY_TIMES	Sets the V_{OUT} OVP mode.
7:4	R/W	MFR_VOUT_UV_ RETRY_TIMES	Sets the V_{OUT} UVP mode.
3:0	R/W	MFR_OCP_RETRY_ TIMES	Sets the OCP mode, including the total OCP and OCP phase.

MFR_CFG_EXT (F5h)

Format: Unsigned binary

The MFR_CFG_EXT command on Page 0 configures the extended functions of the IC.

Bits	Access	Bit Name	Description
15:14	R/W	MFR_OVP_LEVEL_S	Fixed to 3.
13	R/W	MFR_OVP_BK_CFG	Fixed to 0.
12	R/W	MFR_RST_DEASS_ CFG	Configures whether V_{OUT} goes to VOUT_COMMAND when RST is low. 1'b1: Remains at V_{BOOT} 1'b0: Return to VOUT_COMMAND
11	R/W	MFR_EN_INIT_CFG	Configures when to start system initialization after copying to the NVM. 1'b1: Until CTRL pulls high 1'b0: Immediately after NVM copying finishes
10	R/W	MFR_PG_RST_MIX	Fixed to 0.
9	R/W	MFR_RUN_SIG_CFG	Reserved
8	R/W	MFR_HICCUP_MUX	Fixed to 1.
7	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.

6	R/W	MFR_CLR_FAULT_CFG	Configures whether to clear the FBh register value when sending a 08h command to clear the NVM's last fault. 1'b0: Does not clear the FBh value 1'b1: Clears the FBh value
5	R/W	MFR_FAULT_DET_CFG	Fixed to 1.
4	R/W	MFR_OCP_TIME_SEL	Selects the total OCP time resolution. 1'b1: 100μs/LSB 1'b0: 500μs/LSB
3:2	R/W	MFR_NVM_RCD_CFG	Configures the NVM storage mode. Bit[3] selects whether to store protection information when sending a 15h command. 1'b0: Stores all protection information 1'b1: Does not store protection information Bit[2] selects whether to store the MTP section or only the protection word when the protection record function is enabled. 1'b0: Stores the MTP section 1'b1: Stores only the protection
1	R/W	EN_RST_PRT_CFG	Configures whether the CTRL pin or OPERATION (01h) can reset the hiccup protection counter. 1'b1: Resets 1'b0: Does not reset
0	R/W	MFR_SW_PRD_DBG	Fixed to 0.

MFR_CDROOP_SET (F6h)

Format: Unsigned binary

The MFR_CDROOP_SET command on Page 0 configure the droop capacitor (C_{DROOP}) function for reducing the load transient ring-back.

Bits	Access	Bit Name	Description
15:14	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
13	R/W	DC_FB_SEL	Selects the DC loop feedback point. It is used under AC droop conditions. 1'b1: Feedback V_{DIFF} point. For AC droop 1'b0: Feedback V_{FB} point. For DC droop This bit is fixed to 1.
12	R/W	EN_REF	Enables the signal filter's positive side. 1'b1: Enabled 1'b0: Disabled
11	R/W	EN_SIG	Enables the signal filter's negative side. 1'b1: Enabled 1'b0: Disabled

10:7	R/W	REF_LPF_SEL	Selects the RC filter bandwidth for the signal filter's positive side. 4'b0000: 5.8ns 4'b0001: 190ns 4'b0010: 396ns 4'b0011: 582ns 4'b0100: 846ns 4'b0101: 1.03µs 4'b0110: 1.23µs 4'b0111: 1.42µs 4'b1000: 2.87µs 4'b1001: 3.16µs 4'b1010: 3.47µs 4'b1011: 3.74µs 4'b1100: 4.14µs 4'b1101: 4.40µs 4'b1110: 4.72µs 4'b1111: 4.98µs
6:3	R/W	SIG_LPF_SEL	Selects the RC filter bandwidth for the signal filter's negative side. 4'b0000: 5.8ns 4'b0001: 190ns 4'b0010: 396ns 4'b0011: 582ns 4'b0100: 846ns 4'b0101: 1.03µs 4'b0110: 1.23µs 4'b0111: 1.42µs 4'b1000: 2.87µs 4'b1001: 3.16µs 4'b1010: 3.47µs 4'b1011: 3.74µs 4'b1100: 4.14µs 4'b1101: 4.40µs 4'b1110: 4.72µs 4'b1111: 4.98µs
2:0	R/W	GAIN_SEL	Selects the R_{DROOP} signal gain. 3'b000: 0.25kΩ (0.078125mΩ) 3'b001: 0.5kΩ (0.15625mΩ) 3'b010: 1kΩ (0.3125mΩ) 3'b011: 1.5kΩ (0.46876mΩ) 3'b100: 2kΩ (0.625mΩ) 3'b101: 2.5kΩ (0.78125mΩ) 3'b110: 3kΩ (0.9375mΩ) 3'b111: 3.5kΩ (1.09375mΩ)

MFR_CFG_BACKUP (F7h)

Format: Unsigned binary

The MFR_CFG_BACKUP command on Page 0 configures some backup functions for the IC.

Bits	Access	Bit Name	Description
15:12	R/W	MFR_RSVD	Unused. Writes are ignored and reads are always 0.
11	R/W	MFR_PMBUS_RD_CFG	Reserved.
10	R/W	MFR_UCP_BLK_EN	Configures whether the NOCP can block start-up. This prevents a current-sense (CS) short condition, during which NOCP is always high and PWM is forced high for some time, resulting in V_{OUT} OVP. 1'b0: Disabled 1'b1: Enabled

9	R/W	MFR_M2S_SEL	Reserved.
8	R/W	MFR_SS_CPL_SEL	Configures the CTRL off/on timing for soft shutdown. If not enabled, when CTRL turns off/on, the system waits until soft shutdown finishes (reverse-voltage protection), then restarts power. If enabled, the CTRL off/on behavior is similar to DVID, meaning it restarts when CTRL is high. 1'b0: Disabled 1'b1: Enabled
7	R/W	MFR_RAMP_1P_ CFG	Reserved.
6:3	R/W	MFR_DCM_LV	Sets the DCM threshold for APS. The DCM entry and exit thresholds are MFR_DCM_LV - MFR_APSI_HYS and MFR_DCM_LV + MFR_APSI_HYS, respectively. 1A/LSB. Do not set this value below MFR_APSI_HYS.
2:0	R/W	MFR_PS_TRANS_ CFG	Configures whether the device exits phase-shedding when the system has a load transient and DVID. Bit[2]: Load adding Bit[1]: Load release Bit[0]: DVID Bits[2:0] are configured as below: 1'b0: Disabled. Does not exit phase-shedding 1'b1: Enabled. Exits phase-shedding When configured with PMBus phase-shedding, bits[2:0] automatically changes to 3'b000. This indicates PMBus phase-shedding mode, meaning the device does not exit phase-shedding when a load transient and DVID occur.

CHECK_SUM_FUNC (F8h)

Format: Unsigned binary

The CHECK_SUM_FUNC command on Page 0 returns the CRC value of the user code. It is a read-only command.

Bits	Access	Bit Name	Description
15:0	R	CHECK_SUM_FUNC	This is read-only.

PROTECTION (FAh)

Format: Unsigned binary

The PROTECTION command on Page 0 returns the protection information. The information is lost after shutdown.

Bits	Access	Bit Name	Description
15	R	INIT_FAULT	Indicates a fault in the initial system phase number.
14	R	NVM_CRC_ERROR	Indicates that the restored NVM has a fault.
13	R	NVM_FAULT	Indicates that the NVM signature has a fault.
12	R	OC_PHASE_FAULT	Indicates over-current protection (OCP) per-phase current fault.
11	R	OTP_SELF_FAULT	Indicates that the controller has an over-temperature OT fault.
10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9	R	SWITCH_PRD_ FAULT	Indicates that the VOUT_SCALE_LOOP register value is unmatched with the divider resistor.
8	R	VIN_OV_FAULT	Indicates a V_{IN} over-voltage (OV) fault.
7	R	VOUT_OV_FAULT	Indicates a V_{OUT} OV fault.
6	R	VOUT_UV_FAULT	Indicates a V_{OUT} under-voltage (UV) fault.

5	R	OC_TOT_FAULT	Indicates a total OC fault.
4	R	VIN_UVLO_FAULT	Indicates a V_{IN} under-voltage lockout (UVLO) fault.
3	R	DRMOS_OTP	Indicates a DrMOS OT fault.
2:0	R	FAULT_TYPE	Unused. Writes are ignored and reads are always 0.

PROTECTION_LAST (FBh)

Format: Unsigned binary

The PROTECTION_LAST command on Page 0 records the latest protection information.

Bits	Access	Bit Name	Description
15	R	INIT_FAULT	Indicates a fault in the initial system phase number.
14	R	NVM_CRC_ERROR	Indicates that the restored NVM has a fault.
13	R	NVM_FAULT	Indicates that the NVM signature has a fault.
12	R	OC_PHASE_FAULT	Indicates an over-current protection (OCP) per-phase current fault.
11	R	OTP_SELF_FAULT	Indicates that the controller has an over-temperature (OT) fault.
10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9	R	SWITCH_PRD_ FAULT	Indicates that the VOUT_SCALE_LOOP register value is unmatched with the divider resistor.
8	R	VIN_OV_FAULT	Indicates a V_{IN} over-voltage (OV) fault.
7	R	VOUT_OV_FAULT	Indicates a V_{OUT} OV fault.
6	R	VOUT_UV_FAULT	Indicates a V_{OUT} under-voltage (UV) fault.
5	R	OC_TOT_FAULT	Indicates a total OC fault.
4	R	VIN_UVLO_FAULT	Indicates a V_{IN} under-voltage lockout (UVLO) fault.
3	R	DRMOS_OTP	Indicates a DrMOS OT fault.
2:0	R	FAULT_TYPE	Unused. Writes are ignored and reads are always 0.

MFR_VBOOT_CFG (FCh)

Format: Unsigned binary

The MFR_VBOOT_CFG command on Page 0 configures the register that sets V_{BOOT}.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:0	R/W	MFR_VBOOT_CFG	Sets V_{BOOT} when the VBOOT pin is set according to the register setting. Linear mode: V_{BOOT} = VID_REF/LSB; LSB = 1.953125mV/LSB. VID mode or direct mode: V_{BOOT} = VID_REF/LSB; LSB = 1.5625mV/LSB.

CLEAR_NVM_FAULT (FEh)

The CLEAR_NVM_FAULT command on Page 0 clears the NVM fault. When restored from the NVM, it may be the NVM signature fault or CRC fault. These faults block the system's regular operation. If these faults can be ignored, the user can send this command to clear the NVM fault, allowing the system to operate normally.

APPLICATION INFORMATION

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Use ceramic capacitors for the best performance. During the layout, place the input capacitors as close to VIN as possible.

The capacitance can vary significantly with temperature. Ceramic capacitors with X5R and X7R dielectrics are recommended because they are fairly stable across a wide temperature range.

The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current with Equation (4):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (4)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (5):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current.

The input capacitance determines the converter's input voltage ripple. Select a capacitance that can meet any input voltage ripple requirement. Estimate the input voltage ripple with Equation (6):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (7):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (7)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. The output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (8)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, calculate the output voltage ripple with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

When using capacitors with a larger ESR (e.g. POSCAP and OSCON), the ESR dominates the impedance at the switching frequency, which means that the output voltage ripple can be determined by the ESR. For simplification, estimate the output voltage ripple with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (10)$$

Selecting the Inductor

The inductor supplies constant current to the output load while being driven by the switching input voltage. A larger-value inductor results in less ripple current and a lower output voltage ripple, but it also has a larger physical size, higher series resistance, and lower saturation current. Select an inductor value that sets the inductor's peak-to-peak ripple current to be between 30% and 40% of the maximum switch current limit. Design for a peak inductor current that is below the maximum switch current limit. Calculate the inductance with Equation (11):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under the maximum inductor peak current. The peak inductor current can be estimated with Equation (12):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 21 and follow the guidelines below:

1. Place a solid PGND layer on the first inner layer immediately below the MPQ8785 layer. The solid PGND layer should be continuous and uninterrupted with at least 1.5 times that of the POL area.
2. Place the input MLCC capacitors as close to the VIN and PGND pins as possible. Place a 0402 MLCC capacitor between the VIN and PGND pins.
3. Place the major MLCC capacitors on the same layer as the MPQ8785.
4. Maximize the VIN and PGND copper plane to minimize parasitic impendence.
5. Place vias close to the PGND/VIN pins and input capacitors pads to minimize parasitic impendence and thermal resistance.
6. Place the VCC and VDD18 decoupling capacitors on the same layer as the MPQ8785, and as close as possible to the decoupled pins.
7. Keep the AGND trace 20mil or wider to minimize the parasitic impedance.
8. Connect AGND and PGND with a 0Ω resistor, or connect AGND directly to PGND.
9. Place the BST capacitor as close to the BST and PHASE pins as possible. Use a trace width of 20mils or higher to route the path. It is recommended to use 0.1μF to 0.22μF bootstrap capacitor.
10. Place the output remote sense traces (VSEN+/VSEN-) in a differential pair and place the sense pair on a quiet layer away from noisy signals, such as the SW signal, the VIN-related plane/trace/vias, and PMBus communication signals.

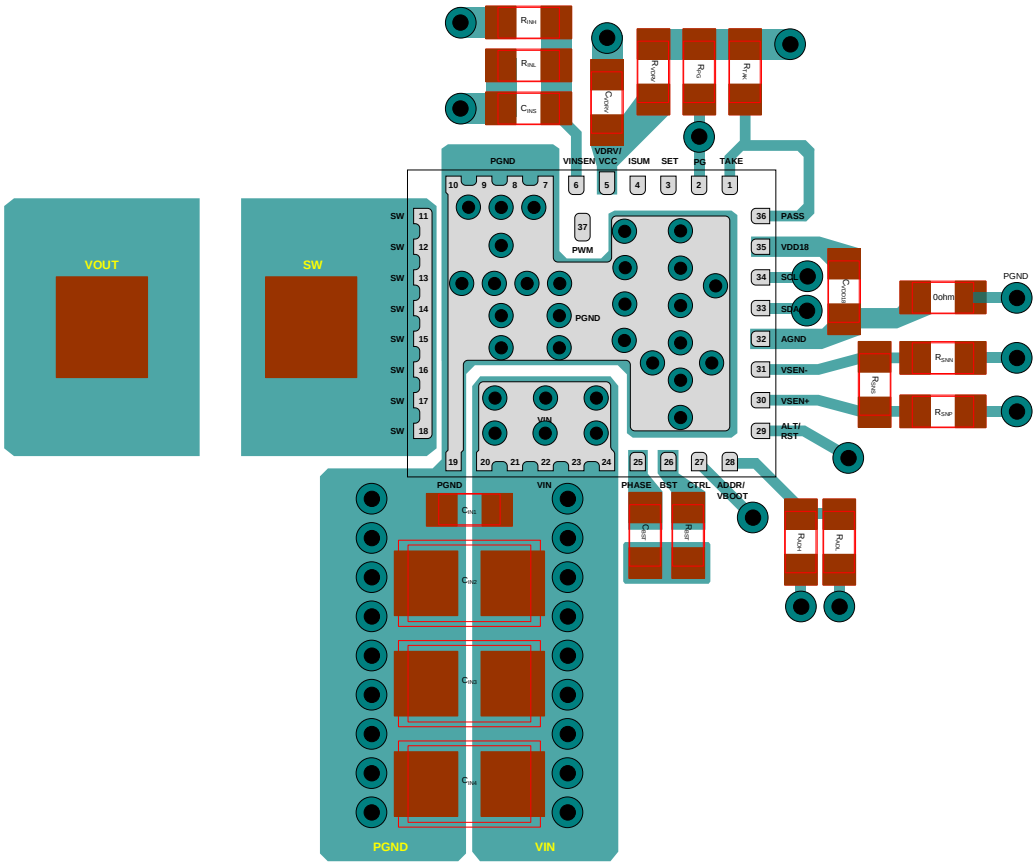


Figure 21: Example of PCB Layout (Placement and Top Layer PCB)

TYPICAL APPLICATION CIRCUIT

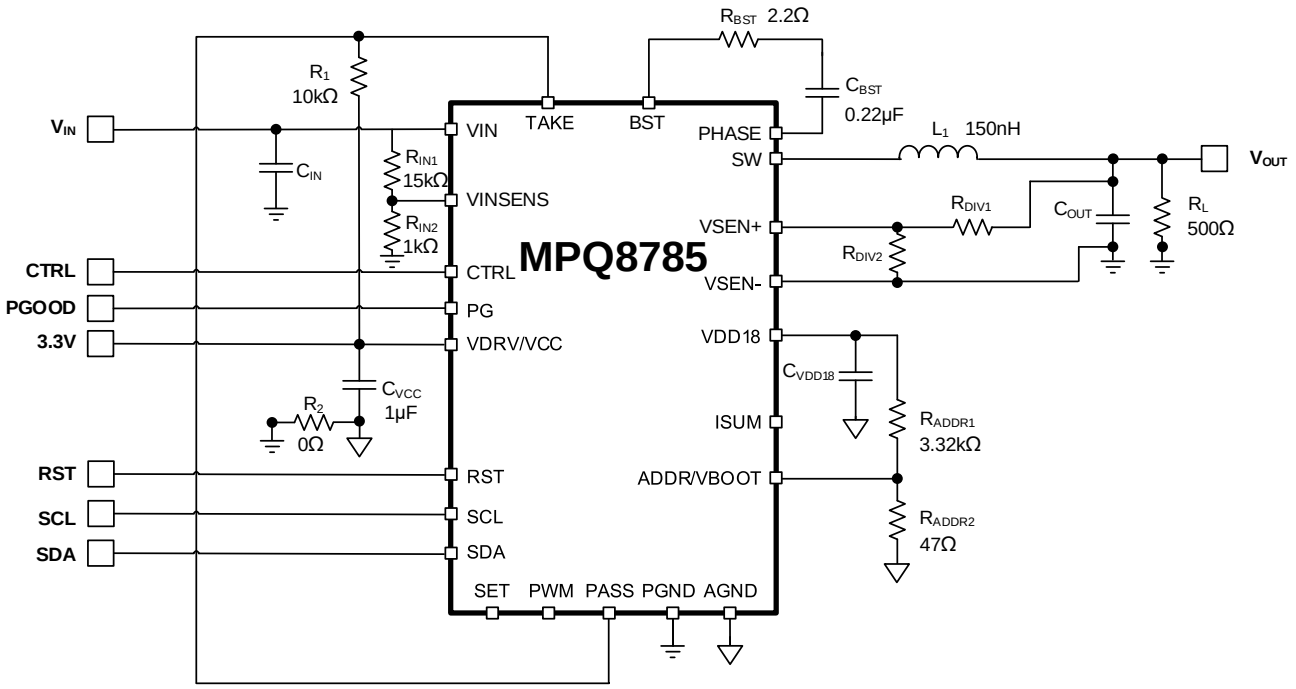
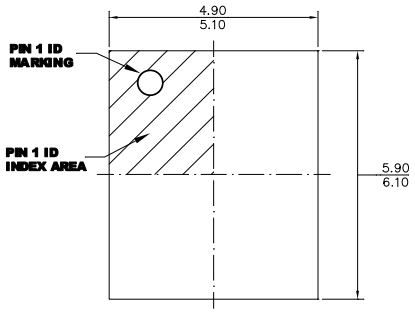


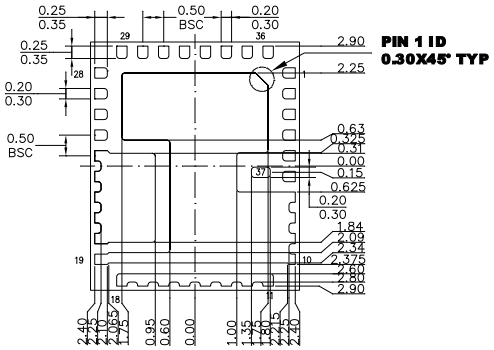
Figure 22: Typical Application Circuit with Resistor Divider for >3.1V Output

PACKAGE INFORMATION

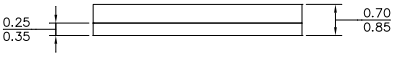
TLGA-37 (5mmx6mm)



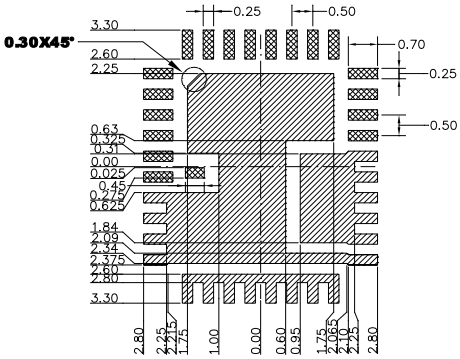
TOP VIEW



BOTTOM VIEW

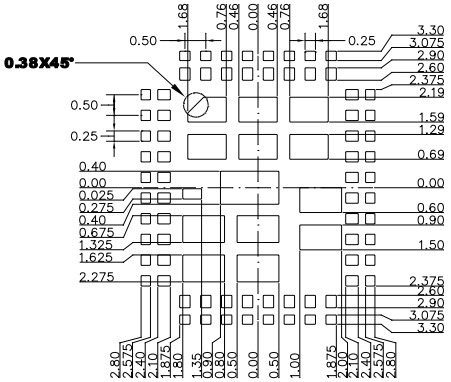


SIDE VIEW



NSMD PAD SMD PAD

RECOMMENDED LAND PATTERN

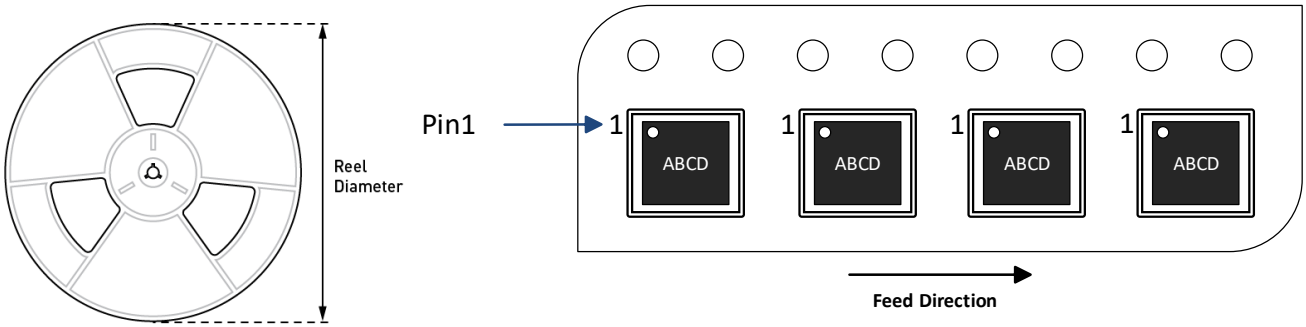


RECOMMENDED STENCIL OPENING

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.
5) THE ACCURACY FOR COMPONENT PLACEMENT SHOULD BE ADJUSTED TO ±30 MICROMETRES.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ8785GMJT-xxxx-Z	TLGA-37 (5mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/10/2024	Initial Release	-