MPQ6634-AEC1

35V, 2A Peak, 3-Phase, Sensorless BLDC Motor Driver, AEC-Q100 Qualified

DESCRIPTION

The MPQ6634-AEC1 is a 3-phase, sensorless brushless DC (BLDC) motor driver with integrated power MOSFETs. It features sensorless field-oriented control (FOC) for improved efficiency and low vibration, with up to 2A of peak current. The input voltage (V_{IN}) ranges between 4.5V and 35V.

The MPQ6634-AEC1 controls the motor speed through the pulse-width modulation (PWM) signal with a PWM input frequency between 50Hz and 20kHz. The device also supports DC input speed control.

The MPQ6634-AEC1 provides rotational speed detection. The rotational speed detector (the FG/RD pin) is an open-drain output. In addition, the direction can be controlled via the DIR pin's input.

Rich protections include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, phase-loss protection (PLOS), over-current protection (OCP), and thermal shutdown (TSD).

The MPQ6634-AEC1 is available in a TQFN-12 (3mmx4mm) wettable flank package. It is available in AEC-Q100 Grade 1.

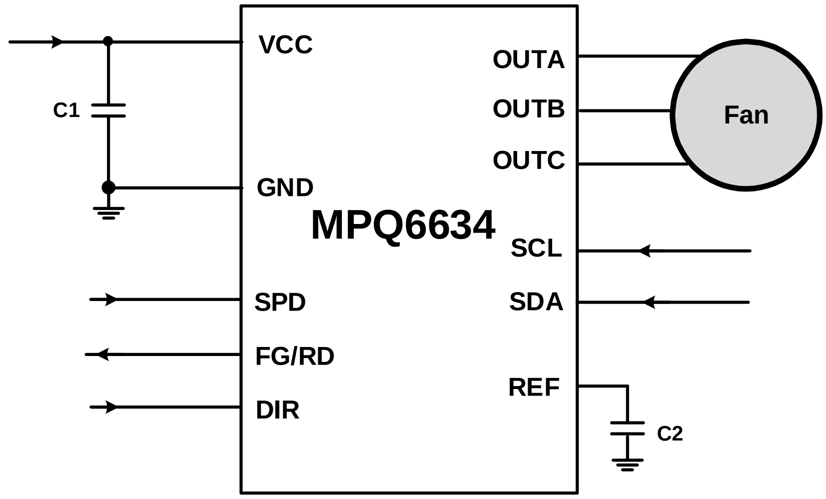
FEATURES

- 4.5V to 35V Operating Input Voltage (V_{IN}) Range
- Up to Maximum 2A of Peak Current
- Sensorless Field-Oriented Control (FOC)
- Integrated MOSFETs: High-Side MOSFET (HS-FET) + Low-Side MOSFET (LS-FET) = 450mΩ
- Supports 0V to 3.3V DC Input or 50Hz to 20kHz Pulse-Width Modulation (PWM) Input
- Starting Duty Cycle Set with Hysteresis
- Curve Configurations
- Configurable Speed for Open-Loop and Closed-Loop Control
- Configurable Soft-Start Time
- Configurable Alignment Time
- Direction Control
- Power-Saving Mode
- 24kHz PWM Output Frequency
- Short-Circuit Protection (SCP)
- Over-Voltage Protection (OVP)
- Phase-Loss Protection (PLOS)
- Locked-Rotor Protection
- Selectable FG and RD Outputs
- Available in a TQFN-12 (3mmx4mm) Package with Wettable Flank
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Fans
- Pumps
- Air Purifiers
- General Fans
- Small-Sized Motors

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ6634GLTE-xxxx-AEC1**	TQFN-12 (3mmx4mm) with Wettable Flank	*See Below*	1

For Tape & Reel, add suffix -Z (e.g. MPQ6634GLTE-xxxx-AEC1-Z).

** “xxxx” is the configuration code identifier. The four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number to customize configuration. The default code is “0000”.

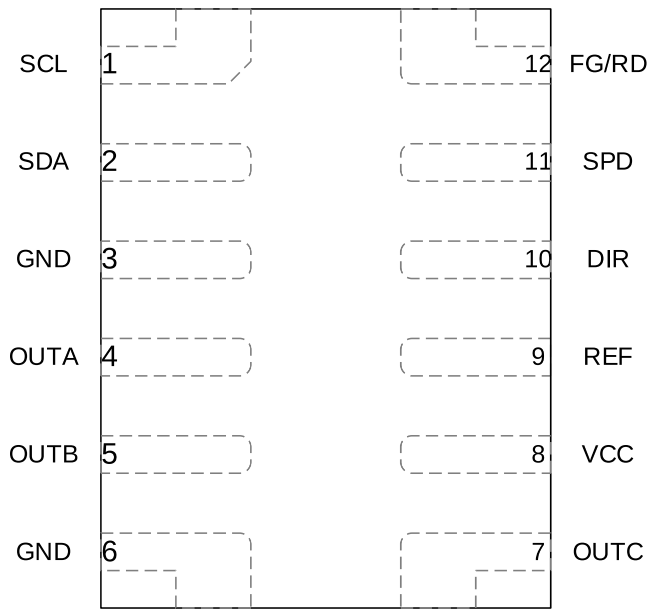
TOP MARKING

MPYW
6634
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
6634: Part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE

TOP VIEW



TQFN-12 (3mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	SCL	**I^2C interface (serial clock line).**
2	SDA	**I^2C interface (serial data line).**
3, 6	GND	**Ground.**
4	OUTA	**Phase A terminal.**
5	OUTB	**Phase B terminal.**
7	OUTC	**Phase C terminal.**
8	VCC	**Power supply.** The VCC pin must be bypassed locally.
9	REF	**5V LDO output.** The REF pin must be bypassed locally.
10	DIR	**Direction control.** Pull the DIR pin high for reverse rotation and pull it low for forward rotation. This pin is pulled low internally.
11	SPD	**Speed control input.** Supports a 50Hz to 20kHz PWM input frequency or a 0V to 3.3V DC input. This pin is internally pulled high with a 360kΩ resistor.
12	FG/RD	**Speed indicator (FG) and locked-rotor indicator (RD) output.** The FG/RD pin is an open-drain output that must be pulled up externally.

ABSOLUTE MAXIMUM RATINGS (1)

VCC, FG/RD ....-0.3V to +40V
OUTA, OUTB, OUTC...........-0.3V to V_{CC} + 0.3V
All other pins ....-0.3V to +6V
Junction temperature (T_J) ....150°C
Lead temperature ....260°C
Continuous power dissipation (T_A = 25°C) (2)
.... 2.5W

ESD Ratings

Human body model (HBM) .... ±2000V
Charged-device model (CDM)................±1500V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ....4.5V to 35V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance (4) ***θJA*** ***θJC***

TQFN-12-WF (3mmx4mm)......48.......11....°C/W

Notes:

1) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

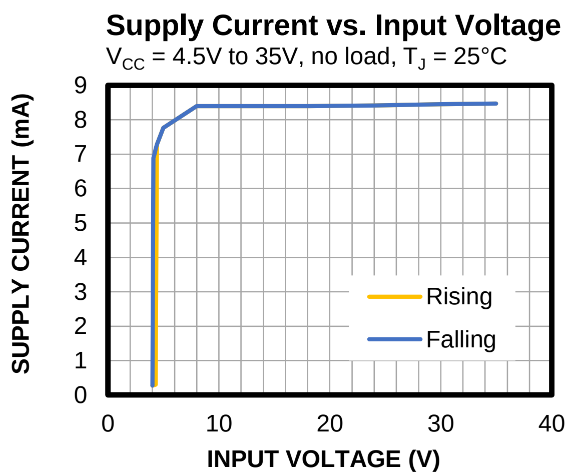
ELECTRICAL CHARACTERISTICS

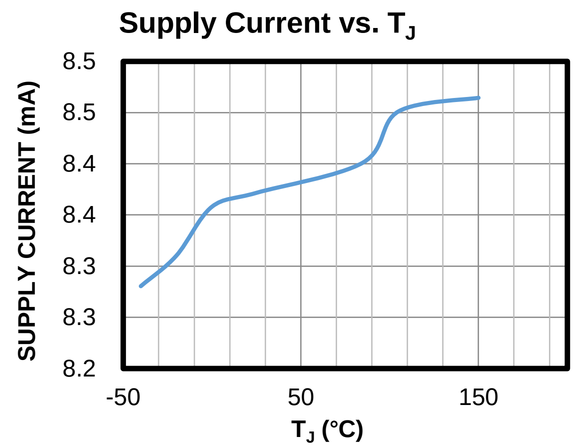
V_{CC} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

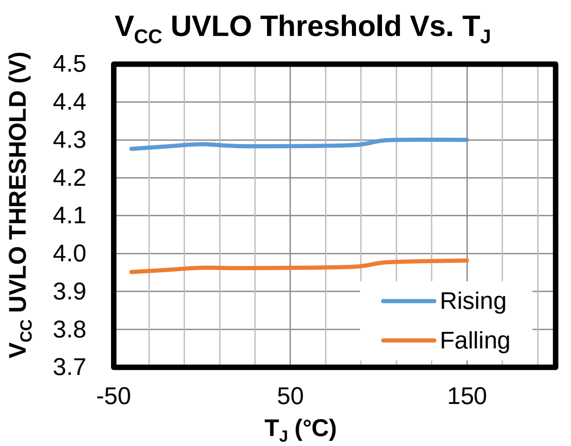
Parameter	Symbol	Condition	Min	Typ	Max	Units
VCC voltage (V_{CC}) under-voltage lockout (UVLO) rising threshold	V_{UVLO_R}			4.2	4.45	V
V_{CC} UVLO hysteresis	V_{UVLO_HYS}		0.2	0.3		V
Operating supply current	I_{CC}	SPD = high, no load		8.3	10	mA
Standby current	I_{STD}	SPD = low			40	μA
SPD input high threshold	V_{PWM_H}	PWM input mode	2			V
SPD input low threshold	V_{PWM_L}	PWM input mode			0.8	V
SPD internal pull-up resistance	R_{SPD}			360		kΩ
SPD DC input high threshold	V_{DCH}	DC input mode		3.3		V
SPD DC input low threshold	V_{DCL}	DC input mode		0		mV
DIR input high threshold	V_{DIR_H}		2			V
DIR input low threshold	V_{DIR_L}				0.8	V
DIR internal pull-low resistance	R_{DIR}			50	100	kΩ
FG/RD output low level	V_{FG_L}	$I_{FG/RD}$ = 3mA		0.3	0.5	V
Switching frequency	f_{SW}	T_J = 25°C	23.64	24	24.36	kHz
		T_J = -40°C to +150°C	23	24	24.84	kHz
High-side MOSFET (HS-FET) on resistance	R_{HS_ON}	I_{OUT} = 100mA		300		mΩ
Low-side MOSFET (LS-FET) on resistance	R_{LS_ON}	I_{OUT} = 100mA		150		mΩ
Peak current limit	I_{LIM}		2.4	3	3.6	A
5V LDO output voltage	V_{5V}		4.75	5	5.25	V
5V LDO load capability	I_{5V}	I_{REF} = 30mA	4.7			V
Locked-rotor retry time	t_{RE}			5.5		s
Over-voltage protection (OVP) threshold	V_{OVP_H}	OVP_EN = 1, UIN_SEL = 1		33	35	V
	V_{OVP_L}	OVP_EN = 1, UIN_SEL = 0		19	21	V
OVP hysteresis	V_{OVP_HYS}			2	3	V
Thermal shutdown threshold	T_{ST}			175		°C
Thermal shutdown hysteresis	T_{ST_HYS}			20		°C
I²C Interface						
Input logic low	V_{IL}				0.8	V
Input logic high	V_{IH}		2			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				400	kHz

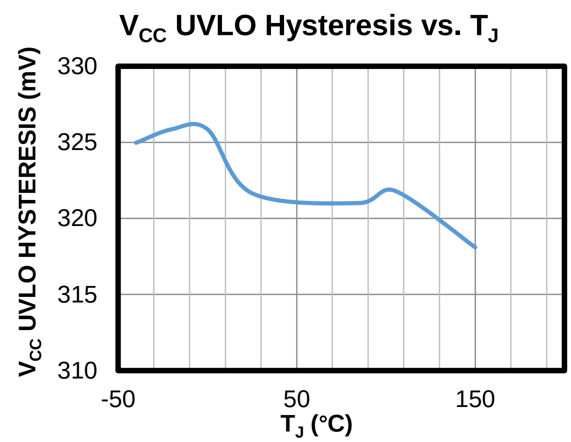
TYPICAL CHARACTERISTICS

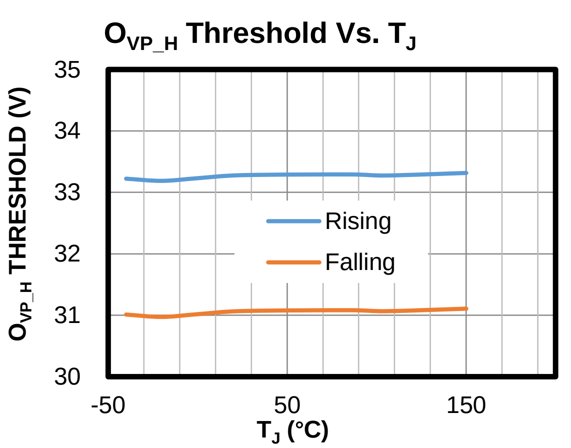
V_{CC} = 12V, T_J = -40°C to 150°C, unless otherwise noted.

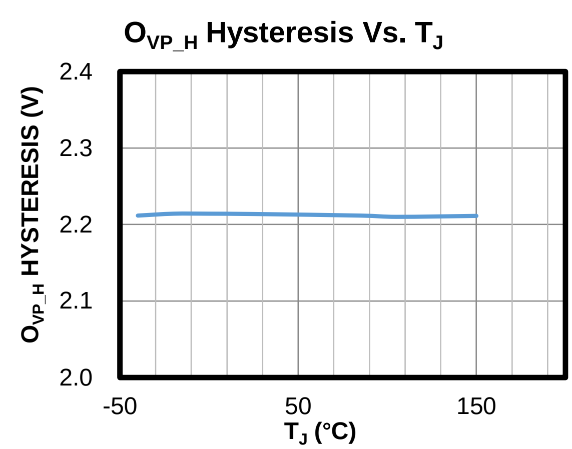






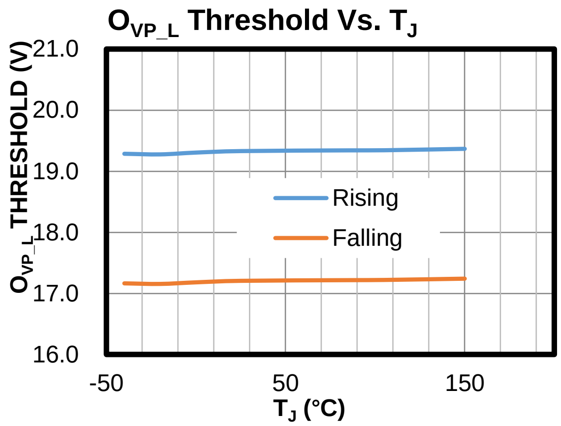


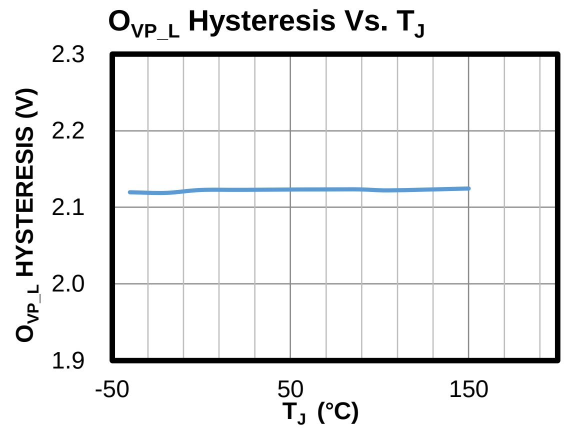


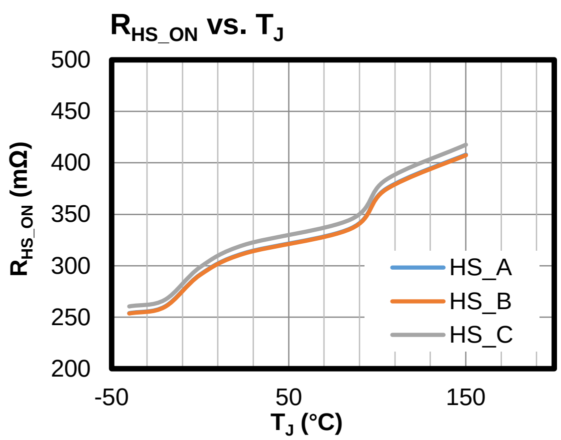


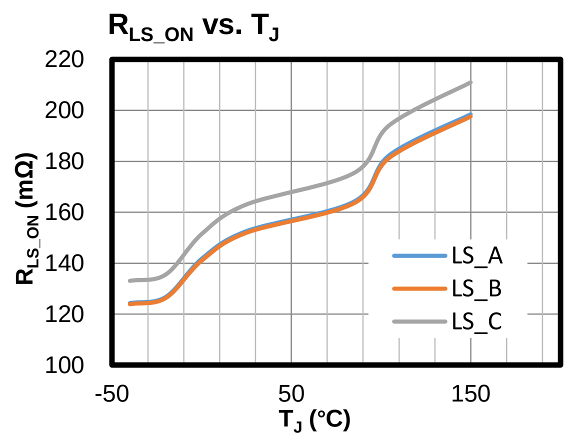
TYPICAL CHARACTERISTICS *(continued)*

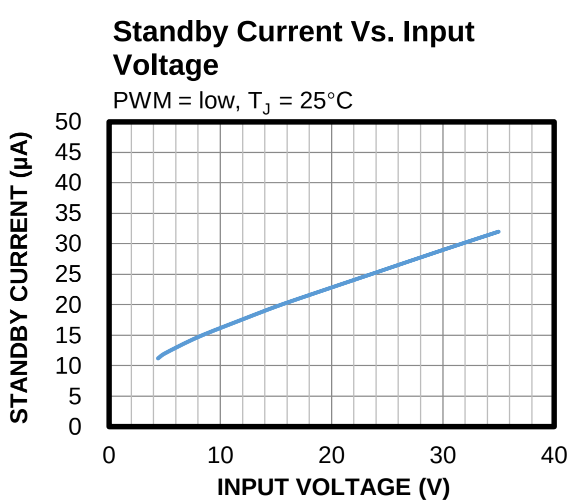
V_{CC} = 12V, T_J = -40°C to 150°C, unless otherwise noted.

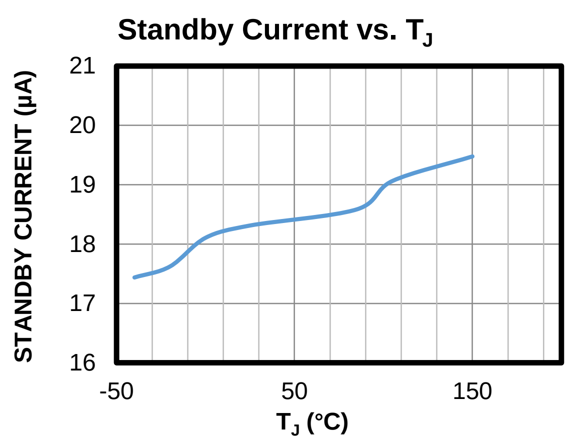






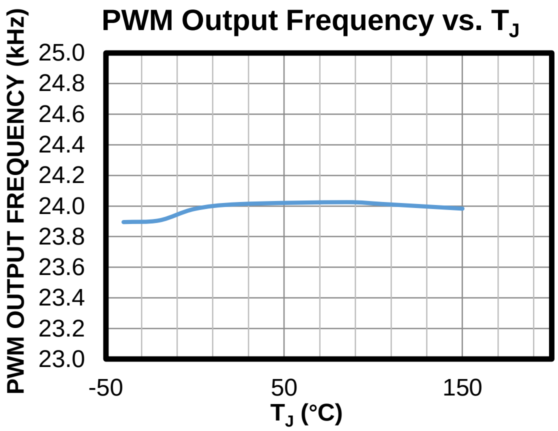


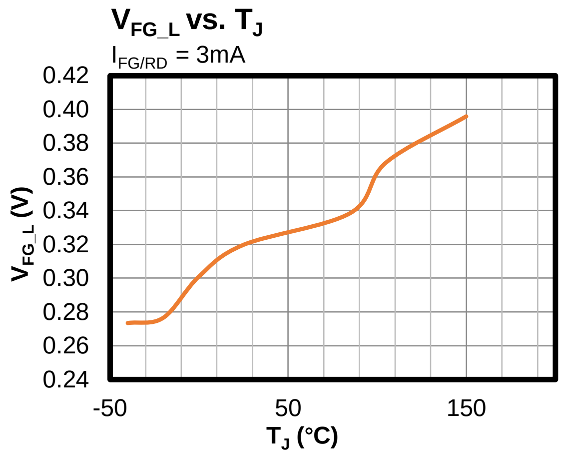




TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_J = -40°C to 150°C, unless otherwise noted.



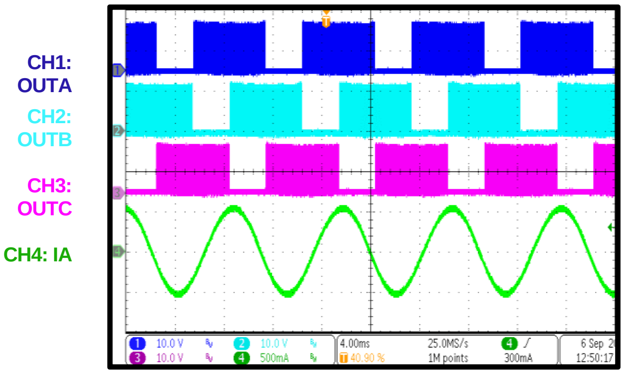


TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, PWM input frequency = 100Hz, load = seat fan, unless otherwise noted.

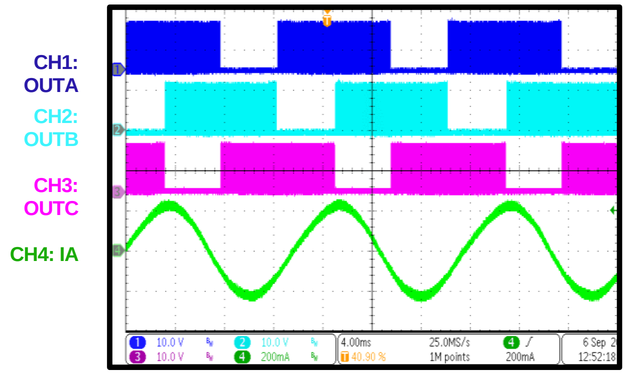
Steady State

PWM duty cycle = 100%, DIR = low



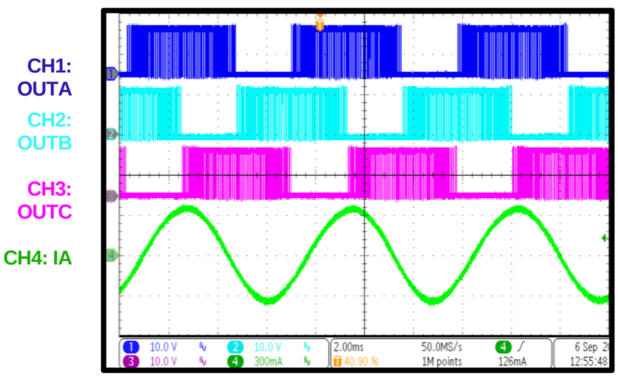
Steady State

PWM duty cycle = 50%, DIR = low



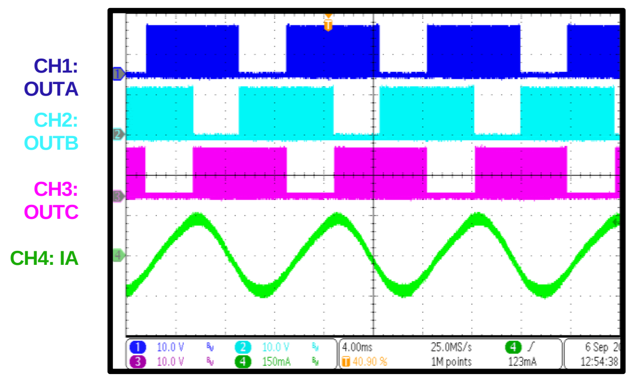
Steady State

PWM duty cycle = 100%, DIR = high



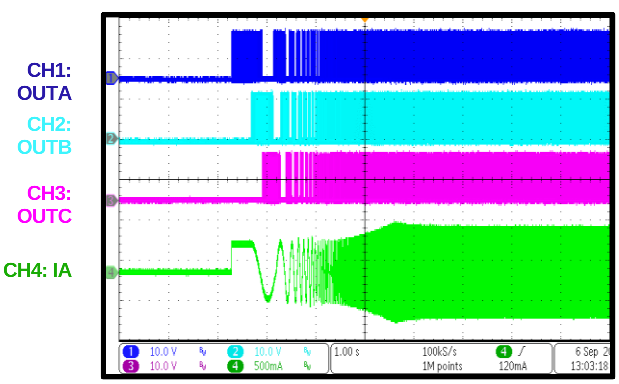
Steady State

PWM duty cycle = 50%, DIR = high



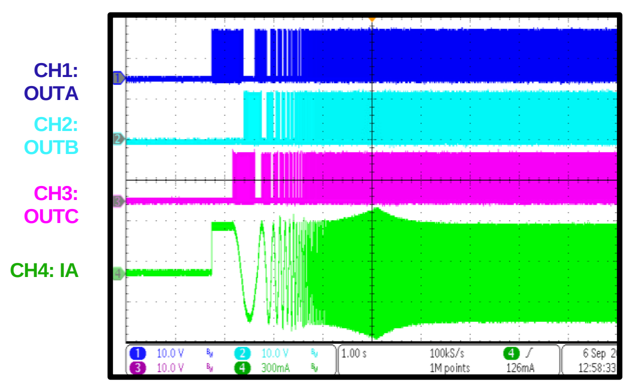
PWM On

PWM duty cycle = 0% to 100%, DIR = low



PWM On

PWM duty cycle = 0% to 100%, DIR = high

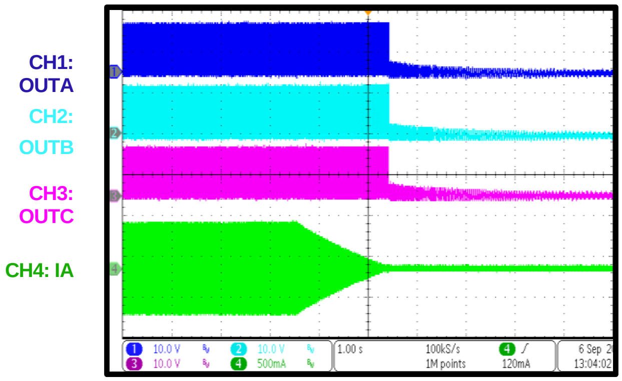


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, PWM input frequency = 100Hz, load = seat fan, unless otherwise noted.

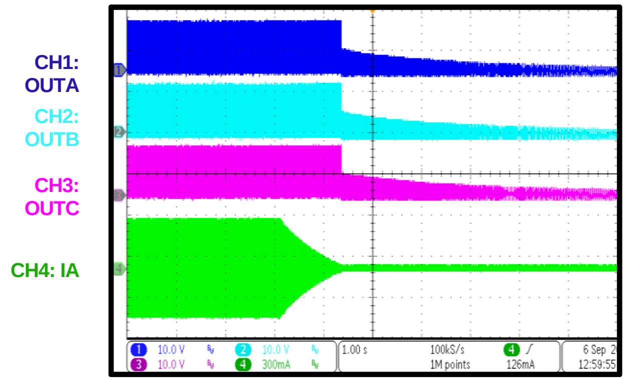
PWM Off

PWM duty cycle = 100% to 0%, DIR = low



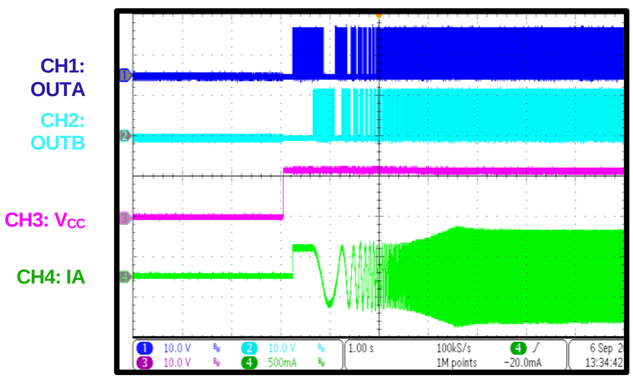
PWM Off

PWM duty cycle = 100% to 0%, DIR = high



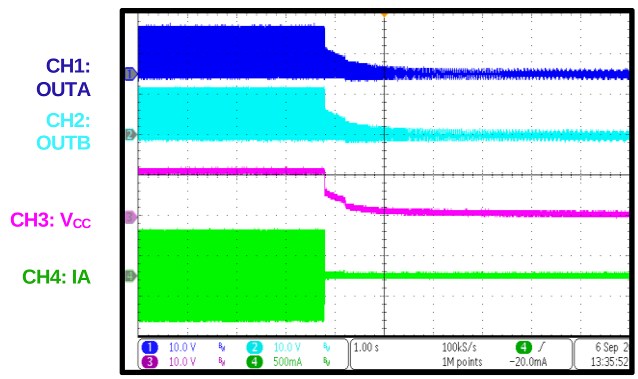
Start-Up via VCC

V_{CC} = 0V to 12V, PWM duty cycle = 100%, DIR = low



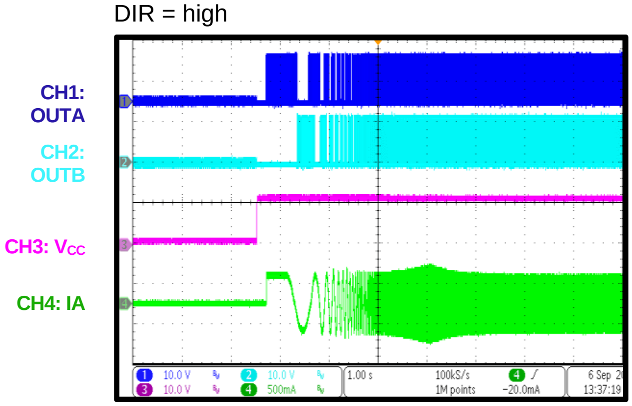
Shutdown via VCC

V_{CC} = 12V to 0V, PWM duty cycle = 100%, DIR = low



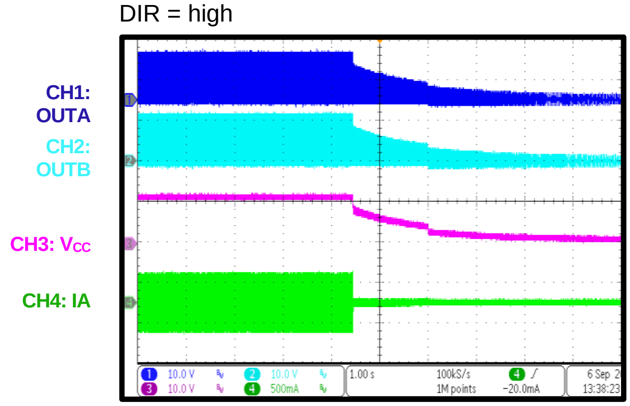
Start-Up via VCC

V_{CC} = 0V to 12V, PWM duty cycle = 100%, DIR = high



Shutdown via VCC

V_{CC} = 12V to 0V, PWM duty cycle = 100%, DIR = high

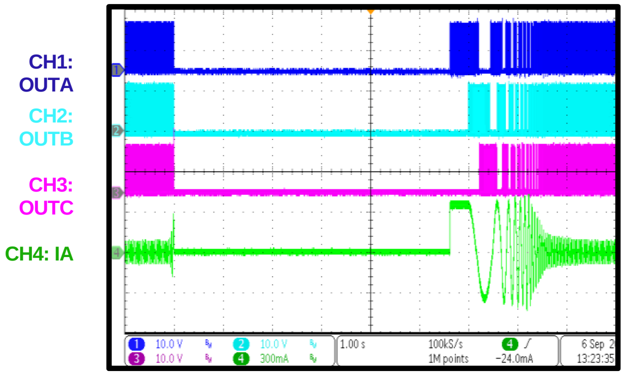


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, PWM input frequency = 100Hz, load = seat fan, unless otherwise noted.

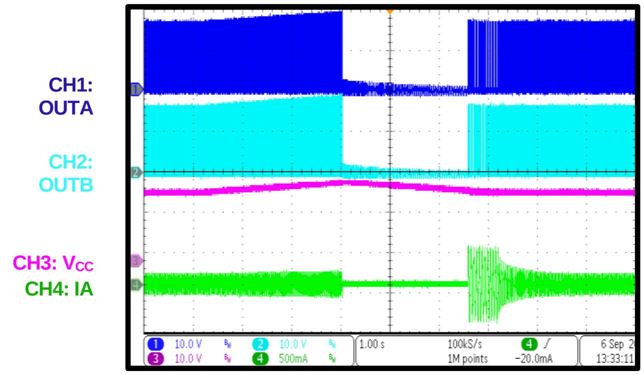
Rotor Lock and Retry

PWM duty cycle = 20%, enable RD_MODE1 and RD_MODE2



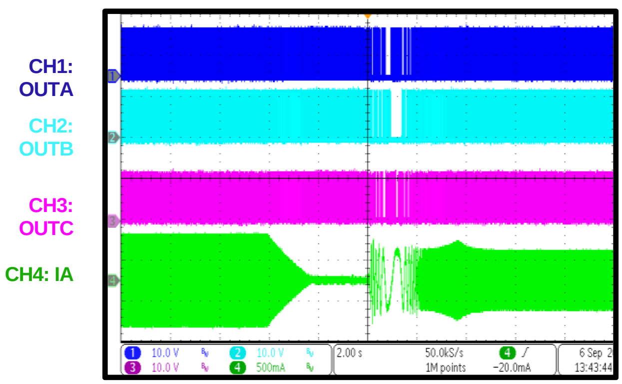
OVP

PWM duty cycle = 20%, UIN_SEL = 0



Direction Change

PWM duty cycle = 100%, enable SOFT_DOWN, DIR = low to high



FUNCTIONAL BLOCK DIAGRAM

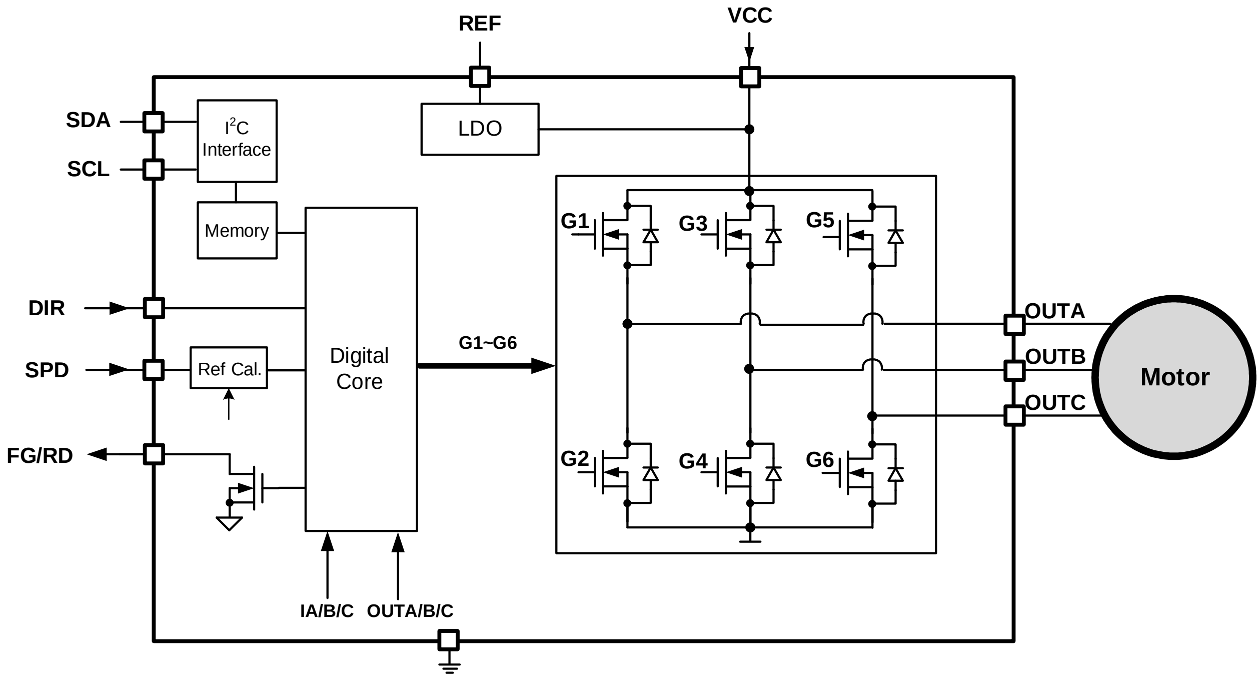


Figure 1: Functional Block Diagram

OPERATION

The MPQ6634-AEC1 is a 3-phase, sensorless brushless DC (BLDC) motor driver with integrated power MOSFETs. It features sensorless field-oriented control (FOC) for better efficiency and low vibration with up to 2A of peak current. The input voltage (V_{IN}) ranges between 4.5V to 35V.

Figure 2 shows the sensorless FOC drive.

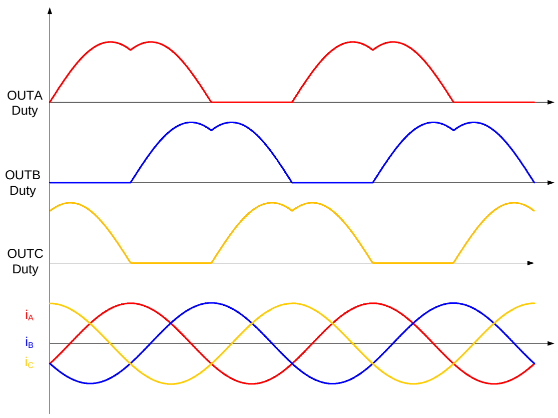


Figure 2: Sensorless FOC Drive

Speed Control

The SPD pin controls the motor speed either in open-loop or closed-loop operation by applying a pulse-width modulation (PWM) signal or a DC voltage to SPD. It accepts a wide 50Hz to 20kHz input frequency range, or a voltage from 0V to 3.3V.

If PWM_DC = 1, the motor speed is controlled by the DC voltage on the SPD pin. If PWM_DC = 0, the motor speed is controlled by the input PWM signal duty cycle.

Direction Control

The rotation direction is controlled by the polarity of the DIR pin's input and internal DIR bit.

By default, the MPQ6634-AEC1 operates in forward rotation (OUTA to OUTB to OUTC to OUTA…). when the DIR input is low. The device rotates in reverse (OUTA to OUTC to OUTB to OUTA…) when the DIR input is high.

There is a register bit that can reverse the polarity of DIR input. If this bit is set, the motor rotates in reverse when the DIR input is low, and it rotates in the forward direction when the DIR input is high.

When the rotating direction changes during operation (by changing the DIR input polarity or setting the bit), the output's duty cycle decreases first to slow down the motor speed, then the motor is driven in the commanded rotating direction.

Rotor Alignment

If the motor is stationary, a certain voltage vector is applied for a configurable time to align the rotor to the certain position. The voltage vector amplitude is configured via the U_START[3:0] bits. ALIGN_TIME[1:0] sets different alignment times for different motors.

Open-Loop Acceleration

After rotor alignment, the motor accelerates openly by increasing the driven vector amplitude and frequency.

The minimum output duty cycle at the beginning of the start-up stage, the acceleration ramp, the acceleration target for the electrical frequency, and the open-loop to closed-loop handoff threshold can be configured via the registers for different types of motors.

Figure 3 shows the electrical frequency in the V/F stage.

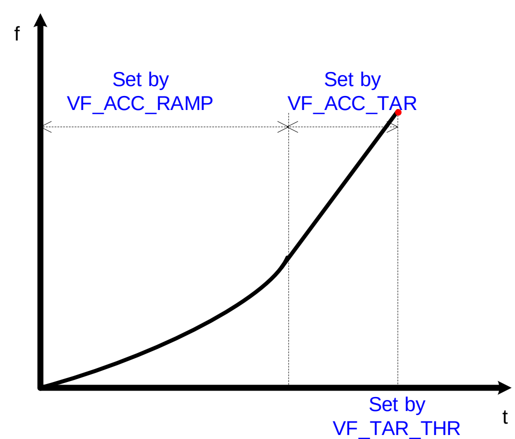


Figure 3: Electrical Frequency in the VF Stage

Once the motor reaches the handoff speed, the MPQ6634-AEC1 enters the sensorless FOC stage.

Open-/Closed-Loop Speed Control

The MPQ6634-AEC1 supports either open-loop or closed-loop speed control, as configured via the V_LOOP bit.

In closed-loop speed mode (V_LOOP = 1), the IC internally detects the speed and feedbacks to the control loop, which adjusts the output PWM duty cycle in a closed loop. In closed-loop control, the motor speed follows the reference exactly.

In open-loop speed mode (V_LOOP = 0), the output duty cycle directly depends on the PWM input's duty cycle.

Starting Duty Cycle and Stopping Duty Cycle

The input starting duty cycle can be configured via the D0[7:0] bits. The stopping duty cycles depends on the HZERO_THR bit when the SPD_HZERO function is enabled.

The operation when the input duty cycle is below the starting duty cycle is configured by the SPD_LZERO bit.

If SPD_LZERO = 0, the speed/output duty cycle maintains the setting from the S0[7:0] bits (see Figure 4).

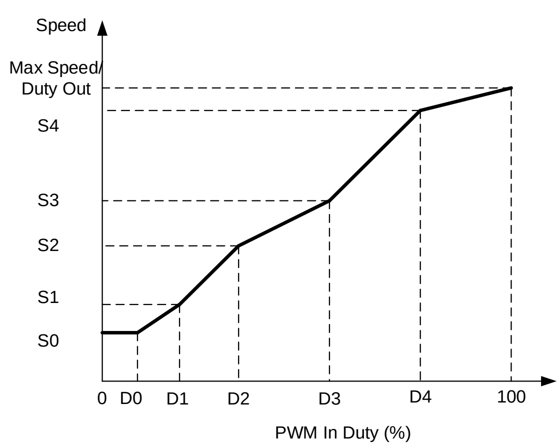


Figure 4: Curve Configuration (SPD_LZERO = 0)

If SPD_LZERO = 1, the fan stops (see Figure 5).

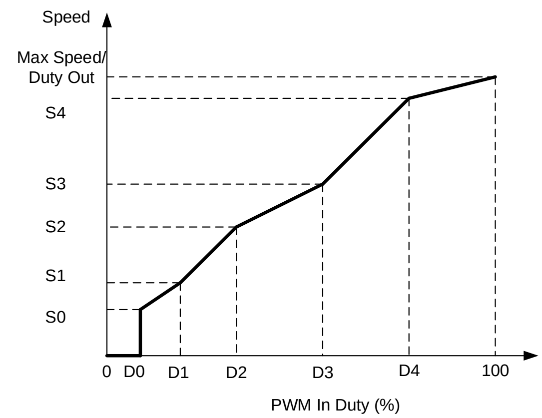


Figure 5: Curve Configuration (SPD_LZERO = 1)

The MPQ6634-AEC1 can be configured for fan shutdown when the input duty cycle exceeds the stopping duty cycle set via the SPD_HZERO bit.

- If SPD_HZERO = 1, the speed is at 0 (see Figure 6).
- If SPD_HZERO = 0, the speed/output duty cycle follows the configured curve (see Figure 7 on page 15).
- The stopping duty cycle threshold is configured via the HZERO_THR bit.

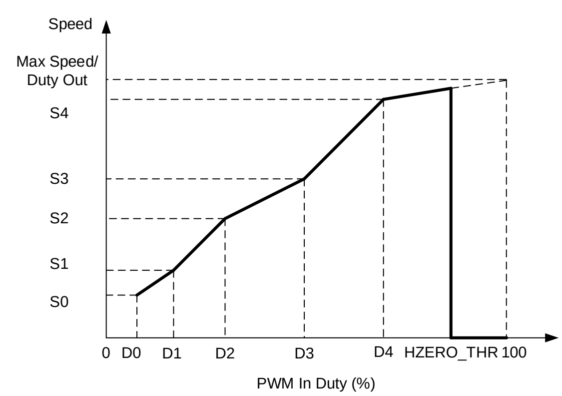


Figure 6: Curve Configuration (SPD_HZERO = 1)

Curve Configurations

The MPQ6634-AEC1 provides a curve configuration function. Both the input duty cycle and output duty cycle/speed can be configured via this register (see Figure 7 on page 15).

The SPD_MAX[11:0] bits support 6 configurations for the maximum speed in closed-loop speed control.

The SPD_MAX[7:0] bits configure the output duty cycle during open-loop speed control when the input duty cycle is 100%.

The S0[7:0] bits set the speed/output duty cycle when the input duty cycle is D0, which is set by the D0[7:0] bits.

The S1[7:0], S2[7:0], S3[7:0], and S4[7:0] bits set the speed/output duty cycle when the input duty cycle is set via the D1[7:0], D2[7:0], D3[7:0], and D4[7:0] bits, respectively (see Figure 7).

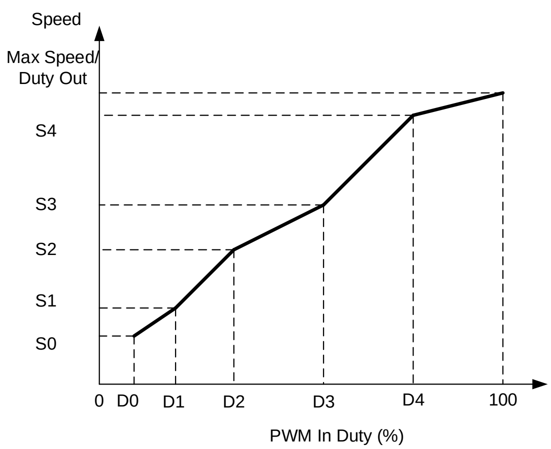


Figure 7: Curve Configurations

Standby Mode

If the VCC voltage (V_{CC}) exceeds its under-voltage lockout (UVLO) rising threshold and the SPD pin stays low for more than 85ms after the IC stops switching, the IC is in standby mode. When entering standby mode, the low-dropout (LDO) regulator's output is controlled via the SLP_REF bit. The IC exits standby mode when the PWM input signal is detected or power is cycled.

Rotor Speed Indication (FG)

The FG/RD pin can be configured for speed indication, locked-rotor indication, or fault indication:

- If FGRD = 00, the FG/RD pin outputs 1 cycle in every 1 electrical cycle.
- If FGRD = 01, the FG/RD pin outputs 2 cycles in every 1 electrical cycle.
- If FGRD = 10, the FG/RD pin outputs RD.
- If FGRD = 11, the FG/RD pin is a fault indicator.

Protection Circuits

The MPQ6634-AEC1 is fully protected in the event of over-voltage (OV), under-voltage (UV), over-current (OC), and over-temperature (OT) events.

Short-Circuit Protection (SCP)

The MPQ6634-AEC1 has internal overload and short-circuit protection (SCP) by detecting the current flowing through each MOSFET. If the current flowing through any MOSFET exceeds the over-current protection (OCP) threshold (typically 3A), after a blanking time, all MOSFETs turn off immediately and resume operation after a locked retry time.

Over-Current Protection (OCP)

During normal switching, if the current flowing through the MOSFET exceeds the threshold setting via the OC_THR bits after a blanking time, the output duty cycle decreases to limit the output current. The OCP threshold can be set to 1A or 2A.

OCP can be disabled via the OCP_EN bit.

Thermal Shutdown (TSD)

Thermal monitoring is also integrated into the MPQ6634-AEC1. If the die temperature exceeds 175°C, all MOSFETs turn off. The IC resumes operation when the die temperature drops to the lower threshold.

Under-Voltage Lockout (UVLO)

If V_{CC} ever falls below the UVLO threshold, all circuitry in the device is disabled and the internal logic is reset. Operation resumes when V_{CC} rises above the UVLO threshold.

Rotor Dead-Lock Protection (RD)

The MPQ6634-AEC1 has rotor dead-lock protection. If this protection is triggered, the MPQ6634-AEC1 turns off the MOSFETs. By default, the IC resumes normal operation after a 5.5s lock-retry time. The protection behavior can be configured to latch-off mode or retry mode, as determined by the RETRY bit.

Over-Voltage Protection (OVP)

The MPQ6634-AEC1 employs two OVP thresholds for different applications. The OVP threshold can be configured via the UIN_SEL bit.

If V_{CC} exceeds its OV threshold (typically 19V or 33V), the IC turns off all MOSFETs. The IC resumes normal operation when V_{CC} drops below the OVP threshold falling.

OVP can be disabled via the OVP_EN bit.

Phase-Loss Protection (PLOS)

The MPQ6634-AEC1 monitors each phase's voltage and current. If phase-loss protection (PLOS) is triggered, the IC stops switching and latches off.

PLOS can be disabled via the PL_EN bit.

Fault Diagnosis

The OCP, SCP, TSD, OVP, PLOS and rotor dead-lock protections have relative fault bits to indicate the fault if the corresponding fault is enabled. The fault bit(s) can be reset after the fault bit(s) is read.

Test Mode and Factory Mode

To configure the internal registers, the MPQ6634-AEC1 supports test mode. In test mode, all internal registers can be read/written. After the design is finalized, the register value can be configured to the non-volatile memory (NVM), which can be configured twice. Refer to the MPS Fan Driver GUI Software to change parameters easily and configure the memory.

REGISTER DESCRIPTION

Add	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h (OTP/REG)	SPEED_CONST[7:0]							
01h (OTP/REG)	KC[7:0]							
02h (OTP/REG)	KU[7:0]							
03h (OTP/REG)	SPD_MAX[7:0]							
04h (OTP/REG)	SPD_MAX[11:8]				U_START[3:0]			
05h (OTP/REG)	KI[7:4]				KP[3:0]			
06h (OTP/REG)	SPD KI[7:4]				ID_KI[3:0]			
07h (OTP/REG)	VF_TAR_THR [1:0]		VF_ACC_RAMP[1:0]		VF_ACC_TAR[1:0]		ALIGN_TIME[1:0]	
08h (OTP/REG)	UIN_COM	SOFT_ DOWN	SPD_ HZERO	SPD_ LZERO	FGRD_SEL[3:2]		TSS[1:0]	
09h (OTP/REG)	DIR_POR	PWM_POR	PWM_MD	PWM_DC	RETRY	OC_THR	OVP_EN	V_LOOP
0Ah (OTP/REG)	RD_MODE2	RD_ MODE1	RD_THR	UIN_SEL	RESERVE D	SLP_REF	GAIN[1:0]	
0Bh (OTP/REG)	D0[7:0]							
0Ch (OTP/REG)	D1[7:0]							
0Dh (OTP/REG)	D2[7:0]							
0Eh (OTP/REG)	D3[7:0]							
0Fh (OTP/REG)	D4[7:0]							
10h (OTP/REG)	S0[7:0]							
11h (OTP/REG)	S1[7:0]							
12h (OTP/REG)	S2[7:0]							
13h (OTP/REG)	S3[7:0]							
14h (OTP/REG)	S4[7:0]							
15h (OTP/REG)	RESERVED		HZERO_ THR	DIR_BRK	OCP_EN	PL_EN	RESERVE D	OMOD

SPEED_CONST (00h)

The SPEED_CONST command sets the internal calculation coefficient.

Bits	Access	Bit Name	Default	Description
7:0	R/W	SPEED CONST[7:0]	0x00	Used for internal calculation. Must be configured via the GUI.

KC (01h)

The KC command sets the internal calculation coefficient.

Bits	Access	Bit Name	Default	Description
7:0	R/W	KC[7:0]	0x00	Used for internal calculation. Must be configured via the GUI.

KU (02h)

The KU command sets the internal calculation coefficient.

Bits	Access	Bit Name	Default	Description
7:0	R/W	KU[7:0]	0x00	Used for internal calculation. Must be configured via the GUI.

MAX_SPEED_1 (03h)

The MAX_SPEED_1 command sets the lower 8 bits for the maximum speed in closed-loop control, or the output duty cycle in open-loop control when the PWM input duty cycle is 100%.

Bits	Access	Bit Name	Default	Description
7:0	R/W	SPD_MAX[7:0]	0x00	Sets the lower 8 bits for the maximum speed in closed-loop control, or the output duty cycle in open-loop control when the PWM input duty cycle is 100%. For closed-loop speed control, the electrical speed = 22rpm/LSB. For open-loop speed control, the output duty cycle = SPD_MAX[7:0] / 255.

MAX_SPEED_2/U_START (04h)

The MAX_SPEED_2/U_START command sets the higher 4 bits for the maximum speed in closed-loop control, as well as the initial start-up voltage.

Bits	Access	Bit Name	Default	Description
7:4	R/W	SPD_MAX[11:8]	0000	Sets the higher 4 bits for the maximum speed when the input duty cycle is 100%. These bits are combined with SPD_MAX[7:0] to set the maximum speed (electrical speed).
3:0	R/W	U_START[3:0]	0000	Sets the initial voltage during the alignment stage. The U_START voltage can be calculated with the following equation: U_START Voltage = U_START x 32 / VOL_OUT_GAIN If UIN_SEL = 0, VOL_OUT_GAIN = 94.85. If UIN_SEL = 1, VOL_OUT_GAIN = 48.79. Select a suitable initial voltage to ensure that the motor can start up reliably.

KP/KI (05h)

The KP/KI command sets the gain parameters for the internal calculation.

Bits	Access	Bit Name	Default	Description
7:4	R/W	KI[7:4]	0000	Must be configured via the GUI.
3:0	R/W	KP[3:0]	0000	Must be configured via the GUI.

SPD_KI/ID_KI (06h)

The SPD_KI/ID_KI command sets separate parameters for internal loop configuration.

Bits	Access	Bit Name	Default	Description
7:4	R/W	SPD_KI	0000	Must be configured via the GUI.
3:0	R/W	ID_KI	0000	Must be configured via the GUI.

START_UP (07h)

The START_UP command sets parameters and thresholds for V/F mode.

Bits	Access	Bit Name	Default	Description
7:6	R/W	VF_TAR_THR[1:0]	00	Sets the speed handoff threshold from V/F to sensorless control. During open-loop control, these bits set *N*. The handoff speed = 30.5 x V_{CC} x VOL_OUT_GAIN x N / SPEED CONST. See the MAX_SPEED_2/U_START (04h) section on page 18 for more details. 00: *N* = 1 01: *N* = 2 10: *N* = 4 11: *N* = 8 During closed-loop control, these bits set VF_TAR_THR. The handoff speed = SPD_MAX x VF_TAR_THR. 00: 3.125% 01: 6.25% 10: 12.5% 11: 25%
5:4	R/W	VF_ACC_RAMP[1:0]	00	Sets the electrical frequency acceleration ramp during the V/F stage. 00: 754rpm/s^2 01: 1509rpm/s^2 10: 3018rpm/s^2 11: 6035rpm/s^2
3:2	R/W	VF_ACC_TAR[1:0]	00	Sets the electrical frequency acceleration target during the V/F stage. 00: 515rpm/s 01: 1030rpm/s 10: 2060rpm/s 11: 3605rpm/s
1:0	R/W	ALIGN_TIME[1:0]	00	Sets the alignment time before entering the V/F stage. 00: 0.35s 01: 0.7s 10: 1.4s 11: 2s

CFR_1 (08h)

The control function register (CFR_1) sets UIN compensation, the soft-start and soft-dynamic adjustment, start-up duty cycle and stopping duty cycle, and the FG/RD pin's output.

Bits	Access	Bit Name	Default	Description
7	R/W	UIN_COM	0	Enables UIN compensation. This is only for open-loop applications. 0: Disabled 1: Enabled
6	R/W	SOFT_DOWN	0	Enables the soft-dynamic adjustment function to ensure that there is no reverse current during the dynamic process. 0: Disabled 1: Enabled
5	R/W	SPD_HZERO	0	Enables stopping the output switching function when the input PWM duty cycle exceeds the HZERO_THR setting. 0: Disabled 1: Enabled
4	R/W	SPD_LZERO	1	Enables stopping the output switching function when the input PWM duty cycle is below the D0[7:0] setting. 0: Disabled 1: Enabled
3:2	R/W	FGRD_SEL[1:0]	00	Sets the FG/RD pin's output. 00: FG 01: 2 x FG 10: RD 11: Fault indicator (nFT)
1:0	R/W	TSS[1:0]	00	Sets the start-up time for the duty reference to change from 0% to 100%, or from 100% to 0% 00: 2.6s 01: 5.4s 10: 7s 11: 10.5s

CFR_2 (09h)

The CFR_2 command sets the direction polarity and PWM input polarity, PWM input mode, restart mode, over-current protection (OCP) threshold, over-voltage protection (OVP), and loop configuration.

Bits	Access	Bit Name	Default	Description
7	R/W	DIR_POR	0	Sets the direction polarity. 0: Keep the DIR pin's default input 1: Reverse the DIR pin's input
6	R/W	PWM_POR	0	Sets the PWM input polarity, which is only for PWM signal mode applications. 0: Keep the PWM input 1: Reverse the PWM input
5	R/W	PWM_MD	0	Sets the PWM input frequency. 0: 50Hz to 1kHz 1: 1kHz to 20kHz

4	R/W	PWM_DC	0	Sets the PWM input mode. 0: PWM signal input 1: DC voltage
3	R/W	RETRY	0	Sets the restart mode after triggering locked-rotor protection and short-circuit protection (SCP). 0: Repeat 1: Latch-off
2	R/W	OC_THR	0	Sets the over-current (OC) threshold. 0: 2A 1: 1A
1	R/W	OVP_EN	0	Enables OVP. 0: Disabled 1: Enabled
0	R/W	V_LOOP	0	Sets the speed loop control. 0: Open-loop control 1: Closed-loop control

CFR_3 (0Ah)

The CFR_3 command sets the rotor dead-lock protection threshold, input voltage, LDO status under sleep mode, and loop gain.

Bits	Access	Bit Name	Default	Description
7	R/W	RD_MODE2	0	Determines whether the motor is stalled in mode 2. It is recommended to enable RD_MODE1 and RD_MODE2 when it is difficult for the motor to enter lock-off protection. 0: Disabled 1: Enabled
6	R/W	RD_MODE1	0	Determines whether the motor is stalled in mode 1. 0: Disabled 1: Enabled
5	R/W	RD_THR	0	Sets the rotor dead-lock protection threshold, which is only for RD_MODE1 applications. 1: Level 1. This configuration is recommended for most applications 0: Level 2. If a level 1 configuration makes it difficult to trigger lock-off protection, use this configuration instead
4	R/W	UIN_SEL	0	Sets the maximum V_{IN}. 0: 18V 1: 36V
3	NA	RESERVED	0	Reserved.
2	R/W	SLP_REF	0	Sets the LDO working status when entering sleep mode. 0: Disable the LDO 1: Enable the LDO
1:0	R/W	GAIN[1:0]	00	Sets the loop gain for the internal calculation. Must be configured via the GUI. 00: Max 01: High 10: Mid 11: Low

SPEED_CURVE_1 (0Bh)

The SPEED_CURVE_1 command sets the input PWM duty cycle (D0).

Bits	Access	Bit Name	Default	Description
7:0	R/W	D0[7:0]	0x00	Sets the input PWM duty cycle (D0), which can be calculated with the following equation: Input PWM Duty Cycle = D0[7:0] / 256

SPEED_CURVE_2 (0Ch)

The SPEED_CURVE_2 command sets the input PWM duty cycle (D1).

Bits	Access	Bit Name	Default	Description
7:0	R/W	D1[7:0]	0x40	Sets the input PWM duty cycle (D1), which can be calculated with the following equation: Input PWM Duty Cycle = D1[7:0] / 256

SPEED_CURVE_3 (0Dh)

The SPEED_CURVE_3 command sets the input PWM duty cycle (D2).

Bits	Access	Bit Name	Default	Description
7:0	R/W	D2[7:0]	0x80	Sets the input PWM duty cycle (D2), which can be calculated with the following equation: Input PWM Duty Cycle = D2[7:0] / 256

SPEED_CURVE_4 (0Eh)

The SPEED_CURVE_4 command sets the input PWM duty cycle (D3).

Bits	Access	Bit Name	Default	Description
7:0	R/W	D3[7:0]	0XC0	Sets the input PWM duty cycle (D3), which can be calculated with the following equation: Input PWM Duty Cycle = D3[7:0] / 256

SPEED_CURVE_5 (0Fh)

The SPEED_CURVE_5 command sets the input PWM duty cycle (D4).

Bits	Access	Bit Name	Default	Description
7:0	R/W	D4[7:0]	0xFF	Sets the input PWM duty cycle (D4), which can be calculated with the following equation: Input PWM Duty Cycle = D4[7:0] / 256

SPEED_CURVE_6 (10h)

The SPEED_CURVE_6 command configures speed or output duty when the input PWM duty cycle is D0, as set via SPEED_CURVE_1 (0Bh).

Bits	Access	Bit Name	Default	Description
7:0	R/W	S0[7:0]	0x20	Sets the speed or output duty cycle when the input PWM duty cycle = D0. For open-loop control, sets the output duty cycle. The output duty cycle can be calculated with the following equation: Output Duty Cycle = S0[7:0] / 256 For closed-loop control, sets the reference speed. The speed can be calculated with the following equation: Speed = S0[7:0] / 256 x SPD_MAX[11:0]

SPEED_CURVE_7 (11h)

The SPEED_CURVE_7 command configures speed or output duty when the input PWM duty cycle is D1, as set via SPEED_CURVE_2 (0Ch).

Bits	Access	Bit Name	Default	Description
7:0	R/W	S1[7:0]	0x40	Sets the speed or output duty cycle when the input PWM duty cycle = D1. For open-loop control, sets the output duty cycle. The output duty cycle can be calculated with the following equation: Output Duty Cycle = S1[7:0] / 256 For closed-loop control, sets the reference speed. The speed can be calculated with the following equation: Speed = S1[7:0] / 256 x SPD_MAX[11:0]

SPEED_CURVE_8 (12h)

The SPEED_CURVE_8 command configures speed or output duty when the input PWM duty cycle is D2, as set via SPEED_CURVE_3 (0Dh).

Bits	Access	Bit Name	Default	Description
7:0	R/W	S2[7:0]	0x80	Sets the speed or output duty cycle when the input PWM duty cycle = D2. For open-loop control, sets the output duty cycle. The output duty cycle can be calculated with the following equation: Output Duty Cycle = S2[7:0] / 256 For closed-loop control, sets the reference speed. The speed can be calculated with the following equation: Speed = S2[7:0] / 256 x SPD_MAX[11:0]

SPEED_CURVE_9 (13h)

The SPEED_CURVE_9 command configures speed or output duty when the input PWM duty cycle is D3, as set via SPEED_CURVE_4 (0Eh).

Bits	Access	Bit Name	Default	Description
7:0	R/W	S3[7:0]	0xC0	Sets the speed or output duty cycle when the input PWM duty cycle = D3. For open-loop control, sets the output duty cycle. The output duty cycle can be calculated with the following equation: Output Duty Cycle = S3[7:0] / 256 For closed-loop control, sets the reference speed. The speed can be calculated with the following equation: Speed = S3[7:0] / 256 x SPD_MAX[11:0]

SPEED_CURVE_10 (14h)

The SPEED_CURVE_10 command configures speed or output duty when the input PWM duty cycle is D4, as set via SPEED_CURVE_5 (0Fh).

Bits	Access	Bit Name	Default	Description
7:0	R/W	S4[7:0]	0xFF	Sets the speed or output duty cycle when the input PWM duty cycle = D4. For open-loop control, sets the output duty cycle. The output duty cycle can be calculated with the following equation: Output Duty Cycle = S4[7:0] / 256 For closed-loop control, sets the reference speed. The speed can be calculated with the following equation: Speed = S4[7:0] / 256 x SPD_MAX[11:0]

CFR_4 (15h)

The CFR_4 command sets the stopping duty threshold and brake function when the motor runs in reverse rotation; in addition, it enables over-current protection (OCP), phase-loss protection (PLOS), and the over-modulation function.

Bits	Access	Bit Name	Default	Description
7:6	NA	RESERVED	00	Reserved.
5	R/W	HZERO_THR	0	Sets the stopping threshold when the input PWM duty cycle exceeds HZERO_THR. This function takes effect when SPD_HZERO configuration is enabled. 0: 98% 1: 88%
4	R/W	DIR_BRK	0	Enables the brake function when the motor works in reverse rotation. 0: Disabled 1: Enabled
3	R/W	OCP_EN	0	Enables OCP. 0: Disabled 1: Enabled
2	R/W	PL_EN	0	Enables PLOS. 0: Disabled 1: Enabled
1	NA	RESERVED	0	Reserved.
0	R/W	OMOD	0	Enables the over-modulation function. 0: Disabled 1: Enabled

APPLICATION INFORMATION

Selecting the Input Capacitor

Place an input capacitor near VCC to keep V_{IN} stable and reduce the input switching voltage noise and ripple. The input capacitor impedance must be low at the switching frequency (f_{SW}).

Ceramic capacitors with X7R dielectrics are recommended for their low-ESR characteristics. Ensure that the ceramic capacitance is dependent on the voltage rating. The DC biased voltage and value can lose more than 50% of its capacitance at its rated voltage rating.

Leave a sufficient voltage rating margin when selecting the component. For most applications, a 10μF ceramic capacitor is sufficient.

If needed for the application, add an additional, larger-value, electrolytic capacitor to absorb inductor energy.

A voltage-clamping TVS diode is recommended to avoid high voltage spikes that result when the energy stored in the motor charges back to input side.

Selecting the Input Snubber

Due to the input capacitor's energy charge/discharge during the phase transition soft switching, the input current has switching cycle ringing. If needed, add an RC snubber (a 2Ω resistor in series with a 1μF capacitor) in parallel with the input capacitor. This prevents switching cycle ringing.

Selecting the REF Output Capacitor

The REF pin must be locally bypassed with a capacitor to provide power for the gate driver. A minimum 1μF ceramic capacitor with X7R or X5R dielectrics is recommended.

Communication Connection

The MPQ6634-AEC1 has an individual I^2C communication interface; in addition, the MPQ6634-AEC1 can use the SPD and FG/RD pins to act as the I^2C interface to read and write the internal register bits.

Users do not have to enter test mode to use the individual SDA and SCL to cooperate with the external controller to send and receive data.

However, when using SPD and FG/RD for the communication interface, users must be in test mode. In test mode, the SPD pin acts as the data input and output, and the FG/RD pin acts as the clock signal input.

System-Level ESD Enhancement

Some fan products must pass system-level ESD testing. Compared to the HBM ESD ratings, system-level ESD follows the IEC61000-4-2 standard. There are two different modes for the IEC61000-4-2 ESD test: air discharge and contact discharge. Contact discharge mode is the first choice for testing.

Figure 8 shows the equivalent circuit of an HBM ESD circuit.

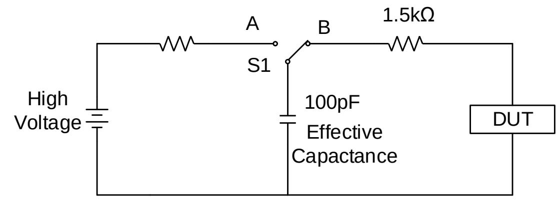


Figure 8: Equivalent Circuit of HBM ESD Circuit

Figure 9 shows that the IEC61000-4-2 sets the equivalent circuit.

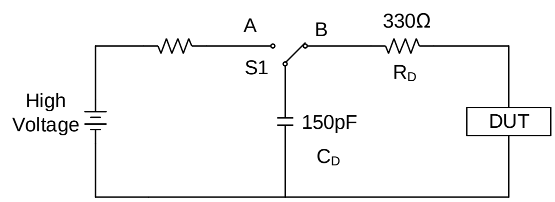


Figure 9: Equivalent Circuit of System-Level ESD

Compared to the HBM ESD ratings, the discharge capacitance exceeds the human body's effective capacitance, and the discharge resistance of the IEC-level ESD is much smaller.

To pass ±8kV for IEC61000-4-2 contact discharge mode, an external circuit may be required to enhance the ESD capability. Figure 10 on page 26 shows an example to enhance the ESD capability with external components. Due to the difference between components, the test results may vary slightly.

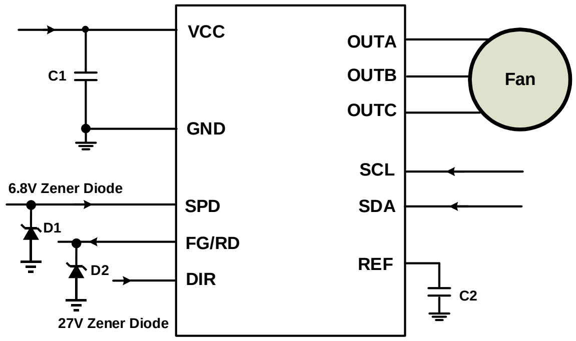


Figure 10: External ESD-Enhanced Circuit

Motor Parameters Measurement

The motor phase resistance and phase inductance are two important parameters for sensorless FOC control. The motor's phase resistance/inductance refers to the resistance/inductance from the phase output to the center tap, respectively.

To obtain the phase resistance, measure the resistance between two phase terminals using a multimeter or LCR meter, then divide the value by two.

The phase inductance is measured by measuring the inductance between two phase terminals via the LCR meter, then dividing this value by two. The LCR frequency and voltage setting are referenced to the 1kHz and 1V measurement.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation and excellent performance. For the best results, refer to Figure 11 and follow the guidelines below.

1. Place C_{IN} as close as possible to the VCC and GND pins.
2. Place the VREG bypass capacitor as close as possible to the VREG and GND pins.

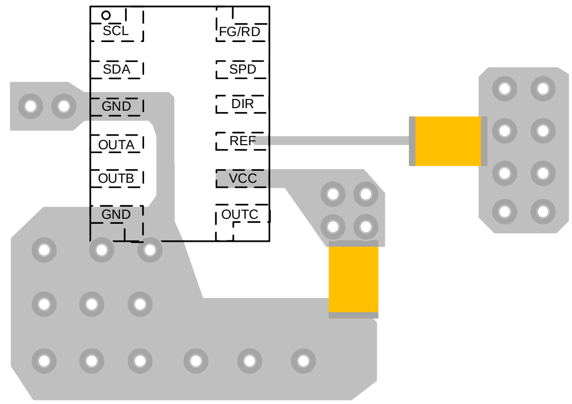


Figure 11: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

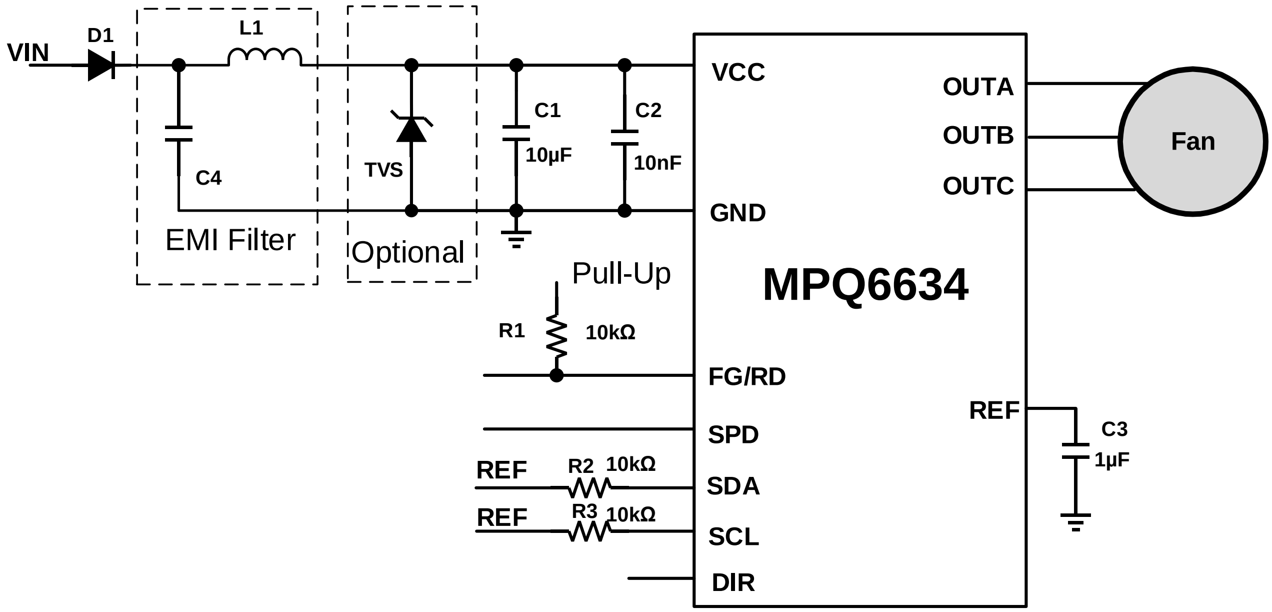
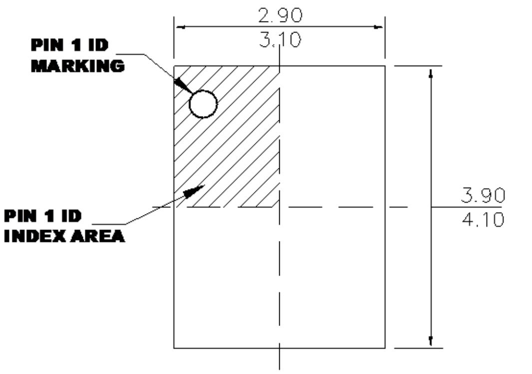


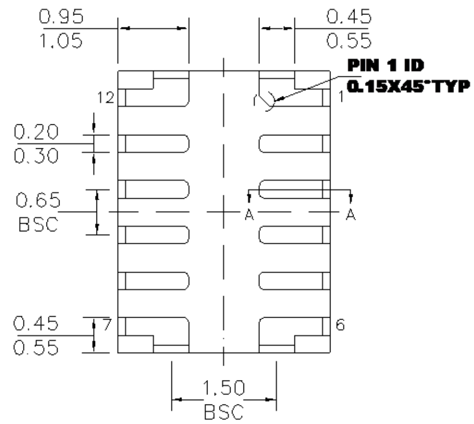
Figure 12: Typical Application Circuit

PACKAGE INFORMATION

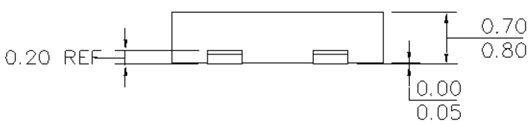
TQFN-12 (3mmx4mm)
Wettable Flank



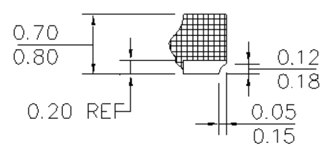
TOP VIEW



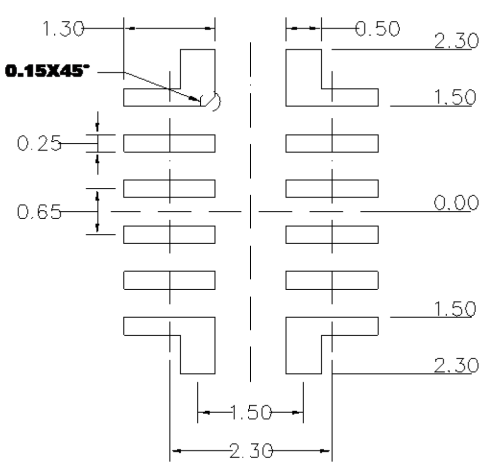
BOTTOM VIEW



SIDE VIEW



SECTION A-A

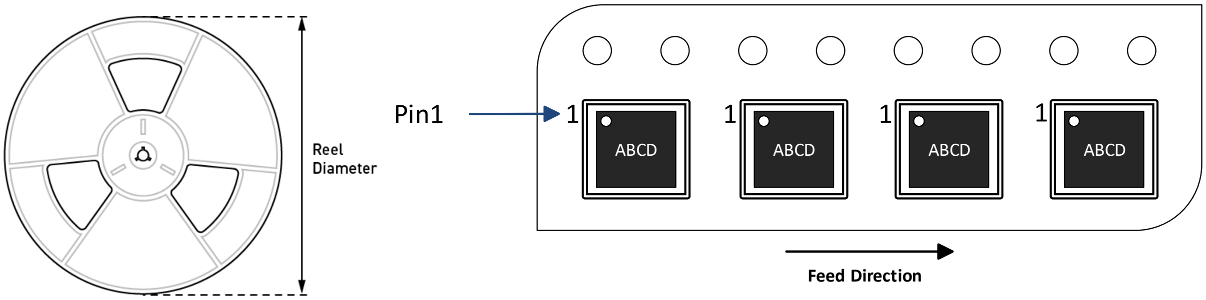


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6634-AEC1GLTE-xxxx-AEC1-Z	TQFN-12-WF (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/25/2024	Initial Release	-