# MPQ6600L

## 35V, 1.5A Stepper Motor Driver with Internal Current Sense, AEC-Q100 Qualified

## HI EDESCRIPTION

The MPQ6600L is a stepper motor driver with current regulation and a built-in translator. The device provides internal current sensing, which does not require external sense resistors. With high integration and a small package size, the MPQ6600L is a space-saving, cost-effective solution for bipolar stepper motor drives.

The MPQ6600L operates from a supply voltage up to 35V and can deliver motor currents up to 1.5A based on the PCB design and thermal conditions. The device can operate a bipolar stepper motor in full-, half-, quarter-, or eighth-step mode. Internal safety features include over-current protection (OCP), input over-voltage protection (OVP), under-voltage lockout (UVLO), and thermal shutdown.

The MPQ6600L is available in a QFN-24 (4mmx4mm) package with wettable flanks, and is AEC-Q100 qualified.

## FEATURES

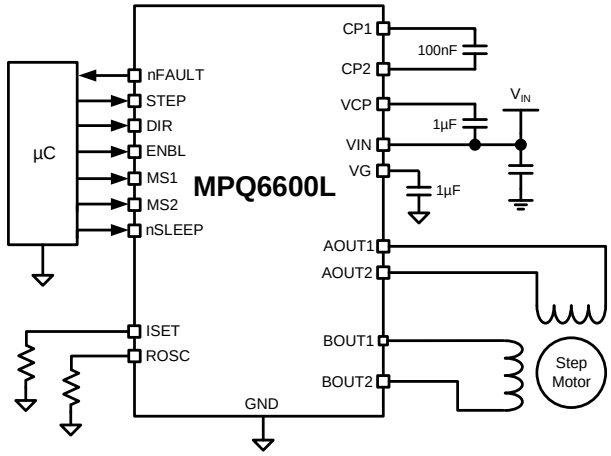
- Wide 4.5V to 35V Input Voltage ($V_{IN}$) Range
- Two Internal Full-Bridge Drivers
- Internal Current Sensing and Regulation
- Low On Resistance ($R_{DS(ON)}$): 195mΩ High-Side MOSFET (HS-FET) and 170mΩ Low-Side MOSFET (LS-FET)
- No Control Power Supply Required
- Simple Logic Interface
- 3.3V and 5V Compatible Logic Supply
- Step Modes from Full Step to Eighth-Step
- Up to 1.5A of Output Current ($I_{OUT}$)
- Automatic Current Decay
- Over-Current Protection (OCP)
- Input Over-Voltage Protection (OVP)
- Thermal Shutdown and Under-Voltage Lockout (UVLO) Protection
- Fault Indication Output
- Available in a QFN-24 (4mmx4mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

## APPLICATIONS

- Bipolar Stepper Motors
- Printers



## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number* | Package | Top Marking | MSL Rating |
|---|---|---|---|
| MPQ6600LGRE-AEC1 | QFN-24 (4mmx4mm) | *See Below* | 1 |

* For Tape & Reel, add suffix -Z (e.g. MPQ6600LGRE-AEC1-Z).

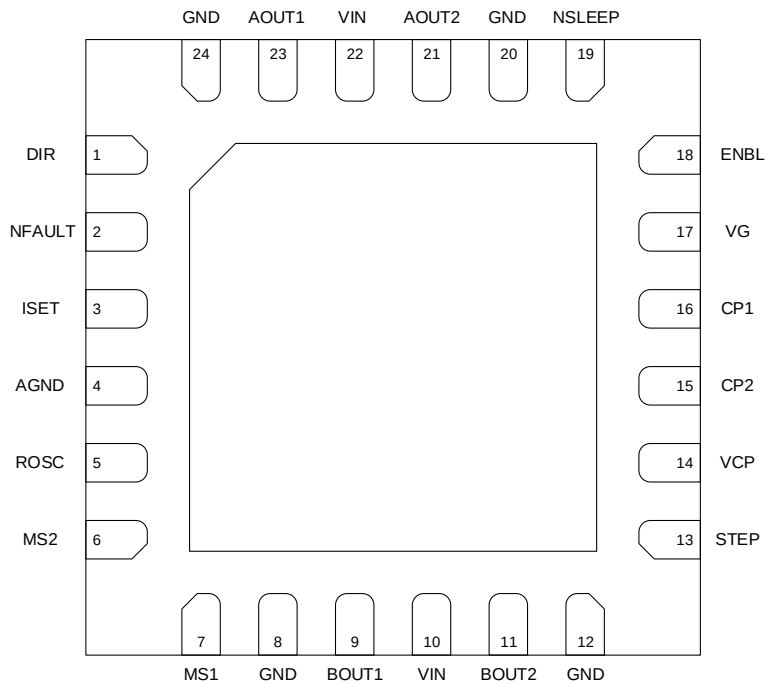
## TOP MARKING

MPSYWW
M6600L
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
M6600L: Part number
LLLLLL: Lot number
E: Wettable flank

## PACKAGE REFERENCE

**TOP VIEW**




**QFN-24 (4mmx4mm) with Wettable Flanks**

## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | DIR | **Direction input.** The DIR pin has an internal pull-down resistor. |
| 2 | nFAULT | **Fault indication.** The nFAULT pin is an open-drain output. If there is a fault condition (e.g. over-current, over-temperature, or over-voltage conditions), pull nFAULT logic low. |
| 3 | ISET | **Current setting configuration.** Place a resistor between the ISET pin and ground to set the current through the motor. |
| 4 | AGND | **Analog ground.** |
| 5 | ROSC | **Constant-off-time (COT) configuration.** A resistor connected between the ROSC pin and ground sets the pulse-width modulation (PWM) off time. |
| 6 | MS2 | **Mode selection.** The MS1 and MS2 pins set the step mode (full-, half-, quarter-, or eighth- step). MS1 and MS2 have an internal pull-down resistor. |
| 7 | MS1 | |
| 8, 12, 20, 24, EP | GND | **Power ground.** |
| 9 | BOUT1 | **Bridge B output terminal 1.** |
| 10, 22 | VIN | **Input supply voltage.** Both VIN pins must be connected to the same supply. Decouple VIN to ground using a minimum 100nF ceramic capacitor. |
| 11 | BOUT2 | **Bridge B output terminal 2.** |
| 13 | STEP | **Step input.** The step signal's rising edge arranges the sequence of the translator and advances the motor by an increment. The STEP pin has an internal pull-down resistor. |
| 14 | VCP | **Charge pump output.** Connect a 1µF, 16V, X7R ceramic capacitor between the VCP and VIN pins. |
| 15 | CP2 | **Charge pump capacitor.** Connect a 100nF, X7R ceramic capacitor rated for the VIN pin voltage ($V_{IN}$) at minimum between the CP2 and CP1 terminals. |
| 16 | CP1 | |
| 17 | VG | **Gate drive voltage of the low-side MOSFETs (LS-FETs).** Connect a 1µF, 16V, X7R ceramic capacitor between the VG pin and ground. |
| 18 | ENBL | **Enable input.** Pull the ENBL pin logic low to disable the bridge outputs and translator operation; pull the pin logic high to enable the bridge outputs and translator operation. ENBL has an internal pull-down resistor. |
| 19 | nSLEEP | **Sleep mode input.** Pull the nSLEEP pin logic high to enable normal operation. nSLEEP has an internal pull-down resistor. |
| 21 | AOUT2 | **Bridge A output terminal 2.** |
| 23 | AOUT1 | **Bridge A output terminal 1.** |

## ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage ($V_{IN}$) .....-0.3V to +40V
xOUTx voltage ($V_{A/BOUT1/2}$).....-0.7V to +40V
VCP, CP2 .....$V_{IN}$ to $V_{IN}$ + 6.5V
All other pins to AGND.....-0.3V to +6.5V
Continuous power dissipation ($T_A$ = 25°C) (2).....
.....2.9W
Storage temperature..... -55°C to +150°C
Junction temperature ($T_J$) .....150°C
Lead temperature (solder) .....260°C

### *ESD Ratings*

Human body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±2kV

### *Recommended Operating Conditions* (3)

Supply voltage ($V_{IN}$) .....4.5V to 35V
Output current ($I_{A/BOUT}$)..... ±1.5A
Operating junction temp ($T_J$).... -40°C to +125°C

### *Thermal Resistance* (4) $\theta_{JA}$ $\theta_{JC}$

QFN-24 (4mmx4mm)..... 42..... 9.... °C/W

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J$ (MAX), the junction-to-ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, a 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 24V, $T_J$ = -40°C to +125°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| Input supply voltage | $V_{IN}$ | | 4.5 | 24 | 35 | V |
| Quiescent current | $I_Q$ | $V_{IN}$ = 24V, ENBL = 1, nSLEEP = 1, with no load | | 1.5 | 5 | mA |
| | $I_{SLEEP}$ | $V_{IN}$ = 24V, nSLEEP = 0 | | | 2.5 | µA |
| **Internal MOSFETs** | | | | | | |
| Output on resistance | $R_{DS(ON)\_HS}$ | $V_{IN}$ = 24V, $I_{OUT}$ = 1A, $T_J$ = 25°C | | 0.195 | 0.3 | Ω |
| | | $V_{IN}$ = 24V, $I_{OUT}$ = 1A, $T_J$ = 125°C | | 0.25 | 0.35 | Ω |
| | $R_{DS(ON)\_LS}$ | $V_{IN}$ = 24V, $I_{OUT}$ = 1A, $T_J$ = 25°C | | 0.17 | 0.3 | Ω |
| | | $V_{IN}$ = 24V, $I_{OUT}$ = 1A, $T_J$ = 125°C | | 0.25 | 0.35 | Ω |
| Body diode forward voltage | $V_F$ | $I_{OUT}$ = 1.5A | | | 1.1 | V |
| **Control Logic** | | | | | | |
| Input logic low threshold | $V_{IL}$ | | | | 0.8 | V |
| Input logic high threshold | $V_{IH}$ | Except nSLEEP | 2.1 | | | V |
| nSLEEP logic high threshold | $V_{IH}$ | | 2.2 | | | V |
| Logic input current | $I_{IN\_H}$ | $V_{IH}$ = 5V | | | 20 | µA |
| | $I_{IN\_L}$ | $V_{IL}$ = 0.8V | | | 5 | µA |
| Internal pull-down resistance | $R_{PD}$ | | | 500 | | kΩ |
| **nFAULT Outputs (Open-Drain Outputs)** | | | | | | |
| Output low voltage | $V_{OL}$ | $I_{OUT}$ = 5mA | | | 0.5 | V |
| Output high leakage current | $I_{OH}$ | $V_{OUT}$ = 3.3V | | | 1 | µA |
| **Protection Circuit** | | | | | | |
| Under-voltage lockout (UVLO) rising threshold | $V_{IN\_UVLO\_R}$ | | 3.3 | 3.6 | 4 | V |
| UVLO falling threshold | $V_{IN\_UVLO\_F}$ | | 3 | 3.3 | 3.7 | V |
| Input over-voltage protection (OVP) threshold | $V_{OVP}$ | | 36 | 37.5 | 39 | V |
| Input OVP hysteresis | $\Delta V_{OVP}$ | | | 1900 | | mV |
| Over-current (OC) trip threshold | $I_{OCP1}$ | Sinking | 3.5 | 6 | 10 | A |
| | $I_{OCP2}$ | Sourcing | 2.5 | 6 | 11 | A |
| OC deglitch time [5] | $t_{OCP}$ | | | 1 | | µs |
| Thermal shutdown [5] | $T_{TSD}$ | | | 165 | | °C |
| Thermal shutdown hysteresis [5] | $\Delta T_{TSD}$ | | | 15 | | °C |
| **Current Regulation** | | | | | | |
| Constant off time | $t_{OFF}$ | $R_T$ = 200kΩ | 19 | 23 | 26 | µs |
| Peak current regulation level | $I_{PEAK}$ | $R_{ISET}$ = 71kΩ | 0.95 | 1 | 1.05 | A |
| ISET voltage | $V_{ISET}$ | | 0.8 | 0.9 | 1 | V |
| ISET current ratio | $A_{ISET}$ | $I_{ISET}$ / $I_{OUT}$ | 11 | 12.676 | 14 | µA/A |
| Blanking time [5] | $t_{BLANK}$ | | | 2 | | µs |
| Current trip accuracy | $\Delta I_{TRIP}$ | $R_{ISET}$ = 71kΩ, 71% to 100% | -5 | | +5 | % of $I_{TRIP}$ |
| | | $R_{ISET}$ = 71kΩ, 38% to 67% | -9 | | +9 | % of $I_{TRIP}$ |
| | | $R_{ISET}$ = 71kΩ, <34% | -12 | | +12 | % of $I_{TRIP}$ |

## TIMING CHARACTERISTICS

**$V_{IN}$ = 24V, $T_J$ = -40°C to +125°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| STEP high time (5) | $t_1$ | | 1 | | | µs |
| STEP low time (5) | $t_2$ | | 1 | | | µs |
| Set-up time of MSx or DIR to rising STEP (5) | $t_3$ | | 200 | | | ns |
| Hold time of rising STEP to MSx or DIR change (5) | $t_4$ | | 200 | | | ns |

**Note:**

5) Not tested in production.

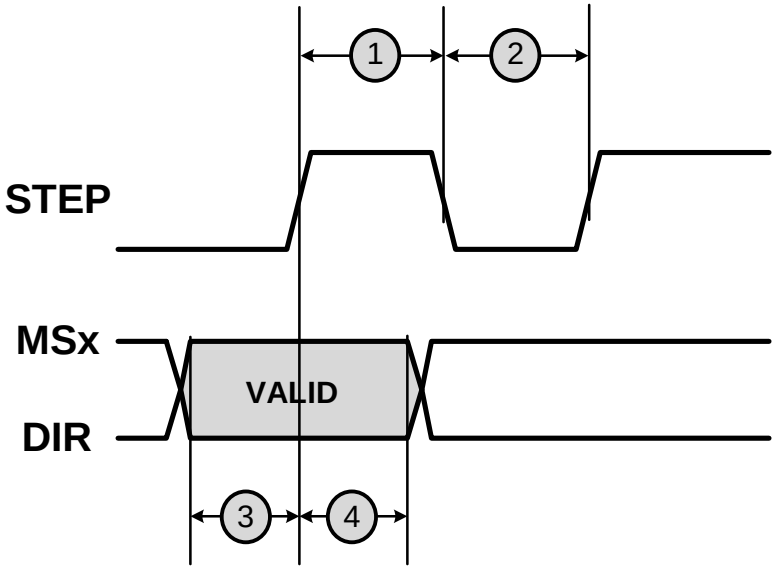
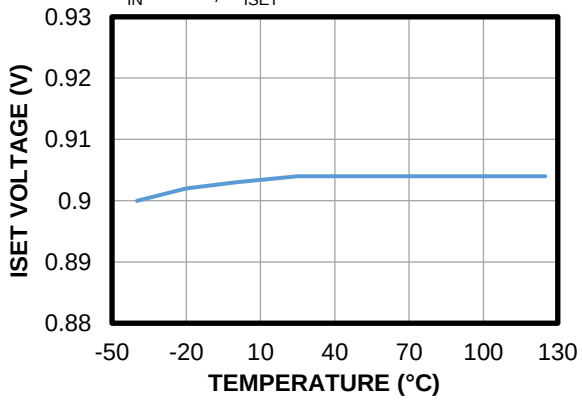



**Figure 1: STEP Timing Diagram**

## TYPICAL CHARACTERISTICS

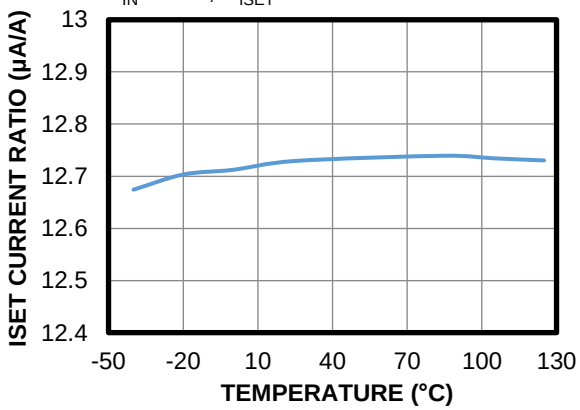
**ISET Voltage vs. Temperature**

$V_{IN}$ = 24V, $R_{ISET}$ = 71kΩ



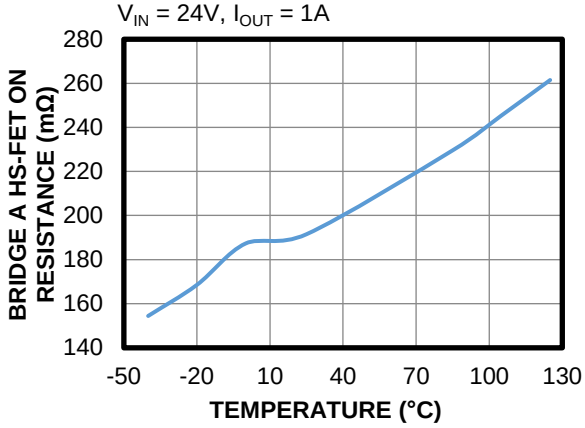

**ISET Current Ratio vs. Temperature**

$V_{IN}$ = 24V, $R_{ISET}$ = 71kΩ



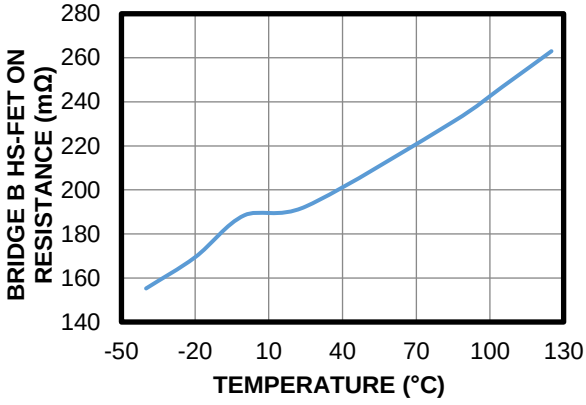

**Bridge A HS-FET On Resistance vs. Temperature**

$V_{IN}$ = 24V, $I_{OUT}$ = 1A



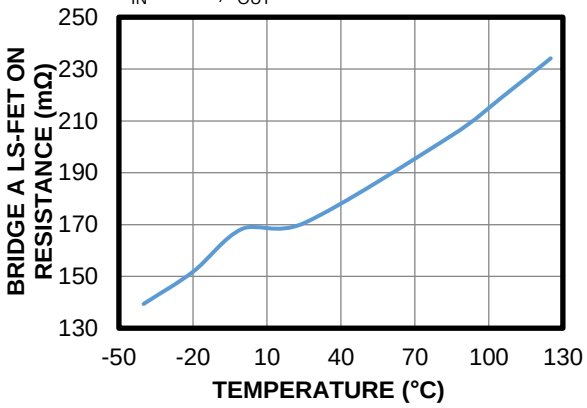

**Bridge B HS-FET On Resistance vs. Temperature**

$V_{IN}$ = 24V, $I_{OUT}$ = 1A



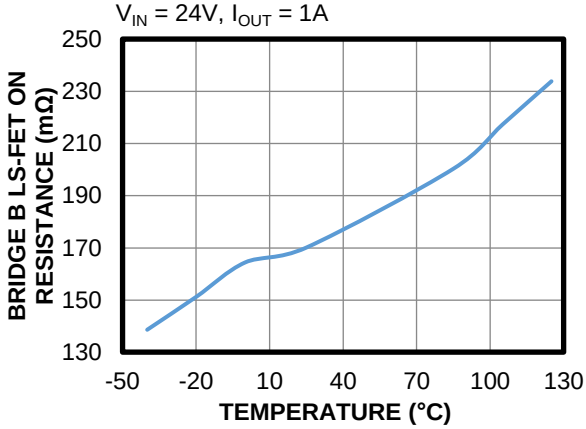

**Bridge A LS-FET On Resistance vs. Temperature**

$V_{IN}$ = 24V, $I_{OUT}$ = 1A



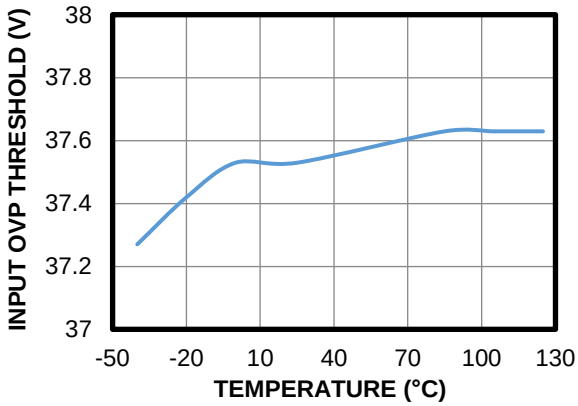

**Bridge B LS-FET On Resistance vs. Temperature**

$V_{IN}$ = 24V, $I_{OUT}$ = 1A



## TYPICAL CHARACTERISTICS *(continued)*

**Input OVP Threshold vs. Temperature**

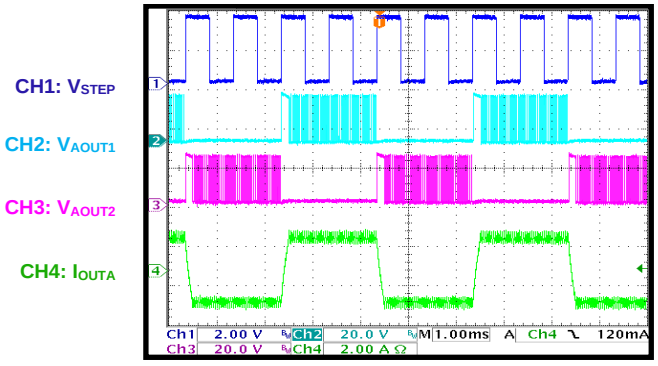


# TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 24V, $f_{STEP}$ = 1kHz, $T_A$ = 25°C, resistor and inductor load: R = 3.3Ω, L = 1.5mH/channel, unless otherwise noted.**

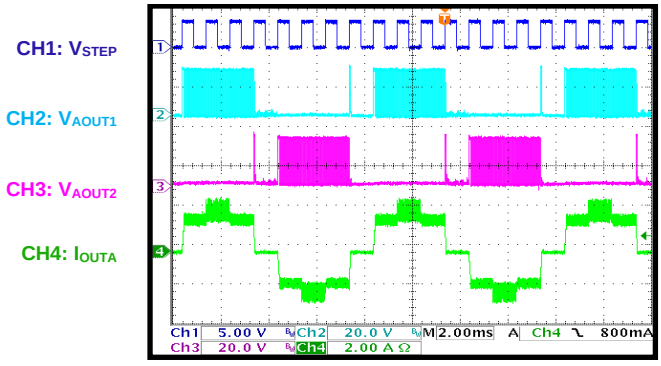
### Steady State

$I_{OUT}$ = 1A, full step



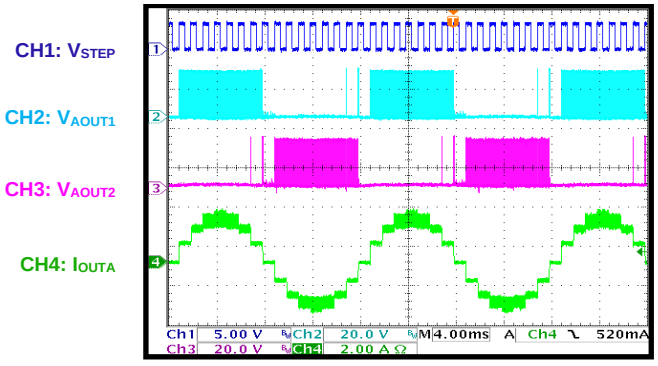

### Steady State

$I_{OUT}$ = 1.5A, half-step



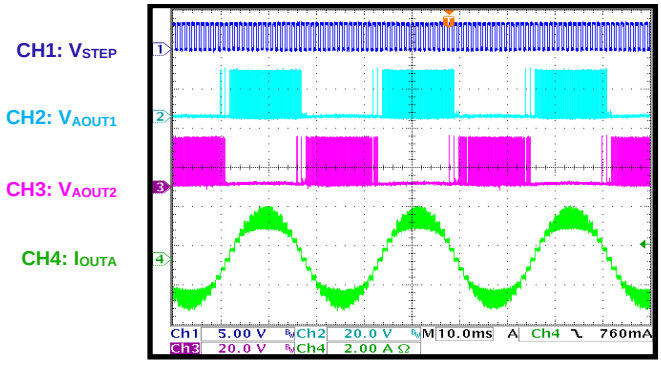

### Steady State

$I_{OUT}$ = 1.5A, quarter-step



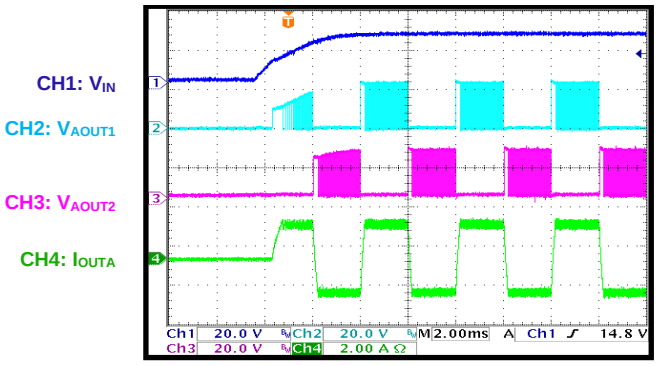

### Steady State

$I_{OUT}$ = 1.5A, eighth-step



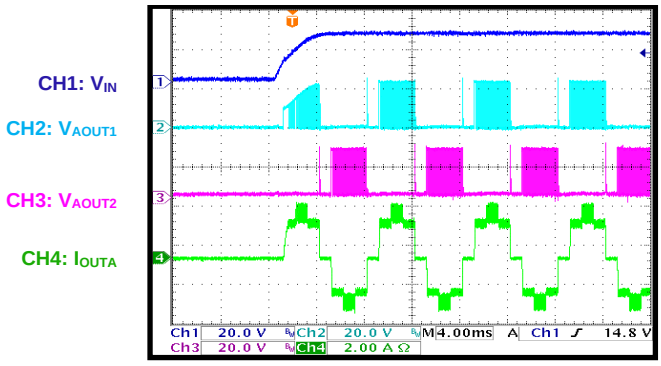

### Power Ramp-Up

$I_{OUT}$ = 1A, full step




### Power Ramp-Up

$I_{OUT}$ = 1.5A, half-step

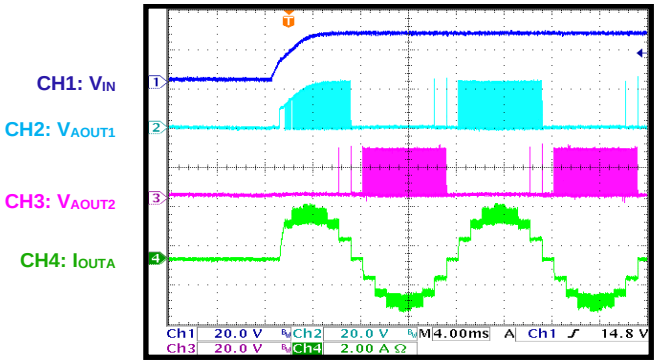


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $f_{STEP}$ = 1kHz, $T_A$ = 25°C, resistor and inductor load: R = 3.3Ω, L = 1.5mH/channel, unless otherwise noted.**

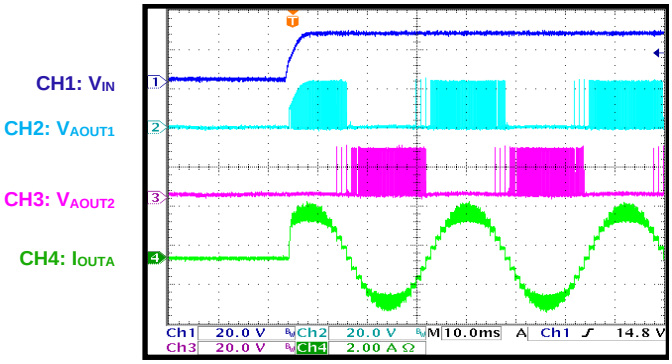
### Power Ramp-Up

$I_{OUT}$ = 1.5A, quarter-step



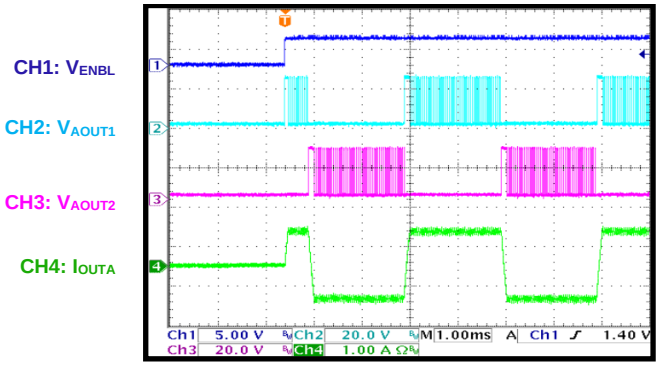

### Power Ramp-Up

$I_{OUT}$ = 1.5A, eighth-step



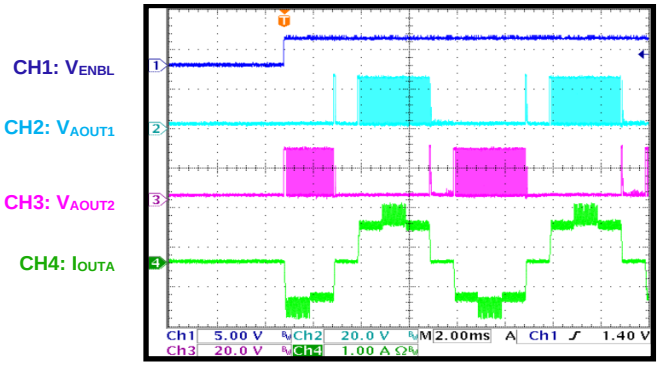

### Enable

$I_{OUT}$ = 1A, full step



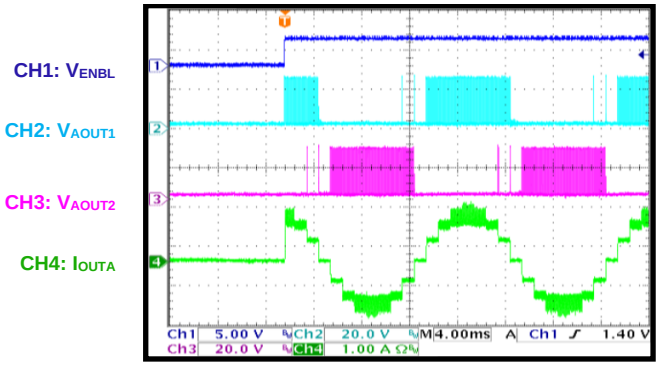

### Enable

$I_{OUT}$ = 1.5A, half-step



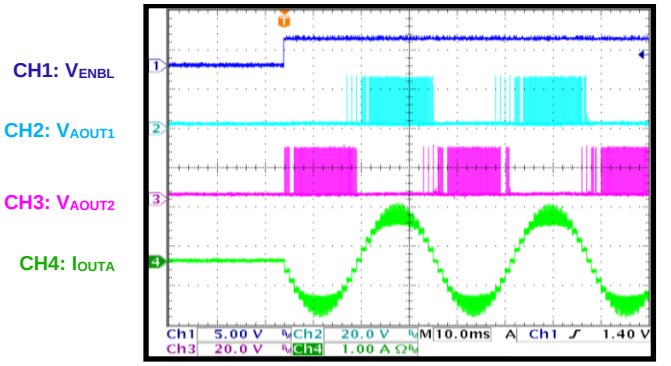

### Enable

$I_{OUT}$ = 1.5A, quarter-step




### Enable

$I_{OUT}$ = 1.5A, eighth-step

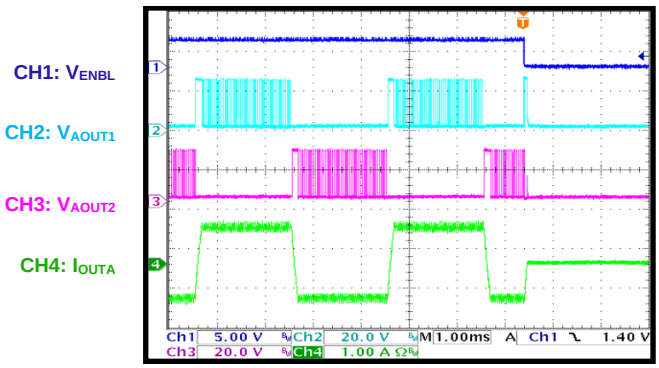


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $f_{STEP}$ = 1kHz, $T_A$ = 25°C, resistor and inductor load: R = 3.3Ω, L = 1.5mH/channel, unless otherwise noted.**

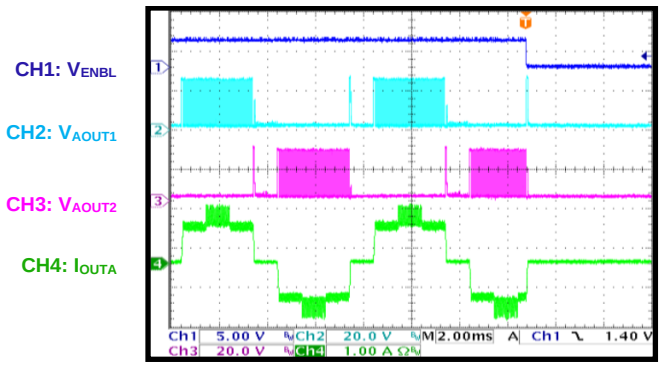
**Disable**

$I_{OUT}$ = 1A, full step



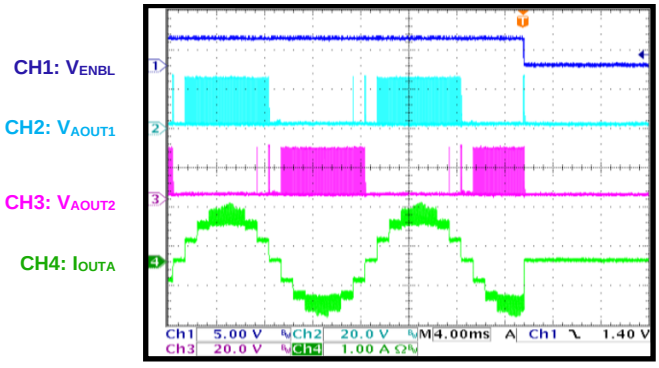

**Disable**

$I_{OUT}$ = 1.5A, half-step



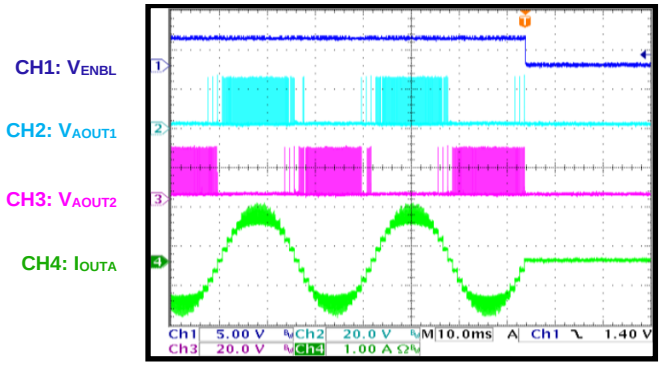

**Disable**

$I_{OUT}$ = 1.5A, quarter-step




**Disable**

$I_{OUT}$ = 1.5A, eighth-step



## FUNCTIONAL BLOCK DIAGRAM

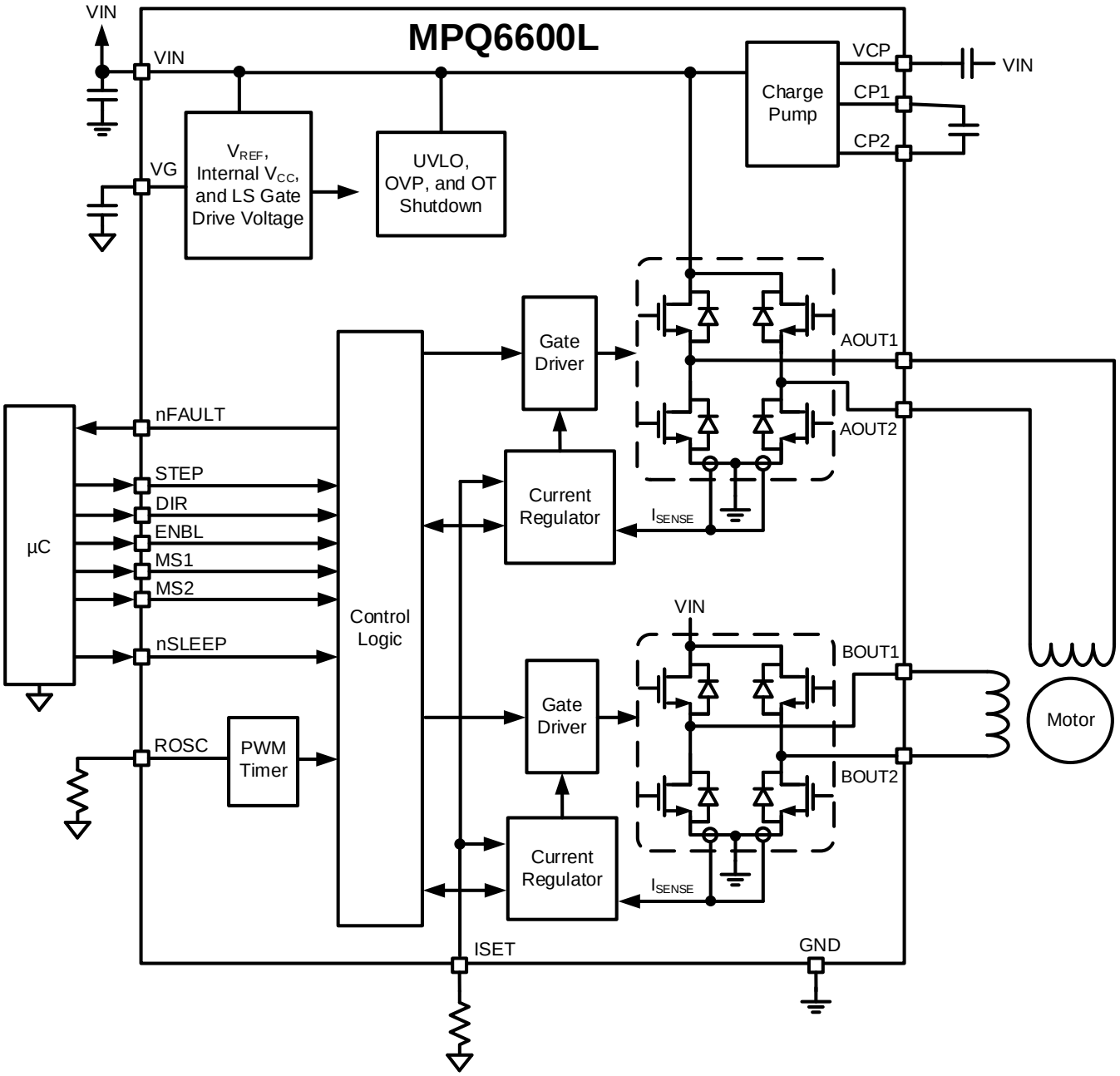



**Figure 2: Functional Block Diagram**

## OPERATION

The MPQ6600L is a bipolar stepper motor driver that integrates eight N-channel power MOSFETs. These MOSFETs are arranged as two full bridges that each have a current capability up to 1.5A. The MPQ6600L operates across a wide 4.5V to 35V input voltage ($V_{IN}$) supply range.

The MPQ6600L is designed to operate bipolar stepper motors in full-, half-, quarter-, and eighth-step modes. At each step, the current of each full bridge is set by the output voltage ($V_{OUT}$) of a digital-to-analog converter (DAC), which is controlled by the translator's output.

The currents in each of the two outputs are regulated with configurable constant-off-time (COT) pulse-width modulation (PWM) control. The MPQ6600L does not require external sense resistors due to its integrated internal current sensing.

### Stepping

The motor moves step by step by applying a series of pulses to the STEP input. A rising edge on STEP arranges the sequence of the translator and advances the motor by an increment. The translator controls the input to the DACs and the direction of current flow in each winding. The amplitude of the increment (step size) is determined by the state of the MS1 and MS2 inputs (see Table 1).

**Table 1: Stepping Format**

| MS2 | MS1 | STEP Mode |
|---|---|---|
| Low | Low | Full step |
| Low | High | Half-step |
| High | Low | Quarter-step |
| High | High | Eighth-step |

The state of DIR determines the direction of the stepper motor's rotation.

The minimum STEP pulse width is 1µs. The logic control inputs (MSx and DIR, where x = 1 or 2) require at least 200ns of set-up time and hold time to the STEP input's rising edge (see Figure 3).

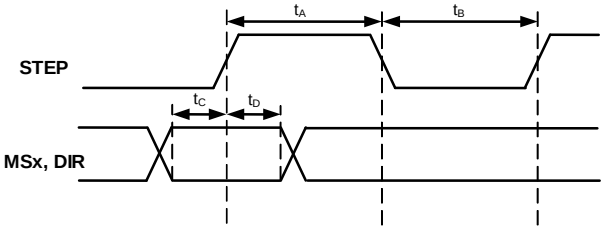



**Figure 3: Set-Up and Hold Times of MSx and DIR**

### Configurable Constant-Off-Time (COT) Current Control

The motor current is regulated by a configurable COT PWM current control circuit. Initially, a diagonal pair of MOSFETs turns on and drives the current through the motor winding. The current increases in the motor winding, which is sensed by an internal current-sense circuit. During the initial blanking time ($t_{BLANK}$), the high-side MOSFET (HS-FET) turns on regardless of current-limit detection.

When the current reaches the current trip threshold, the internal current comparator either shuts down the HS-FET or turns on another diagonal pair of MOSFETs. Shutting down the HS-FET allows the winding inductance current to freewheel through the two low-side MOSFETs (LS-FETs) in slow decay mode. Turning on another diagonal pair of MOSFETs allows the current to flow back to the input in fast decay mode. The current continues decreasing for the COT duration unless a zero-current step is detected. Afterward, the HS-FET is enabled to increase the winding current again. Then the cycle repeats.

The off time ($t_{OFF}$) is determined by an external resistor ($R_{OSC}$). $t_{OFF}$ can be estimated with Equation (1):

$$t_{OFF}(ns) = 115 \times R_{OSC}(k\Omega) \quad (1)$$

The full-scale (100%) regulation current can be calculated with Equation (2):

$$I_{MAX} = 71k\Omega / R_{ISET} \quad (2)$$

The DAC output reduces the trip current in precise steps. The trip current ($I_{TRIP}$) can be calculated with Equation (3):

$$I_{TRIP} = \%I_{TRIP} \times I_{MAX} \quad (3)$$

Where $\%I_{TRIP}$ is % of $I_{MAX}$. See Table 2 on page 17 for the $\%I_{TRIP}$ values at each step.

### Blanking Time

There is typically a current spike during the switching transition due to the body diode's reverse recovery current and the distributed winding capacitance of the motor. This current spike requires filtering to prevent it from erroneously shutting down the HS-FET.

After the PWM cycle begins, the output of the current-sense comparator is ignored for the fixed blanking time. This blanking time results in a minimum on time for the PWM cycle.

### Automatic Decay Mode

The MPQ6600L uses an automatic decay mode to provide accurate current regulation.

Initially, slow decay is used. If the current exceeds the $I_{TRIP}$ threshold at the end of the fixed off time, fast decay mode is initiated by reversing the state of the H-bridge outputs.

Once the current level drops below the $I_{TRIP}$ threshold during this fast decay period, slow decay is engaged again for another fixed off time. After the completion of this second fixed off time, a new PWM cycle begins.

Figure 4 shows automatic decay mode during a current reduction resulting from a step input.

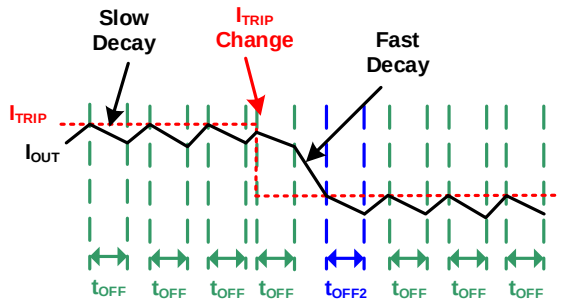



**Figure 4: Automatic Decay Mode during $t_{OFF}$ (Unless $I_{OUT} > I_{TRIP}$ at the End of $t_{OFF}$)**

In the case of high voltage and low inductance, or the regulation of very small currents, the minimum on time of the PWM cycle (set by the fixed blanking time) can cause the current to rise quickly. In this scenario, both slow and fast decay are used (see Figure 5).

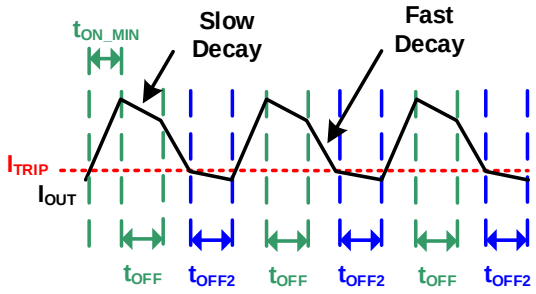



**Figure 5: Current Regulation of Slow and Fast Decay Mode**

### Microstepping Selection (MS1 and MS2)

The step mode is selected by applying logic high and low voltages to the MS1 and MS2 pins (see Table 1 on page 12). The MPQ6600L supports full-, half-, quarter-, and eighth-step modes to progressively refine step resolution and control.

Full-step mode has four states with each motor winding driven by either 70.7% of the maximum positive current or 70.7% of the maximum negative current. This provides four steps per electrical rotation. Half-step mode creates eight steps per electrical rotation. Quarter- and eighth-step modes provide 16 and 32 steps per rotation, respectively.

Table 2 and Table 3 on pages 17 and 18, and Figure 8, Figure 9, Figure 10, and Figure 11 on pages 19 and 20 show the relative current level sequence for different settings of MSx.

The MSx pins have internal pull-down resistors.

### nSLEEP and ENBL Operation

Pulling nSLEEP low makes the MPQ6600L enter a low-power sleep state. In this state, the gate drive charge pump is stopped, and all the internal circuits and H-bridge outputs are disabled. All inputs are ignored when nSLEEP is active low.

When the device wakes up from sleep mode, about 1ms must pass before a STEP command can be issued, which allows the internal circuitry to stabilize. nSLEEP has an internal pull-down resistor.

The ENBL pin controls the output drivers. When ENBL is high, the H-bridge outputs are enabled, and the rising edges on STEP are recognized.

When ENBL is low, the H-bridge outputs are disabled, and the STEP input is ignored. ENBL has an internal pull-down resistor.

### Fault Reporting

The MPQ6600L provides an nFAULT pin that reports whether a fault condition (e.g. over-current, over-temperature, or over-voltage conditions) occurs. nFAULT is an open-drain output and is pulled low if a fault condition occurs. Once the fault condition is removed, nFAULT is pulled high via an external pull-up resistor.

### Over-Current Protection (OCP)

Over-current protection (OCP) circuitry limits the current through the MOSFETs by disabling the gate driver. If the MPQ6600L exceeds the over-current (OC) limit threshold for longer than the OC deglitch time ($t_{OCP}$), then all MOSFETs in the H-bridge are disabled, and nFAULT is pulled low. The driver remains off until either nSLEEP is reset or power is cycled on VIN.

OC conditions on both the high-side and low-side devices (e.g. a short to ground, supply, or across the motor winding) result in an OC shutdown. OCP does not use the current-sense circuitry for PWM current control.

### Over-Voltage Protection (OVP)

If $V_{IN}$ exceeds the over-voltage protection (OVP) threshold, then the H-bridge output is disabled, and nFAULT is pulled low. This protection is removed when $V_{IN}$ drops below 36V.

### Input Under-Voltage Lockout (UVLO) Protection

If $V_{IN}$ falls below the under-voltage lockout (UVLO) threshold, then all circuitry in the device is disabled, and the internal logic resets. Operation resumes when $V_{IN}$ exceeds the UVLO threshold.

### Thermal Shutdown

If the die temperature exceeds the safe limits, then all MOSFETs in the H-bridge are disabled, and nFAULT is pulled low. Once the die temperature drops to a safe level, operation resumes automatically.

# APPLICATION INFORMATION

### VIN Pin Voltage

The VIN pin supplies all power to the device. VIN must be properly bypassed using a capacitor connected to ground.

The normal operating range for $V_{IN}$ is between 4.5V and 35V.

To protect the device, VIN should never exceed the absolute maximum ratings, even for short-term transient conditions. In scenarios where mechanical energy can turn a motor into a generator, it is recommended to use additional OVP, such as a TVS diode placed between VIN and ground.

## COMPONENT SELECTION

### Selecting the External Capacitor

The MPQ6600L requires several capacitors for proper operation.

Connect the charge pump flying capacitor ($C_{CP}$) to the CP1 and CP2 pins. $C_{CP}$ must have a capacitance of 100nF and be rated to withstand the maximum VIN power supply voltage. A X7R ceramic capacitor is recommended.

Connect the VCP output capacitor ($C_{VCP}$) between VCP and VIN pins. $C_{VCP}$ must have a capacitance of 1µF and be rated to withstand 16V. A X7R ceramic capacitor is recommended.

The VG pin is the output of the LS gate drive's voltage regulator. Connect a 1µF bypass capacitor between VG and ground. It is recommended to use a X7R ceramic capacitor rated for a minimum of 16V.

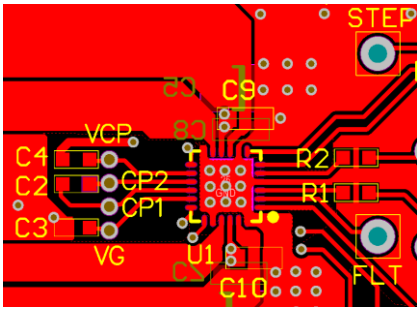
Connect a bypass capacitor between VIN and ground, and place it as close as possible to the device. It is recommended to use a minimum 0.1µF ceramic capacitor with X7R dielectrics. The capacitor must be rated for $V_{IN}$. Additional bulk capacitors may be required. A low-ESR 100µF electrolytic capacitor is recommended.

### PCB Layout Guidelines

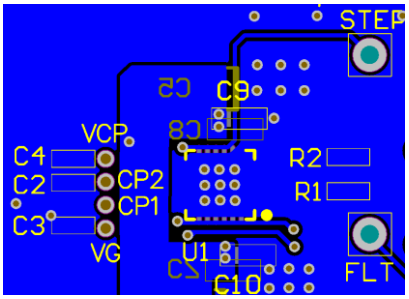
The MPQ6600L relies on thermal conduction to dissipate power. A multi-layer PCB with a solid ground plane provides the best power dissipation and the lowest operating temperature. The top layer is vital for removing heat from the device. Many vias are used (especially on ground) to move heat from the top layer to bottom plane.

For the best results, refer to Figure 6 and follow the guidelines below:

1. Place multiple vias in the exposed pad to extract and move heat to the environment.
2. Place bypass capacitors directly adjacent to the supply pins.
3. Place the VG capacitor (C3) and charge pump capacitor (C2 and C4) as close as possible to the IC.
4. Place the VIN bypass capacitors (C7, C8, C9, and C10) on the top and back side of the PCB.
5. Use multiple vias to connect the VIN and GND pins of the device.
6. Connect GND, AGND, and the exposed pad together under the device.




**Top Layer**




**Bottom Layer**

**Figure 6: Recommended PCB Layout**

## TYPICAL APPLICATION CIRCUIT

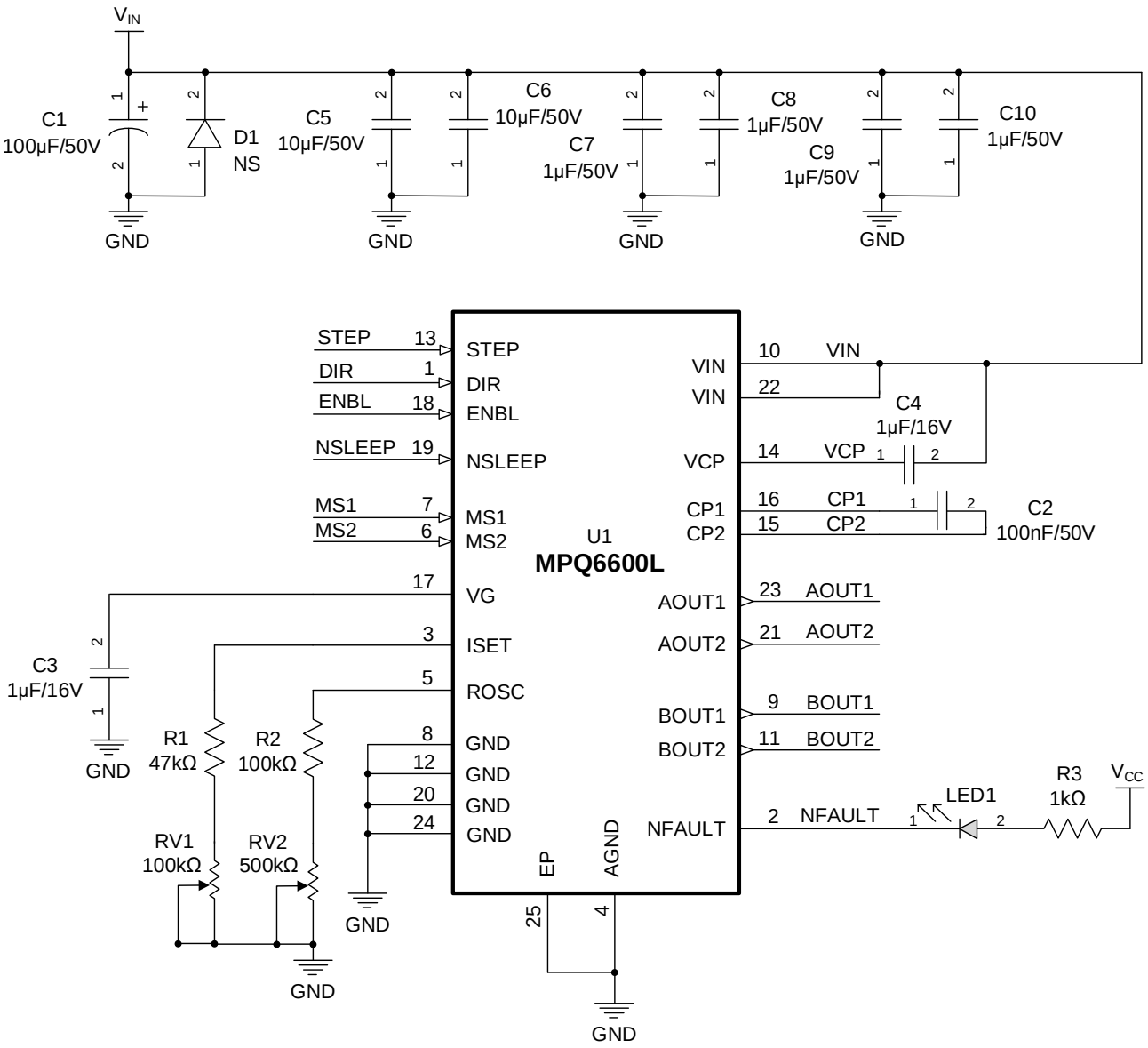



**Figure 7: Typical Application Circuit**

## MICROSTEPPING

**Table 2: Relative Current Level Sequence (DIR = 1)** (6)

| Eighth-Step # | Quarter-Step # | Half-Step # | Full Step # | Phase A Current (% of $I_{MAX}$) | Phase B Current (% of $I_{MAX}$) | Step Angle (°) |
|---|---|---|---|---|---|---|
| 1 | 1 | 1 | - | 100 | 0 | 0 |
| 2 | - | - | - | 98.08 | 19.51 | 11.3 |
| 3 | 2 | - | - | 92.39 | 38.27 | 22.5 |
| 4 | - | - | - | 83.15 | 55.56 | 33.8 |
| 5 | 3 | 2 | 1 | 70.71 | 70.71 | 45 |
| 6 | - | - | - | 55.56 | 83.15 | 56.3 |
| 7 | 4 | - | - | 38.27 | 92.39 | 67.5 |
| 8 | - | - | - | 19.51 | 98.08 | 78.8 |
| 9 | 5 | 3 | - | 0 | 100 | 90 |
| 10 | - | - | - | -19.51 | 98.08 | 101.3 |
| 11 | 6 | - | - | -38.27 | 92.39 | 112.5 |
| 12 | - | - | - | -55.56 | 83.15 | 123.8 |
| 13 | 7 | 4 | 2 | -70.71 | 70.71 | 135 |
| 14 | - | - | - | -83.15 | 55.56 | 146.3 |
| 15 | 8 | - | - | -92.39 | 38.27 | 157.5 |
| 16 | - | - | - | -98.08 | 19.51 | 168.8 |
| 17 | 9 | 5 | - | -100 | 0 | 180 |
| 18 | - | - | - | -98.08 | -19.51 | 191.3 |
| 19 | 10 | - | - | -92.39 | -38.27 | 202.5 |
| 20 | - | - | - | -83.15 | -55.56 | 213.8 |
| 21 | 11 | 6 | 3 | -70.71 | -70.71 | 225 |
| 22 | - | - | - | -55.56 | -83.15 | 236.3 |
| 23 | 12 | - | - | -38.27 | -92.39 | 247.5 |
| 24 | - | - | - | -19.51 | -98.08 | 258.8 |
| 25 | 13 | 7 | - | 0 | -100 | 270 |
| 26 | - | - | - | 19.51 | -98.08 | 281.3 |
| 27 | 14 | - | - | 38.27 | -92.39 | 292.5 |
| 28 | - | - | - | 55.56 | -83.15 | 303.8 |
| 29 | 15 | 8 | 4 | 70.71 | -70.71 | 315 |
| 30 | - | - | - | 83.15 | -55.56 | 326.3 |
| 31 | 16 | - | - | 92.39 | -38.27 | 337.5 |
| 32 | - | - | - | 98.08 | -19.51 | 348.8 |

## MICROSTEPPING *(continued)*

**Table 3: Relative Current Level Sequence (DIR = 0)** (6)

| Eighth-Step # | Quarter-Step # | Half-Step # | Full Step # | Phase A Current (% of $I_{MAX}$) | Phase B Current (% of $I_{MAX}$) | Step Angle (°) |
|---|---|---|---|---|---|---|
| 1 | 1 | 1 | - | 100 | 0 | 0 |
| 2 | - | - | - | 98.08 | -19.51 | 11.3 |
| 3 | 2 | - | - | 92.39 | -38.27 | 22.5 |
| 4 | - | - | - | 83.15 | -55.56 | 33.8 |
| 5 | 3 | 2 | 1 | 70.71 | -70.71 | 45 |
| 6 | - | - | - | 55.56 | -83.15 | 56.3 |
| 7 | 4 | - | - | 38.27 | -92.39 | 67.5 |
| 8 | - | - | - | 19.51 | -98.08 | 78.8 |
| 9 | 5 | 3 | - | 0 | -100 | 90 |
| 10 | - | - | - | -19.51 | -98.08 | 101.3 |
| 11 | 6 | - | - | -38.27 | -92.39 | 112.5 |
| 12 | - | - | - | -55.56 | -83.15 | 123.8 |
| 13 | 7 | 4 | 2 | -70.71 | -70.71 | 135 |
| 14 | - | - | - | -83.15 | -55.56 | 146.3 |
| 15 | 8 | - | - | -92.39 | -38.27 | 157.5 |
| 16 | - | - | - | -98.08 | -19.51 | 168.8 |
| 17 | 9 | 5 | - | -100 | 0 | 180 |
| 18 | - | - | - | -98.08 | 19.51 | 191.3 |
| 19 | 10 | - | - | -92.39 | 38.27 | 202.5 |
| 20 | - | - | - | -83.15 | 55.56 | 213.8 |
| 21 | 11 | 6 | 3 | -70.71 | 70.71 | 225 |
| 22 | - | - | - | -55.56 | 83.15 | 236.3 |
| 23 | 12 | - | - | -38.27 | 92.39 | 247.5 |
| 24 | - | - | - | -19.51 | 98.08 | 258.8 |
| 25 | 13 | 7 | - | 0 | 100 | 270 |
| 26 | - | - | - | 19.51 | 98.08 | 281.3 |
| 27 | 14 | - | - | 38.27 | 92.39 | 292.5 |
| 28 | - | - | - | 55.56 | 83.15 | 303.8 |
| 29 | 15 | 8 | 4 | 70.71 | 70.71 | 315 |
| 30 | - | - | - | 83.15 | 55.56 | 326.3 |
| 31 | 16 | - | - | 92.39 | 38.27 | 337.5 |
| 32 | - | - | - | 98.08 | 19.51 | 348.8 |

**Note:**

6) The reset position is at a 45° step angle.

## MICROSTEPPING *(continued)*

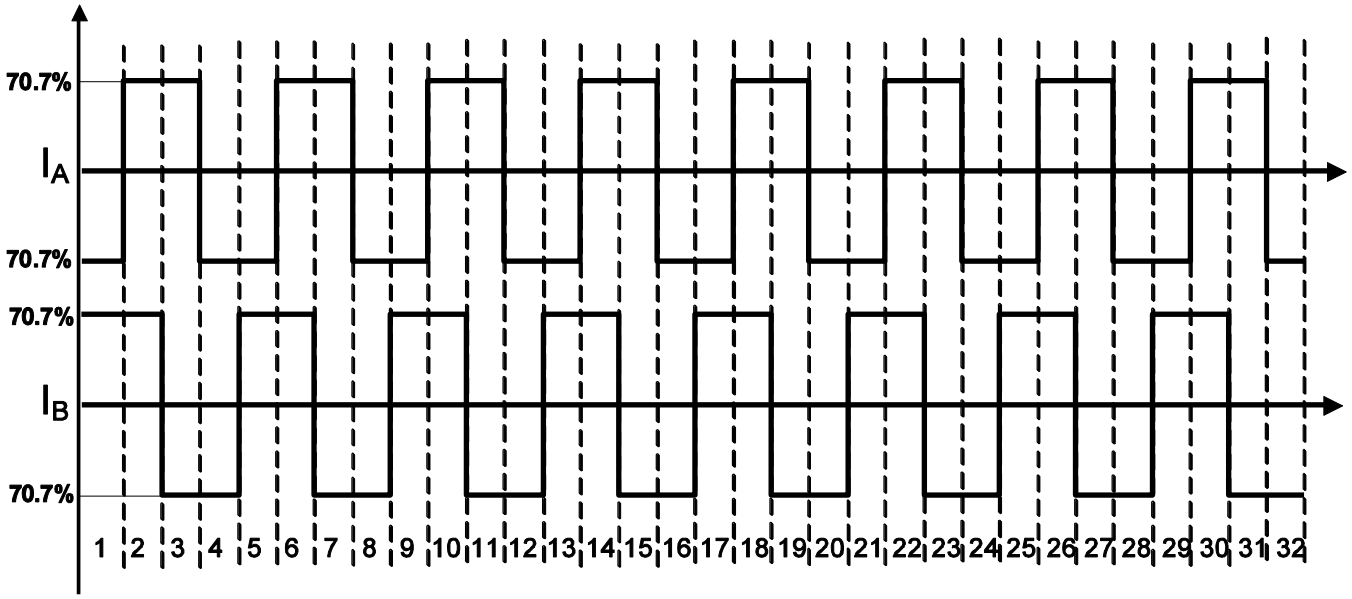



**Figure 8: Full Step (4 Step Sequences, DIR = 0)**

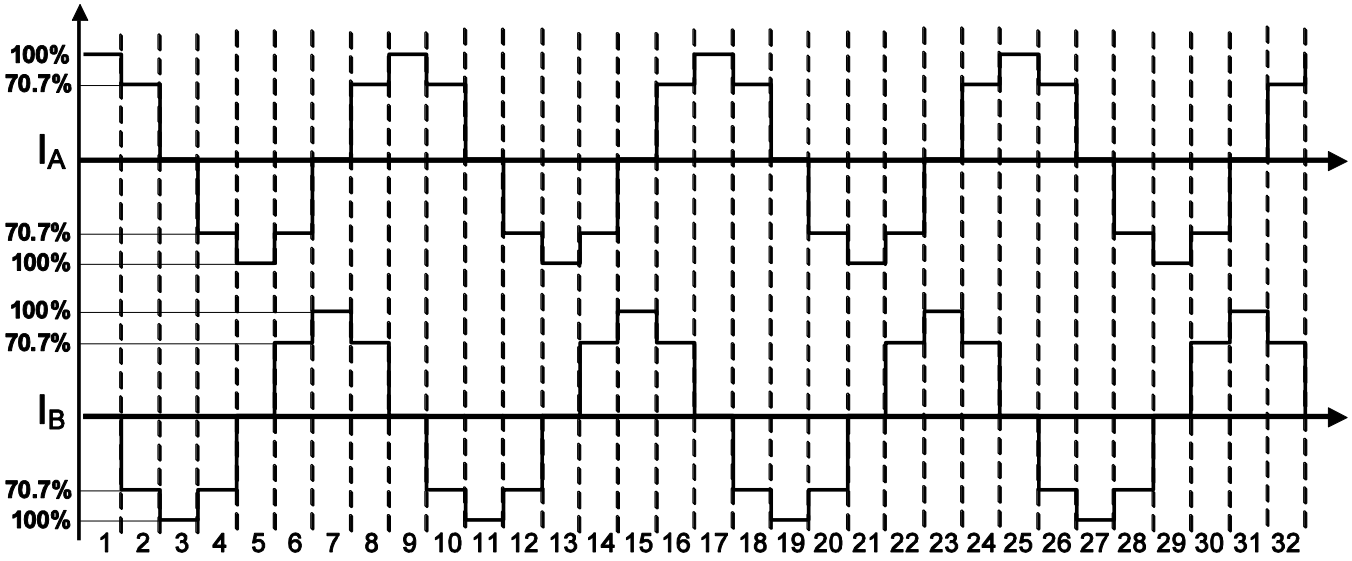



**Figure 9: Half-Step (8 Step Sequences, DIR = 0)**

## MICROSTEPPING *(continued)*

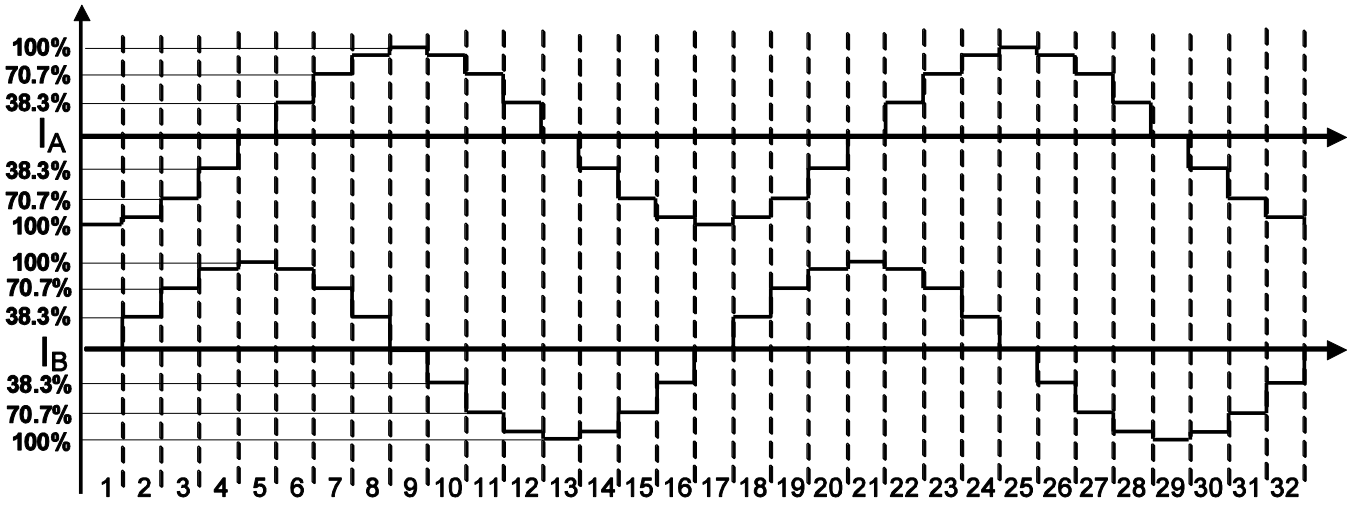



**Figure 10: Quarter-Step (16 Step Sequences, DIR = 0)**

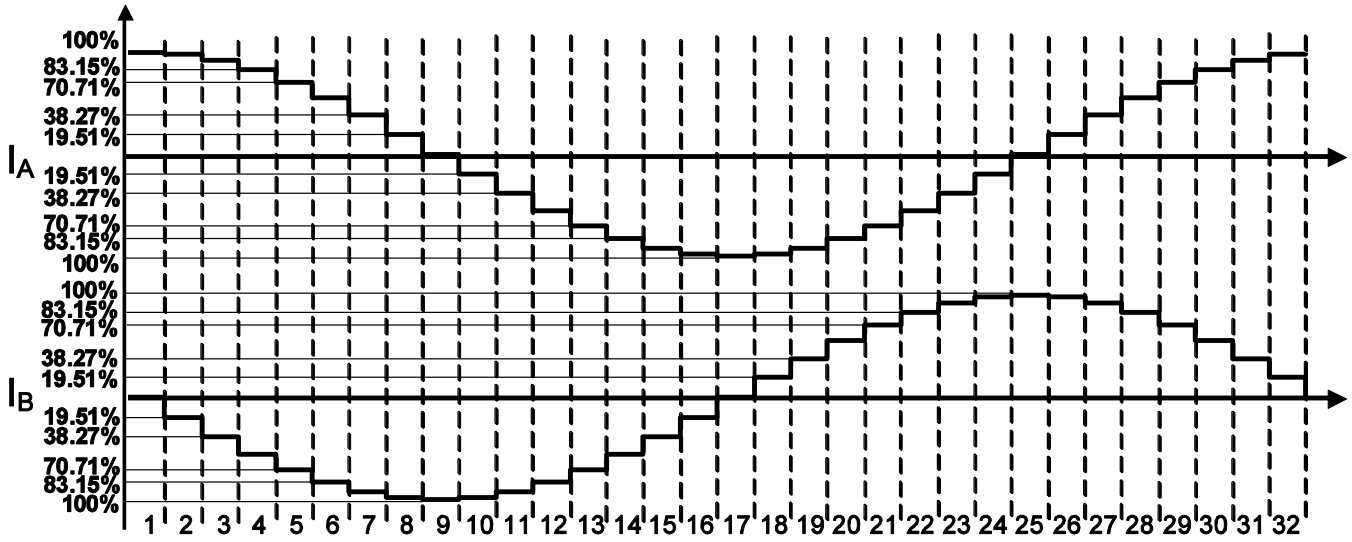
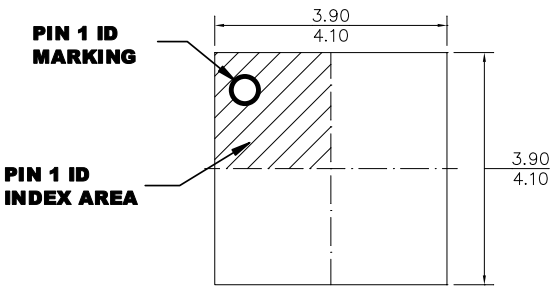


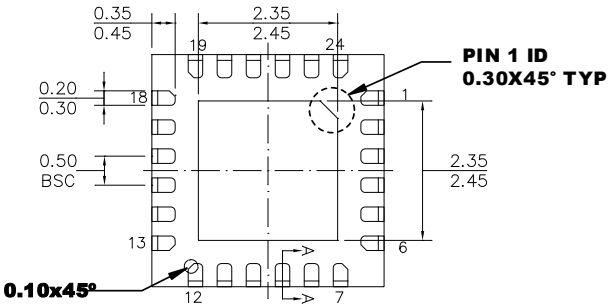

**Figure 11: Eighth-Step (32 Step Sequences, DIR = 0)**

# PACKAGE INFORMATION

## QFN-24 (4mmx4mm)
## Wettable Flanks

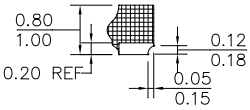



**TOP VIEW**

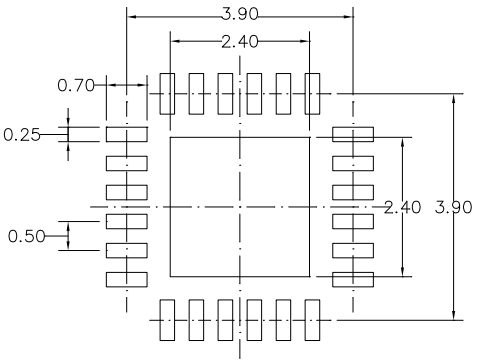



**BOTTOM VIEW**


**SIDE VIEW**




**SECTION A-A**

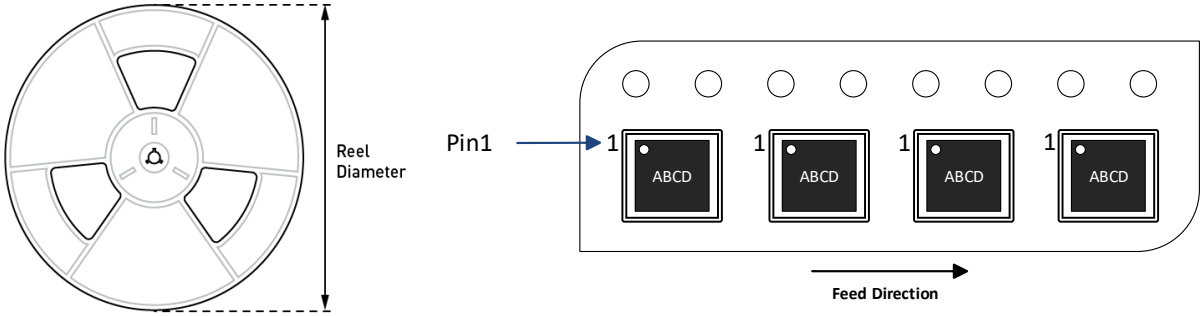



**RECOMMENDED LAND PATTERN**

**NOTE:**

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION




| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---|---|---|---|---|---|---|---|
| MPQ6600LGRE-AEC1-Z | QFN-24 (4mmx4mm) | 5000 | N/A | N/A | 13in | 12mm | 8mm |

## REVISION HISTORY

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 6/28/2024 | Initial Release | - |